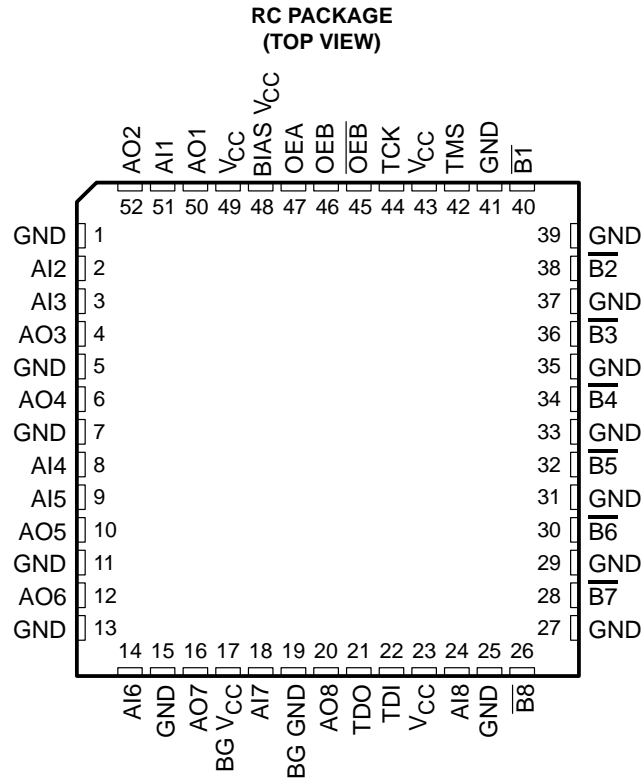


- **Compatible With IEEE Std 1194.1-1991 (BTL)**
- **TTL A Port, Backplane Transceiver Logic (BTL) \bar{B} Port**
- **Open-Collector \bar{B} -Port Outputs Sink 100 mA**
- **High-Impedance State During Power Up and Power Down**
- **BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion or Withdrawal**
- **\bar{B} -Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage**



description

The SN74FB2040 is an 8-bit transceiver designed to translate signals between TTL and backplane transceiver logic (BTL) environments.

The \bar{B} port operates at BTL-signal levels. The open-collector \bar{B} ports are specified to sink 100 mA. Two output enables (OEB and \bar{OEB}) are provided for the \bar{B} outputs. When OEB is high and \bar{OEB} is low, the \bar{B} port is active and reflects the inverse of the data present at the A-input pins. When OEB is low, \bar{OEB} is high, or V_{CC} is less than 2.1 V, the \bar{B} port is turned off.

The A port operates at TTL-signal levels and has separate input and output pins. The A outputs reflect the inverse of the data at the \bar{B} port when the A-port output enable (OEA) is high. When OEA is low or when V_{CC} is less than 2.1 V, the A outputs are in the high-impedance state.

The pins TMS, TCK, TDI, and TDO are nonfunctional, i.e., not intended for use with the IEEE Std 1149.1 (JTAG) test bus. TMS and TCK are not connected, and TDI is shorted to TDO.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74FB2040 8-BIT TTL/BTL TRANSCEIVER

SCBS173N – NOVEMBER 1991 – REVISED MARCH 2002

ORDERING INFORMATION

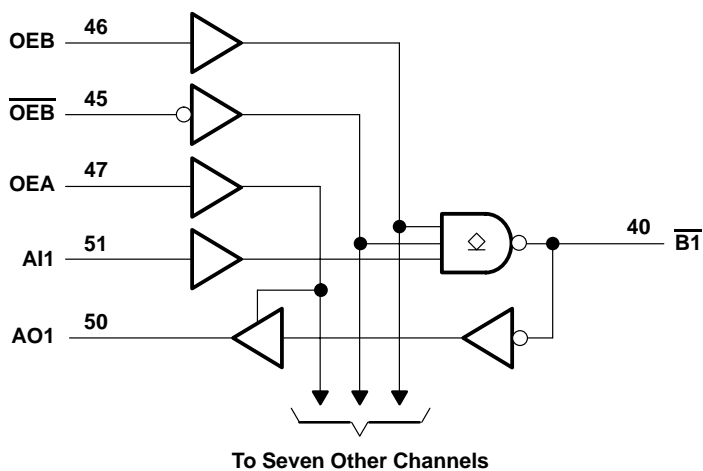
T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	QFP – RC	Tube	SN74FB2040RC	FB2040

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			FUNCTION
OEB	$\overline{\text{OEB}}$	OEA	
L	X	L	Isolation
X	H	L	
L	X	H	$\overline{\text{B}}$ data to AO bus
X	H	H	
H	L	L	$\overline{\text{A}}$ data to B bus
H	L	H	

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I : Except \overline{B} port	–1.2 V to 7 V
\overline{B} port	–1.2 V to 3.5 V
Voltage range applied to any \overline{B} output in the disabled or power-off state, V_O	–0.5 V to 3.5 V
Voltage range applied to any output in the high state, V_O : A port	–0.5 V to V_{CC}
Input clamp current, I_{IK} : Except \overline{B} port	–40 mA
\overline{B} port	–18 mA
Current applied to any single output in the low state, I_O : A port	48 mA
\overline{B} port	200 mA
Package thermal impedance, θ_{JA} (see Note 1)	44°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC} , BIAS V_{CC} , BG V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	\overline{B} port	1.62	2.3	V
		Except \overline{B} port	2		
V_{IL}	Low-level input voltage	\overline{B} port	0.75	1.47	V
		Except \overline{B} port		0.8	
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–3	mA
I_{OL}	Low-level output current	AO port		24	mA
		\overline{B} port		100	
T_A	Operating free-air temperature	0		70	°C

NOTE 2: To ensure proper device operation, all unused inputs must be terminated as follows: A and control inputs to V_{CC} (5 V) or GND, and B inputs to GND only. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74FB2040

8-BIT TTL/BTL TRANSCEIVER

SCBS173N – NOVEMBER 1991 – REVISED MARCH 2002

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}	\overline{B} port	V _{CC} = 4.5 V,	I _I = -18 mA			-1.2	V
	Except \overline{B} port	V _{CC} = 4.5 V,	I _I = -40 mA			-0.5	
V _{OH}	AO port	V _{CC} = 4.5 V,	I _{OH} = -3 mA	2.5	3.3		V
V _{OL}	AO port	V _{CC} = 4.5 V,	I _{OL} = 24 mA		0.35	0.5	V
	\overline{B} port	V _{CC} = 4.5 V	I _{OL} = 80 mA		0.75	1.1	
			I _{OL} = 100 mA			1.15	
I _I	Except \overline{B} port	V _{CC} = 5.5 V,	V _I = 5.5 V			50	μA
I _{IH} ‡	Except \overline{B} port	V _{CC} = 5.5 V,	V _I = 2.7 V			50	μA
I _{IL} ‡	Except \overline{B} port	V _{CC} = 5.5 V,	V _I = 0.5 V			-50	μA
	\overline{B} port	V _{CC} = 5.5 V,	V _I = 0.75 V			-100	
I _{OH}	\overline{B} port	V _{CC} = 0 to 5.5 V,	V _O = 2.1 V			100	μA
I _{OZH}	AO port	V _{CC} = 5.5 V,	V _O = 2.7 V			50	μA
I _{OZL}	AO port	V _{CC} = 5.5 V,	V _O = 0.5 V			-50	μA
I _{OZPU}	A port	V _{CC} = 0 to 2.1 V,	V _O = 0.5 V to 2.7 V			50	μA
I _{OZPD}	A port	V _{CC} = 2.1 V to 0,	V _O = 0.5 V to 2.7 V			-50	μA
I _{OS} §	AO port	V _{CC} = 5.5 V,	V _O = 0	-30		-180	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I _{CC}	A _I port to \overline{B} port	V _{CC} = 5.5 V,	I _O = 0		40		mA
	\overline{B} port to AO port				70		
C _i	A _I port	V _I = V _{CC} or GND			3.5		pF
	Control inputs				3		
C _O	AO port	V _O = V _{CC} or GND			6		pF
C _{io}	\overline{B} port per IEEE Std 1194.1-1991	V _{CC} = 0 to 4.5 V				5	pF
		V _{CC} = 4.5 V to 5.5 V				5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
I _{CC} (BIAS V _{CC})		V _{CC} = 0 to 4.5 V,	V _B = 0 to 2 V,	V _I (BIAS V _{CC}) = 4.5 V to 5.5 V		450	μA
		V _{CC} = 4.5 to 5.5 V,	V _B = 0 to 2 V,	V _I (BIAS V _{CC}) = 4.5 V to 5.5 V		10	
V _O	\overline{B} port	V _{CC} = 0,	V _I (BIAS V _{CC}) = 5 V		1.62	2.1	V
I _O	\overline{B} port	V _{CC} = 0,	V _B = 1 V,	V _I (BIAS V _{CC}) = 4.5 V to 5.5 V		-1	μA
		V _{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V			100	
		V _{CC} = 0 to 2.2 V,	OEB = 0 to 5 V			100	



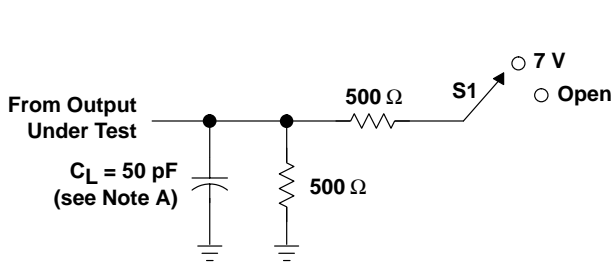
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	AI	\overline{B}	3.2	4.5	6	2.4	6.5	ns
t _{PHL}			2.8	4.2	5.6	2.7	5.8	
t _{PLH}	\overline{B}	AO	2.3	3.8	5.7	1.9	6.2	ns
t _{PHL}			2.3	4.2	5.9	2	8.2	
t _{PLH}	OEB	\overline{B}	3.7	5.1	6.7	3	7	ns
t _{PHL}			3.1	4.6	5.9	3	6.1	
t _{PLH}	\overline{OEB}	\overline{B}	3.6	5.2	6.8	3.3	7	ns
t _{PHL}			2.9	4.4	5.9	2.6	6.1	
t _{PZH}	OEA	AO	2.5	4	5.5	2.1	5.8	ns
t _{PZL}			2.1	3.6	4.8	2	5	
t _{PHZ}	OEA	AO	2.3	4.1	5.9	1.9	6.5	ns
t _{PLZ}			1.6	3.1	4.5	1.4	4.7	
t _{sk(p)}	Skew for any single channel t _{PHL} - t _{PLH} , AI to \overline{B} or \overline{B} to AO		0.5					ns
t _{sk(o)}	Skew between drivers in the same package, AI to \overline{B} or \overline{B} to AO		0.4					ns
t _r	Rise time, 1.3 V to 1.8 V, \overline{B} port		2	2.8	3.8	1.7		ns
t _f	Fall time, 1.8 V to 1.3 V, \overline{B} port		1	1.9	3	1	4.2	ns
t _(pr)	\overline{B} -port input pulse rejection					1	3.4	ns

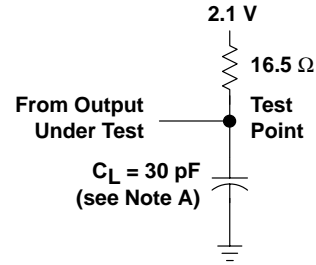
SN74FB2040 8-BIT TTL/BTL TRANSCEIVER

SCBS173N – NOVEMBER 1991 – REVISED MARCH 2002

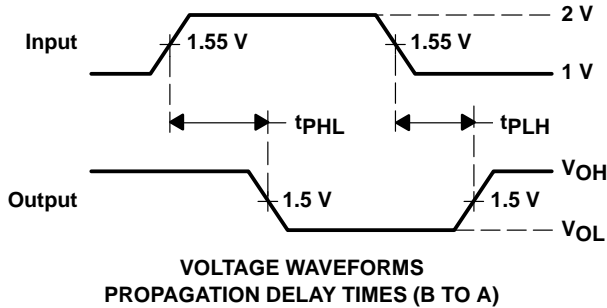
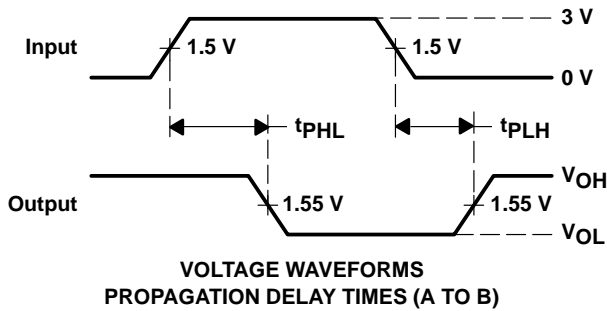
PARAMETER MEASUREMENT INFORMATION



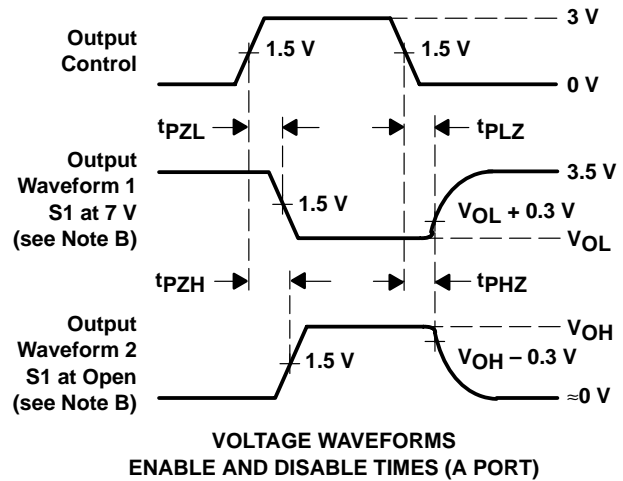
LOAD CIRCUIT FOR A OUTPUTS



LOAD CIRCUIT FOR B OUTPUTS



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: TTL inputs: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns; BTL inputs: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74FB2040RCG3	ACTIVE	QFP	RC	52	96	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 70	FB2040	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

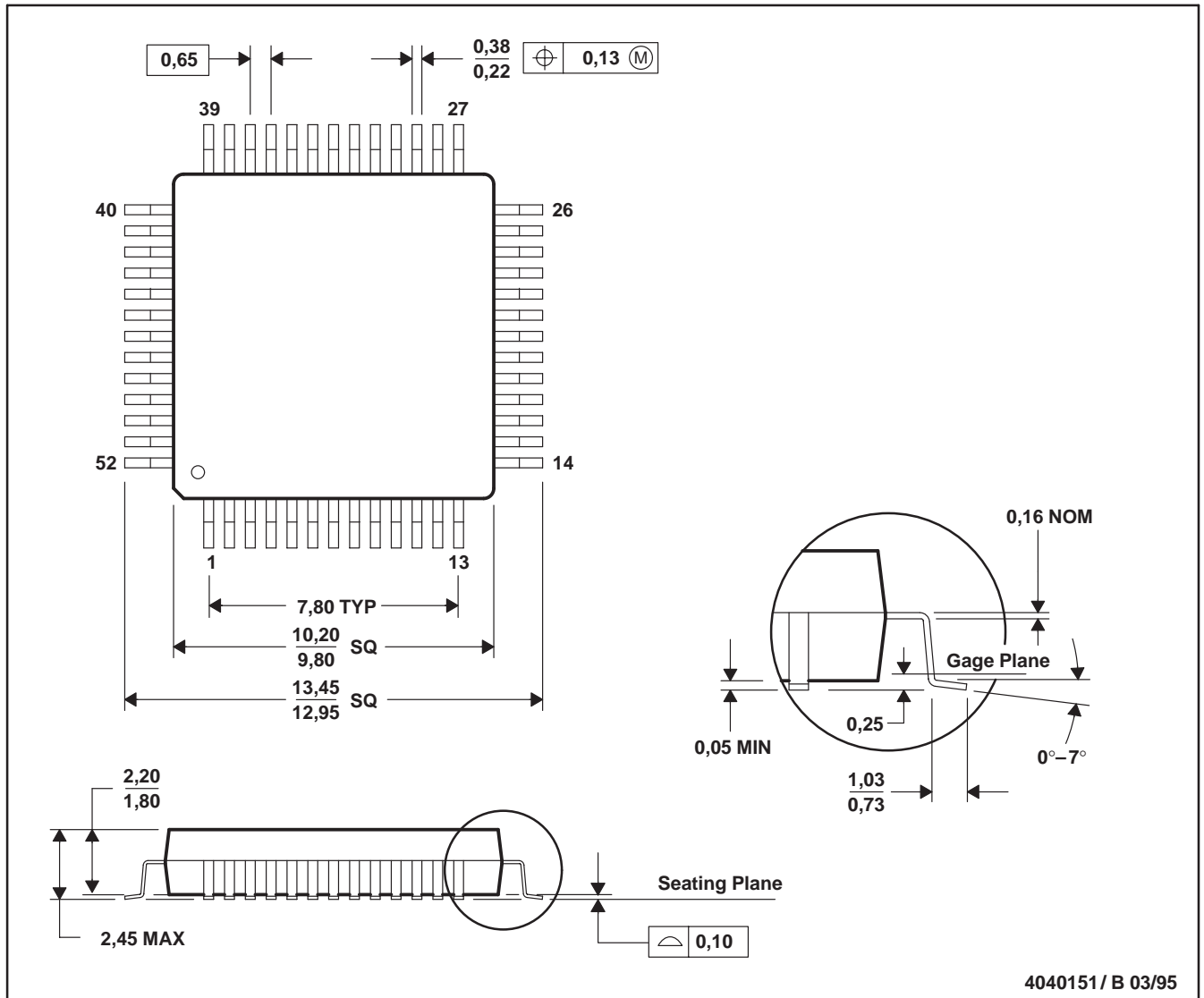
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RC (S-PQFP-G52)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-022

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.