LMV641 10-MHz, 12-V, Low-Power Amplifier

1 Features

- Specified for 2.7-V, and ±5-V Performance
- Low Power Supply Current: 138 µA
- High Unity Gain Bandwidth: 10 MHz
- Max Input Offset Voltage: 500 µV
- CMRR: 120 dB
- PSRR: 105 dB
- Input Referred Voltage Noise: 14 nV/√Hz
- 1/f Corner Frequency: 4 Hz
- Output Swing With 2-kΩ Load 40 mV from Rail
- Total Harmonic Distortion: 0.002% at 1 kHz, 2 kΩ
- Temperature Range −40°C to 125°C

2 Applications

- Portable Equipment
- Battery-Powered Systems
- Sensors and Instrumentation

3 Description

The LMV641 is a low-power, wide-bandwidth operational amplifier with an extended power supply voltage range of 2.7 V to 12 V.

The device features 10 MHz of gain bandwidth product with unity gain stability on a typical supply current of 138 µA. Other key specifications are a PSRR of 105 dB, CMRR of 120 dB, V_{OS} of 500 µV, input referred voltage noise of 14 nV/√Hz, and a THD of 0.002%. This amplifier has a rail-to-rail output stage and a common mode input voltage, which includes the negative supply.

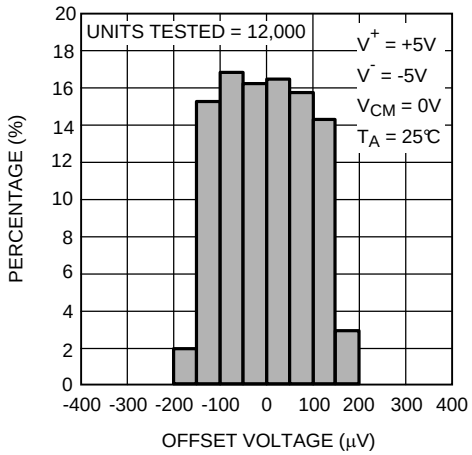
The LMV641 device operates over a temperature range of −40°C to +125°C and is offered in the board-space-saving 5-Pin SC70, SOT-23, and 8-Pin SOIC packages.

Device Information(1)

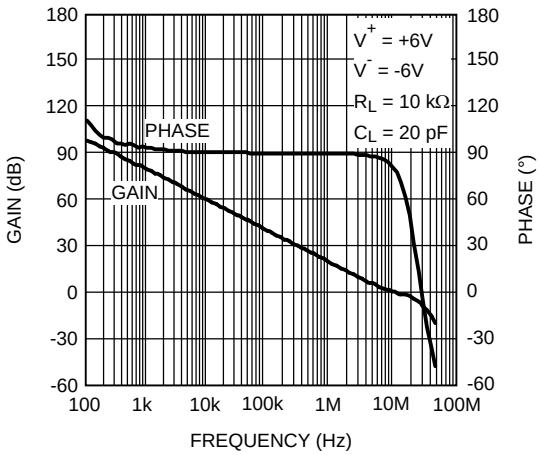
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMV641	SOIC (8)	4.90 mm × 3.91 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
	SC70 (5)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Offset Voltage Distribution



Open Loop Gain and Phase vs Frequency



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2013) to Revision D **Page**

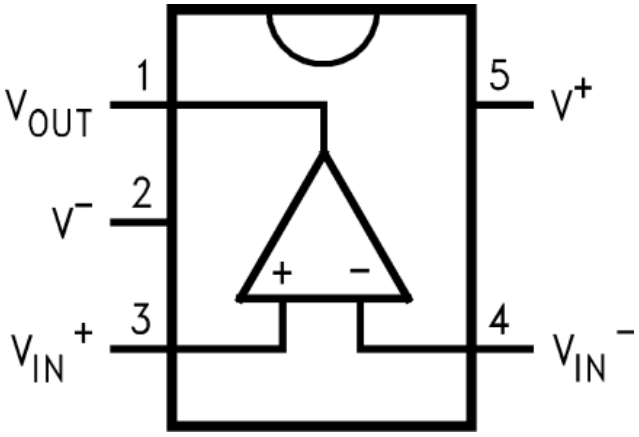
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Moved Package thermal resistance ($R_{\theta JA}$) rows from *Recommended Operating Conditions* to *Thermal Information* ... 4

Changes from Revision B (February 2013) to Revision C **Page**

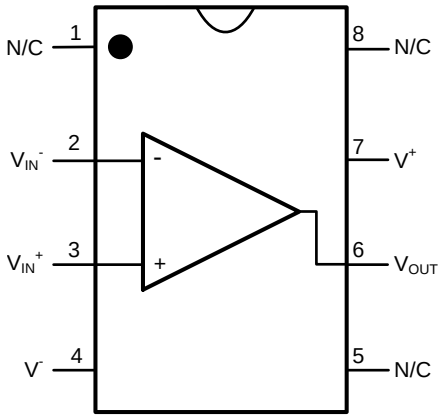
- Changed layout of National Semiconductor Data Sheet to TI Format ... 1

5 Pin Configuration and Functions

DBV and DCK Packages
5-Pin SOT-23 and SC70
Top View



D Package
8-Pin SOIC
Top View



Pin Functions

PIN				TYPE(1)	DESCRIPTION
NAME	SOT-23	SC70	SOIC		
V_{IN}+	3	3	3	I	Noninverting Input
V_{IN}-	4	4	2	I	Inverting Input
V_{OUT}	1	1	6	O	Output
V^+	5	5	7	P	Positive supply input
V^-	2	2	4	P	Supply negative input

(1) I = input; O = output; P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Differential input V_{ID}	±0.3	±0.3	V
Supply voltage ($V_S = V^+ - V^-$)		13.2	V
Input and output pin voltage	(V^- −0.3)	V^+ +0.3	V
Junction temperature (3)		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For ensured specifications and the test conditions, see the *Electrical Characteristics* Tables.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office / Distributors for availability and specifications.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), (1)	±2000	V
		Machine model (MM)	±200	

(1) Human Body Model, applicable std. MIL-STD-883, Method 3015.7.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Temperature (1)	–40		125	°C
Supply voltage ($V_S = V^+ – V^-$)	2.7		12	V

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

6.4 Thermal Information

THERMAL METRIC(1)		LMV641			UNIT
		DBV (SOT-23)	DCK (SC70)	D (SOIC)	
		5 PINS	5 PINS	8 PINS	
$R_{\theta JA}$ (2)	Junction-to-ambient thermal resistance	325	456	166	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	178.1	121.8	93.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.8	68.9	90.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	57.7	5.3	38.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	60.2	68.1	90.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

6.5 DC Electrical Characteristics: 2.7 V

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 2.7 V, V^- = 0 V, V_O = V_{CM} = V^+/2, and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		MIN (1)	TYP (2)	MAX (1)	UNIT
V_{OS}	Input offset voltage	T_A = 25°C			30	500	µV
		Temperature extremes				750	
TC V_{OS}	Input offset average drift				0.1		µV/°C
I_B	Input bias current	T_A = 25°C (3)			75	95	nA
		Temperature extremes				110	
I_{OS}	Input offset current				0.9	5	nA
CMRR	Common-mode rejection ratio	0 V ≤ V_{CM} ≤ 1.7 V	T_A = 25°C (3)	89	114		dB
			Temperature extremes	84			
PSRR	Power supply rejection ratio	2.7 V ≤ V^+ ≤ 10 V, V_{CM} = 0.5	T_A = 25°C (3)	94.5	105		dB
			Temperature extremes	92.5			
		2.7 V ≤ V^+ ≤ 12 V, V_{CM} = 0.5	T_A = 25°C (3)	94	100		
			Temperature extremes	92			
CMVR	Input common-mode voltage range	CMRR ≥ 80 dB	T_A = 25°C (3)	0		1.8	V
		CMRR ≥ 68 dB	Temperature extremes	0		1.8	
A_{VOL}	Large signal voltage gain	0.3 V ≤ V_O ≤ 2.4 V, R_L = 2 kΩ to V^+/2		82	88		dB
		0.4 V ≤ V_O ≤ 2.3 V, R_L = 2 kΩ to V^+/2		78			
		0.3 V ≤ V_O ≤ 2.4 V, R_L = 10 kΩ to V^+/2	T_A = 25°C (3)	86	98		
		0.4 V ≤ V_O ≤ 2.3 V, R_L = 10 kΩ to V^+/2	Temperature extremes	82			
V_O	Output swing high	R_L = 2 kΩ to V^+/2, V_{IN} = 100 mV	T_A = 25°C (3)		42	58	mV from rail
			Temperature extremes			68	
		R_L = 10 kΩ to V^+/2, V_{IN} = 100 mV	T_A = 25°C (3)		22	35	
			Temperature extremes			40	
	Output swing low	R_L = 2 kΩ to V^+/2, V_{IN} = 100 mV	T_A = 25°C (3)		38	48	
			Temperature extremes			58	
		R_L = 10 kΩ to V^+/2, V_{IN} = 100 mV			18	30	
						35	
I_{OUT}	Sourcing and sinking output current	V_{IN_DIFF} = 100 mV to V_O = V^+/2 (4)	Sourcing		22		mA
			Sinking		25		
I_S	Supply current	T_A = 25°C (3)			138	170	µA
		Temperature extremes				220	
SR	Slew rate	A_V = 1, V_O = 1 V_{PP}	Rising (10% to 90%)		2.3		V/µs
			Falling (90% to 10%)		1.6		
GBW	Gain bandwidth product				10		MHz
e_n	Input-referred voltage noise	f = 1 kHz			14		nV/√Hz
i_n	Input-referred current noise	f = 1 kHz			0.15		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = 2, R_L = 2 kΩ			0.014%		

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using Statistical Quality Control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(3) Positive current corresponds to current flowing into the device.
(4) The part is not short-circuit protected and is not recommended for operation with low resistive loads. Typical sourcing and sinking output current curves are provided in *Typical Characteristics* and should be consulted before designing for heavy loads.

6.6 DC Electrical Characteristics: 10 V

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 10 V, V^- = 0 V, $V_O = V_{CM} = V^+/2$, and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		MIN (1)	TYP (2)	MAX (1)	UNIT
V_{OS}	Input offset voltage	T_A = 25°C (3)			5	500	µV
		Temperature extremes				750	
TC V_{OS}	Input offset average drift				0.1		µV/°C
I_B	Input bias current	(3)	T_A = 25°C (3)		70	90	nA
			Temperature extremes			105	
I_{OS}	Input offset current				0.7	5	nA
CMRR	Common-mode rejection ratio	0 V ≤ V_{CM} ≤ 9 V	T_A = 25°C (3)	94	120		dB
			Temperature extremes	90			
PSRR	Power supply rejection ratio	2.7 V ≤ V^+ ≤ 10 V, V_{CM} = 0.5 V	T_A = 25°C (3)	94.5	105		dB
			Temperature extremes	92.5			
		2.7 V ≤ V^+ ≤ 12 V, V_{CM} = 0.5 V	T_A = 25°C (3)	94	100		
			Temperature extremes	92			
CMVR	Input common-mode voltage range	CMRR ≥ 80 dB	T_A = 25°C (3)	0		9.1	V
		CMRR ≥ 76 dB	Temperature extremes	0		9.1	
A_{VOL}	Large signal voltage gain	0.3 V ≤ V_O ≤ 9.7 V, R_L = 2 kΩ to $V^+/2$ 0.4 V ≤ V_O ≤ 9.6 V, R_L = 2 kΩ to $V^+/2$	T_A = 25°C (3)	90	99		dB
			Temperature extremes	85			
		0.3 V ≤ V_O ≤ 9.7 V, R_L = 10 kΩ to $V^+/2$ 0.4 V ≤ V_O ≤ 9.6 V, R_L = 10 kΩ to $V^+/2$	T_A = 25°C (3)	97	104		
			Temperature extremes	92			
V_O	Output Swing High	R_L = 2 kΩ to $V^+/2$, V_{IN} = 100 mV	T_A = 25°C (3)		68	95	mV from rail
			Temperature extremes			125	
		R_L = 10 kΩ to $V^+/2$, V_{IN} = 100 mV	T_A = 25°C (3)		37	55	
			Temperature extremes			65	
	Output Swing Low	R_L = 2 kΩ to $V^+/2$, V_{IN} = 100 mV	T_A = 25°C (3)		65	90	
			Temperature extremes			110	
		R_L = 10 kΩ to $V^+/2$, V_{IN} = 100 mV	T_A = 25°C (3)		32	42	
			Temperature extremes			52	
I_{OUT}	Sourcing and sinking output current	V_{IN_DIFF} = 100 mV to $V_O = V^+/2$ (4)	Sourcing		26		mA
			Sinking		112		
I_S	Supply current	T_A = 25°C (3)			158	190	µA
		Temperature extremes				240	
SR	Slew rate	A_V = 1, V_O = 2 V to 8 V_{PP}	Rising (10% to 90%)		2.6		V/µs
			Falling (90% to 10%)		1.6		

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using Statistical Quality Control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(3) Positive current corresponds to current flowing into the device.
(4) The part is not short-circuit protected and is not recommended for operation with low resistive loads. Typical sourcing and sinking output current curves are provided in *Typical Characteristics* and should be consulted before designing for heavy loads.

DC Electrical Characteristics: 10 V (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 10 V, V^- = 0 V, $V_O = V_{CM} = V^+/2$, and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
GBW	Gain bandwidth product			10		MHz
e_n	Input-referred voltage noise	f = 1 kHz		14		nV/√Hz
i_n	Input-referred current noise	f = 1 kHz		0.15		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = 2, R_L = 2 kΩ		0.002%		

6.7 Typical Characteristics

Unless otherwise specified, T_A = 25°C, V^+ = 10 V, V^- = 0 V, V_{CM} = V_S/2.

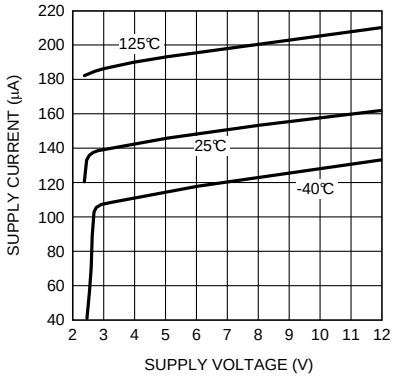


Figure 1. Supply Current vs Supply Voltage

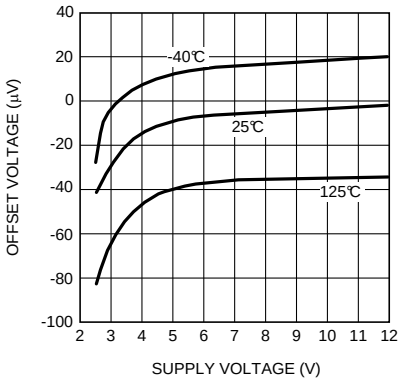


Figure 2. Offset Voltage vs Supply Voltage

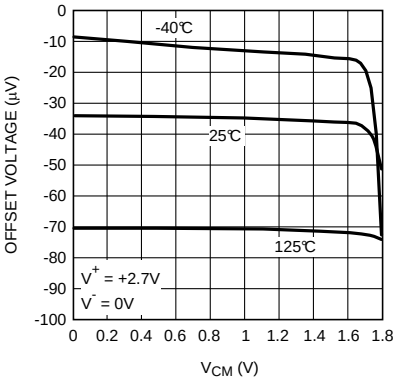


Figure 3. Offset Voltage vs V_{CM}

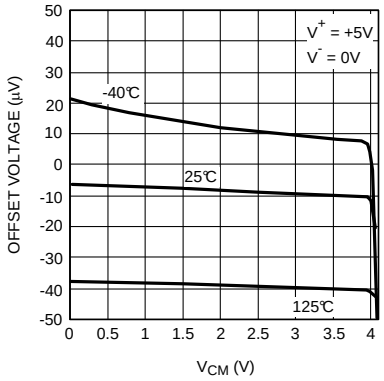


Figure 4. Offset Voltage vs V_{CM}

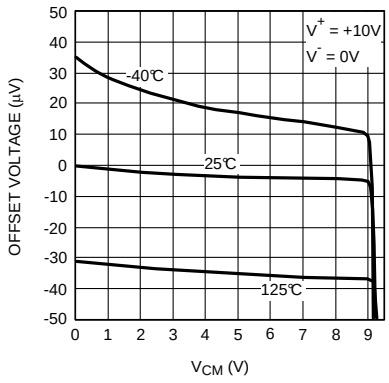


Figure 5. Offset Voltage vs V_{CM}

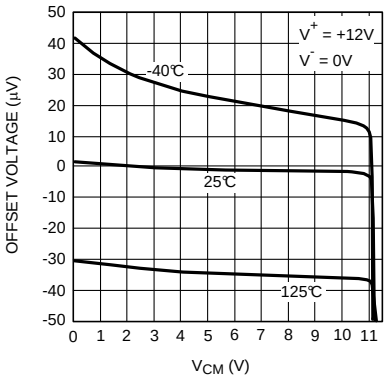


Figure 6. Offset Voltage vs V_{CM}

Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^+ = 10 V, V^- = 0 V, V_{CM} = V_S/2.

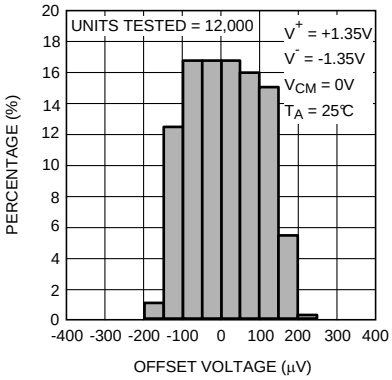


Figure 7. Offset Voltage Distribution

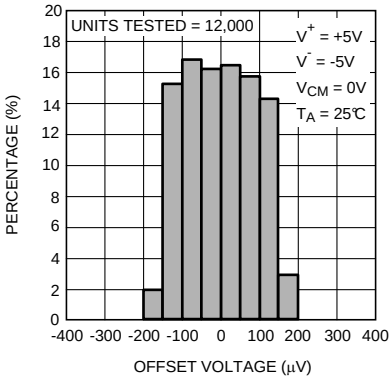


Figure 8. Offset Voltage Distribution

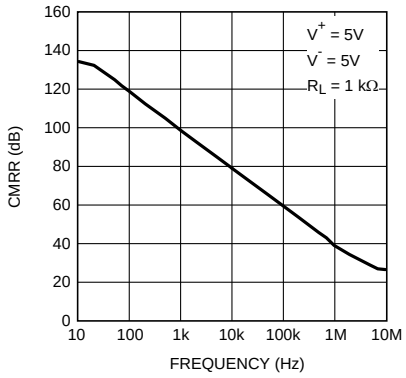


Figure 9. CMRR vs Frequency

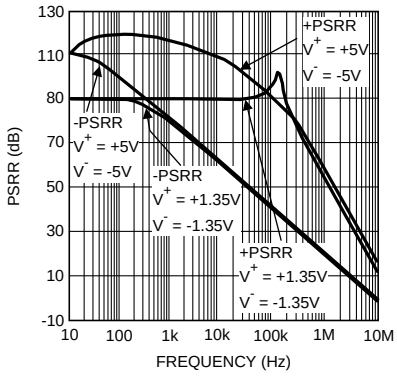


Figure 10. PSRR vs Frequency

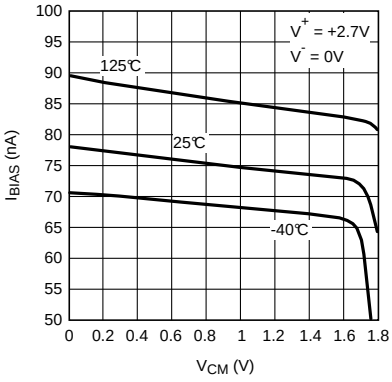


Figure 11. Input Bias Current vs V_{CM}

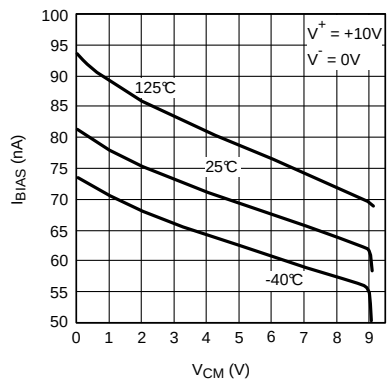


Figure 12. Input Bias Current vs V_{CM}

Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^+ = 10 V, V^- = 0 V, V_{CM} = V_S/2.

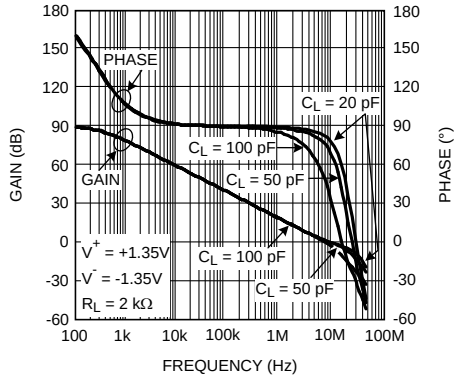


Figure 13. Open-Loop Gain and Phase With Capacitive Load

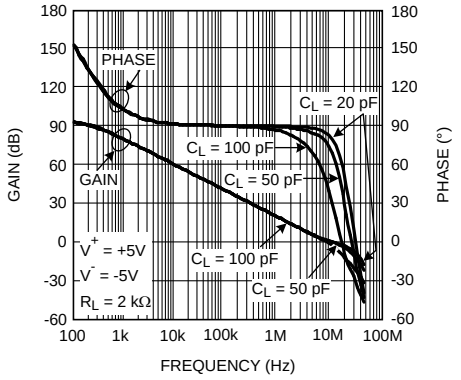


Figure 14. Open-Loop Gain and Phase With Capacitive Load

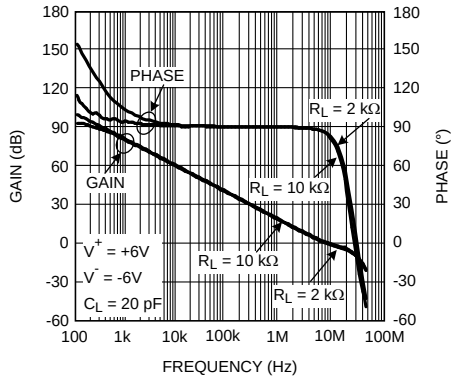


Figure 15. Open-Loop Gain and Phase With Resistive Load

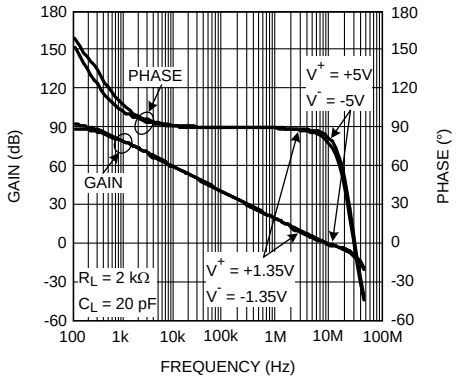


Figure 16. Open-Loop Gain and Phase With Supply Voltage

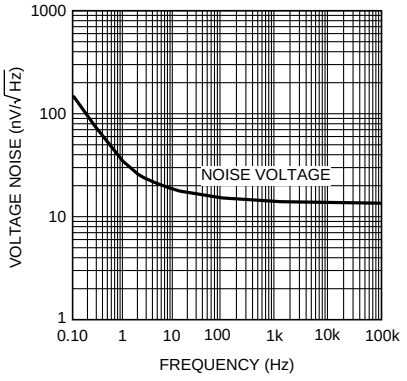


Figure 17. Input Referred Noise Voltage vs Frequency

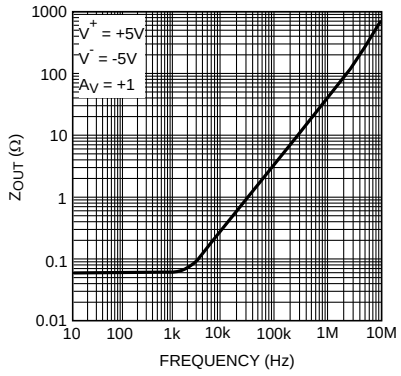


Figure 18. Close Loop Output Impedance vs Frequency

Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^+ = 10 V, V^- = 0 V, V_{CM} = V_S/2.

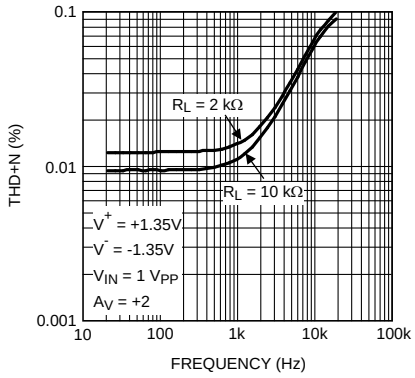


Figure 19. THD+N vs Frequency

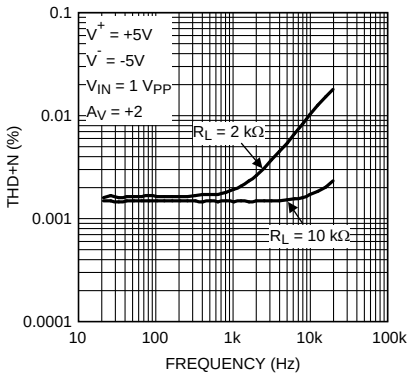


Figure 20. THD+N vs Frequency

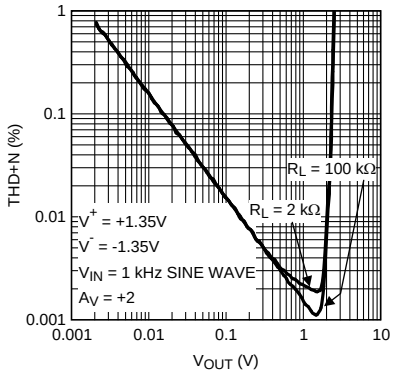


Figure 21. THD+N vs V_{OUT}

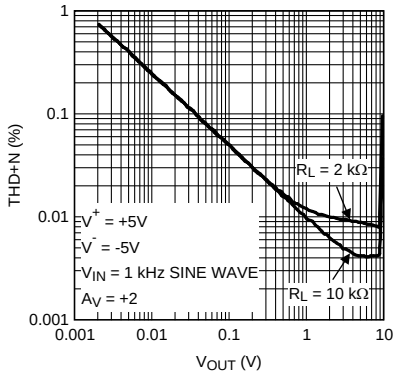


Figure 22. THD+N vs V_{OUT}

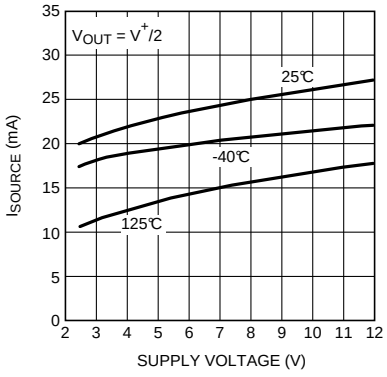


Figure 23. Sourcing Current vs Supply Voltage

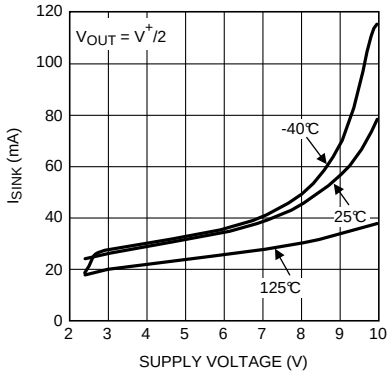


Figure 24. Sinking Current vs Supply Voltage

Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^+ = 10 V, V^- = 0 V, V_{CM} = V_S/2.

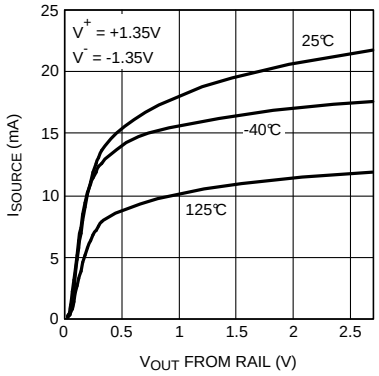


Figure 25. Sourcing Current vs V_{OUT}

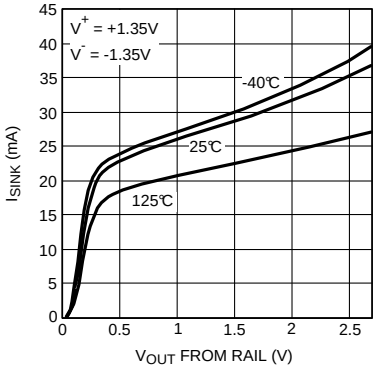


Figure 26. Sinking Current vs V_{OUT}

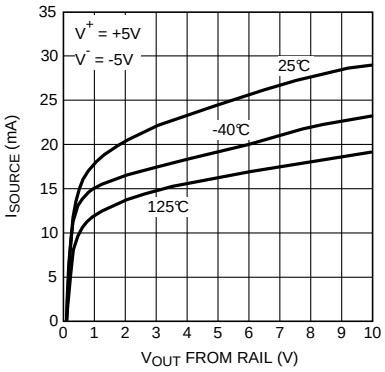


Figure 27. Sourcing Current vs V_{OUT}

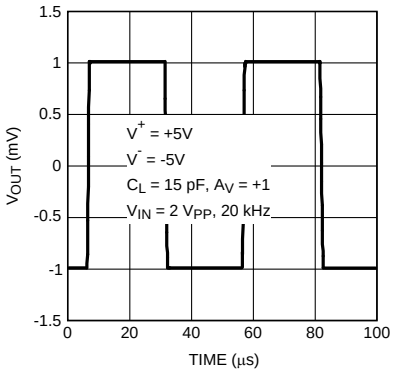


Figure 28. Large-Signal Transient

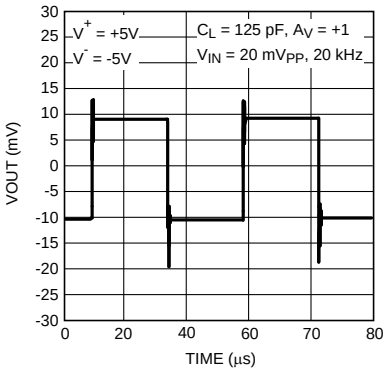


Figure 29. Small-Signal Transient Response

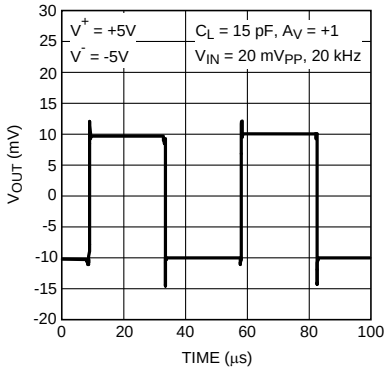


Figure 30. Small-Signal Transient Response

Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^+ = 10 V, V^- = 0 V, V_{CM} = V_S/2.

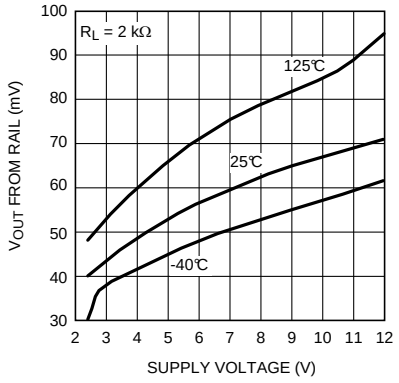


Figure 31. Output Swing High vs Supply Voltage

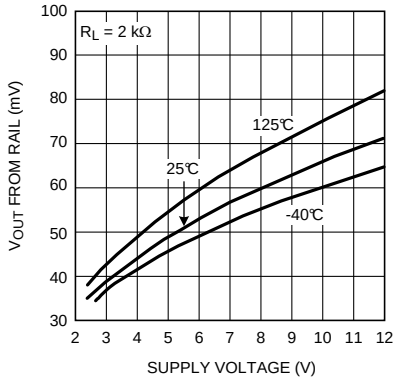


Figure 32. Output Swing Low vs Supply voltage

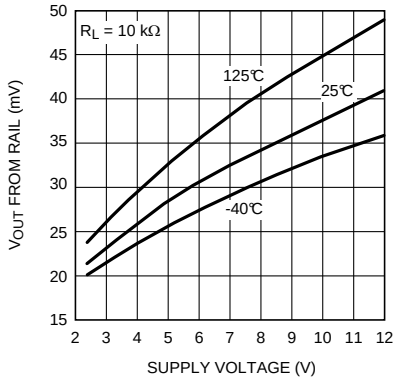


Figure 33. Output Swing High vs Supply Voltage

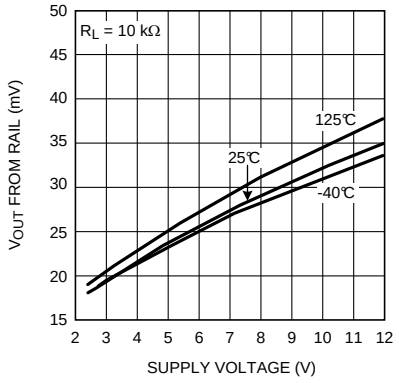


Figure 34. Output Swing Low and Supply Voltage

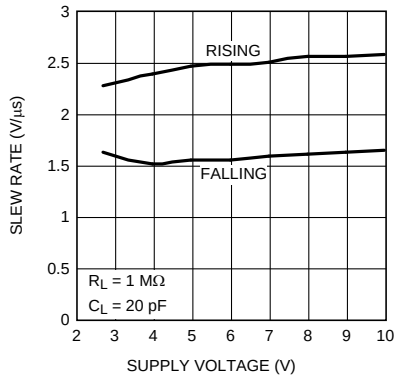


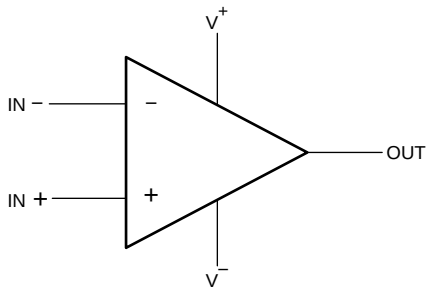
Figure 35. Slew Rate vs Supply Voltage

7 Detailed Description

7.1 Overview

The LMV641 is a wide-bandwidth, low-power operational amplifier with an extended power supply voltage range of 2.7 V to 12 V. The device is unity-gain stable with a 10 MHz of gain bandwidth product. Operating on a typical supply current of 138 µA, it provides a PSRR of 105 dB, CMRR of 120 dB, V_{OS} of 500 µV, input referred voltage noise of 14 nV/√Hz, and a THD of 0.002%. This amplifier has a rail-to-rail output stage and a common mode input voltage which includes the negative supply.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Low-Voltage and Low-Power Operation

The LMV641 has performance guaranteed at supply voltages of 2.7 V and 10 V. It is ensured to be operational at all supply voltages between 2.7 V and 12 V. The LMV641 draws a low supply current of 138 µA. The LMV641 provides the low-voltage and low-power amplification, which is essential for portable applications.

7.3.2 Wide Bandwidth

Despite drawing the very low supply current of 138 µA, the LMV641 manages to provide a wide unity gain bandwidth of 10 MHz. This is easily one of the best bandwidth to power ratios ever achieved, and allows this op amp to provide wideband amplification while using the minimum amount of power. This makes the LMV641 ideal for low power signal processing applications such as portable media players and other accessories.

7.3.3 Low Input Referred Noise

The LMV641 provides a flatband input referred voltage noise density of 14 nV/√Hz, which is significantly better than the noise performance expected from a low-power op amp. This op amp also feature exceptionally low 1/f noise, with a very low 1/f noise corner frequency of 4 Hz. Because of this the LMV641 is ideal for low-power applications which require decent noise performance, such as PDAs and portable sensors.

7.3.4 Ground Sensing and Rail-to-Rail Output

The LMV641 has a rail-to-rail output stage, which provides the maximum possible output dynamic range. This is especially important for applications requiring a large output swing. The input common mode range of this part includes the negative supply rail which allows direct sensing at ground in a single supply operation.

7.3.5 Small Size

The small footprint of the packages for the LMV641 saves space on printed-circuit boards, and enables the design of smaller and more compact electronic products. Long traces between the signal source and the op amp make the signal path susceptible to noise. By using a physically smaller package, these op amps can be placed closer to the signal source, reducing noise pickup and enhancing signal integrity.

7.4 Device Functional Modes

7.4.1 Stability of Op Amp Circuits

If the phase margin of the LMV641 is plotted with respect to the capacitive load (C_L) at its output, and if C_L is increased beyond 100 pF then the phase margin reduces significantly. This is because the op amp is designed to provide the maximum bandwidth possible for a low supply current. Stabilizing the LMV641 for higher capacitive loads would have required either a drastic increase in supply current, or a large internal compensation capacitance, which would have reduced the bandwidth. Hence, if this device is to be used for driving higher capacitive loads, it will have to be externally compensated.

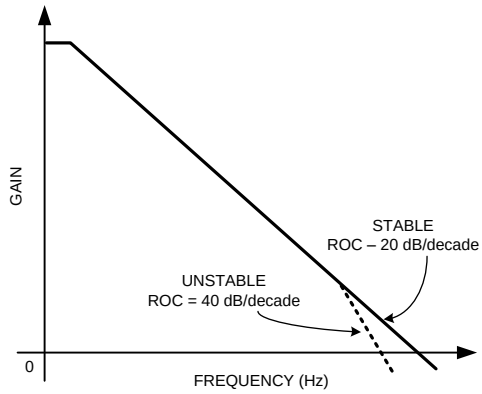


Figure 36. Gain vs Frequency for an Op Amp

An op amp, ideally, has a dominant pole close to DC which causes its gain to decay at the rate of 20 dB/decade with respect to frequency. If this rate of decay, also known as the rate of closure (ROC), remains the same until the op amp's unity gain bandwidth, then the op amp is stable. If, however, a large capacitance is added to the output of the op amp, it combines with the output impedance of the op amp to create another pole in its frequency response before its unity gain frequency (Figure 36). This increases the ROC to 40 dB/decade and causes instability.

In such a case, a number of techniques can be used to restore stability to the circuit. The idea behind all these schemes is to modify the frequency response such that it can be restored to an ROC of 20 dB/decade, which ensures stability.

7.4.1.1 In The Loop Compensation

Figure 37 illustrates a compensation technique, known as *in the loop* compensation, that employs an RC feedback circuit within the feedback loop to stabilize a non-inverting amplifier configuration. A small series resistance, R_S, is used to isolate the amplifier output from the load capacitance, C_L, and a small capacitance, C_F, is inserted across the feedback resistor to bypass C_L at higher frequencies.

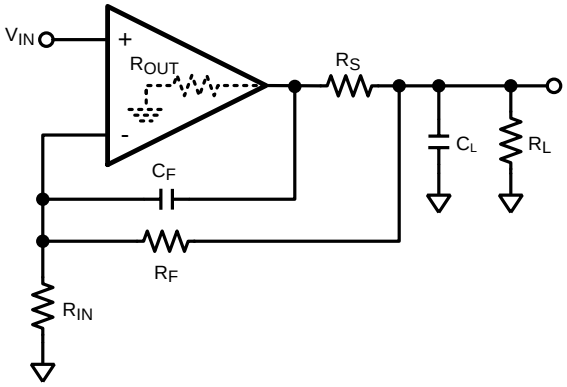


Figure 37. In the Loop Compensation

Device Functional Modes (continued)

The values for R_S and C_F are decided by ensuring that the zero attributed to C_F lies at the same frequency as the pole attributed to C_L. This ensures that the effect of the second pole on the transfer function is compensated for by the presence of the zero, and that the ROC is maintained at 20 dB/ decade. For the circuit shown in Figure 37 the values of R_S and C_F are given by Equation 1. Values of R_S and C_F required for maintaining stability for different values of C_L, as well as the phase margins obtained, are shown in Table 1. R_F and R_{IN} are 10 kΩ, R_L is 2 kΩ, while R_{OUT} is 680Ω.

$$R_S = \frac{R_{OUT}R_{IN}}{R_F}$$

$$C_F = \left(\frac{R_F + 2R_{IN}}{R_F^2}\right) C_L R_{OUT} \quad (1)$$

Table 1. Loop Compensation Stability

C_L (nF)	R_S (Ω)	C_F (pF)	PHASE MARGIN (°)
0.5	680	10	17.4
1	680	20	12.4
1.5	680	30	10.1

The LMV641 is capable of driving heavy capacitive loads of up to 1 nF without oscillating, however it is recommended to use compensation should the load exceed 1 nF. Using this methodology will reduce any excessive ringing and help maintain the phase margin for stability. The values of the compensation network tabulated above illustrate the phase margin degradation as a function of the capacitive load.

Although this methodology provides circuit stability for any load capacitance, it does so at the price of bandwidth. The closed loop bandwidth of the circuit is now limited by R_F and C_F.

7.4.1.2 Compensation by External Resistor

In some applications it is essential to drive a capacitive load without sacrificing bandwidth. In such a case, in the loop compensation is not viable. A simpler scheme for compensation is shown in Figure 38. A resistor, R_{ISO}, is placed in series between the load capacitance and the output. This introduces a zero in the circuit transfer function, which counteracts the effect of the pole formed by the load capacitance, and ensures stability. The value of R_{ISO} to be used should be decided depending on the size of C_L and the level of performance desired. Values ranging from 5Ω to 50Ω are usually sufficient to ensure stability. A larger value of R_{ISO} will result in a system with less ringing and overshoot, but will also limit the output swing and the short circuit current of the circuit.

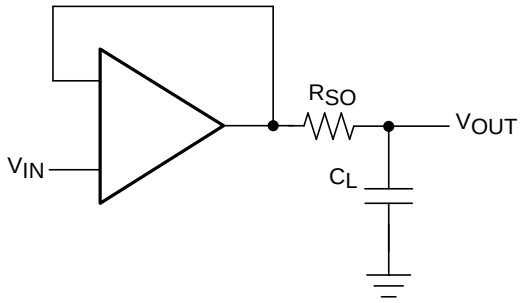


Figure 38. Compensation by Isolation Resistor

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMV641 is a low-power, low noise, wide-bandwidth operational amplifier with an extended power supply voltage range of 2.7 V to 12 V. With 10 MHz of gain bandwidth, 14 nV/√Hz input referred noise, and supply current of 138 μA, the LMV641 is well suited for portable applications that require precision while amplifying at high gains.

8.2 Typical Applications

8.2.1 High-Gain, Low-Power Inverting Amplifiers

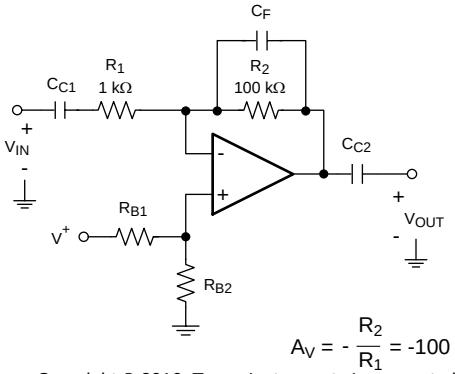


Figure 39. High-Gain Inverting Amplifier

8.2.1.1 Design Requirements

The wide unity-gain bandwidth allows these parts to provide large gain over a wide frequency range, while driving loads as low as 2 kΩ with less than 0.003% distortion.

8.2.1.2 Detailed Design Procedure

Figure 39 is an inverting amplifier, with a 100-kΩ feedback resistor, R_2, and a 1-kΩ input resistor, R_1, and provides a gain of −100. With the LMV641, these circuits can provide gain of −100 with a −3-dB bandwidth of 120 kHz, for a quiescent current as low as 116 μA. Coupling capacitors C_{C1} and C_{C2} can be added to isolate the circuit from DC voltages, while R_{B1} and R_{B2} provide DC biasing. A feedback capacitor C_F can also be added to improve compensation.

Typical Applications (continued)

8.2.1.3 Application Curve

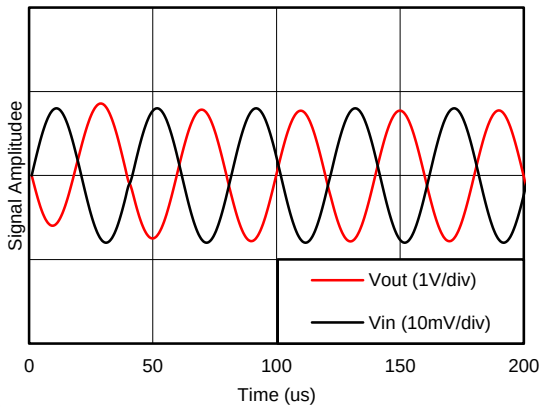


Figure 40. High Gain Inverting Amplifier Results

8.2.2 Anisotropic Magnetoresistive Sensor

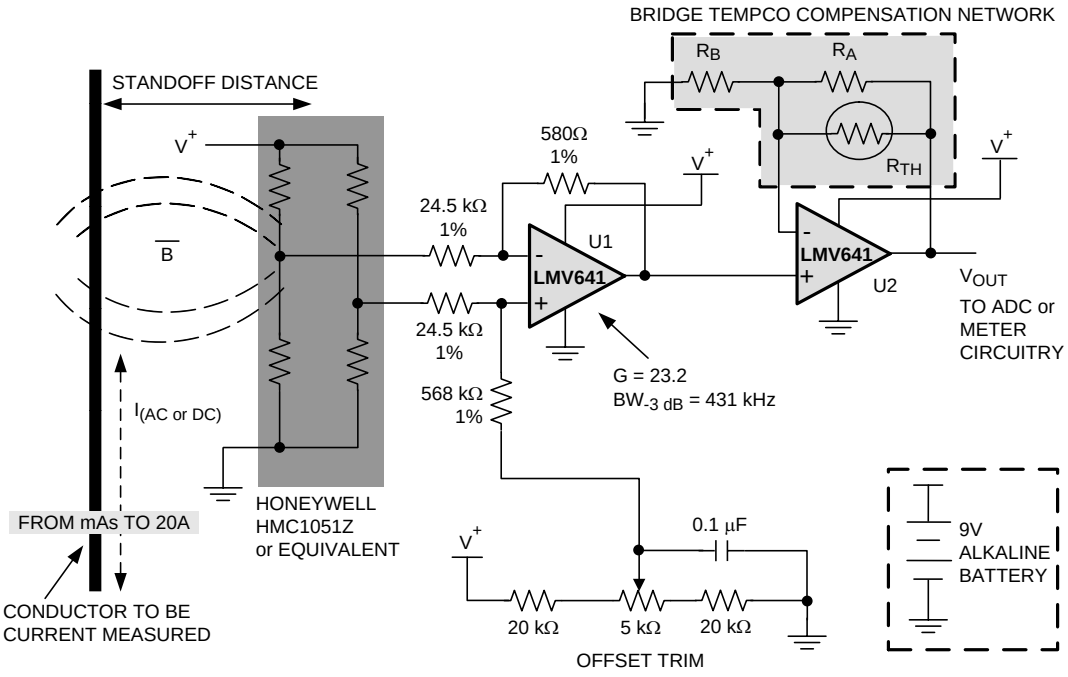


Figure 41. A Battery-Operated System for Contact-Less Current Sensing Using an Anisotropic Magnetoresistive Sensor

8.2.2.1 Design Requirements

The low operating current of the LMV641 makes it a good choice for battery-operated applications. Figure 41 shows two LMV641s in a portable application with a magnetic field sensor. The LMV641s condition the output from an anisotropic magnetoresistive (AMR) sensor. The sensor is arranged in the form of a Wheatstone bridge. This type of sensor can be used to accurately measure the current (either DC or AC) flowing in a wire by measuring the magnetic flux density, **B**, emanating from the wire.

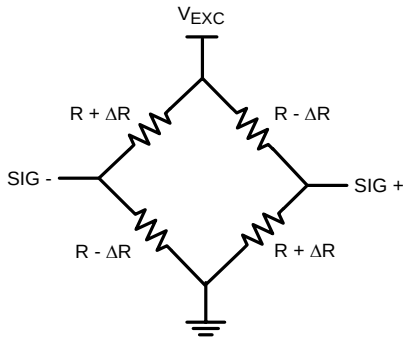
Typical Applications (continued)

8.2.2.2 Detailed Design Procedure

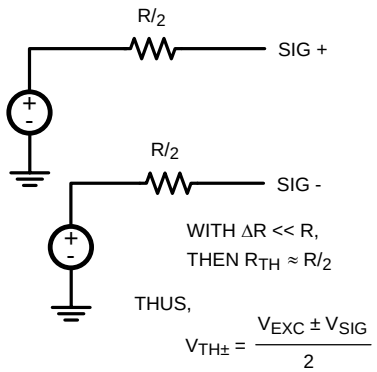
In this circuit, the use of a 9-V alkaline battery exploits the LMV641's high voltage and low supply current for a low-power, portable-current-sensing application. The sensor converts an incident magnetic field (through the magnetic flux linkage) in the sensitive direction, to a balanced voltage output. The LMV641 can be used for moderate to high current sensing applications (from a few milliamps and up to 20 A) using a nearby external conductor providing the sensed magnetic field to the bridge. The circuit shows a Honeywell HMC1051Z used as a current sensor. Note that the circuit must be calibrated based on the final displacement of the sensed conductor relative to the measurement bridge. Typically, once the sensor has been oriented properly, with respect to the conductor to be measured, the conductor can be placed about one centimeter away from the bridge and have reasonable capability of measuring from tens of milliamperes to beyond 20 amperes.

In Figure 41, U1 is configured as a single differential input amplifier. Its input impedance is relatively low, however, and requires that the source impedance of the sensor be considered in the gain calculations. Also, the asymmetrical loading on the bridge will produce a small offset voltage that can be cancelled out with the offset trim circuit shown in Figure 41.

Figure 42 shows a typical magnetoresistive Wheatstone bridge and the Thevenin equivalent of its resistive elements. As we shall see, the Thevenin equivalent model of the sensor is useful in calculating the gain needed in the differential amplifier.



(a)



(b)

Figure 42. Anisotropic Magnetoresistive Wheatstone Bridge Sensor, (a), and Thevenin Equivalent Circuit, (b)

Typical Applications (continued)

Using Thevenin's Theorem, the bridge can be reduced to two voltage sources with series resistances. ΔR is normally very small in comparison to R, thus the Thevenin equivalent resistance, commonly called the source resistance, can be taken to be R. When a bias voltage is applied between V_{EXC} and ground, in the absence of a magnetic field, all of the resistances are considered equal. The voltage at Sig+ and Sig− is half V_{EXC}, or 4.5 V, and Sig+ - Sig− = 0. Bridges are designed such that, when immersed in a magnetic field, opposite resistances in the bridge change by ±ΔR with an amount proportional to the strength of the magnetic field. This causes the bridge's output differential voltage, to change from its half V_{EXC} value. Thus Sig+ - Sig− = Vsig ≠ 0. With four active elements, the output voltage is:

$$V_{SIG} = V_{EXC} \times \frac{\Delta R}{R} \tag{2}$$

Because ΔR is proportional to the field strength, B_S, the amount of output voltage from the sensor is a function of sensor sensitivity, S. This expression can rewritten as , where

$$V_{SIG} = V_{EXC} \cdot S \cdot B_S \tag{3}$$

where

- S = material constant (nominally 1 mV/V/gauss)
- B_S = magnetic flux in gauss

A simplified schematic of a single op amp, differential amplifier is shown in Figure 43. The Thevenin equivalent circuit of the sensor can be used to calculate the gain of this amplifier.

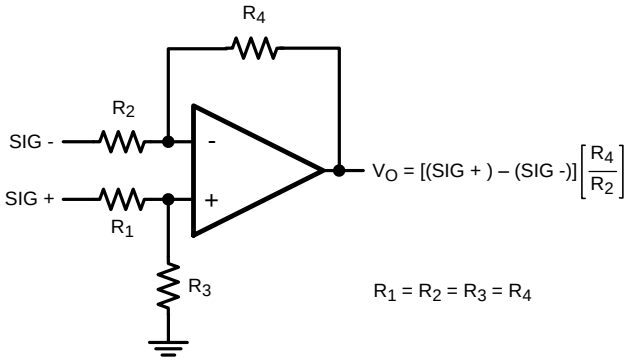


Figure 43. Differential Input Amplifier

The Honeywell HMC1051Z AMR sensor has nominal 1-kΩ elements and a sensitivity of 1 mV/V/gauss and is being used with 9 V of excitation with a full scale magnetic field range of ±6 gauss. At full-scale, the resistors will have ΔR ≈ 12 Ω and 108 mV will be seen from Sig− to Sig+ (see Figure 44).

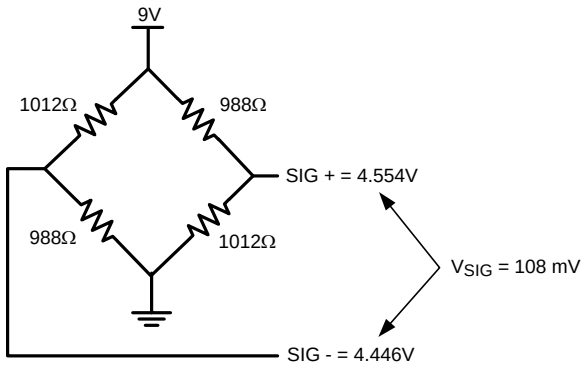


Figure 44. Sensor Output with No Load

Typical Applications (continued)

Referring to the simplified diagram in Figure 43, and assuming that required full scale at the output of the amplifier is 2.5 V, a gain of 23.2 is needed for U1. It is clear from the Thevenin equivalent circuit in Figure 45 that a sensor Thevenin equivalent source resistance, R_{THEV}, of 500 Ω will be in series with both the inverting and noninverting inputs of the LMV641. Therefore, the required gain is:

$$A_{VCL} = \frac{R_4}{R_{THEV} + R_2} = 23.2 \quad (4)$$

Choosing $R_1 = R_2 = 24.5$ kΩ, then R_4 will be approximately 580 kΩ. The actual values chosen will depend on the full-scale needs of the succeeding circuitry as well as bandwidth requirements. The values shown here provide a −3-dB bandwidth of approximately 431 kHz, and are found as follows.

$$BW_{-3\ dB} = \frac{\text{GAIN-BANDWIDTH PRODUCT}}{A_{VCL}} = \frac{10\ MHz}{23.2} = 431\ kHz$$

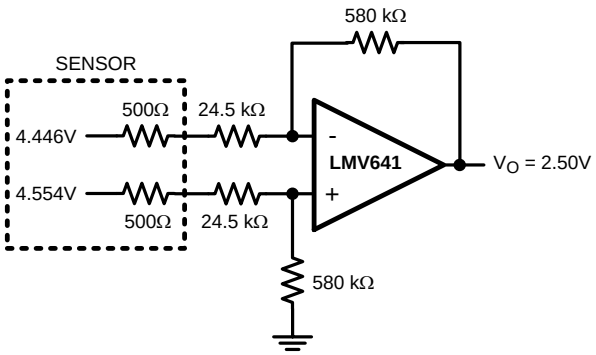


Figure 45. Thevenin Equivalent Showing Required Gain

By choosing input resistor values for R_1 and R_2 that are four to ten times the bridge element resistance, the bridge is minimally loaded and the offset errors induced by the op amp stages are minimized. These resistors should have 1% tolerance, or better, for the best noise rejection and offset minimization.

Referring once again to Figure 41, U2 is an additional gain stage with a thermistor element, R_{TH}, in the feedback loop. It performs a temperature compensation function for the bridge so that it will have greater accuracy over a wide range of operational temperatures. With mangetoresistive sensors, temperature drift of the bridge sensitivity is negative and linear, and in the case of the sensor used here, is nominally −3000 PP/M. Thus the gain of U2 needs to increase proportionally with increasing temperature, suggesting a thermistor with a positive temperature coefficient. Selection of the temperature compensation resistor, R_{TH}, depends on the additional gain required, on the thermistor chosen, and is dependent on the thermistor's %/°C shift in resistance. For best op amp compatibility, the thermistor resistance should be greater than 1000 Ω. R_{TH} should also be much less than R_A, the feedback resistor. Because the temperature coefficient of the AMR bridge is largely linear, R_{TH} also needs to behave in a linear fashion with temperature, thus R_A is placed in parallel with R_{TH}, which acts to linearize the thermistor.

8.2.2.2.1 Gain Error and Bandwidth Consideration if Using an Analog to Digital Converter

The bandwidth available from Figure 41 is dependent on the system closed loop gain required and the maximum gain-error allowed if driving an analog to digital converter (ADC). If the output from the sensor is intended to drive an ADC, the bandwidth will be considerably reduced from the closed-loop corner frequency. This is because the gain error of the pre-amplifier stage needs to be taken into account when calculating total error budget. Good practice dictates that the gain error of the amplifier be less than or equal to half LSB (preferably less in order to allow for other system errors that will eat up a portion of the available error budget) of the ADC. However, at the −3 dB corner frequency the gain error for any amplifier is 29.3%. In reality, the gain starts rolling off long before the −3 dB corner is reached. For example, if the amplifier is driving an 8-bit ADC, the minimum gain error allowed for half LSB would be approximately 0.2%. To achieve this gain error with the op amp, the maximum frequency of interest can be no higher than

Typical Applications (continued)

$$\sqrt{\frac{1}{\left(1 - \frac{1}{2^{n+1}}\right)^2} - 1} \times f_{-3\ dB}$$

where

- n is the bit resolution of the ADC
- $f_{-3\ dB}$ is the closed loop corner frequency. (5)

Given that the LMV641 has a GBW of 10 MHz, and is operating with a closed loop gain of 26.3, its closed loop bandwidth is 380 kHZ, therefore

$$\text{MAX FREQ} = \sqrt{\frac{1}{\left(1 - \frac{1}{2^{n+1}}\right)^2} - 1} = 0.062 \times f_{-3\ dB}$$

$$= 0.062 \times 380\ kHz = 23.56\ kHz \quad (6)$$

which is the highest frequency that can be measured with required accuracy.

8.2.3 Voiceband Filter

The majority of the energy of recognizable speech is within a band of frequencies between 200 Hz and 4 kHz. Therefore, it is beneficial to design circuits which transmit telephone signals that pass only certain frequencies and eliminate unwanted signals (noise) that could interfere with conversations and introduce error into control signals. The pass band of these circuits is defined as the ranges of frequencies that are passed. A telephone system voice frequency (VF) channel has a pass band of 0 Hz to 4 kHz. Specifically for human voices most of the energy content is found from 300 Hz to 3 kHz and any signal within this range is considered an in-band signal. Alternatively, any signal outside this range but within the VF channel is considered an out-of-band signal.

To properly recover a voice signal in applications such as cellular phones, cordless phones, and voice pagers, a low power bandpass filter that is matched to the human voice spectrum can be implemented using an LMV641 op amp. Figure 46 shows a multi-feedback, multi-pole filter (2^{nd} order response) with a gain of −1. The lower 3 dB cutoff frequency which is set by the DC blocking capacitor C_1 and resistor R_1 is 60 Hz and the upper cutoff frequency is 3.5 kHz.

The total current consumption is a mere 138 µA. The LV641 is operating with a gain of −1, but the circuit is easily modified to add gain. The op amp is powered from a single supply, hence the need for offset (common-mode) adjustment of its output, which is set to ½ V_S via its non-inverting input.

This filter is also useful in applications for battery operated talking toys and games.

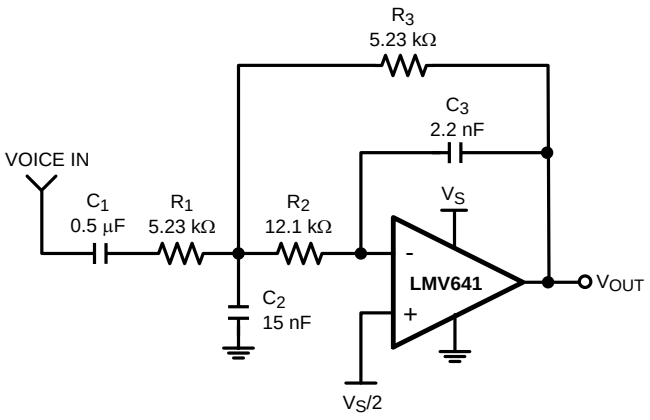


Figure 46. Low Power Voice In-Band Receive Filter for Battery-Powered Portable Use

9 Power Supply Recommendations

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines, TI recommends that 10-nF capacitors be placed as close as possible to the op amp power supply pins. For single supply, place a capacitor between V+ and V− supply leads. For dual supplies, place one capacitor between V+ and ground, and one capacitor between V– and ground.

10 Layout

10.1 Layout Guidelines

To properly bypass the power supply, several locations on a printed circuit board need to be considered. A 6.8 µF or greater tantalum capacitor should be placed at the point where the power supply for the amplifier is introduced onto the board. Another 0.1-µF ceramic capacitor should be placed as close as possible to the power supply pin of the amplifier. If the amplifier is operated in a single power supply, only the V+ pin needs to be bypassed with a 0.1-µF capacitor. If the amplifier is operated in a dual power supply, both V+ and V− pins need to be bypassed. It is good practice to use a ground plane on a printed-circuit board to provide all components with a low-inductive ground connection.

10.2 Layout Example

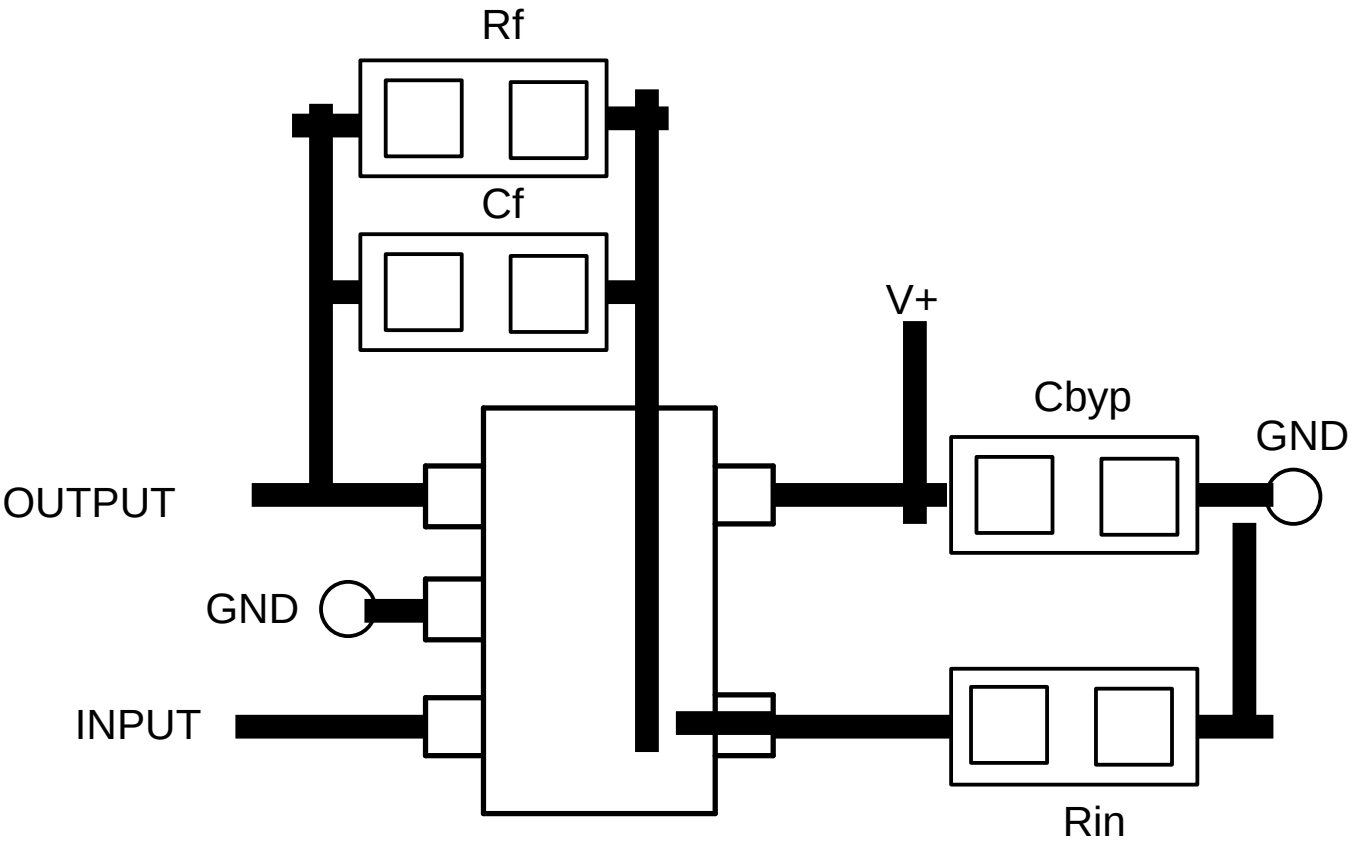


Figure 47. LMV641 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For development support see the following:

- LMV641 PSPICE Model
- TINA-TI SPICE-Based Analog Simulation Program
- DIP Adapter Evaluation Module
- TI Universal Operational Amplifier Evaluation Module
- TI Filterpro Software

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Absolute Maximum Ratings for Soldering* (SNOA549)
- AN-29 *IC Op Amp Beats FETs on Input Current* (SNOA624)
- AN-31 *Op Amp Circuit Collection* (SNLA140)
- AN-71 *Micropower Circuits Using the LM4250 Programmable Op Amp* (SNOA652)
- AN-127 *LM143 Monolithic High Voltage Operational Amplifier Applications* (SNVA516)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV641MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LMV64 1MA	Samples
LMV641MAE/NOPB	ACTIVE	SOIC	D	8	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LMV64 1MA	Samples
LMV641MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LMV64 1MA	Samples
LMV641MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM		AB9A	Samples
LMV641MFE/NOPB	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM		AB9A	Samples
LMV641MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM		AB9A	Samples
LMV641MG/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	A99	Samples
LMV641MGE/NOPB	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	A99	Samples
LMV641MGX/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	A99	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

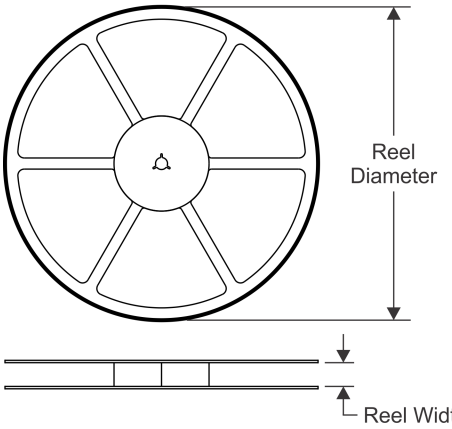
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

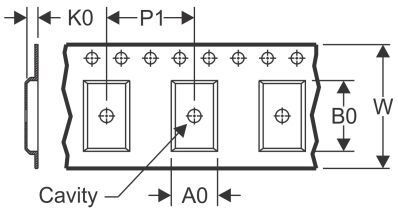
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

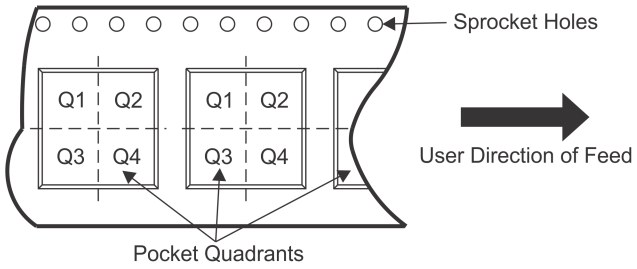


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

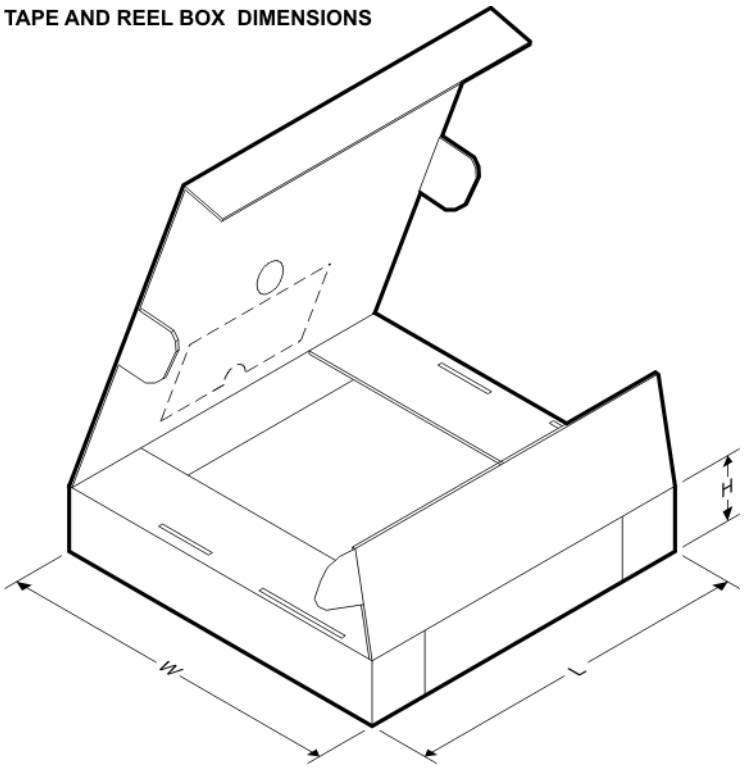
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV641MAE/NOPB	SOIC	D	8	250	178.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV641MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV641MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV641MFE/NOPB	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV641MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV641MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV641MGE/NOPB	SC70	DCK	5	250	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV641MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

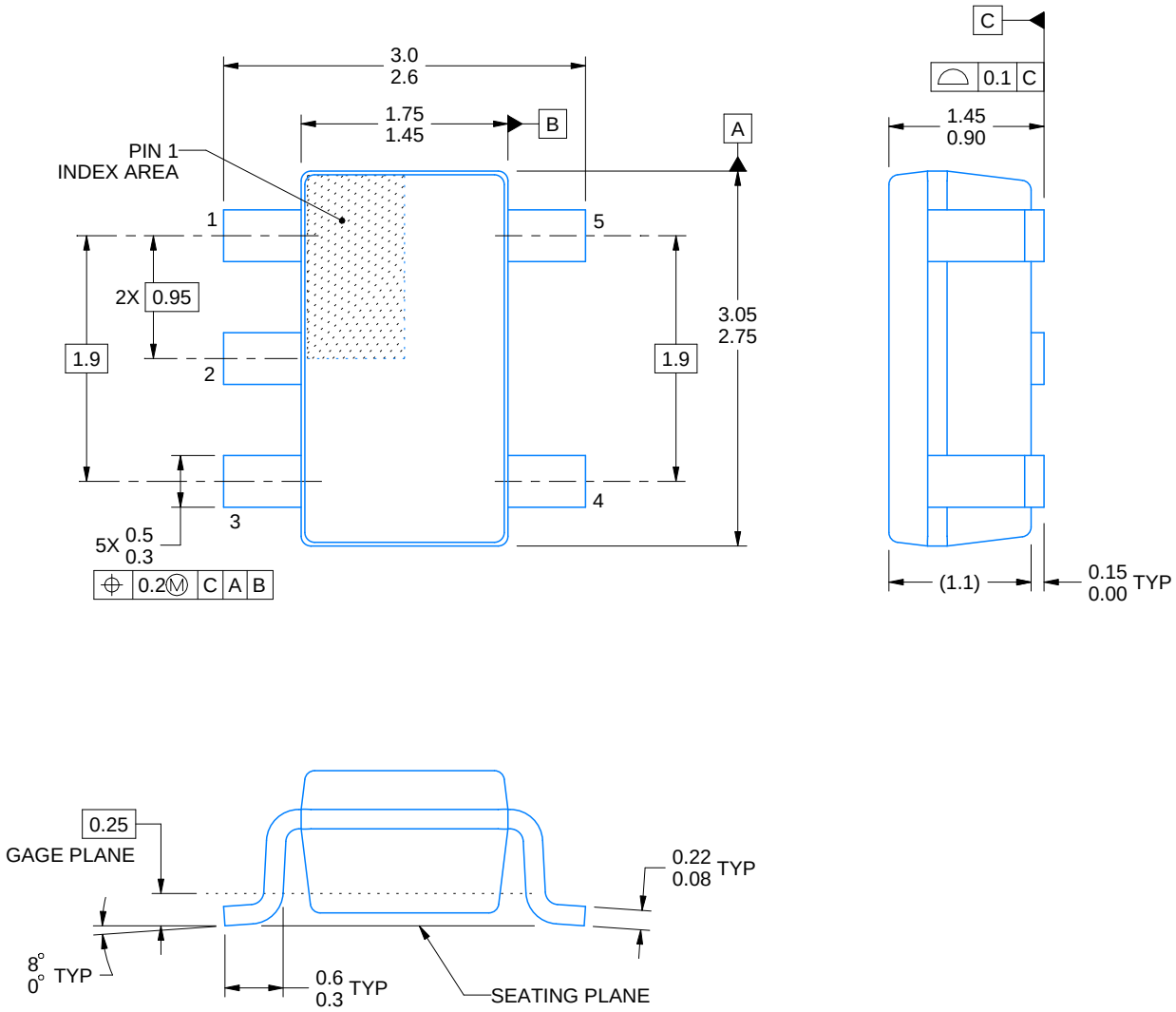
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV641MAE/NOPB	SOIC	D	8	250	210.0	185.0	35.0
LMV641MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV641MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV641MFE/NOPB	SOT-23	DBV	5	250	210.0	185.0	35.0
LMV641MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV641MG/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV641MGE/NOPB	SC70	DCK	5	250	210.0	185.0	35.0
LMV641MGX/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

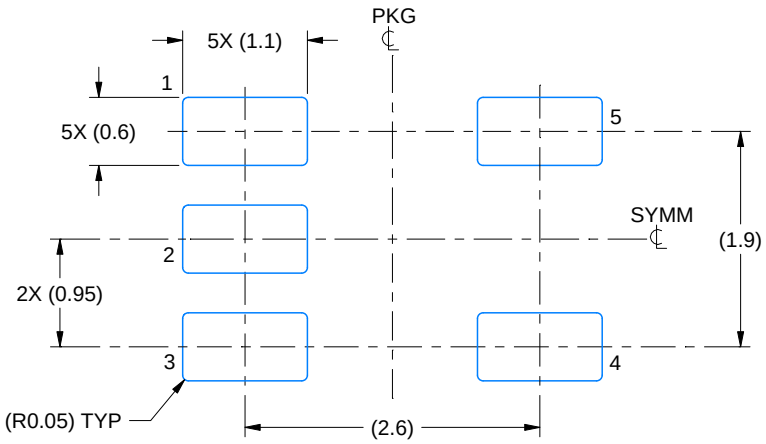
SMALL OUTLINE TRANSISTOR



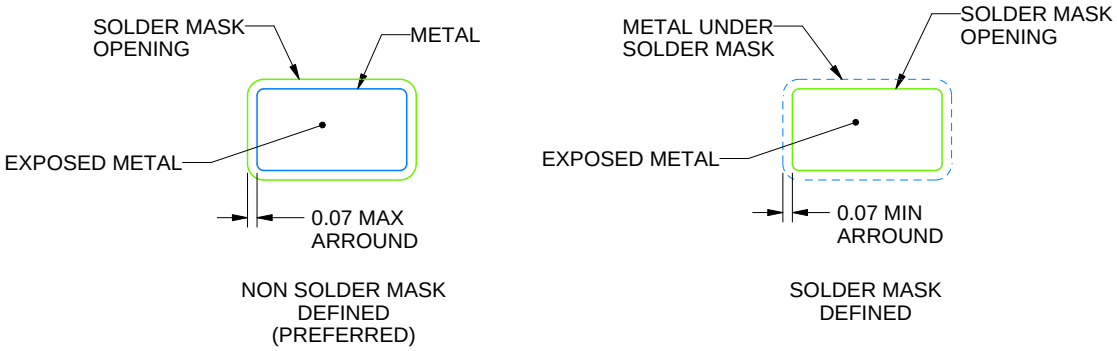
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

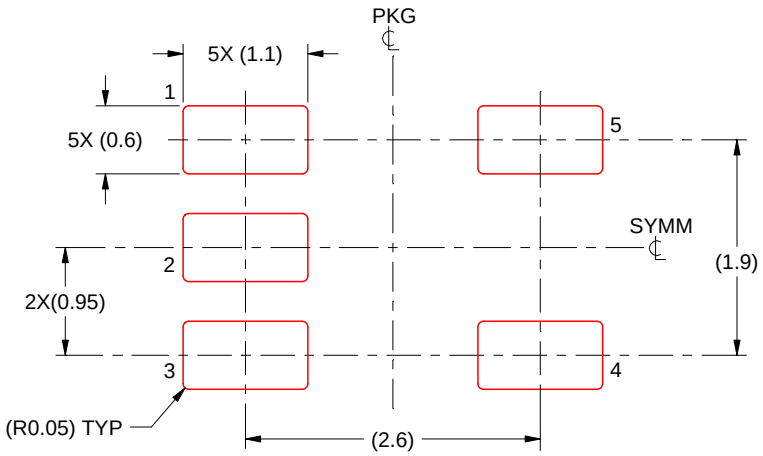


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

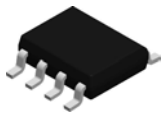


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

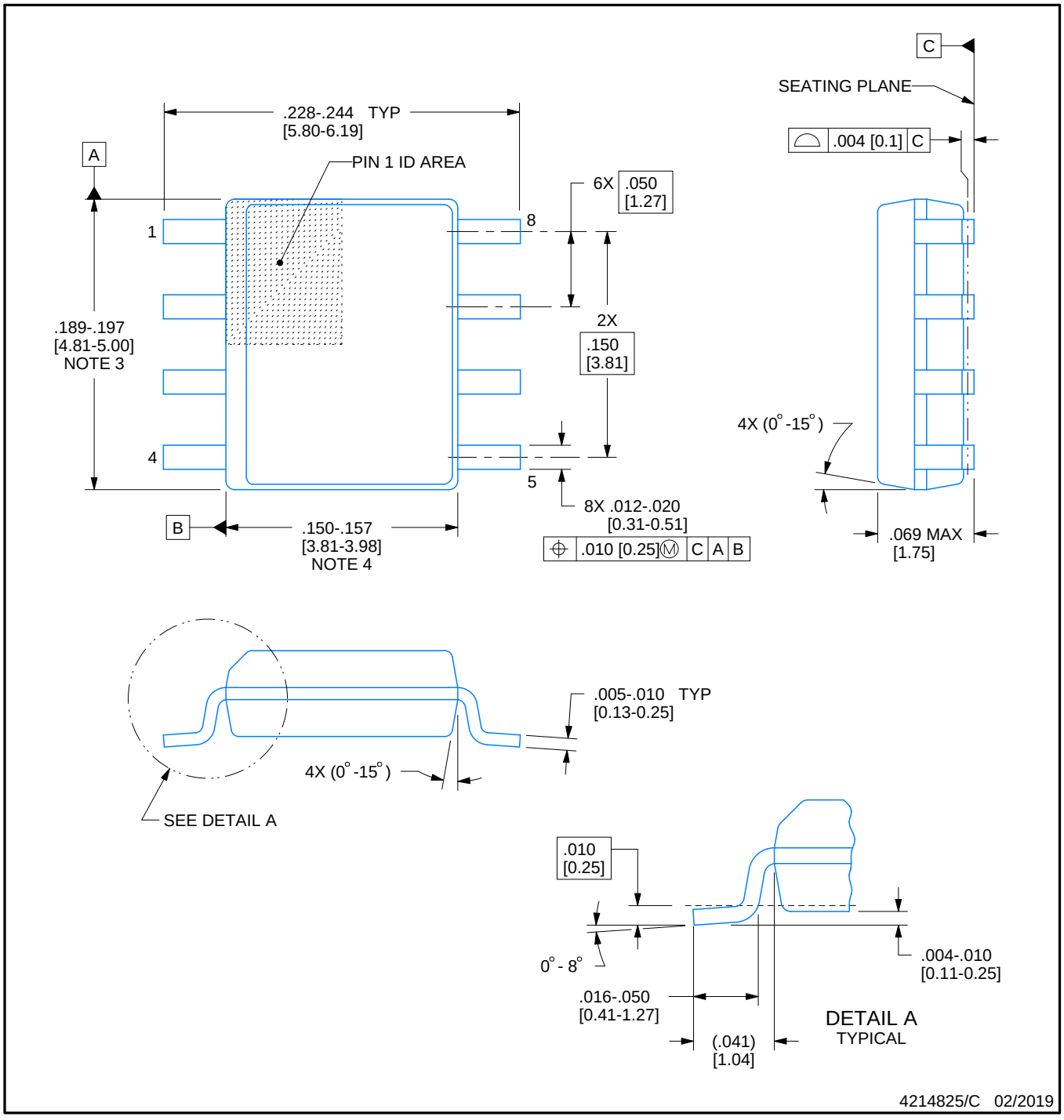


PACKAGE OUTLINE

D0008A

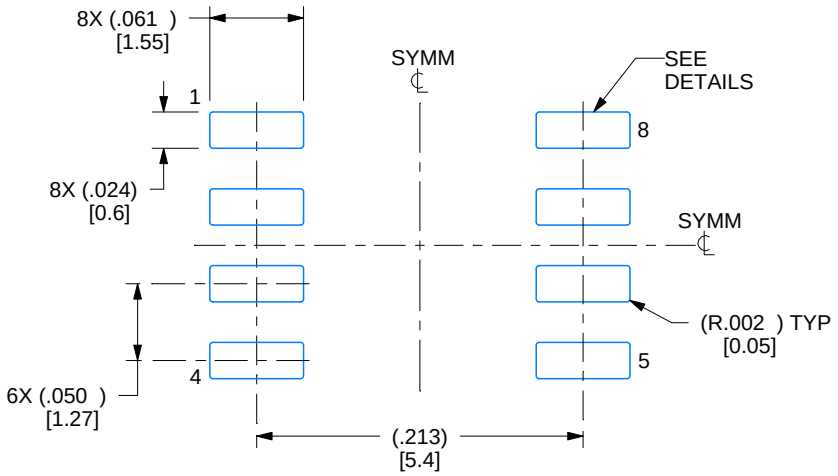
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

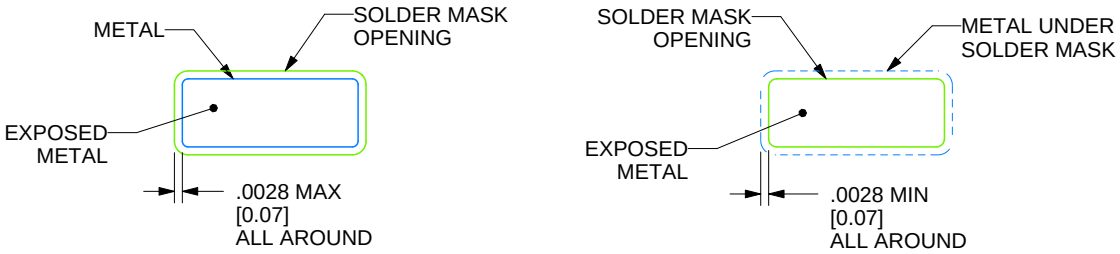


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

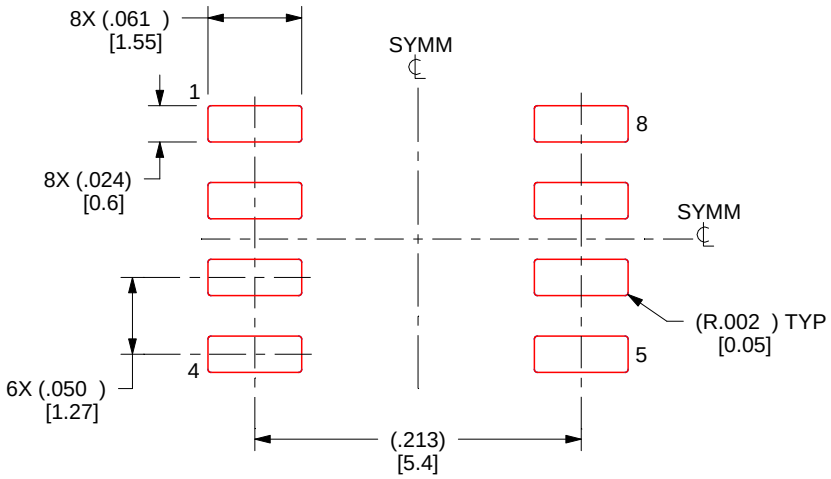
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



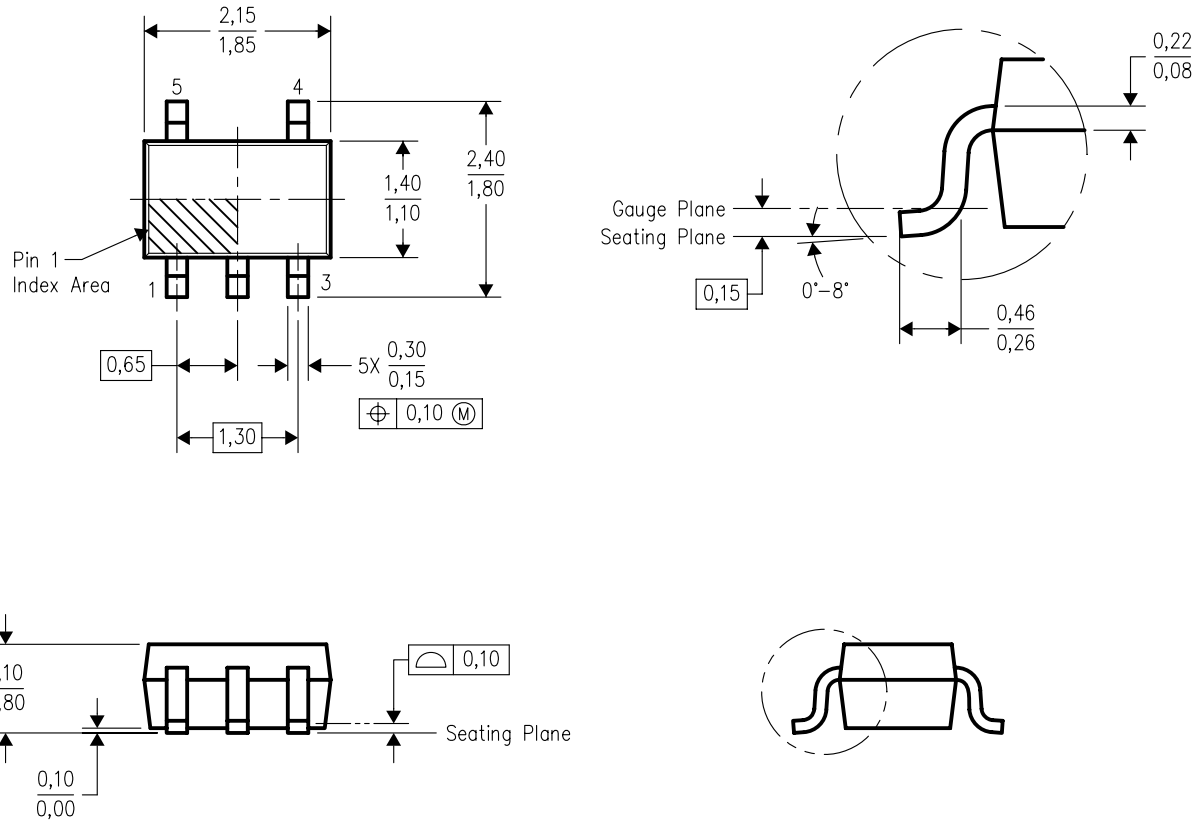
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

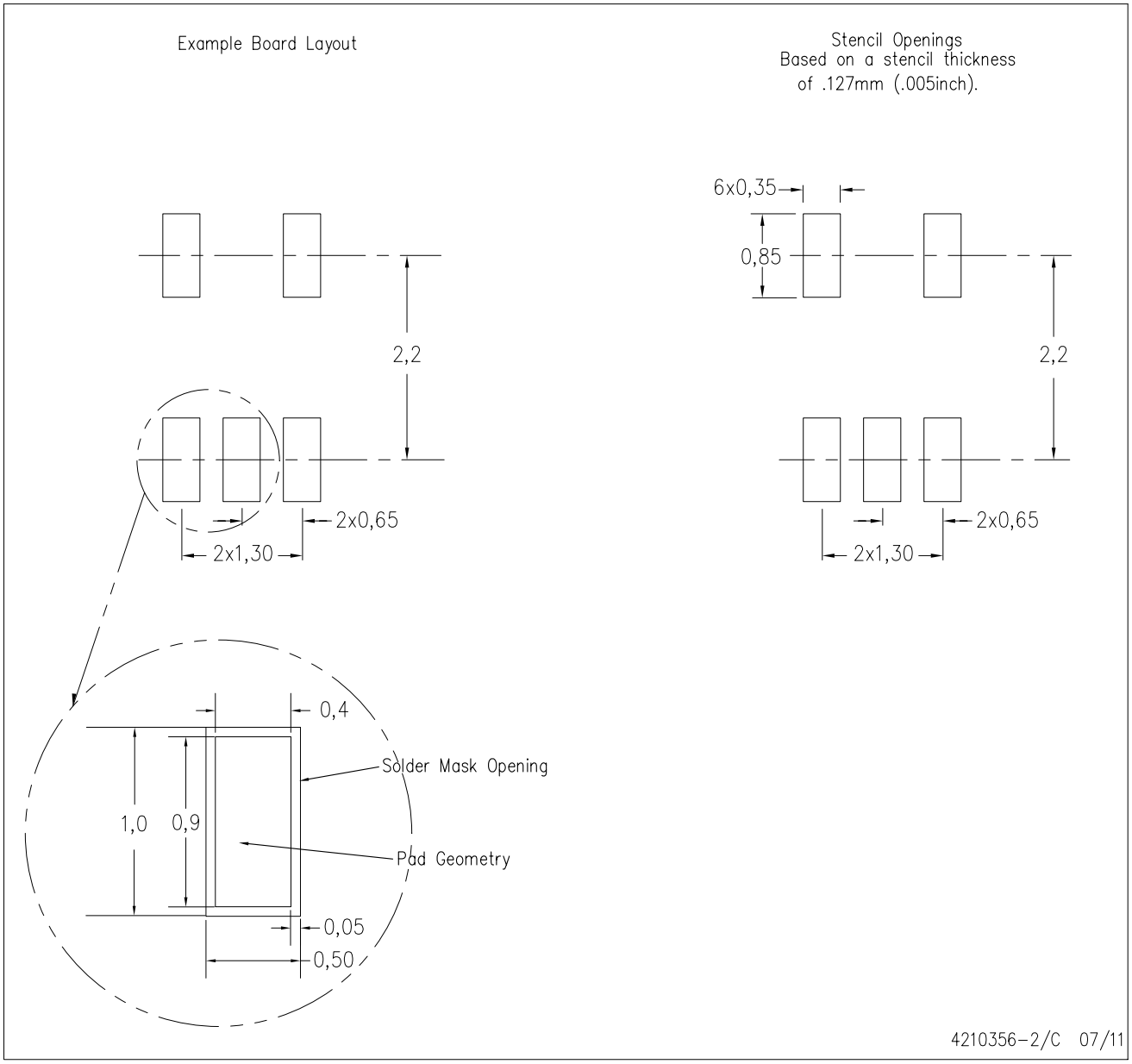
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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