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**THIS SPEC IS OBSOLETE**

Spec No: 38-05356

Spec Title: CY7C1461AV33/CY7C1463AV33, 36-MBIT (1M X 36/2M X 18)  
FLOW-THROUGH SRAM WITH NOBL(TM) ARCHITECTURE

Replaced by: None

## 36-Mbit (1M × 36/2M × 18) Flow-Through SRAM with NoBL™ Architecture

### Features

- No Bus Latency™ (NoBL™) architecture eliminates dead cycles between write and read cycles
- Supports up to 133 MHz bus operations with zero wait states
  - Data is transferred on every clock
- Pin compatible and functionally equivalent to ZBT™ devices
- Internally self timed output buffer control to eliminate the need to use OE
- Registered inputs for flow through operation
- Byte write capability
- 3.3 V and 2.5 V I/O power supply
- Fast clock-to-output times
  - 6.5 ns (for 133 MHz device)
- Clock Enable ( $\overline{CEN}$ ) pin to enable clock and suspend operation
- Synchronous self timed writes
- Asynchronous Output Enable
- CY7C1461AV33, CY7C1463AV33 available in JEDEC-standard Pb-free 100-pin TQFP package.
- Three chip enables for simple depth expansion
- Automatic power down feature available using ZZ mode or CE deselect
- Burst capability – linear or interleaved burst order
- Low standby power

### Functional Description

The CY7C1461AV33/CY7C1463AV33 are 3.3 V, 1M × 36/2M × 18 Synchronous Flow-Through Burst SRAMs designed specifically to support unlimited true back-to-back read and write operations without the insertion of wait states. The CY7C1461AV33/CY7C1463AV33 is equipped with the advanced NoBL logic required to enable consecutive read and write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data through the SRAM, especially in systems that require frequent write-read transitions.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable ( $\overline{CEN}$ ) signal, which when deasserted suspends operation and extends the previous clock cycle. Maximum access delay from the clock rise is 6.5 ns (133 MHz device).

Write operations are controlled by the two or four Byte Write Select ( $BW_x$ ) and a Write Enable ( $\overline{WE}$ ) input. All writes are conducted with on-chip synchronous self timed write circuitry.

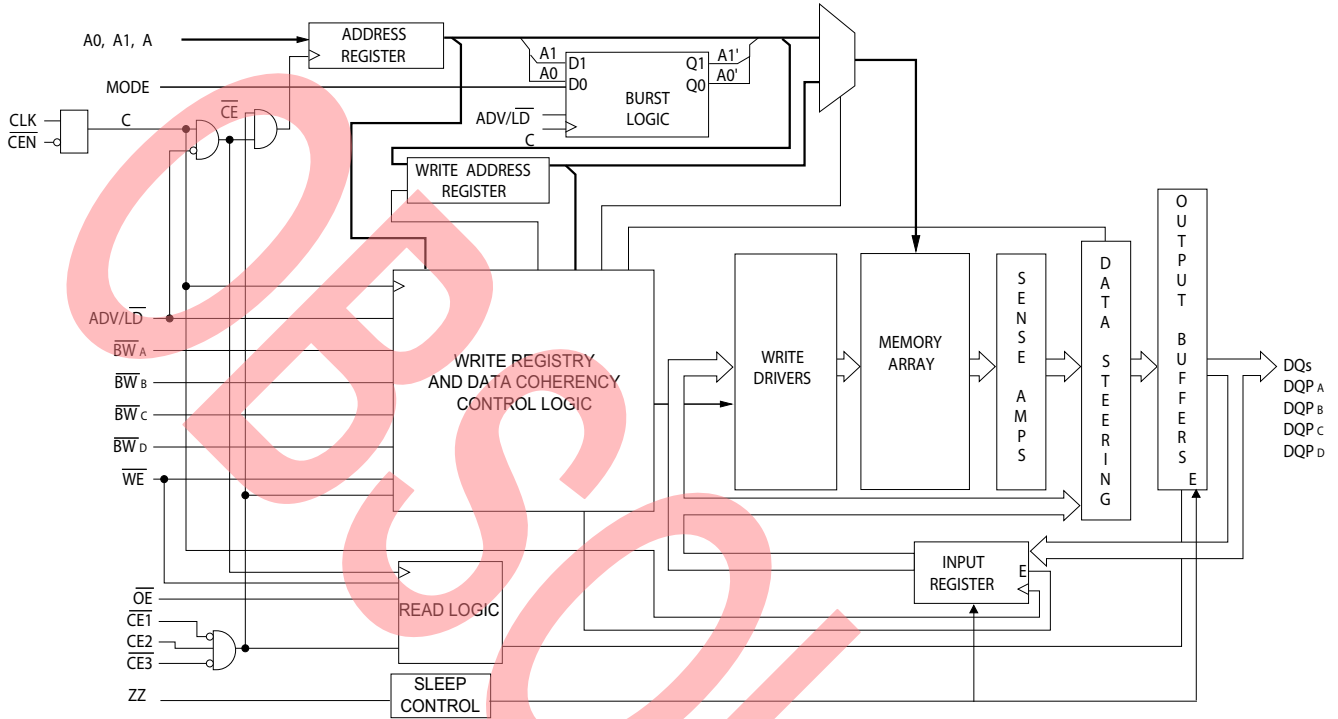
Three synchronous Chip Enables ( $\overline{CE}_1$ ,  $\overline{CE}_2$ ,  $\overline{CE}_3$ ) and an asynchronous Output Enable ( $\overline{OE}$ ) provide for easy bank selection and output tri-state control. To avoid bus contention, the output drivers are synchronously tri-stated during the data portion of a write sequence.

For a complete list of related documentation, click [here](#).

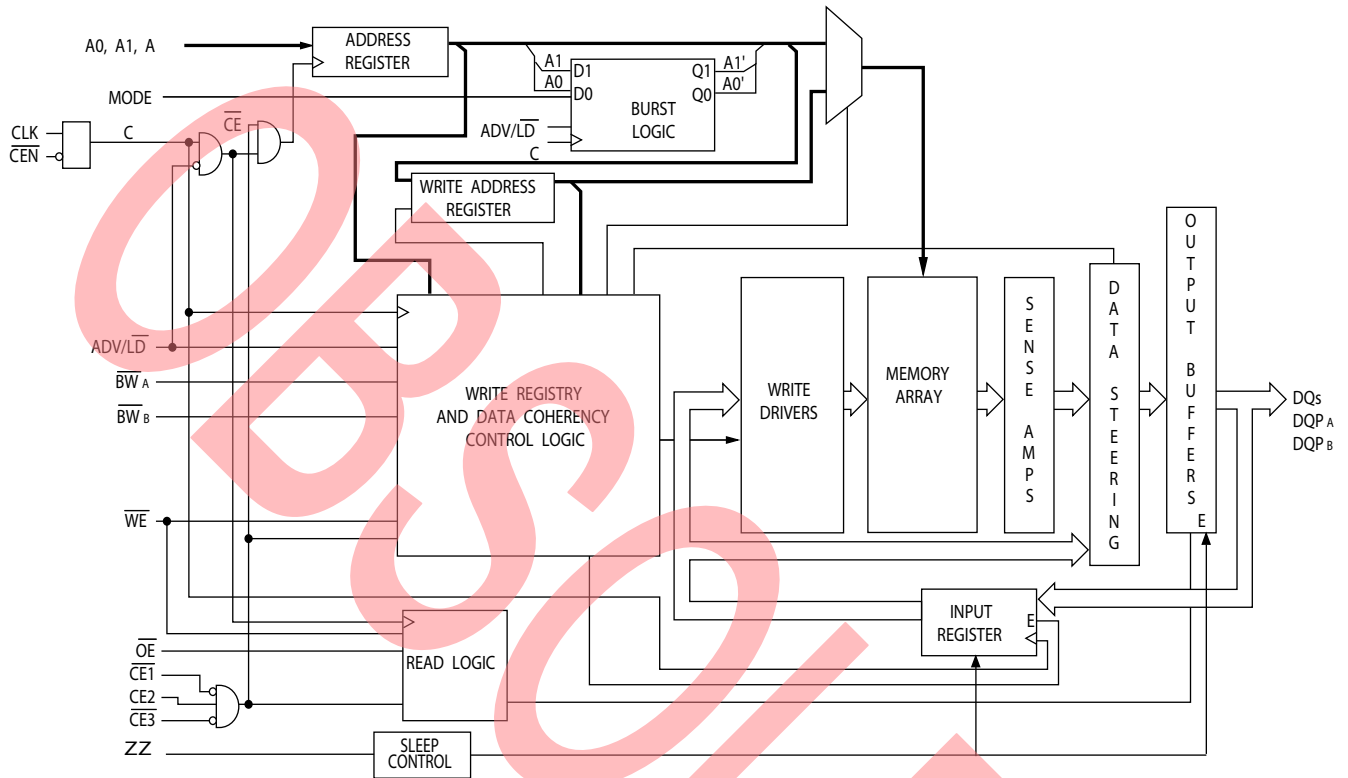
### Selection Guide

Description	133 MHz	Unit
Maximum Access Time	6.5	ns
Maximum Operating Current	310	mA
Maximum CMOS Standby Current	120	mA

**Logic Block Diagram – CY7C1461AV33**



**Logic Block Diagram – CY7C1463AV33**

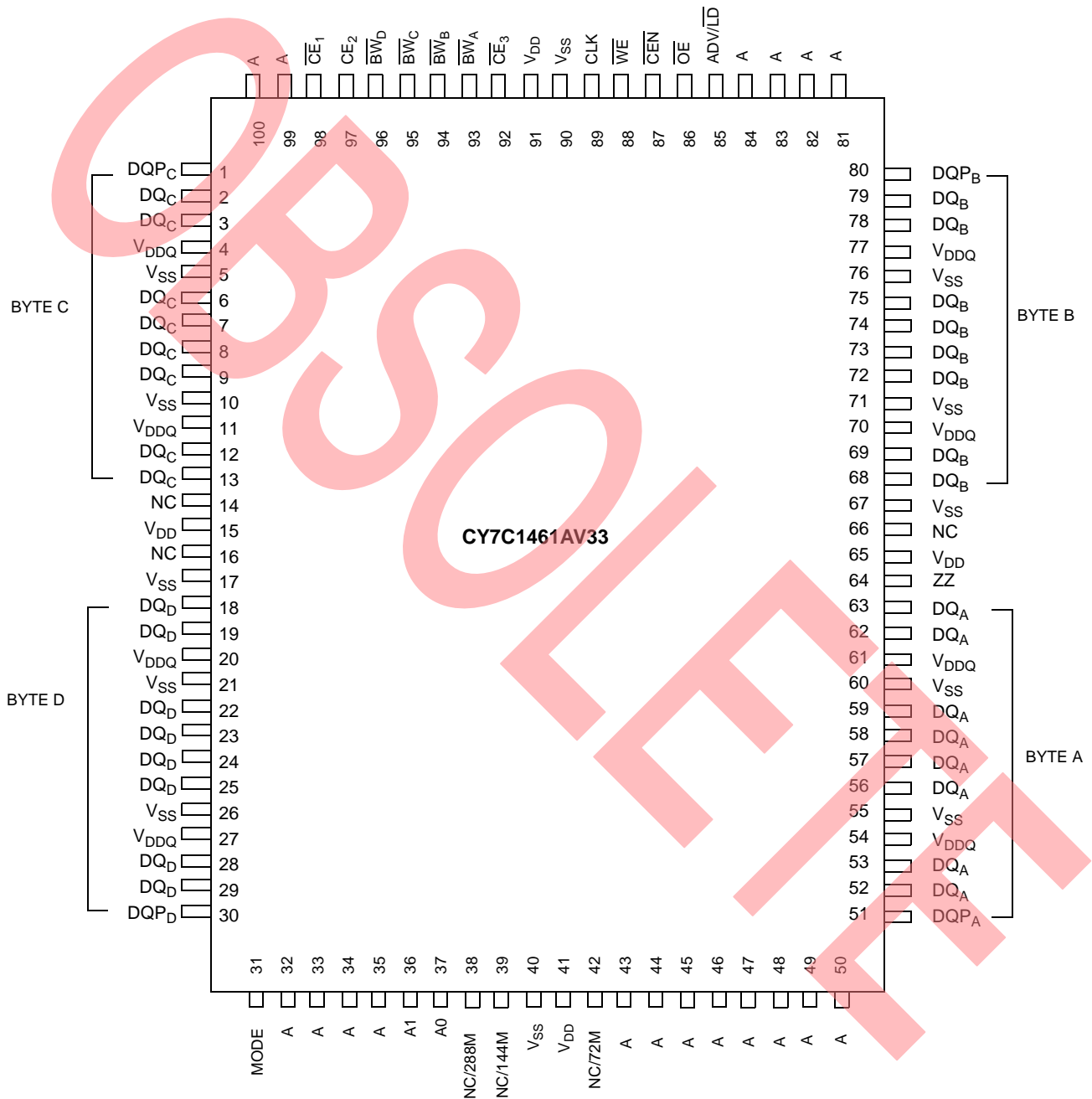


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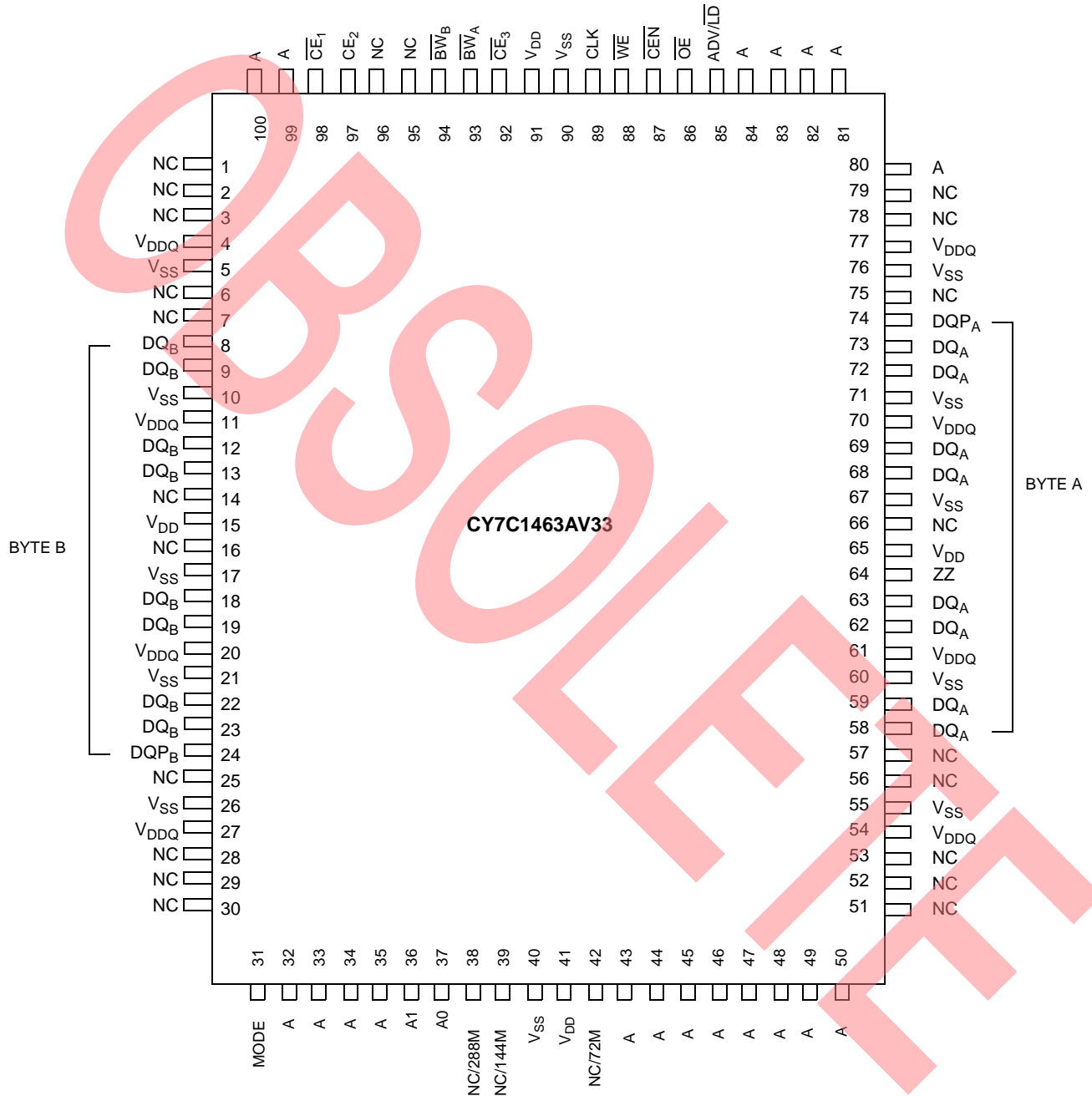
### Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout



**Pin Configurations** (continued)

**Figure 2. 100-pin TQFP (14 × 20 × 1.4 mm) pinout**





## Pin Definitions

Pin Name	I/O	Description
A <sub>0</sub> , A <sub>1</sub> , A	Input-Synchronous	<b>Address Inputs.</b> Used to select one of the address locations. Sampled at the rising edge of the CLK. A <sub>[1:0]</sub> are fed to the two-bit burst counter.
$\overline{BW}_A$ , $\overline{BW}_B$ , $\overline{BW}_C$ , $\overline{BW}_D$	Input-Synchronous	<b>Byte Write Inputs, Active LOW.</b> Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{WE}$	Input-Synchronous	<b>Write Enable Input, Active LOW.</b> Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/LD	Input-Synchronous	<b>Advance or Load Input.</b> Used to advance the on-chip address counter or load a new address. When HIGH (and CEN is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After deselection, drive ADV/LD LOW to load a new address.
CLK	Input-Clock	<b>Clock Input.</b> Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$ . CLK is only recognized if CEN is active LOW.
$\overline{CE}_1$	Input-Synchronous	<b>Chip Enable 1 Input, Active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_2$ and $\overline{CE}_3$ to select or deselect the device.
$\overline{CE}_2$	Input-Synchronous	<b>Chip Enable 2 Input, Active HIGH.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select or deselect the device.
$\overline{CE}_3$	Input-Synchronous	<b>Chip Enable 3 Input, Active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_2$ to select or deselect the device.
$\overline{OE}$	Input-Asynchronous	<b>Output Enable, Asynchronous Input, Active LOW.</b> Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected.
$\overline{CEN}$	Input-Synchronous	<b>Clock Enable Input, Active LOW.</b> When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Because deasserting $\overline{CEN}$ does not deselect the device, use CEN to extend the previous cycle when required.
ZZ	Input-Asynchronous	<b>ZZ “Sleep” Input.</b> This active HIGH input places the device in a non time critical sleep condition with data integrity preserved. During normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull down.
DQ <sub>s</sub>	I/O-Synchronous	<b>Bidirectional Data I/O lines.</b> As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ . When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ <sub>s</sub> and DQP <sub>[A:D]</sub> are placed in a tri-state condition. The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$ .
DQP <sub>x</sub>	I/O-Synchronous	<b>Bidirectional Data Parity I/O Lines.</b> Functionally, these signals are identical to DQ <sub>s</sub> . During write sequences, DQP <sub>x</sub> is controlled by $\overline{BW}_x$ correspondingly.
MODE	Input Strap Pin	<b>Mode Input.</b> Selects the burst order of the device. When tied to Gnd selects linear burst sequence. When tied to V <sub>DD</sub> or left floating selects interleaved burst sequence.
V <sub>DD</sub>	Power Supply	<b>Power Supply Inputs to the Core of the Device.</b>
V <sub>DDQ</sub>	I/O Power Supply	<b>Power Supply for I/O Circuitry.</b>
V <sub>SS</sub>	Ground	<b>Ground for the Device.</b>
NC	N/A	<b>No Connects.</b> Not internally connected to the die.
NC/72M	N/A	<b>Not Connected to the Die.</b> Can be tied to any voltage level.
NC/144M	N/A	<b>Not Connected to the Die.</b> Can be tied to any voltage level.
NC/288M	N/A	<b>Not Connected to the Die.</b> Can be tied to any voltage level.

## Pin Definitions (continued)

Pin Name	I/O	Description
NC/576M	N/A	<b>Not Connected to the Die.</b> Can be tied to any voltage level.
NC/1G	N/A	<b>Not Connected to the Die.</b> Can be tied to any voltage level.

## Functional Overview

The CY7C1461AV33/CY7C1463AV33 is a synchronous flow through burst SRAM designed specifically to eliminate wait states during Write-Read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the clock enable input signal (CEN). If CEN is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with CEN. Maximum access delay from the clock rise ( $t_{CDV}$ ) is 6.5 ns (133 MHz device).

Accesses can be initiated by asserting all three chip enables ( $\overline{CE}_1$ ,  $\overline{CE}_2$ ,  $\overline{CE}_3$ ) active at the rising edge of the clock. If CEN is active LOW and  $\overline{ADV/LD}$  is asserted LOW, the address presented to the device is latched. The access can either be a read or write operation, depending on the status of the write enable ( $\overline{WE}$ ).  $\overline{BW}_X$  can be used to conduct byte write operations.

Write operations are qualified by the Write Enable ( $\overline{WE}$ ). All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous chip enables ( $\overline{CE}_1$ ,  $\overline{CE}_2$ ,  $\overline{CE}_3$ ) and an asynchronous output enable ( $\overline{OE}$ ) simplify depth expansion. All operations (reads, writes, and deselections) are pipelined.  $\overline{ADV/LD}$  must be driven LOW after the device is deselected to load a new address for the next operation.

### Single Read Accesses

A read access is initiated when these conditions are satisfied at clock rise:

- $\overline{CEN}$  is asserted LOW
- $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$  are ALL asserted active
- The write enable input signal  $\overline{WE}$  is deasserted HIGH
- $\overline{ADV/LD}$  is asserted LOW

The address presented to the address inputs is latched into the address register and presented to the memory array and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the output buffers. The data is available within 6.5 ns (133 MHz device) provided  $\overline{OE}$  is active LOW. After the first clock of the read access, the output buffers are controlled by  $\overline{OE}$  and the internal control logic.  $\overline{OE}$  must be driven LOW for the device to drive out the requested data. On the subsequent clock, another operation (Read/Write/Deselect) can be initiated. When the SRAM is deselected at clock rise by one of the chip enable signals, its output is tri-stated immediately.

### Burst Read Accesses

The CY7C1461AV33/CY7C1463AV33 has an on-chip burst counter that provides the ability to supply a single address and conduct up to four reads without reasserting the address inputs.  $\overline{ADV/LD}$  must be driven LOW to load a new address into the

SRAM, as described in the [Single Read Accesses](#) section. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and wraps around when incremented sufficiently. A HIGH input on  $\overline{ADV/LD}$  increments the internal burst counter regardless of the state of chip enable inputs or  $\overline{WE}$ .  $\overline{WE}$  is latched at the beginning of a burst cycle. Therefore, the type of access (read or write) is maintained throughout the burst sequence.

### Single Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1) CEN is asserted LOW, (2)  $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$  are ALL asserted active, and (3) the write signal  $\overline{WE}$  is asserted LOW. The address presented to the address bus is loaded into the address register. The write signals are latched into the control logic block. The data lines are automatically tri-stated regardless of the state of the  $\overline{OE}$  input signal. This allows the external logic to present the data on DQs and  $\overline{DQP}_X$ .

On the next clock rise the data presented to DQs and  $\overline{DQP}_X$  (or a subset for byte write operations, see [Truth Table on page 10](#) for details) inputs is latched into the device and the write is complete. Additional accesses (read/write/deselect) can be initiated on this cycle.

The data written during the write operation is controlled by  $\overline{BW}_X$  signals. The CY7C1461AV33/CY7C1463AV33 provides byte write capability that is described in the truth table. Asserting the ( $\overline{WE}$ ) with the selected byte write select input selectively writes to only the desired bytes. Bytes not selected during a byte write operation remains unaltered. A synchronous self timed write mechanism is provided to simplify the write operations. Byte write capability is included to greatly simplify Read/Modify/Write sequences, which can be reduced to simple byte write operations.

Because the CY7C1461AV33/CY7C1463AV33 is a common I/O device, data must not be driven into the device when the outputs are active. The  $\overline{OE}$  can be deasserted HIGH before presenting data to the DQs and  $\overline{DQP}_X$  inputs. This tri-states the output drivers. As a safety precaution, DQs and  $\overline{DQP}_X$  are automatically tri-stated during the data portion of a write cycle, regardless of the state of  $\overline{OE}$ .

### Burst Write Accesses

The CY7C1461AV33/CY7C1463AV33 has an on-chip burst counter that provides the ability to supply a single address and conduct up to four write operations without reasserting the address inputs.  $\overline{ADV/LD}$  must be driven LOW to load the initial address, as described in the [Single Write Accesses on page 8](#). When  $\overline{ADV/LD}$  is driven HIGH on the subsequent clock rise, the chip enables ( $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$ ) and  $\overline{WE}$  inputs are ignored and the burst counter is incremented. The correct  $\overline{BW}_X$  inputs must be driven in each cycle of the burst write, to write the correct bytes of data.

### Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation sleep mode. Two clock cycles are required to enter into or exit from this sleep mode. When in this mode, data integrity is guaranteed. Accesses pending when entering the sleep mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the sleep mode. CE<sub>1</sub>, CE<sub>2</sub>, and CE<sub>3</sub>, must remain inactive for the duration of t<sub>ZZREC</sub> after the ZZ input returns LOW.

### Interleaved Burst Address Table

(MODE = Floating or V<sub>DD</sub>)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

### Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

### ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I <sub>DDZZ</sub>	Sleep mode standby current	ZZ ≥ V <sub>DD</sub> - 0.2 V	–	100	mA
t <sub>ZZS</sub>	Device operation to ZZ	ZZ ≥ V <sub>DD</sub> - 0.2 V	–	2t <sub>CYC</sub>	ns
t <sub>ZZREC</sub>	ZZ recovery time	ZZ ≤ 0.2 V	2t <sub>CYC</sub>	–	ns
t <sub>ZZI</sub>	ZZ active to sleep current	This parameter is sampled	–	2t <sub>CYC</sub>	ns
t <sub>RZZI</sub>	ZZ Inactive to exit sleep current	This parameter is sampled	0	–	ns

## Truth Table

The truth table for CY7C1461AV33/CY7C1463AV33 follows.

Operation [1, 2, 3, 4, 5, 6, 7]	Address Used	$\overline{CE}_1$	$CE_2$	$\overline{CE}_3$	ZZ	$\overline{ADV/LD}$	$\overline{WE}$	$\overline{BW}_x$	$\overline{OE}$	$\overline{CEN}$	CLK	DQ
Deselect Cycle	None	H	X	X	L	L	X	X	X	L	L->H	Tristate
Deselect Cycle	None	X	X	H	L	L	X	X	X	L	L->H	Tristate
Deselect Cycle	None	X	L	X	L	L	X	X	X	L	L->H	Tristate
Continue Deselect Cycle	None	X	X	X	L	H	X	X	X	L	L->H	Tristate
Read Cycle (Begin Burst)	External	L	H	L	L	L	H	X	L	L	L->H	Data Out (Q)
Read Cycle (Continue Burst)	Next	X	X	X	L	H	X	X	L	L	L->H	Data Out (Q)
NOP/Dummy Read (Begin Burst)	External	L	H	L	L	L	H	X	H	L	L->H	Tristate
Dummy Read (Continue Burst)	Next	X	X	X	L	H	X	X	H	L	L->H	Tristate
Write Cycle (Begin Burst)	External	L	H	L	L	L	L	L	X	L	L->H	Data In (D)
Write Cycle (Continue Burst)	Next	X	X	X	L	H	X	L	X	L	L->H	Data In (D)
NOP/Write Abort (Begin Burst)	None	L	H	L	L	L	L	H	X	L	L->H	Tristate
Write Abort (Continue Burst)	Next	X	X	X	L	H	X	H	X	L	L->H	Tristate
Ignore Clock Edge (Stall)	Current	X	X	X	L	X	X	X	X	H	L->H	-
Sleep Mode	None	X	X	X	H	X	X	X	X	X	X	Tristate

### Notes

1. X = "Don't Care." H = logic HIGH, L = logic LOW.  $\overline{BW}_x = L$  signifies at least one byte write select is active,  $\overline{BW}_x = Valid$  signifies that the desired byte write selects are asserted, see truth table for details.
2. Write is defined by  $\overline{BW}_x$ , and  $\overline{WE}$ . See truth table for read or write.
3. When a write cycle is detected, all IOs are tristated, even during byte writes.
4. The DQs and  $\overline{DQP}_x$  pins are controlled by the current cycle and the  $\overline{OE}$  signal.  $\overline{OE}$  is asynchronous and is not sampled with the clock.
5.  $\overline{CEN} = H$ , inserts wait states.
6. Device powers up deselected and the IOs in a tri-state condition, regardless of  $\overline{OE}$ .
7.  $\overline{OE}$  is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQs and  $\overline{DQP}_x = Tri-state$  when  $\overline{OE}$  is inactive or when the device is deselected, and DQs and  $\overline{DQP}_x = data$  when  $\overline{OE}$  is active.

**Truth Table for Read/Write**

Function (CY7C1461AV33) <sup>[8, 9]</sup>	$\overline{WE}$	$\overline{BW}_A$	$\overline{BW}_B$	$\overline{BW}_C$	$\overline{BW}_D$
Read	H	X	X	X	X
Write – No Bytes Written	L	H	H	H	H
Write Byte A – (DQ <sub>A</sub> and DQP <sub>A</sub> )	L	L	H	H	H
Write Byte B – (DQ <sub>B</sub> and DQP <sub>B</sub> )	L	H	L	H	H
Write Byte C – (DQ <sub>C</sub> and DQP <sub>C</sub> )	L	H	H	L	H
Write Byte D – (DQ <sub>D</sub> and DQP <sub>D</sub> )	L	H	H	H	L
Write All Bytes	L	L	L	L	L

**Truth Table for Read/Write**

Function (CY7C1463AV33) <sup>[8, 9]</sup>	$\overline{WE}$	$\overline{BW}_b$	$\overline{BW}_a$
Read	H	X	X
Write – No Bytes Written	L	H	H
Write Byte a – (DQ <sub>a</sub> and DQP <sub>a</sub> )	L	H	L
Write Byte b – (DQ <sub>b</sub> and DQP <sub>b</sub> )	L	L	H
Write Both Bytes	L	L	L

**Notes**

8. X = "Don't Care." H = logic HIGH, L = logic LOW.  $\overline{BW}_x = L$  signifies at least one byte write select is active,  $\overline{BW}_x = \text{Valid}$  signifies that the desired byte write selects are asserted, see truth table for details.
9. Table only lists a partial listing of the byte write combinations. Any combination of  $\overline{BW}_x$  is valid. Appropriate write is done based on which byte write is active.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65 °C to +150 °C  
 Ambient Temperature with Power Applied ..... -55 °C to +125 °C  
 Supply Voltage on V<sub>DD</sub> Relative to GND ..... -0.5 V to +4.6 V  
 Supply Voltage on V<sub>DDQ</sub> Relative to GND ..... -0.5 V to +V<sub>DD</sub>  
 DC Voltage Applied to Outputs in Tri-State ..... -0.5 V to V<sub>DDQ</sub> + 0.5 V

DC Input Voltage ..... -0.5 V to V<sub>DD</sub> + 0.5 V  
 Current into Outputs (LOW) ..... 20 mA  
 Static Discharge Voltage (MIL-STD-883, Method 3015) ..... > 2001 V  
 Latch Up Current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	V <sub>DD</sub>	V <sub>DDQ</sub>
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V <sub>DD</sub>
Industrial	-40 °C to +85 °C		

## Electrical Characteristics

Over the Operating Range

Parameter <sup>[10, 11]</sup>	Description	Test Conditions	Min	Max	Unit
V <sub>DD</sub>	Power supply voltage		3.135	3.6	V
V <sub>DDQ</sub>	I/O supply voltage	for 3.3 V I/O	3.135	V <sub>DD</sub>	V
		for 2.5 V I/O	2.375	2.625	V
V <sub>OH</sub>	Output HIGH voltage	for 3.3 V I/O, I <sub>OH</sub> = -4.0 mA	2.4	-	V
		for 2.5 V I/O, I <sub>OH</sub> = -1.0 mA	2.0	-	V
V <sub>OL</sub>	Output LOW voltage	for 3.3 V I/O, I <sub>OL</sub> = 8.0 mA	-	0.4	V
		for 2.5 V I/O, I <sub>OL</sub> = 1.0 mA	-	0.4	V
V <sub>IH</sub>	Input HIGH voltage <sup>[10]</sup>	for 3.3 V I/O	2.0	V <sub>DD</sub> + 0.3 V	V
		for 2.5 V I/O	1.7	V <sub>DD</sub> + 0.3 V	V
V <sub>IL</sub>	Input LOW voltage <sup>[10]</sup>	for 3.3 V I/O	-0.3	0.8	V
		for 2.5 V I/O	-0.3	0.7	V
I <sub>X</sub>	Input leakage current except ZZ and MODE	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub>	-5	5	μA
	Input current of MODE	Input = V <sub>SS</sub>	-30	-	μA
		Input = V <sub>DD</sub>	-	5	μA
	Input current of ZZ	Input = V <sub>SS</sub>	-5	-	μA
Input = V <sub>DD</sub>		-	30	μA	
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub> , Output Disabled	-5	5	μA
I <sub>DD</sub>	V <sub>DD</sub> operating supply current	V <sub>DD</sub> = Max, I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	-	310	mA
I <sub>SB1</sub>	Automatic CE power down current – TTL Inputs	V <sub>DD</sub> = Max, Device Deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> ; f = f <sub>MAX</sub> , Inputs Switching	-	180	mA
I <sub>SB2</sub>	Automatic CE power down current – CMOS Inputs	V <sub>DD</sub> = Max, Device Deselected, V <sub>IN</sub> ≤ 0.3 V or V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.3 V, f = 0, Inputs Static	-	120	mA
I <sub>SB3</sub>	Automatic CE power down current – CMOS Inputs	V <sub>DD</sub> = Max, Device Deselected, V <sub>IN</sub> ≤ 0.3 V or V <sub>IN</sub> ≥ V <sub>DDQ</sub> - 0.3 V, f = f <sub>MAX</sub> , Inputs Switching	-	180	mA
I <sub>SB4</sub>	Automatic CE Power down current – TTL Inputs	V <sub>DD</sub> = Max, Device Deselected, V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.3 V or V <sub>IN</sub> ≤ 0.3 V, f = 0, Inputs Static	-	135	mA

### Notes

10. Overshoot: V<sub>IH(AC)</sub> < V<sub>DD</sub> + 1.5 V (Pulse width less than t<sub>CYC</sub>/2), undershoot: V<sub>IL(AC)</sub> > -2 V (Pulse width less than t<sub>CYC</sub>/2).  
 11. T<sub>Power-up</sub>: Assumes a linear ramp from 0 V to V<sub>DD(min)</sub> within 200 ms. During this time V<sub>IH</sub> < V<sub>DD</sub> and V<sub>DDQ</sub> ≤ V<sub>DD</sub>.



## Capacitance

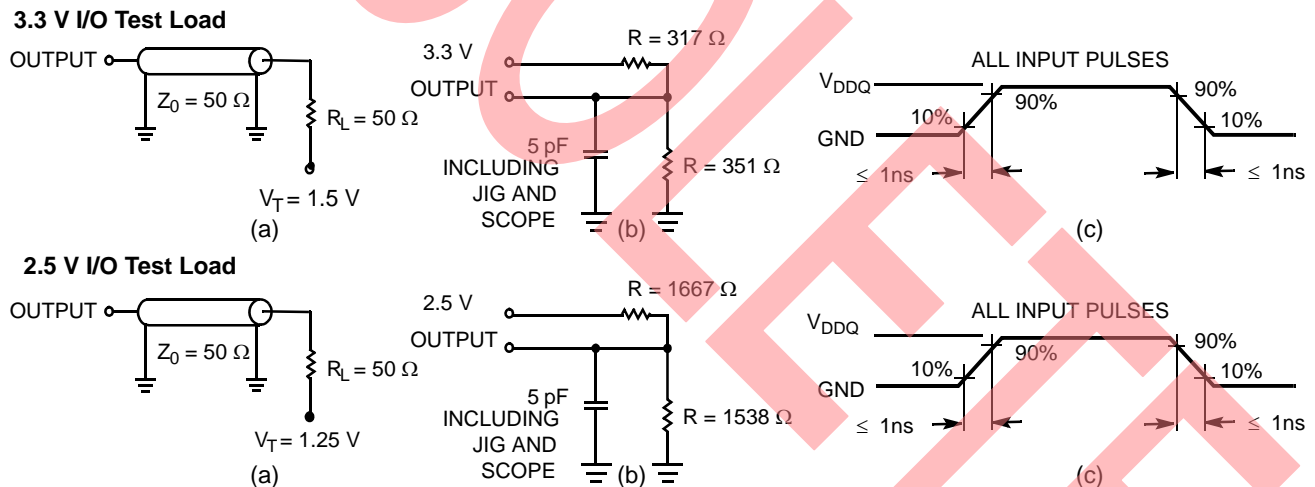
Parameter <sup>[12]</sup>	Description	Test Conditions	100-pin TQFP Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25\text{ }^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{DD} = 3.3\text{ V}$ , $V_{DDQ} = 2.5\text{ V}$	6.5	pF
$C_{CLK}$	Clock input capacitance		3	pF
$C_{IO}$	Input/Output capacitance		5.5	pF

## Thermal Resistance

Parameter <sup>[12]</sup>	Description	Test Conditions	100-pin TQFP Package	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA/JESD51.	25.21	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		2.28	$^\circ\text{C/W}$

## AC Test Loads and Waveforms

**Figure 3. AC Test Loads and Waveforms**



**Note**

12. Tested initially and after any design or process change that may affect these parameters.

## Switching Characteristics

Over the Operating Range

Parameter [13, 14]	Description	133 MHz		Unit
		Min	Max	
$t_{POWER}^{[15]}$		1	–	ms
<b>Clock</b>				
$t_{CYC}$	Clock Cycle Time	7.5	–	ns
$t_{CH}$	Clock HIGH	2.5	–	ns
$t_{CL}$	Clock LOW	2.5	–	ns
<b>Output Times</b>				
$t_{CDV}$	Data Output Valid after CLK Rise	–	6.5	ns
$t_{DOH}$	Data Output Hold after CLK Rise	2.5	–	ns
$t_{CLZ}$	Clock to Low Z [16, 17, 18]	2.5	–	ns
$t_{CHZ}$	Clock to High Z [16, 17, 18]	–	3.8	ns
$t_{OEV}$	$\overline{OE}$ LOW to Output Valid	–	3.0	ns
$t_{OELZ}$	$\overline{OE}$ LOW to Output Low Z [16, 17, 18]	0	–	ns
$t_{OEHZ}$	$\overline{OE}$ HIGH to Output High Z [16, 17, 18]	–	3.0	ns
<b>Setup Times</b>				
$t_{AS}$	Address Setup before CLK Rise	1.5	–	ns
$t_{ALS}$	ADV/LD Setup before CLK Rise	1.5	–	ns
$t_{WES}$	$\overline{WE}$ , $\overline{BW}_X$ Setup before CLK Rise	1.5	–	ns
$t_{CENS}$	$\overline{CEN}$ Setup before CLK Rise	1.5	–	ns
$t_{DS}$	Data Input Setup before CLK Rise	1.5	–	ns
$t_{CES}$	Chip Enable Setup before CLK Rise	1.5	–	ns
<b>Hold Times</b>				
$t_{AH}$	Address Hold after CLK Rise	0.5	–	ns
$t_{ALH}$	ADV/LD Hold after CLK Rise	0.5	–	ns
$t_{WEH}$	$\overline{WE}$ , $\overline{BW}_X$ Hold after CLK Rise	0.5	–	ns
$t_{CENH}$	$\overline{CEN}$ Hold after CLK Rise	0.5	–	ns
$t_{DH}$	Data Input Hold after CLK Rise	0.5	–	ns
$t_{CEH}$	Chip Enable Hold after CLK Rise	0.5	–	ns

### Notes

13. Timing reference level is 1.5 V when  $V_{DDQ} = 3.3$  V and is 1.25 V when  $V_{DDQ} = 2.5$  V.

14. Test conditions shown in (a) of Figure 3 on page 13 unless otherwise noted.

15. This part has a voltage regulator internally;  $t_{POWER}$  is the time that the power needs to be supplied above  $V_{DD(minimum)}$  initially, before a read or write operation can be initiated.

16.  $t_{CHZ}$ ,  $t_{CLZ}$ ,  $t_{OELZ}$ , and  $t_{OEHZ}$  are specified with AC test conditions shown in part (b) of Figure 3 on page 13. Transition is measured  $\pm 200$  mV from steady-state voltage.

17. At any voltage and temperature,  $t_{OEHZ}$  is less than  $t_{OELZ}$  and  $t_{CHZ}$  is less than  $t_{CLZ}$  to eliminate bus contention between SRAMs when sharing the same data bus.

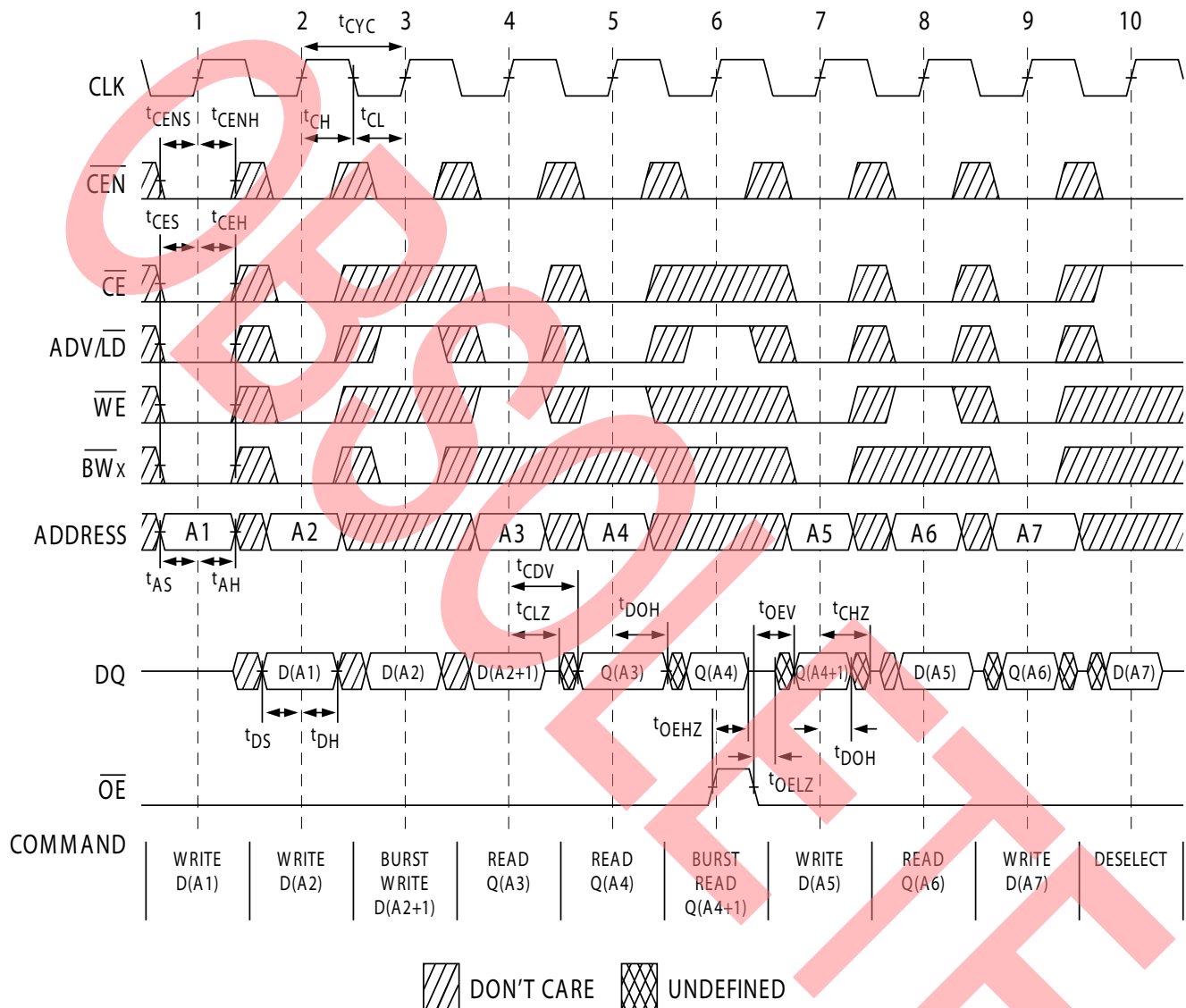
These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z prior to Low Z under the same system conditions.

18. This parameter is sampled and not 100% tested.



## Switching Waveforms

Figure 4. Read/Write Waveforms [19, 20, 21]



### Notes

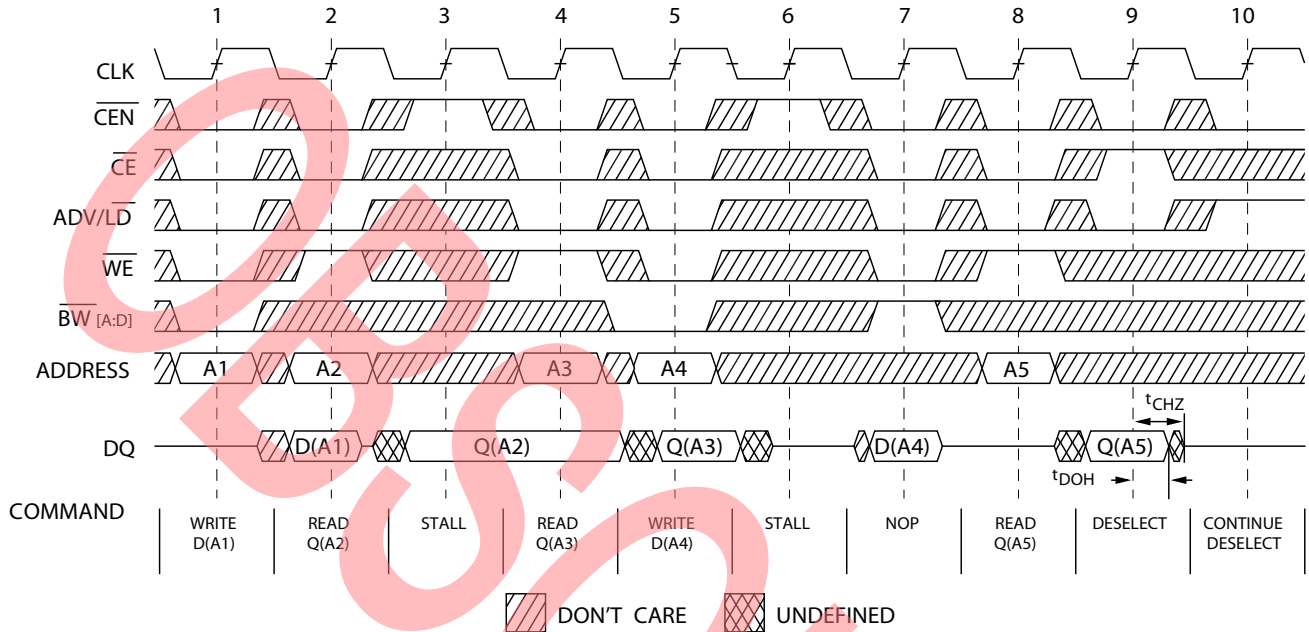
19. For this waveform ZZ is tied LOW.

20. When  $\overline{CE}$  is LOW,  $\overline{CE}_1$  is LOW,  $CE_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH,  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW or  $\overline{CE}_3$  is HIGH.

21. Order of the burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved). Burst operations are optional.

**Switching Waveforms** (continued)

**Figure 5. NOP, STALL, and DESELECT Cycles** [22, 23, 24]

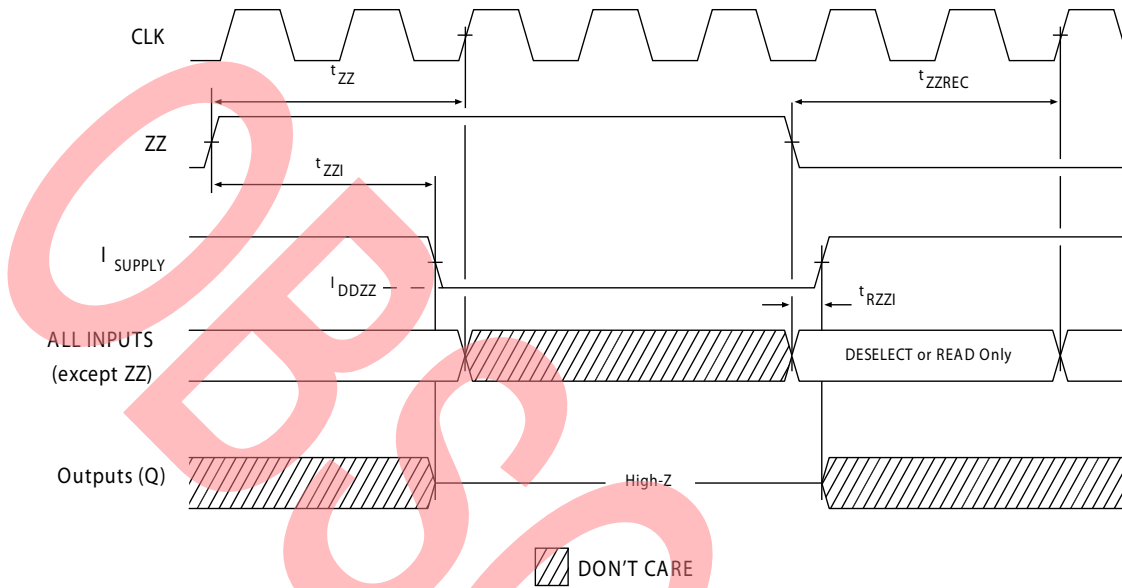


**Notes**

- 22. For this waveform  $\overline{ZZ}$  is tied LOW.
- 23. When  $\overline{CE}$  is LOW,  $\overline{CE}_1$  is LOW,  $\overline{CE}_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH,  $\overline{CE}_1$  is HIGH or  $\overline{CE}_2$  is LOW or  $\overline{CE}_3$  is HIGH.
- 24. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrates  $\overline{CEN}$  being used to create a pause. A write is not performed during this cycle.

Switching Waveforms (continued)

Figure 6. ZZ Mode Timing [25, 26]



Notes

- 25. Device must be deselected when entering ZZ mode. See truth table for all possible signal conditions to deselect the device.
- 26. DQs are in High Z when exiting ZZ sleep mode.

## Ordering Information

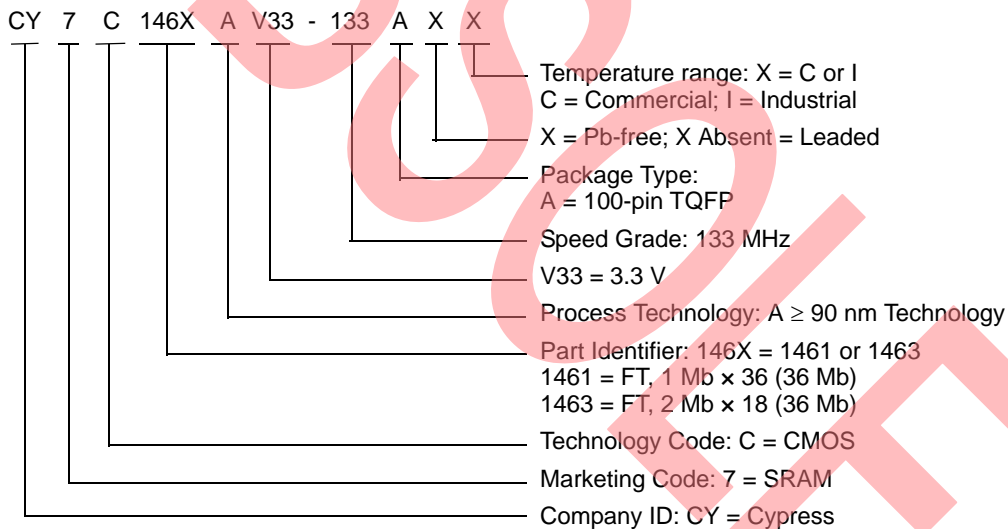
Cypress offers other versions of this type of product in different configurations and features. The following table contains only the list of parts that are currently available.

For a complete listing of all options, visit the Cypress website at [www.cypress.com](http://www.cypress.com) and refer to the product summary page at <http://www.cypress.com/products>, or contact your local sales representative.

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at <http://www.cypress.com/go/datasheet/offices>.

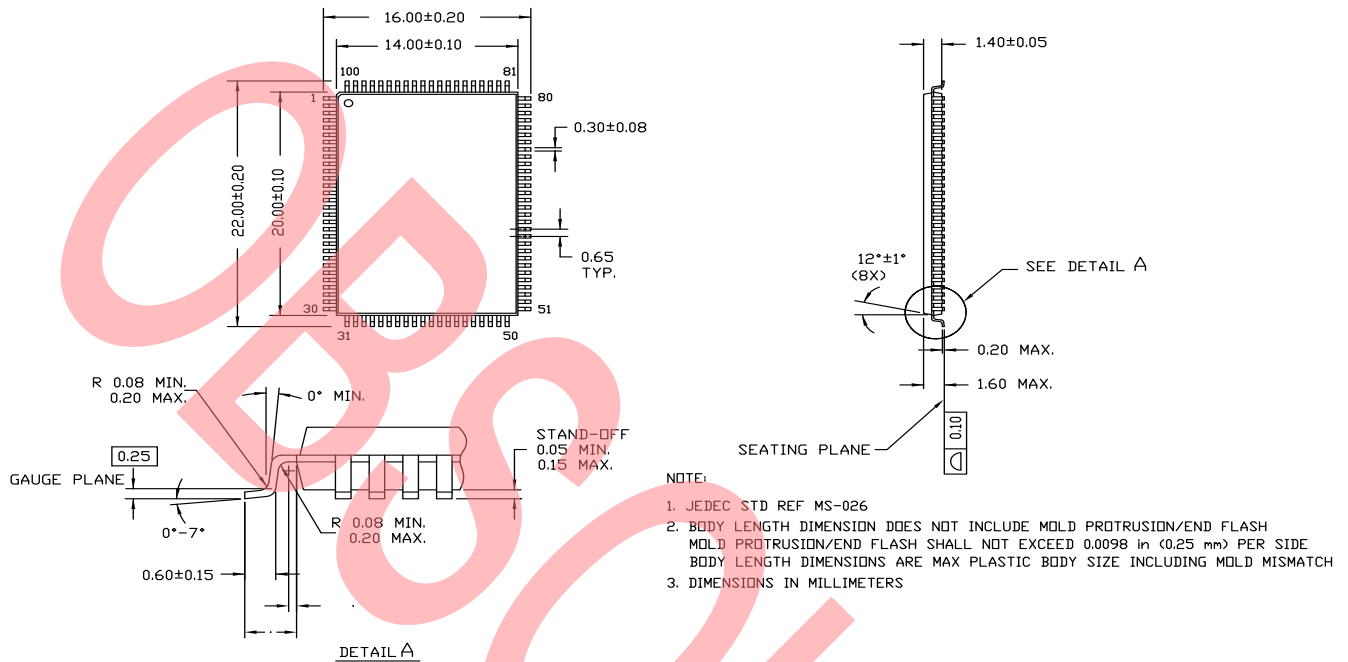
Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
133	CY7C1461AV33-133AXC	51-85050	100-pin TQFP (14 x 20 x 1.4 mm) Pb-free	Commercial
	CY7C1463AV33-133AXC			
	CY7C1461AV33-133AXI	51-85050	100-pin TQFP (14 x 20 x 1.4 mm) Pb-free	Industrial

## Ordering Code Definitions



Package Diagrams

Figure 7. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



51-85050 \*E

## Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
$\overline{CEN}$	Clock Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
LSB	Least Significant Bit
MSB	Most Significant Bit
NoBL	No Bus Latency
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
$^{\circ}\text{C}$	degree Celsius
MHz	megahertz
$\mu\text{A}$	microampere
mA	milliampere
mV	millivolt
mm	millimeter
ms	millisecond
ns	nanosecond
$\Omega$	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7C1461AV33/CY7C1463AV33, 36-Mbit (1M x 36/2M x 18) Flow-Through SRAM with NoBL™ Architecture Document Number: 38-05356				
Revision	ECN No.	Issue Date	Orig. of Change	Description of Change
**	254911	See ECN	SYT	New data sheet. Part number changed from previous revision (New and old part number differ by the letter "A").
*A	300131	See ECN	SYT	Updated <b>Features</b> (Removed 150 MHz and 117 MHz frequencies related information). Updated <b>Selection Guide</b> (Removed 150 MHz and 117 MHz frequencies related information). Updated <b>Electrical Characteristics</b> (Removed 150 MHz and 117 MHz frequencies related information). Updated <b>Thermal Resistance</b> (Replaced values of $\Theta_{JA}$ and $\Theta_{JC}$ parameters from TBD to 25.21 °C/W and 2.58 °C/W respectively for 100-pin TQFP package). Updated <b>Switching Characteristics</b> (Removed 150 MHz and 117 MHz frequencies related information). Updated <b>Ordering Information</b> (Added Pb-free information for 100-pin TQFP, 165-ball FBGA and 209-ball FBGA packages, added "Pb-free BG and BZ packages availability" comment below the Ordering Information).
*B	320813	See ECN	SYT	Updated <b>Pin Configurations</b> (Changed H9 pin from $V_{SSQ}$ to $V_{SS}$ for 209-ball FBGA). Updated <b>Electrical Characteristics</b> (Changed the test condition for $V_{OL}$ parameter from $V_{DD} = \text{Min.}$ to $V_{DD} = \text{Max.}$ , replaced the TBD's with their respective values for $I_{DD}$ , $I_{SB1}$ , $I_{SB2}$ , $I_{SB3}$ and $I_{SB4}$ parameters). Updated <b>Thermal Resistance</b> (Replaced values of $\Theta_{JA}$ and $\Theta_{JC}$ parameters from TBD to respective Thermal Values for 165-ball FBGA and 209-ball FBGA Packages). Updated <b>Capacitance</b> (Changed values of $C_{IN}$ , $C_{CLK}$ and $C_{I/O}$ parameters to 6.5 pF, 3 pF and 5.5 pF from 5 pF, 5 pF and 7 pF for 100-pin TQFP Package). Updated <b>Ordering Information</b> (Removed "Pb-free BG packages availability" comment below the Ordering Information).
*C	331551	See ECN	SYT	Updated <b>Pin Configurations</b> (Modified Address Expansion balls in the pinouts for 165-ball FBGA and 209-ball FBGA Packages according to JEDEC standards). Updated <b>Pin Definitions</b> . Updated <b>Functional Overview</b> (Updated <b>ZZ Mode Electrical Characteristics</b> (Changed maximum value of $I_{DDZZ}$ parameter from TBD to 100 mA)). Updated <b>Operating Range</b> (Added Industrial Temperature Range). Updated <b>Electrical Characteristics</b> (Updated test conditions for $V_{OL}$ and $V_{OH}$ parameters, changed maximum value of $I_{SB2}$ parameter from 100 mA to 120 mA, changed maximum value of $I_{SB4}$ parameter from 110 mA to 135 mA respectively). Updated <b>Capacitance</b> (Changed values of $C_{IN}$ , $C_{CLK}$ and $C_{I/O}$ parameters to 7 pF, 7 pF and 6 pF from 5 pF, 5 pF and 7 pF for 165-ball FBGA Package). Updated <b>Ordering Information</b> (By shading and unshading MPNs according to availability).

**Document History Page** (continued)

Document Title: CY7C1461AV33/CY7C1463AV33, 36-Mbit (1M x 36/2M x 18) Flow-Through SRAM with NoBL™ Architecture Document Number: 38-05356				
Revision	ECN No.	Issue Date	Orig. of Change	Description of Change
*D	417547	See ECN	R XU	<p>Changed status from Preliminary to Final.</p> <p>Changed address of Cypress Semiconductor Corporation from “3901 North First Street” to “198 Champion Court”.</p> <p>Updated <a href="#">Electrical Characteristics</a> (Updated Note 11 (Changed test condition from <math>V_{IH} \leq V_{DD}</math> to <math>V_{IH} &lt; V_{DD}</math>), changed “Input Load Current except ZZ and MODE” to “Input Leakage Current except ZZ and MODE”, changed minimum value of <math>I_X</math> parameter (corresponding to Input current of MODE (Input = <math>V_{SS}</math>)) from <math>-5 \mu A</math> to <math>-30 \mu A</math>, changed maximum value of <math>I_X</math> parameter (corresponding to Input current of MODE (Input = <math>V_{DD}</math>)) from <math>30 \mu A</math> to <math>5 \mu A</math> respectively, changed minimum value of <math>I_X</math> parameter (corresponding to Input current of ZZ (Input = <math>V_{SS}</math>)) from <math>-30 \mu A</math> to <math>-5 \mu A</math>, changed maximum value of <math>I_X</math> parameter (corresponding to Input current of ZZ (Input = <math>V_{DD}</math>)) from <math>5 \mu A</math> to <math>30 \mu A</math> respectively).</p> <p>Updated <a href="#">Ordering Information</a> (Updated part numbers, replaced Package Name column with Package Diagram in the Ordering Information table).</p> <p>Updated <a href="#">Package Diagrams</a>.</p>
*E	473650	See ECN	VKN	<p>Updated <a href="#">Maximum Ratings</a> (Added the Maximum Rating for Supply Voltage on <math>V_{DDQ}</math> Relative to GND).</p> <p>Updated TAP AC Switching Characteristics (Changed minimum value of <math>t_{TH}</math> and <math>t_{TL}</math> parameters from 25 ns to 20 ns, changed maximum value of <math>t_{TDOV}</math> parameter from 5 ns to 10 ns).</p> <p>Updated <a href="#">Ordering Information</a> (Updated part numbers).</p>
*F	1274733	See ECN	VKN / AESA	Updated <a href="#">Switching Waveforms</a> (Updated <a href="#">Figure 5</a> (Corrected typo)).
*G	2499107	See ECN	VKN / PYRS	Updated Logic Block Diagram – CY7C1465AV33 (Corrected typo).
*H	2897278	03/22/2010	NJY	Updated <a href="#">Ordering Information</a> (Removed obsolete part numbers). Updated <a href="#">Package Diagrams</a> .
*I	3208774	03/29/2011	NJY	Updated <a href="#">Ordering Information</a> (Updated part numbers) and added <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagrams</a> . Updated to new template.
*J	3309506	07/12/2011	OSN	Updated <a href="#">Package Diagrams</a> . Added <a href="#">Acronyms and Units of Measure</a> .



**Document History Page** (continued)

Document Title: CY7C1461AV33/CY7C1463AV33, 36-Mbit (1M × 36/2M × 18) Flow-Through SRAM with NoBL™ Architecture Document Number: 38-05356				
Revision	ECN No.	Issue Date	Orig. of Change	Description of Change
*K	3591743	05/10/2012	NJY / PRIT	<p>Updated <a href="#">Features</a> (Removed CY7C1465AV33 related information, removed 165-ball FBGA package, 209-ball FBGA package related information).</p> <p>Updated <a href="#">Functional Description</a> (Removed CY7C1465AV33 related information, removed the Note “For best practices recommendations, refer to the Cypress application note <i>System Design Guidelines</i> on <a href="http://www.cypress.com">www.cypress.com</a>.” and its reference).</p> <p>Updated <a href="#">Selection Guide</a> (Removed 100 MHz frequency related information). Removed Logic Block Diagram – CY7C1465AV33.</p> <p>Updated <a href="#">Pin Configurations</a> (Removed 165-ball FBGA package (corresponding to CY7C1461AV33 and CY7C1463AV33), 209-ball FBGA package (corresponding to CY7C1465AV33) related information).</p> <p>Updated <a href="#">Pin Definitions</a> (Removed JTAG related information).</p> <p>Updated <a href="#">Functional Overview</a> (Removed CY7C1465AV33 related information).</p> <p>Updated <a href="#">Truth Table</a> (Removed CY7C1465AV33 related information). Removed Truth Table for Read/Write (Corresponding to CY7C1465AV33). Removed IEEE 1149.1 Serial Boundary Scan (JTAG). Removed <a href="#">TAP Controller State Diagram</a>. Removed <a href="#">TAP Controller Block Diagram</a>. Removed <a href="#">TAP Timing</a>. Removed <a href="#">TAP AC Switching Characteristics</a>. Removed <a href="#">3.3 V TAP AC Test Conditions</a>. Removed <a href="#">3.3 V TAP AC Output Load Equivalent</a>. Removed <a href="#">2.5 V TAP AC Test Conditions</a>. Removed <a href="#">2.5 V TAP AC Output Load Equivalent</a>. Removed <a href="#">TAP DC Electrical Characteristics</a> and Operating Conditions. Removed <a href="#">Identification Register Definitions</a>. Removed <a href="#">Scan Register Sizes</a>. Removed <a href="#">Identification Codes</a>. Removed <a href="#">Boundary Scan Order</a> (Corresponding to 165-ball FBGA package). Removed <a href="#">Boundary Scan Order</a> (Corresponding to 209-ball FBGA package). Updated <a href="#">Electrical Characteristics</a> (Removed 100 MHz frequency related information). Updated <a href="#">Capacitance</a> (Removed 209-ball FBGA package related information). Updated <a href="#">Thermal Resistance</a> (Removed 209-ball FBGA package related information). Updated <a href="#">Switching Characteristics</a> (Removed 100 MHz frequency related information). Updated <a href="#">Package Diagrams</a> (Removed 165-ball FBGA package, 209-ball FBGA package related information). Replaced all instances of IO with I/O across the document.</p>
*L	3690005	07/24/2012	PRIT	<p>No technical updates. Completing Sunset Review.</p>
*M	4572829	11/18/2014	PRIT	<p>Updated <a href="#">Functional Description</a>: Added “For a complete list of related documentation, click <a href="#">here</a>.” at the end.</p> <p>Updated <a href="#">Package Diagrams</a>: spec 51-85050 – Changed revision from *D to *E.</p>
*N	4865506	07/30/2015	PRIT	<p>Updated to new template. Completing Sunset Review.</p>
*O	5373812	07/26/2016	PRIT	<p>Obsolete document. Completing Sunset Review.</p>

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