PD - 95579A

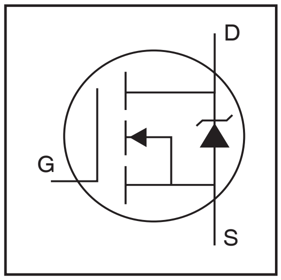
International
IOR Rectifier

IRL3705ZPbF
IRL3705ZSPbF
IRL3705ZLPbF

HEXFET® Power MOSFET

Features

- Logic Level
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free



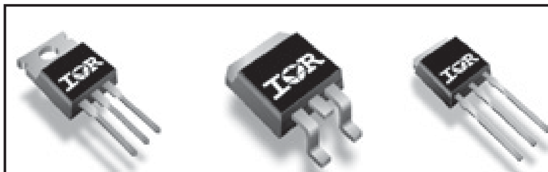
V_{DSS} = 55V

$R_{DS(on)}$ = 8.0mΩ

I_D = 75A

Description

This HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in a wide variety of applications.



TO-220AB	D²Pak	TO-262
IRL3705ZPbF	IRL3705ZSPbF	IRL3705ZLPbF

Absolute Maximum Ratings

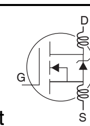
	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	86	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	61	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	75	
I_{DM}	Pulsed Drain Current ①	340	
P_D @T_C = 25°C	Power Dissipation	130	W
	Linear Derating Factor	0.88	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy②	120	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy Tested Value ⑥	180	
I_{AR}	Avalanche Current ①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw ⑦	10 lbf•in (1.1N•m)	

Thermal Resistance

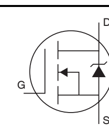
	Parameter	Typ.	Max.	Units
$R_{θJC}$	Junction-to-Case	–––	1.14	°C/W
$R_{θCS}$	Case-to-Sink, Flat Greased Surface ⑦	0.50	–––	
$R_{θJA}$	Junction-to-Ambient ⑦	–––	62	
$R_{θJA}$	Junction-to-Ambient (PCB Mount) ⑧	–––	40	

10/01/10

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	–––	–––	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.055	–––	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	6.5	8.0	mΩ	V_{GS} = 10V, I_D = 52A ③
		–––	–––	11		V_{GS} = 5.0V, I_D = 43A ③
		–––	–––	12		V_{GS} = 4.5V, I_D = 30A ③
$V_{GS(th)}$	Gate Threshold Voltage	1.0	–––	3.0	V	V_{DS} = V_{GS}, I_D = 250µA
gfs	Forward Transconductance	150	–––	–––	V	V_{DS} = 25V, I_D = 52A
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	20	µA	V_{DS} = 55V, V_{GS} = 0V
		–––	–––	250		V_{DS} = 55V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	200	nA	V_{GS} = 16V
	Gate-to-Source Reverse Leakage	–––	–––	-200		V_{GS} = -16V
Q_g	Total Gate Charge	–––	40	60	nC	I_D = 43A
Q_{gs}	Gate-to-Source Charge	–––	12	–––		V_{DS} = 44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	21	–––		V_{GS} = 5.0V ③
$t_{d(on)}$	Turn-On Delay Time	–––	17	–––	ns	V_{DD} = 28V
t_r	Rise Time	–––	240	–––		I_D = 43A
$t_{d(off)}$	Turn-Off Delay Time	–––	26	–––		R_G = 4.3 Ω
t_f	Fall Time	–––	83	–––		V_{GS} = 5.0V ③
L_D	Internal Drain Inductance	–––	4.5	–––	nH	Between lead, 6mm (0.25in.)
L_S	Internal Source Inductance	–––	7.5	–––		from package and center of die contact 
C_{iss}	Input Capacitance	–––	2880	–––	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	–––	420	–––		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	–––	220	–––		f = 1.0MHz
C_{oss}	Output Capacitance	–––	1500	–––		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	–––	330	–––		V_{GS} = 0V, V_{DS} = 44V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	–––	510	–––		V_{GS} = 0V, V_{DS} = 0V to 44V ④

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	75	A	MOSFET symbol showing the
I_{SM}	Pulsed Source Current (Body Diode) ①	–––	–––	340		integral reverse p-n junction diode. 
V_{SD}	Diode Forward Voltage	–––	–––	1.3	V	T_J = 25°C, I_S = 52A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	–––	16	24	ns	T_J = 25°C, I_F = 43A, V_{DD} = 28V
Q_{rr}	Reverse Recovery Charge	–––	7.4	11	nC	di/dt = 100A/µs ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

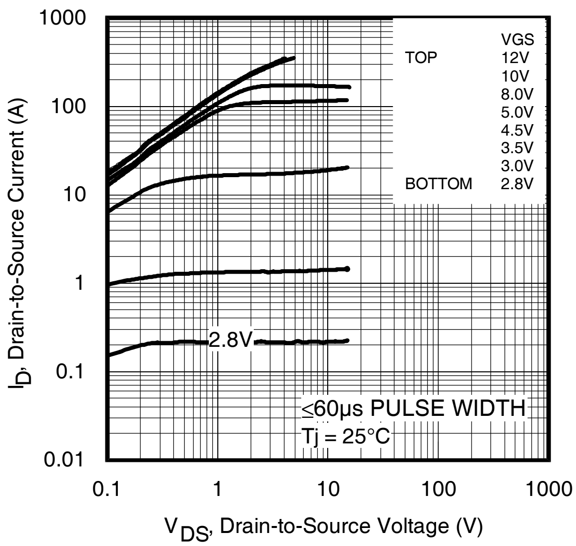


Fig 1. Typical Output Characteristics

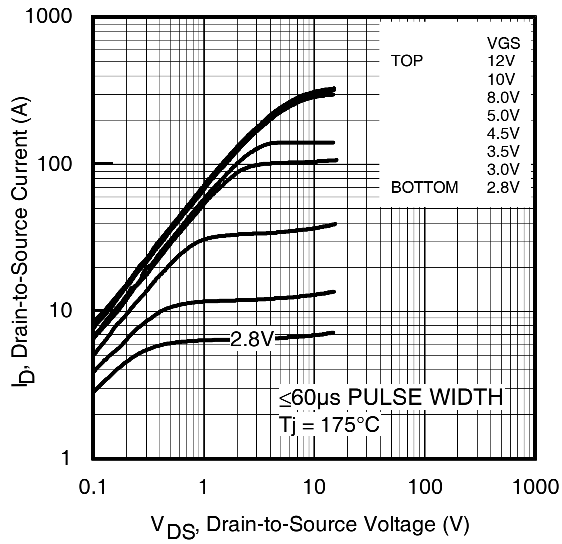


Fig 2. Typical Output Characteristics

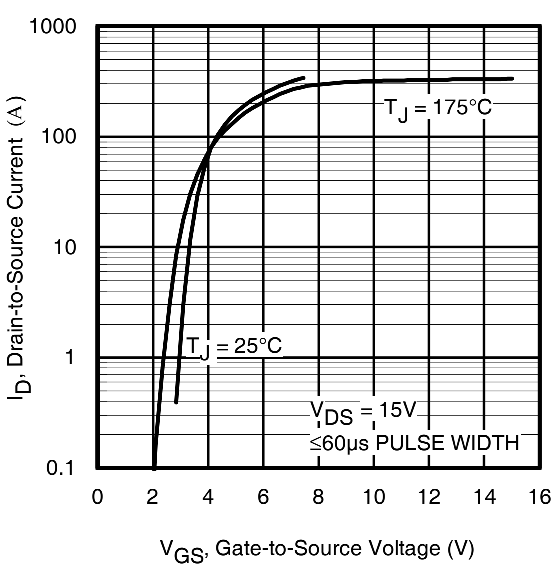


Fig 3. Typical Transfer Characteristics

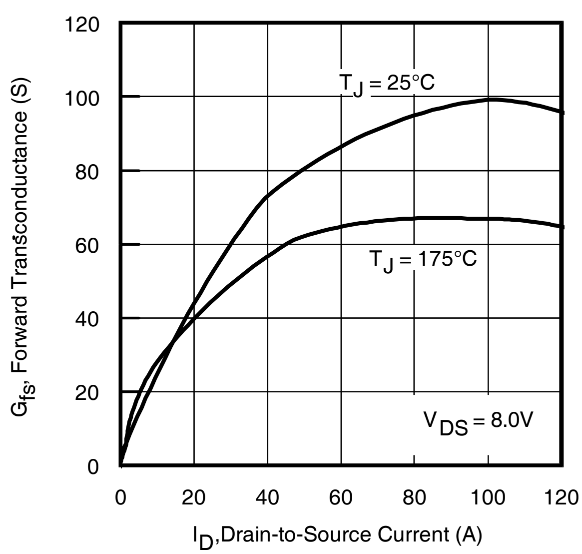


Fig 4. Typical Forward Transconductance vs. Drain Current

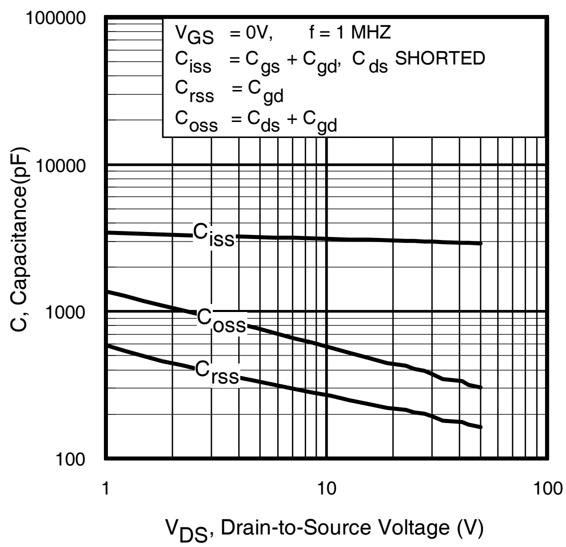


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

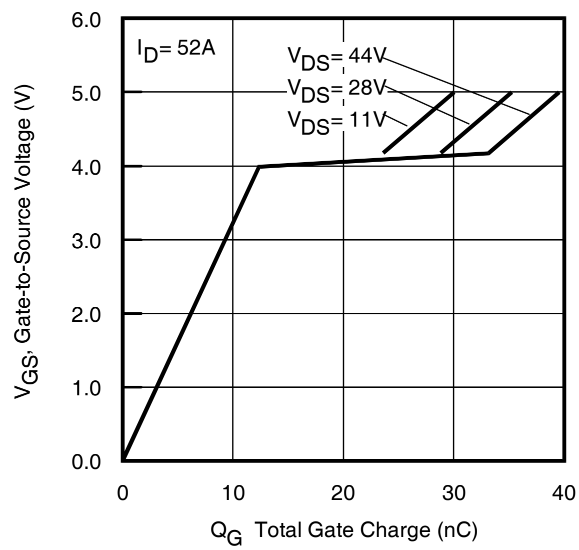


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

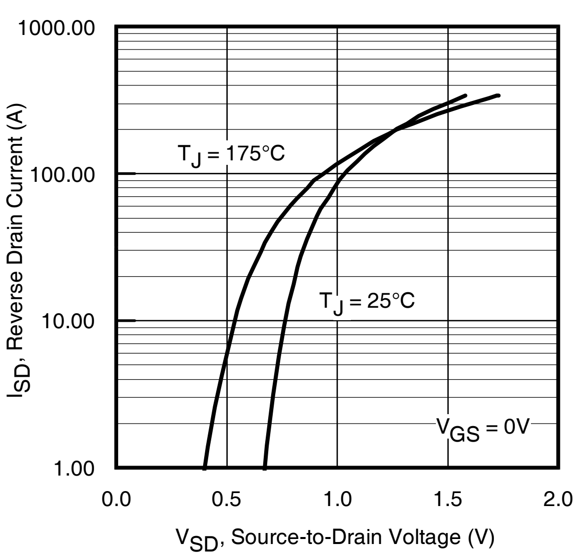


Fig 7. Typical Source-Drain Diode Forward Voltage

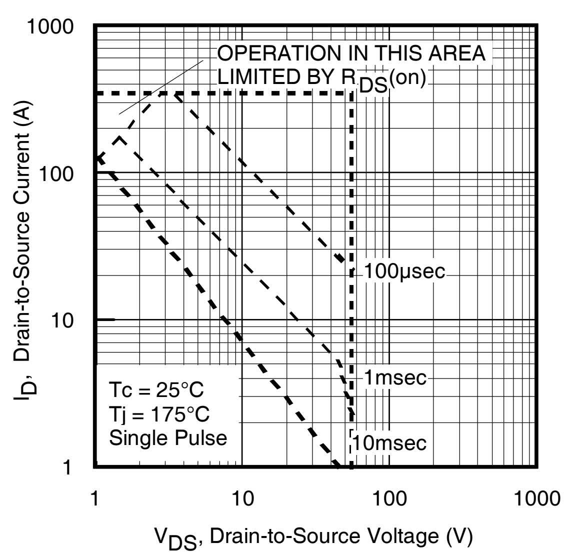


Fig 8. Maximum Safe Operating Area

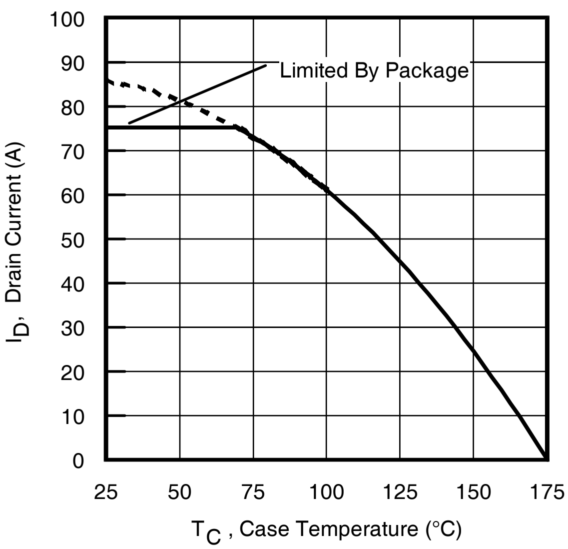


Fig 9. Maximum Drain Current vs. Case Temperature

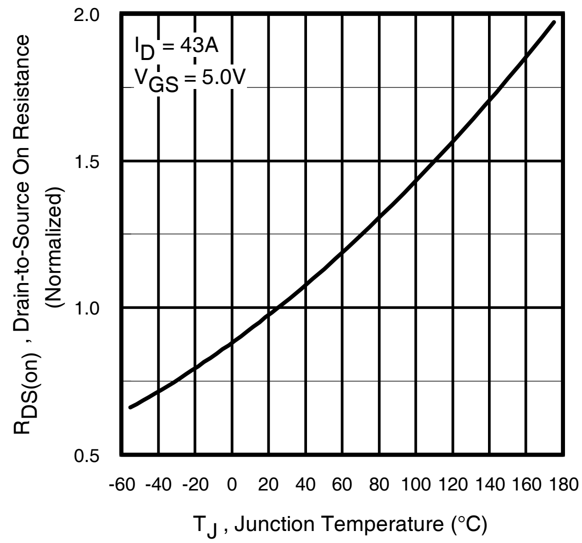


Fig 10. Normalized On-Resistance vs. Temperature

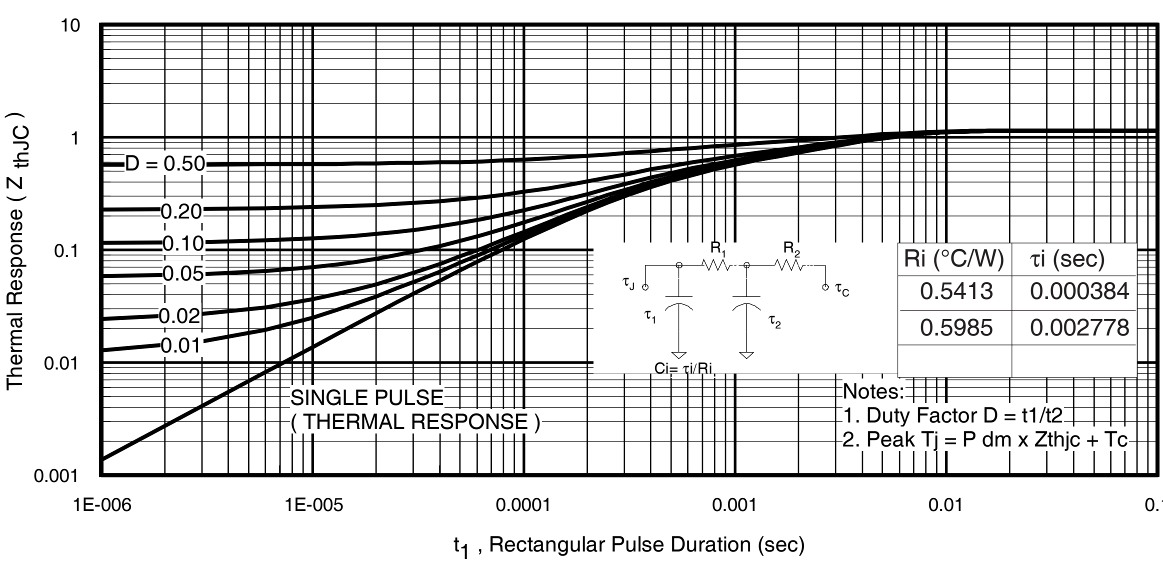


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

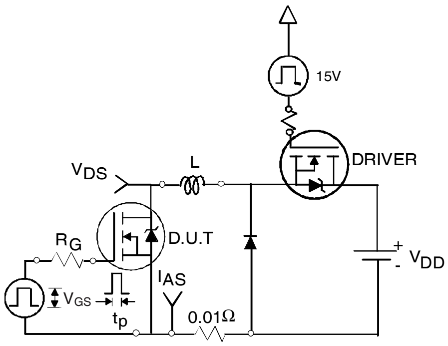


Fig 12a. Unclamped Inductive Test Circuit

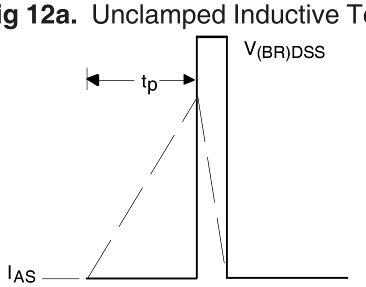


Fig 12b. Unclamped Inductive Waveforms

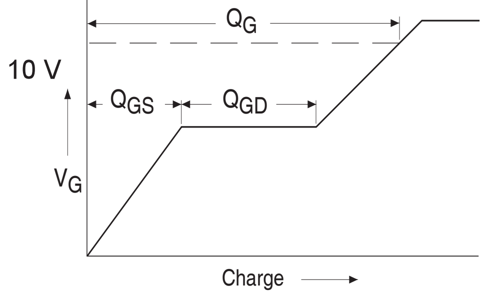


Fig 13a. Basic Gate Charge Waveform

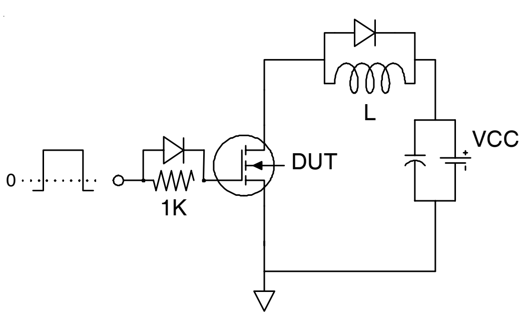


Fig 13b. Gate Charge Test Circuit

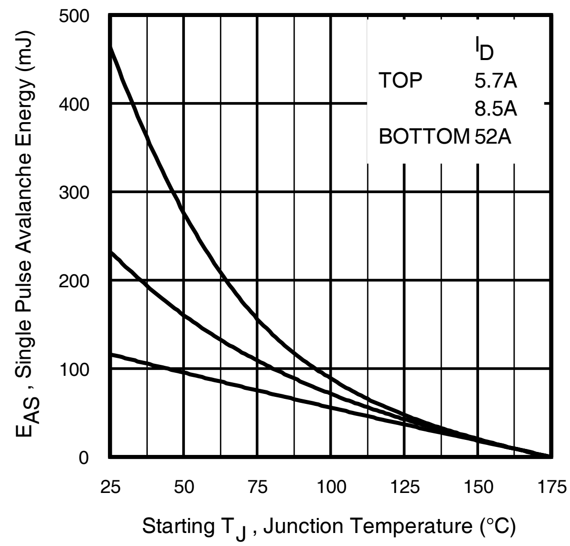


Fig 12c. Maximum Avalanche Energy vs. Drain Current

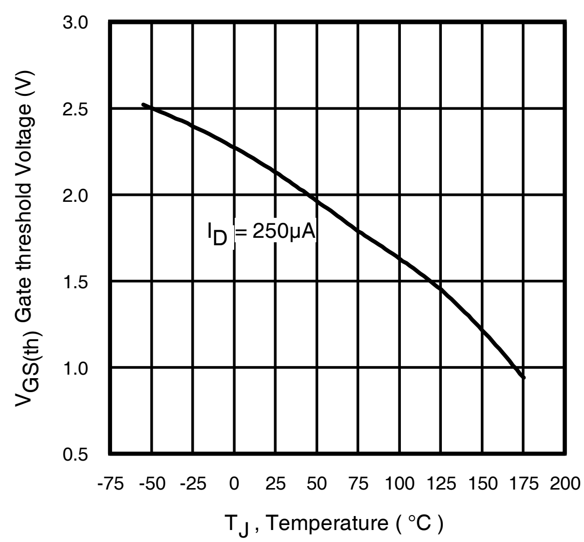


Fig 14. Threshold Voltage vs. Temperature

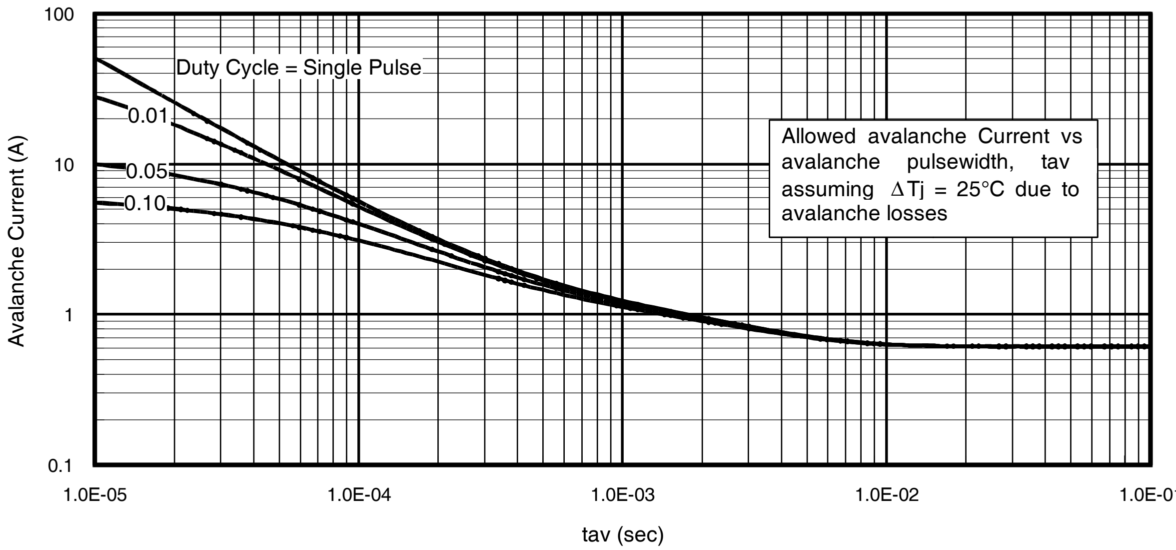


Fig 15. Typical Avalanche Current vs.Pulsewidth

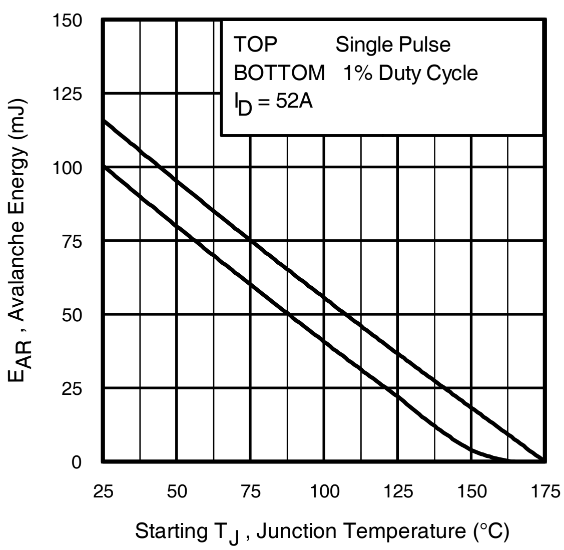


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

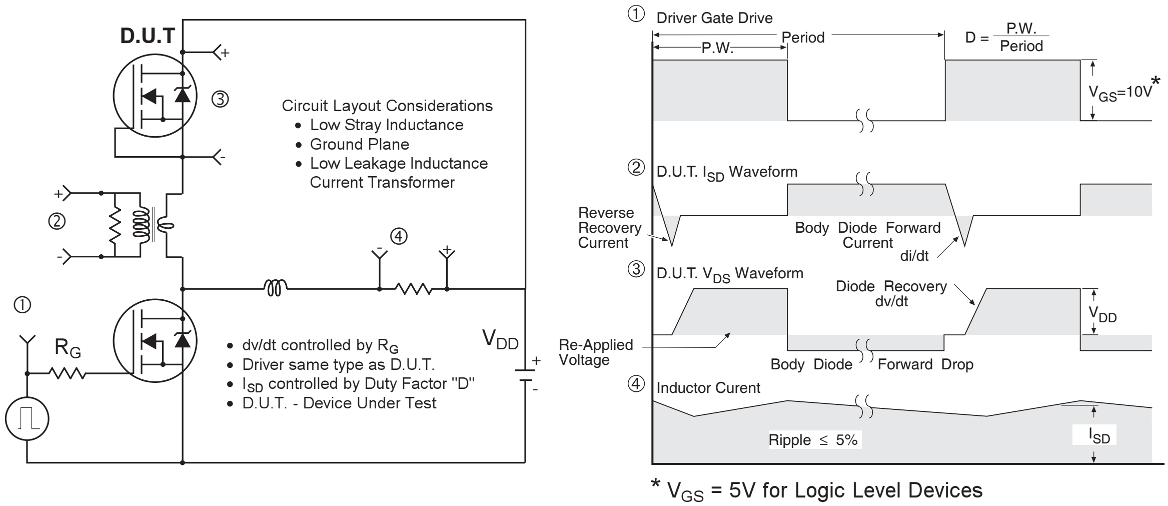


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

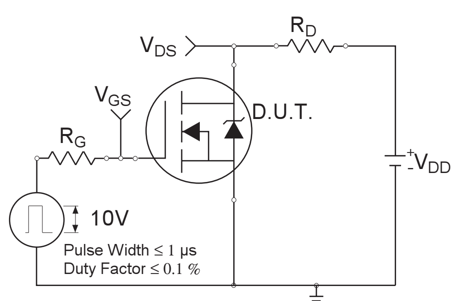


Fig 18a. Switching Time Test Circuit

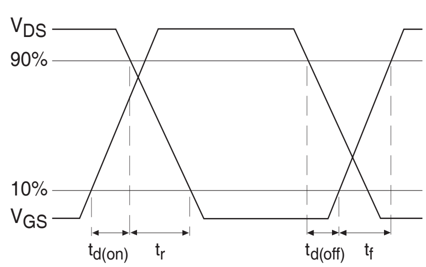
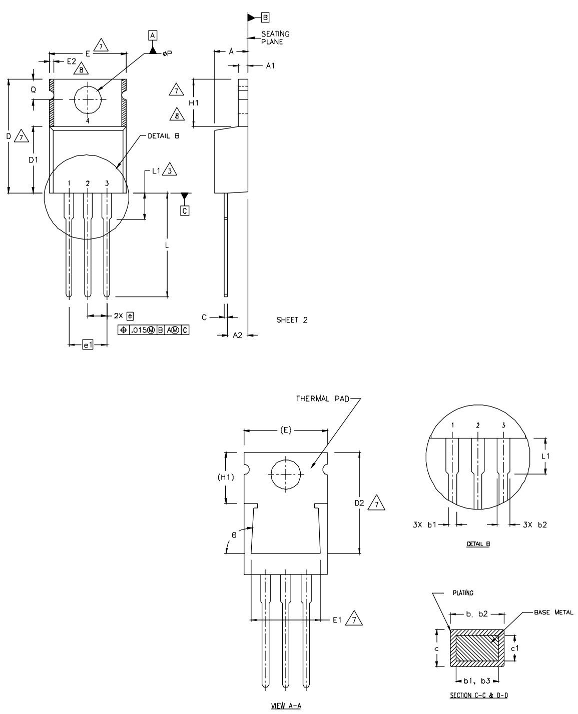


Fig 18b. Switching Time Waveforms

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
2 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5 DIMENSION b1 & c1 APPLY TO BASE METAL ONLY.
6 CONTROLLING DIMENSION : INCHES.
7 THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
8 DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.82	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.04	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.96	.015	.038	5
b2	1.15	1.77	.045	.070	
b3	1.15	1.73	.045	.068	
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	12.19	12.88	.480	.507	7
E	9.66	10.66	.380	.420	4,7
E1	8.38	8.89	.330	.350	7
e	2.54 BSC		.100 BSC		
e1	5.08		.200 BSC		
H1	5.85	6.55	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	-	6.35	-	.250	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	
ø	90°-93°		90°-93°		

LEAD ASSIGNMENTS

HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE

IGBTs, CoPACK

1.- GATE
2.- COLLECTOR
3.- EMITTER

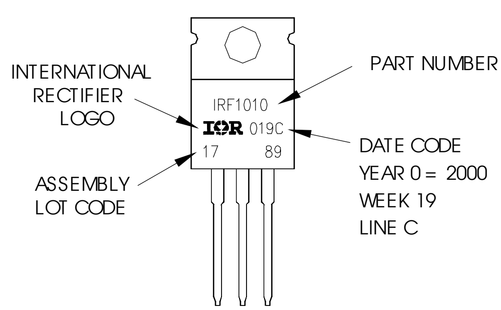
DIODES

1.- ANODE/OPEN
2.- CATHODE
3.- ANODE

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 2000
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



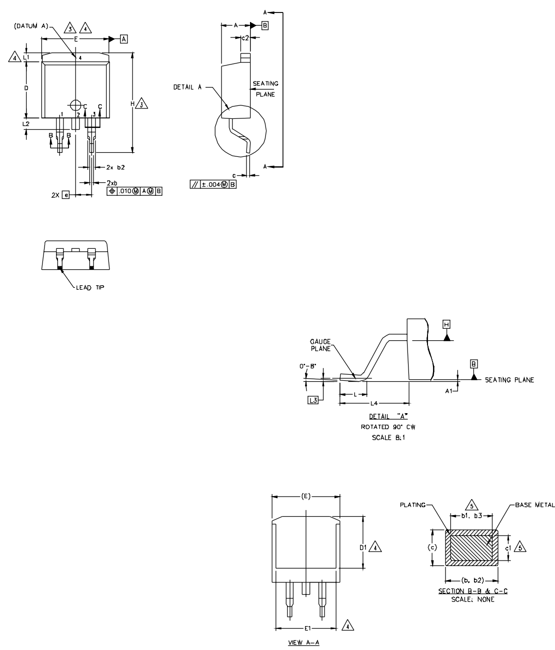
Notes:

1. For an Automotive Qualified version of this part please see http://www.irf.com/product-info/auto/

2. For the most current drawing please refer to IR website at http://www.irf.com/package/

D²Pak (TO-263AB) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270		4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245		4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.65	–	.066	4
L2	1.27	1.78	–	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

LEAD ASSIGNMENTS

HEXFET

1.- GATE
2, 4.- DRAIN
3.- SOURCE

IGBTs, CoPACK

1.- GATE
2, 4.- COLLECTOR
3.- EMITTER

DIODES

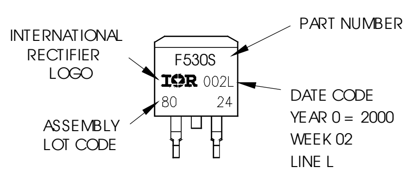
1.- ANODE *
2, 4.- CATHODE
3.- ANODE

* PART DEPENDENT.

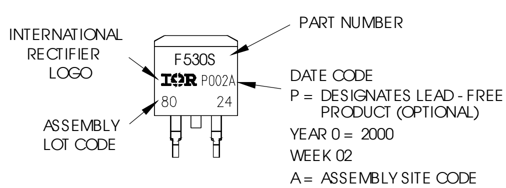
D²Pak (TO-263AB) Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position
indicates "Lead – Free"



OR



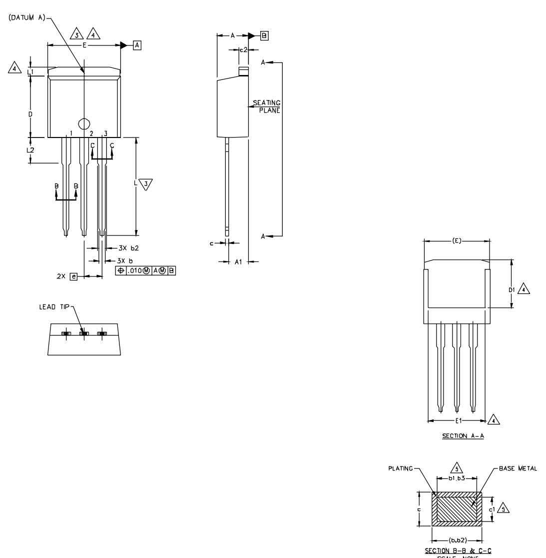
Notes:

1. For an Automotive Qualified version of this part please see http://www.irf.com/product-info/auto/

2. For the most current drawing please refer to IR website at http://www.irf.com/package/

TO-262 Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

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4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7.- OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270	–	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245		4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	–	1.65	–	.065	4
L2	3.56	3.71	.140	.146	

LEAD ASSIGNMENTS

HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

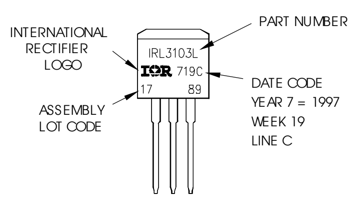
IGBTs, CoPACK

1.- GATE
2.- COLLECTOR
3.- EMITTER
4.- COLLECTOR

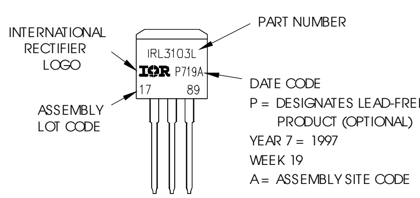
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



OR



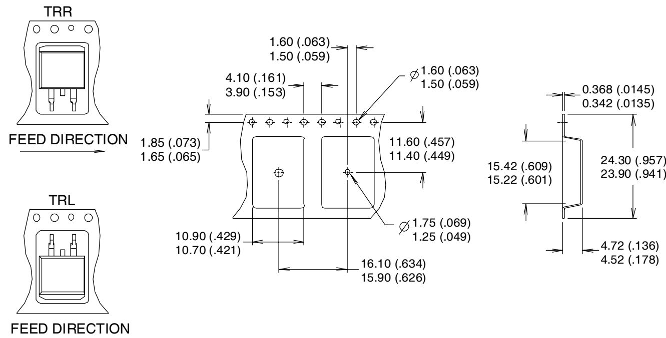
Notes:

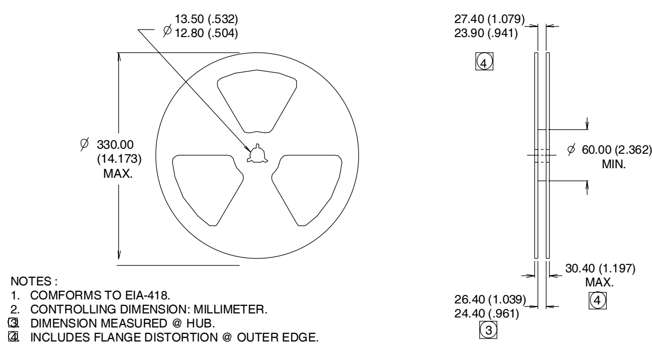
1. For an Automotive Qualified version of this part please see<u>http://www.irf.com/product-info/auto/</u>

2. For the most current drawing please refer to IR website at <u>http://www.irf.com/package/</u>

D^2Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)





Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Limited by T_{Jmax}, starting $T_J = 25°C$, L = 0.09mH $R_G = 25\Omega$, $I_{AS} = 52A$, V_{GS} =10V. Part not recommended for use above this value.

③ Pulse width $\leq$ 1.0ms; duty cycle $\leq$ 2%.

④ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑤ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

⑥ This value determined from sample failure population. 100% tested to this value in production.

⑦ This is only applied to TO-220AB pakcage.

⑧ This is applied to D^2Pak, when mounted on 1" square PCB (FR- 4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

⑨ R_θ is measured at T_J of approximately 90°C.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

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