Low Power Stereo Audio Codec With Embedded miniDSP

Check for Samples: TLV320AIC36

1 INTRODUCTION

1.1 Features

- Stereo Audio DAC
  - 100-dBA Signal-to-Noise Ratio
  - 16/20/24/32-Bit Data
  - Supports Rates From 8 to 192 kHz
  - Programmable DAC Filter Engine
- Stereo Audio ADC
  - 92-dBA Signal-to-Noise Ratio
  - Supports Rates from 8 to 192 kHz
  - Programmable ADC Filter Engine
- Three Dedicated Microphone Inputs
  - Supports Single-Ended, Balanced Differential, and Unbalanced Differential Configurations
- Stereo Line-Level Inputs
- Audio Output Drivers
  - Ground-Referenced Cap-Free Stereo 16Ω Single-Ended Headphone Drivers
  - Ground-Referenced Cap-Free Stereo 16Ω Single-Ended Receiver Drivers
  - Fully Differential Stereo Line Outputs
- Programmable Input/Output Gains
- Automatic Gain Control (AGC) for Record
- Dual Programmable Microphone Bias Generators
- Programmable PLL for Flexible Clock Generation
- Advanced Microphone Impedance Detection
- I^2C™ Control Bus
- Audio Serial Data Bus Supports I^2S™, Left/Right Justified, DSP, and TDM Modes
- Alternate Serial PCM/I2S Data Bus
- Stereo Digital Microphone Input
- Extensive Modular Power Control
  - Integrated Charge Pump
  - Integrated Programmable LDOs
- Package: 5 x 5 mm 80-VFBGA

1.2 Applications

- Portable Navigation Devices (PND)
- Portable Media Players (PMP)
- Mobile Handsets
- Communication
- Portable Computing

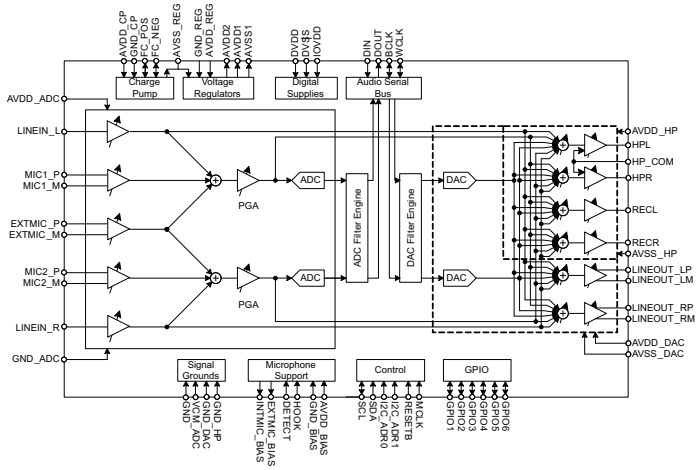

Figure 1-1. Simplified Block Diagram

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1.3 Description

The TLV320AIC36 (sometimes referred to as the *AIC36*) is a flexible, low-power, low-voltage stereo audio codec with programmable inputs and outputs, fully programmable miniDSP, fixed predefined and parameterizable signal processing blocks, integrated PLL, integrated LDOs, and flexible digital interfaces.

1.3.1 Detailed Description

The TLV320AIC36 features two fully programmable miniDSP cores that support application-specific algorithms in the record and/or the playback path of the device. The miniDSP cores are fully software controlled.

Extensive Register based control of power, input/output channel configuration, gains, effects, pin-multiplexing, and clocks is included, allowing the device to be precisely targeted to its application. The device can cover operations from 8-kHz mono voice playback to audio stereo 192-kHz DAC playback, making it ideal for portable battery-powered audio and telephony applications.

The record path of the TLV320AIC36 covers operations from 8-kHz mono to 192-kHz stereo recording, and contains programmable input channel configurations covering single-ended and differential setups, as well as floating or mixing input signals. It also includes a digitally controlled stereo microphone preamplifier and integrated microphone bias. Digital signal processing blocks can remove audible noise that may be introduced by mechanical coupling (for example, optical zooming in a digital camera).

The playback path offers signal-processing blocks for filtering and effects, and supports flexible mixing of DAC and analog input signals as well as programmable volume controls. The playback path has four ground-referenced capacitor-free 16Ω output drivers to support single-ended headphone and receivers.

Two fully differential ground-centered 10KΩ line output drivers are also available.

An extensive power-management unit with an integral charge pump and three programmable LDOs is available to create all positive and negative analog supply voltages required by the TLV320AIC36 from a single positive 2.1-V to 2.8-V supply. Alternatively, the charge pump and LDOs may be individually bypassed to support a wide variety of power supply configurations.

The required internal clock of the TLV320AIC36 can be derived from multiple sources, including the MCLK pin, the BCLK pin, the GPIO pin, or the output of the internal PLL, where the input to the PLL again can be derived from the MCLK pin, the BCLK or GPIO pins. Although using the PLL makes sure that a suitable clock signal is available, it is not recommended for the lowest power settings. The PLL is highly programmable and can accept available input clocks in the range of 512 kHz to 50 MHz.

The device is available in the 5-mm × 5-mm, MicroStar Junior™ 80-VFBGA package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

2 PACKAGE AND SIGNAL DESCRIPTIONS

2.1 Packaging/Ordering Information(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	OPERATING TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLV320AIC36	BGA-80	ZQE	–40°C to 85°C	TLV320AIC36IZQE	Trays, 360
				TLV320AIC36IZQER	Tape and reel, 2500

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the TLV320AIC36 product folder at www.ti.com.

2.2 Pin Assignments

5x5 mm 80 Pin BGA (ZQE) Package
(Bottom View)

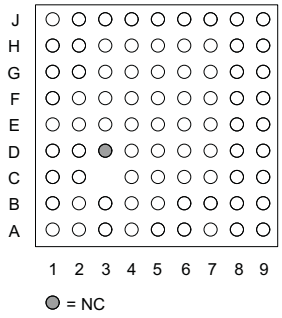


Figure 2-1. Pin Assignments (not to scale)

Pin Functions

PIN		DESCRIPTION
BALL	NAME	
G9	AVDD_ADC	Positive supply for ADC and PLL
G6	LINEIN_L	Left line input
J6	MIC1_P	Internal mic #1 input (plus)
H6	MIC1_M	Internal mic #1 input (minus)
H7	EXTMIC_P	External mic input (plus)
J7	EXTMIC_M	External mic input (minus)
H8	MIC2_P	Internal mic #2 input (plus)
G8	MIC2_M	Internal mic #2 input (minus)
G7	LINEIN_R	Right line input
J9	VCM_ADC	ADC common mode level
H9	GND_ADC	Analog ground for ADC and PLL
E8,E9	AVDD_HP	Positive supply for headphone amps
F9	HPL	Left headphone output
J8	HP_COM	Headphone amp common (signal ground)
F7	HPR	Right headphone output
F8, C9	AVSS_HP	Negative supply for headphone amps
D8	RECL	Left receiver out
E7	GND_HP	Signal ground for HP and receiver amps
D9	RECR	Right receiver out
A6	AVDD_DAC	Positive supply for DAC and lineout amps
B7	GND_DAC	Signal ground for DAC
B6	LINEOUT_LP	Left line output (Pos)
A7	LINEOUT_LM	Left line output (Neg)
C6	LINEOUT_RP	Right line out (Pos)
A8	LINEOUT_RM	Right line out (Neg)
B8	AVSS_DAC	Negative supply for DAC and lineout amps
A9	AVDD_BIAS	Supply for mic bias and detect blocks
C8	EXTMIC_BIAS	Bias voltage for external microphone
B9	INTMIC_BIAS	Bias voltage for internal microphone
C7	DETECT	Microphone impedance detect
D6	HOOK	Hookswitch detect
D7	GND_BIAS	Ground for mic bias and detect blocks
A1, B2	AVDD_CP	Charge pump supply
C1,D2	GND_CP	Charge pump ground
B1,C2	FC_POS	Flying capacitor for charge pump
D1, E2	FC_NEG	Flying capacitor for charge pump
H1,G3	AVDD_REG	Positive regulator supply input
F3	GND_REG	Regulator ground
E1, E3	AVSS_REG	Negative regulator supply input/charge pump output
G1,G2	AVDD1	Primary positive LDO output (DAC VDD LDO)
F1, F2	AVSS1	Primary negative LDO output (DAC VSS LDO)
J1	AVDD2	Secondary positive LDO output (ADC VDD LDO)
A3	BCLK	Audio serial bus bit clock
B4	WCLK	Audio serial bus word clock
C5	DIN	Audio serial bus data input (DAC Data)
B3	DOUT	Audio serial bus data output (ADC Data)

Pin Functions (continued)

PIN		DESCRIPTION
BALL	NAME	
H4	SCL	I^2C serial clock
G5	SDA	I^2C data I/O
F5	I^2C_ADR1	I^2C address Pin 1
G4	I^2C_ADR0	I^2C address Pin 0
A4	MCLK	Master clock
C4	GPIO1	Interrupt request/GPIO
D4	GPIO2	External amplifier power control/GPIO/Secondary serial WCLK
J3	GPIO3/DIGMIC_CLK	Clock for digital mic/GPIO/Secondary serial BCLK/PLL Clock Output
H3	GPIO4/DIGMIC_DATA	Data from digital mic/GPIO/Secondary serial DIN
J2	GPIO5/BITSTREAM_CLK	Clock for class-D amp/GPIO
H2	GPIO6/BITSTREAM_DATA	Data for class-D amp/GPIO
E5	RESETB	Reset
H5,B5	DVDD	Core digital supply
J5, A5	DVSS	Digital Ground
J4,A2	IOVDD	I/O digital supply
D5,E6,E4,F4	GND	Substrate ground. Connect to analog ground
F6		Reserved
D3	N/C	No connect

3 ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

			VALUE	UNIT
Supply voltage range (2)		AVDD_REG, AVDD_CP, AVDD_BIAS	–0.5 to 3.6	V
		AVSS_REG	–3.6 to +0.5	V
		AVDD_DAC, AVDD_ADC, AVDD_AMP	–0.5 to +1.8	V
		All other AVSS	–1.8 to +0.5	V
		DVDD	–0.5 to 1.95	V
		IOVDD	–0.5 to 3.6	V
Voltage between		AGND and DGND	–0.3 to 0.5	V
		AVDD to DVDD	–3.6 to 3.6	V
Digital input voltage to DVSS			–0.3 to IOVDD + 0.3	V
Analog input voltage to GND			–0.3-AVSS to AVDD + 0.3	V
Operating free-air temperature range, T_A			–40 to +85	°C
Storage temperature range			–65 to +105	°C
Junction temperature, T_{JMax}			125	°C
Power dissipation			$(T_{JMax} – T_A)/\theta_{JA}$	W
Thermal impedance, BGA package, θ_{JA}			55	°C/W
ESD Ratings	CDM	All Pins	1	kV
	HBM	All Pins except the following:	2	
	HBM	IOVDD, AVDD_BIAS, VCM_ADC	1.5	
	HBM	AVDD_HP, HOOK, LINEIN_L, LINEIN_R, MIC1_P, MIC1_M, EXTMIC_P, EXTMIC_M, MIC2_P, MIC2_M, AVDD_ADC	1	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) AVDD_REG-AVSS_REG must be less than 5.6V.

3.2 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
SUPPLIES					
T_A	Operating free-air temperature	–40		85	°C
AVDD_CP	Charge pump supply voltage	1.7 (1)	2.5	2.8	V
AVDD_BIAS	Mic bias supply voltage	1.7 (2)	2.5	2.8	V
AVDD_REG	Positive regulator input voltage (3)	1.7 (1)	2.5	2.8	V
AVSS_REG	Negative regulator input voltage (3)	–1.7	–2.5	–2.8	V
AVDD_ADC	Positive supply voltages (4)	1.65 (5)	1.8	1.9	V
AVDD_DAC, AVDD_HP	Positive supply voltages (4)	1.4	1.65	1.8	V
AVSS_DAC, AVSS_HP	Negative supply voltages (4)	–1.4	–1.65	–1.8	V
DVDD	Digital supply voltage	1.65 (5)	1.8	1.95	V
IOVDD	Output driver supply voltage	1.1	1.8	3.6	V

(1) Valid for lowest power mode when bypassing negative regulator. Otherwise, MIN=2.1V.
(2) Minimum 2.0 V for 1.8 V bias voltage
(3) Only relevant if charge pump is not used
(4) Only relevant if charge pump and voltage regulators are not used
(5) AVDD_ADC, DVDD min =1.4V for low power modes (see section 5.18.3)

3.3 Electrical Characteristics – ADC Channel

At 25°C, AVDD_REG=AVDD_CP = 2.5 V, IOVDD = 3.3 V, DVDD = 1.8 V, Fs = 48-kHz, 16-bit audio data (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Full-scale input signal, differential inputs	0 dB gain		1		V_{RMS}
Full-scale input, single ended	6 dB gain		0.5		V_{RMS}
Signal-to-noise ratio, mic inputs(1) (2)	0 dB gain		92		dB
	+38 dB gain(3)		69		
Signal-to-noise ratio, line inputs(1) (2)	0 dB gain	80	92		dB
	+38 dB gain(4)		66		dB
Dynamic range, all inputs(1) (2)	0 dB gain, –60 dB input at 1-kHz		92		dB
Total harmonic distortion, line, internal mic, and external mic inputs	0 dB gain, –1 dB input at 1-kHz		–85	–75	dB
PSRR, all inputs	< 1-kHz, single-ended input		78		dB
	< 1-kHz, differential input		100		
	10-kHz, differential input		80		
PSRR, all inputs, unregulated(5)	< 1-kHz, single-ended input		55		dB
	< 1-kHz, differential input		55		
Channel separation(6)	0 dB gain, –2 dB input at 1-kHz		–70		dB
Gain error	0 dB gain, 1-kHz input		0.7		dB
Programmable Gain Amplifier (PGA) maximum gain			59.5		dB
PGA gain step			0.5		dB
Input resistance, line inputs	0 dB input mix gain		10		kΩ
	–12 dB input mix gain		40		
Input resistance, mic inputs	6 dB input mix gain		10		kΩ
	-6 dB input mix gain		40		
Input capacitance, all inputs			10		pF
DIGITAL DECIMATION FILTER(7)					
Filter gain from 0 to 0.39 Fs			0.1		dB
Filter gain at 0.4125 Fs			–0.25		dB
Filter gain at 0.45 Fs			–3		dB
Filter gain at 0.5 Fs			–17.5		dB
Filter gain from 0.55 Fs to 64 Fs			–75		dB
Filter group delay			17/Fs		sec
MICROPHONE BIAS GENERATORS					
Bias voltage	Programmable settings, 1 kΩ load		1.3		V
			1.5		
		1.6	1.8	2.0	
Current sourcing				2	mA
Power supply rejection ratio	< 1-kHz		80		dB

(1) Ratio of output level with 1-kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.
(3) +6 dB input mix gain, +26 dB PGA gain
(4) 0 dB input mix gain, +38 dB PGA gain
(5) AVDD_DAC and AVSS_DAC connected directly to supply
(6) Channel separation for any input connected to the ADC left channel and any other input connected to the ADC right channel
(7) Default filter configuration

3.4 Electrical Characteristics – DAC Channel

At 25°C, AVDD AVDD_REG=AVDD_CP = 2.5 V, IOVDD = 3.3 V, DVDD = 1.8 V, Fs = 48-kHz, 16-bit audio data (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INTERPOLATION FILTER(1)					
Passband	High-pass filter disabled			0.45×Fs	Hz
Passband ripple	High-pass filter disabled		0.06		dB
Transition band		0.45×Fs		0.55×Fs	Hz
Stop band		0.55×Fs		7.5×Fs	Hz
Stop band attenuation			65		dB
Group delay			21/Fs		sec
LINE OUTPUTS AT LOAD = 10 kΩ, 50 pF DIFFERENTIAL					
Full-scale output voltage	0 dB gain		1.414		V_{RMS}
Maximum output level gain setting			9		dB
Output level gain setting step			1		dB
Signal-to-noise ratio(2)	0 dB gain, A-weighted, Full-scale output at 1-kHz	90	102		dB
Dynamic range	0 dB gain, A-weighted, –60 dB input at 1 kHz		100		dB
Total harmonic distortion	0 dB gain, Full-scale output at 1 kHz		–94	–75	dB
PSRR	< 1 kHz		90		dB
	10 kHz		70		
Channel separation	0 dB gain, Full-scale input at 1 kHz		–100		dB
Gain mismatch			0.1		dB
Gain error			–0.4		dB
RECEIVER AND HEADPHONE OUTPUTS(3)					
Full-scale output voltage	0 dB gain		0.707		V_{RMS}
Full-scale output power	0 dB gain, full-scale output at 1 kHz, 16Ω load		31		mW
Maximum output level gain setting			9		dB
Output level gain setting step			1		dB
Signal-to-noise ratio(2)	0 dB gain, A-weighted, Full-scale output at 1 kHz		98		dB
Total harmonic distortion	0 dB gain, full-scale output at 1 kHz, 32Ω load		–90		dB
	0 dB gain, –3 dB output at 1 kHz, 32Ω load		–95		
	0 dB gain, full-scale output at 1 kHz, 16Ω load		–86	–75	
	0 dB gain, –3 dB output at 1 kHz, 16Ω load		–90		
PSRR	< 1 kHz		90		dB
	10 kHz		70		
Channel separation	2 dB gain, full-scale output at 1 kHz		–90		dB
Mute attenuation	1 kHz output		107		dB

(1) Default filter configuration
(2) Ratio of output level with 1-kHz full-scale sine wave input, to the output level playing an all-zero signal, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
(3) Measurements performed with stereo signals out of phase.

3.5 Electrical Characteristics – Power

At 25°C, AVDD_REG=AVDD_CP = 2.5 V, IOVDD = 3.3 V, DVDD = 1.8 V, Fs = 48-kHz, 16-bit audio data (unless otherwise noted)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT(1)						
Mono ADC channel, 8 kHz	AVDD_2P5(1)	PLL off, AGC off		4.6		mA
	DVDD			0.4		
Stereo ADC channel, 8 kHz	AVDD_2P5(1)	PLL off, AGC off		7.2		mA
	DVDD			0.5		
Stereo ADC channel, 48 kHz	AVDD_2P5(1)	PLL off, AGC off		8.6		mA
	DVDD			2.1		
Stereo DAC headphone, 48 kHz	AVDD_2P5(1)	Quiescent current (no signal)		10.4		mA
	DVDD			2.4		
Stereo DAC headphone(2), 48 kHz	AVDD_HP, AVDD_DAC	Quiescent current (no signal)		4.0		mA
	AVSS_HP, AVSS_DAC			–4.1		
	DVDD			2.4		
Stereo DAC headphone, Low Power Mode	AVDD_2P5	1.8V operation. See section 5.18.3.		5.7		mA
	DVDD			2.1		
Stereo DAC headphone, Ultra Low Power Mode	AVDD_2P5	1.5V operation. See section 5.18.3.		4.8		mA
	DVDD			1.9		
Stereo line in to lineout	AVDD_2P5(1)	Quiescent current (no signal)		11		mA
	DVDD			0.2		
PLL	AVDD_ADC	Additional power consumed when PLL is powered		1.3		mA
	DVDD			0.6		
Power down	AVDD_2P5(1)	All supply voltages applied, all blocks programmed in lowest power state		0.2		µA
	DVDD			0.5		

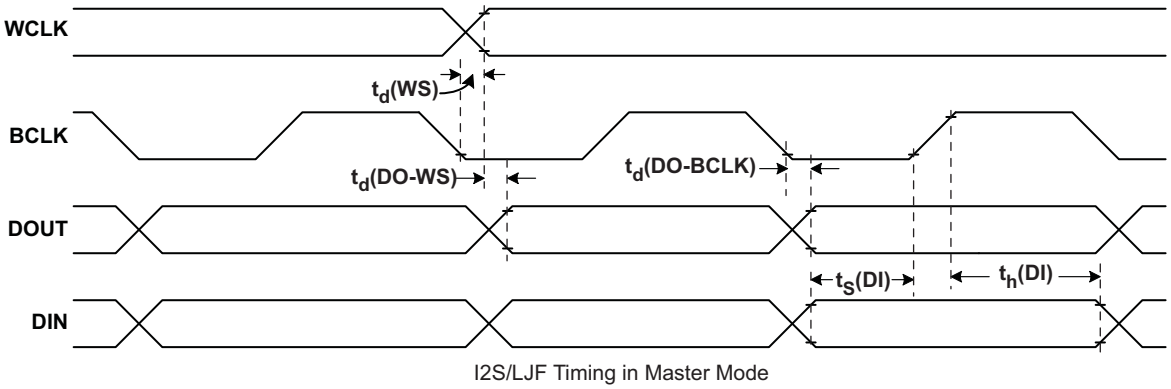
(1) Charge pump and regulators used. AVDD_2P5=AVDD_CP=AVDD_REG=AVDD_BIAS=2.5V
(2) Charge pump and regulators not used. AVDD_ADC=AVDD_HP=AVDD_DAC=AVDD_BIAS=1.65, AVSS_HP=AVSS_DAC=–1.65

3.6 Electrical Characteristics – I/O

At 25°C, DVDD = 1.8 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC FAMILY				**CMOS**		
V_{IH}	Logic level	I_{IH} = 5 μA, IOVDD > 1.6 V	0.7 × IOVDD			V
		I_{IH} = 5 μA, 1.2 V ≤ IOVDD <1.6 V	0.9 × IOVDD			V
		I_{IH} = 5 μA, IOVDD < 1.2 V	IOVDD			V
V_{IL}		I_{IL} = 5 μA, IOVDD > 1.6 V	–0.3		0.3 × IOVDD	V
		I_{IL} = 5 μA, 1.2 V ≤ IOVDD <1.6 V			0.1 × IOVDD	V
		I_{IL} = 5 μA, IOVDD < 1.2 V			0	V
V_{OH}		I_{OH} = 2 TTL loads	0.8 × IOVDD			V
V_{OL}		I_{OL} = 2 TTL loads			0.1 × IOVDD	V
	Capacitive load			10		pF
CLOCK INPUT MCLK						
		Rate			50	MHz
$t_{w(H)}$	Clock pulse width high		10			ns
$t_{w(L)}$	Clock pulse width low		10			ns
DIGMIC INPUT						
t_s	Setup relative to DIGMIC_CLK edge		25			ns
t_h	Hold relative to DIGMIC_CLK edge		0			ns

3.7 Timing — Audio Data Serial Interface Timing



NOTE: All numbers are from characterization and are not tested in final production.

Figure 3-1. I²S/LJF/RJF Timing in Master Mode

3.8 TYPICAL TIMING CHARACTERISTICS (see Figure 3-1)

All specifications at 25°C, DVdd = 1.8V

Table 3-1. I²S/LJF/RJF Timing in Master Mode

PARAMETER		IOVDD=1.8 V		IOVDD=3.3 V		UNITS
		MIN	MAX	MIN	MAX	
t_d(WS)	WCLK delay		25		15	ns
t_d(DO-WS)	WCLK to DOUT delay (for LJF Mode only)		20		10	ns
t_d(DO-BCLK)	BCLK to DOUT delay		40		30	ns
t_s(DI)	DIN setup	8		6		ns
t_h(DI)	DIN hold	8		6		ns
t_r	Rise time		9		4	ns
t_f	Fall time		9		4	ns

Note: All timing specifications are measured at characterization but are not tested at final test.

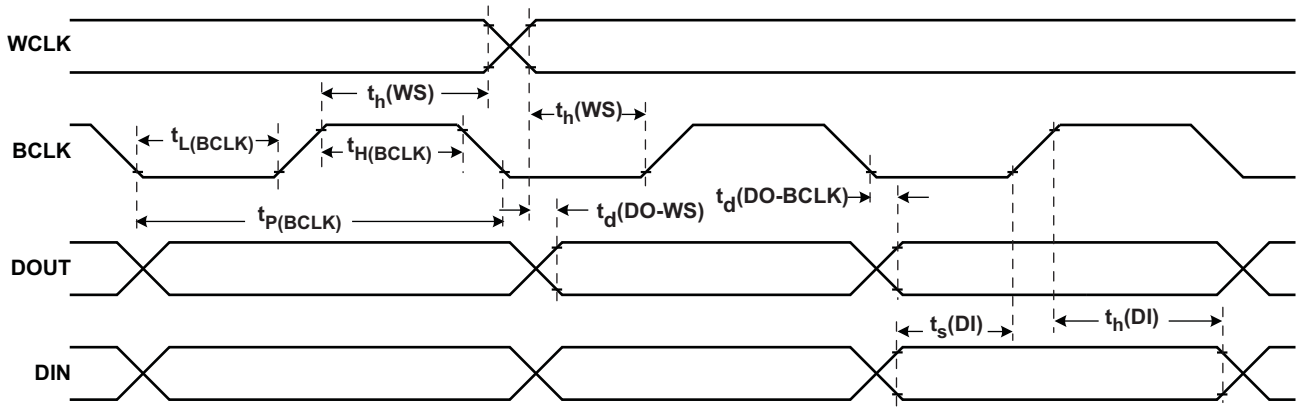


Figure 3-2. I²S/LJF/RJF Timing in Slave Mode

3.9 TYPICAL TIMING CHARACTERISTICS (see Figure 3-2)

All specifications at 25°C, DVdd = 1.8V

Table 3-2. I²S/LJF/RJF Timing in Slave Mode

PARAMETER		IOVDD=1.8 V		IOVDD=3.3 V		UNITS
		MIN	MAX	MIN	MAX	
$BCLK_H$(BCLK)	BCLK high period	35		35		ns
$BCLK_L$(BCLK)	BCLK low period	35		35		
t_s(WS)	WCLK setup	8		8		
t_h(WS)	WCLK hold	8		8		
t_d(DO-WS)	WCLK to DOUT delay (for LJF mode only)		30		20	
t_d(DO-BCLK)	BCLK to DOUT delay		30		20	
t_s(DI)	DIN setup	8		6		
t_h(DI)	DIN hold	8		6		
t_r	Rise time		8		4	
t_f	Fall time		8		4	

Note: All timing specifications are measured at characterization but are not tested at final test.

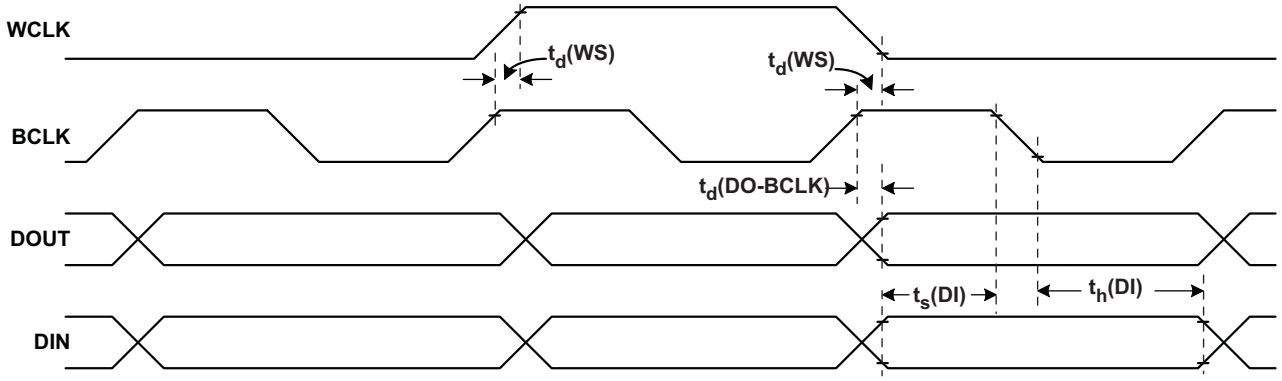


Figure 3-3. DSP Timing in Master Mode

3.9.1 Typical Timing Characteristics (see Figure 3-3)

All specifications at 25°C, DVdd = 1.8 V

Table 3-3. DSP Timing in Master Mode

PARAMETER		IOVDD=1.8 V		IOVDD=3.3 V		UNITS
		MIN	MAX	MIN	MAX	
t_d(WS)	WCLK delay		30		15	ns
t_d(DO-BCLK)	BCLK to DOUT delay		35		20	ns
t_s(DI)	DIN setup	8		6		ns
t_h(DI)	DIN hold	8		6		ns
t_r	Rise time		9		4	ns
t_f	Fall time		9		4	ns

Note: All timing specifications are measured at characterization but are not tested at final test.

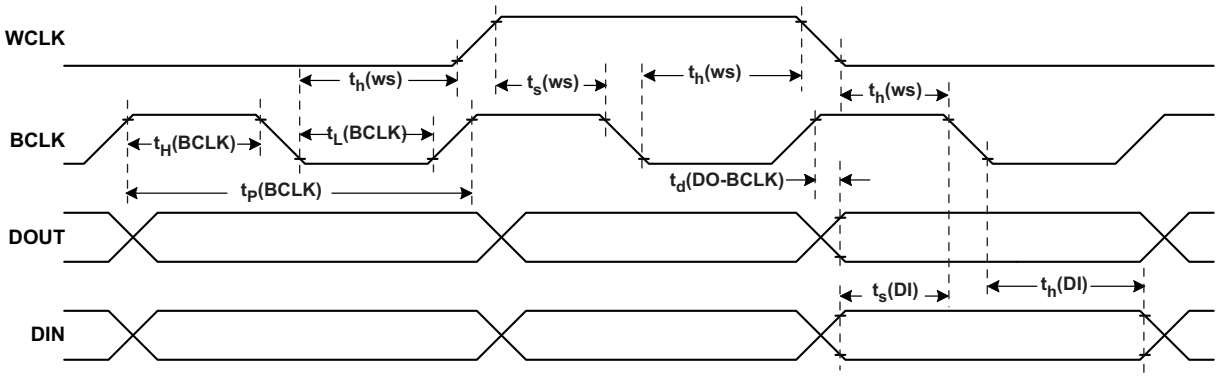


Figure 3-4. DSP Timing in Slave Mode

3.9.2 Typical Timing Characteristics (see Figure 3-4)

All specifications at 25°C, DVdd = 1.8 V

Table 3-4. DSP Timing in Slave Mode

PARAMETER		IOVDD=1.8 V		IOVDD=3.3 V		UNITS
		MIN	MAX	MIN	MAX	
t_H(BCLK)	BCLK high period	35		35		ns
t_L(BCLK)	BCLK low period	35		35		ns
t_s(WS)	WCLK setup	8		6		ns
t_h(WS)	WCLK hold	8		6		ns
t_d(DO-BCLK)	BCLK to DOUT delay		30		20	ns
t_s(DI)	DIN setup	8		6		ns
t_h(DI)	DIN hold	8		6		ns
t_r	Rise time		8		4	ns
t_f	Fall time		8		4	ns

Note: All timing specifications are measured at characterization but not tested at final test.

3.10 I²C Interface Timing

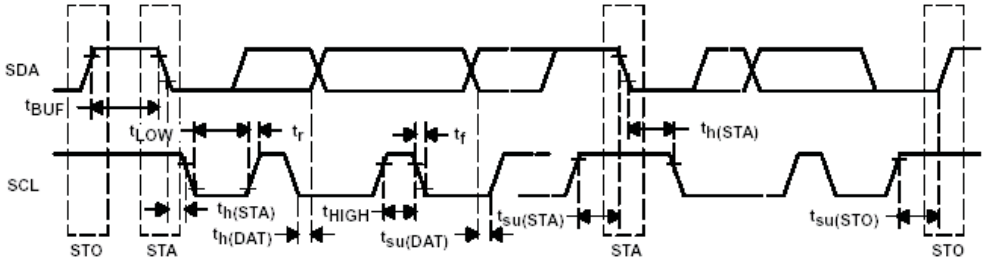


Figure 3-5.

Table 3-5. I²C INTERFACE TIMING

PARAMETER		TEST CONDITION	Standard-Mode			Fast-Mode			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{SCL}	SCL clock frequency		0		100	0		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.		4.0			0.8			µs
t_{LOW}	LOW period of the SCL clock		4.7			1.3			µs
t_{HIGH}	HIGH period of the SCL clock		4.0			0.6			µs
$t_{SU;STA}$	Setup time for a repeated START condition		4.7			0.8			µs
$t_{HD;DAT}$	Data hold time: For I²C bus devices		0		3.45	0		0.9	µs
$t_{SU;DAT}$	Data set-up time		250			100			ns
t_r	SDA and SCL rise time				1000	20+0.1C_b		300	ns
t_f	SDA and SCL fall time				300	20+0.1C_b		300	ns
$t_{SU;STO}$	Set-up time for STOP condition		4.0			0.8			µs
t_{BUF}	Bus free time between a STOP and START condition		4.7			1.3			µs
C_b	Capacitive load for each bus line				400			400	pF

3.11 Electrical Characteristics – ADC Channel Ultra Low Power Mode

At 25°C, AVDD_REG=AVDD_CP = 1.5 V, IOVDD = 1.5 V, DVDD = 1.5 V, Fs = 48-kHz, 16-bit audio data (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Full-scale input signal, differential inputs	0 dB gain		0.5		V_{RMS}
Full-scale input, single ended	6 dB gain		0.25		V_{RMS}
Signal-to-noise ratio, mic inputs(1) (2)	0 dB gain		87		dB
	+38 dB gain(3)		66		
Signal-to-noise ratio, line inputs(1) (2)	6 dB gain		87		dB
	+44 dB gain(4)		60		dB
Dynamic range, all inputs(1) (2)	0 dB gain, –60 dB input at 1-kHz		87		
Total harmonic distortion, line, internal mic, and external mic inputs	0 dB gain, –1 dB input at 1-kHz		–80		dB

(1) Ratio of output level with 1-kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.
(3) +6 dB input mix gain, +32 dB PGA gain
(4) +6 dB input mix gain, +38 dB PGA gain

Electrical Characteristics – ADC Channel Ultra Low Power Mode *(continued)*

At 25°C, AVDD_REG=AVDD_CP = 1.5 V, IOVDD = 1.5 V, DVDD = 1.5 V, Fs = 48-kHz, 16-bit audio data (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PSRR, all inputs, unregulated(5)	< 1-kHz, single-ended input		50		dB
	< 1-kHz, differential input		50		
Channel separation(6)	0 dB gain, –2 dB input at 1-kHz		–70		dB
Gain error	0 dB gain, 1-kHz input		0.7		dB
Programmable Gain Amplifier (PGA)	maximum gain		59.5		dB
PGA gain step			0.5		dB
Input resistance, line inputs	0 dB input mix gain		10		kΩ
	–12 dB input mix gain		40		
Input resistance, mic inputs	6 dB input mix gain		10		kΩ
	–6 dB input mix gain		40		
Input capacitance, all inputs			10		pF
DIGITAL DECIMATION FILTER(7)					
Filter gain from 0 to 0.39 Fs			0.1		dB
Filter gain at 0.4125 Fs			–0.25		dB
Filter gain at 0.45 Fs			–3		dB
Filter gain at 0.5 Fs			–17.5		dB
Filter gain from 0.55 Fs to 64 Fs			-75		dB
Filter group delay			17/Fs		sec
MICROPHONE BIAS GENERATORS					
Bias voltage	Programmable settings, 1 kΩ load		1.3		V
Current sourcing				2	mA
Power supply rejection ratio	< 1-kHz		48		dB

(5) AVDD_DAC and AVSS_DAC connected directly to supply
(6) Channel separation for any input connected to the ADC left channel and any other input connected to the ADC right channel
(7) Default filter configuration

3.12 Electrical Characteristics – DAC Channel Ultra Low Power Mode

At 25°C, AVDD AVDD_REG=AVDD_CP = 1.5 V, IOVDD = 1.5 V, DVDD = 1.5 V, Fs = 48-kHz, 16-bit audio data (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INTERPOLATION) FILTER(1)					
Passband	High-pass filter disabled			0.45×Fs	Hz
Passband ripple	High-pass filter disabled		0.06		dB
Transition band		0.45×Fs		0.55×Fs	Hz
Stop band		0.55×Fs		7.5×Fs	Hz
Stop band attenuation			65		dB
Group delay			21/Fs		sec
LINE OUTPUTS AT LOAD = 10 kΩ, 50 pF DIFFERENTIAL					
Full-scale output voltage	–5 dB gain		0.8		V_{RMS}
Maximum output level gain setting			–5		dB
Output level gain setting step			1		dB
Signal-to-noise ratio(2)	–5 dB gain, A-weighted, Full-scale output at 1-kHz		94		dB
Dynamic range	0 dB gain, A-weighted, –60 dB input at 1 kHz		94		dB
Total harmonic distortion	–5 dB gain, Full-scale output at 1 kHz		90		dB

(1) Default filter configuration
(2) Ratio of output level with 1-kHz full-scale sine wave input, to the output level playing an all-zero signal, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.

Electrical Characteristics – DAC Channel Ultra Low Power Mode *(continued)*

At 25°C, AVDD AVDD_REG=AVDD_CP = 1.5 V, IOVDD = 1.5 V, DVDD = 1.5 V, Fs = 48-kHz, 16-bit audio data (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	< 1 kHz		70		dB
	10 kHz		50		
Channel separation	-5 dB gain, Full-scale input at 1 kHz		–50		dB
Gain mismatch			0.1		dB
Gain error			–0.4		dB
RECEIVER AND HEADPHONE OUTPUTS(3)					
Full-scale output voltage	–5 dB gain		0.4		V_{RMS}
Full-scale output power	–5 dB gain, full-scale output at 1 kHz, 16Ω load		10		mW
Maximum output level gain setting			–5		dB
Output level gain setting step			1		dB
Signal-to-noise ratio(2)	–5 dB gain, A-weighted, Full-scale output at 1 kHz		89		dB
Total harmonic distortion	–5 dB gain, full-scale output at 1 kHz, 32Ω load		–80		dB
	–5 dB gain, –3 dB output at 1 kHz, 32Ω load		–80		
	–5 dB gain, full-scale output at 1 kHz, 16Ω load		–7		
	–5 dB gain, –3 dB output at 1 kHz, 16Ω load		–77		
PSRR	< 1 kHz		50		dB
	10 kHz		35		
Channel separation	–5 dB gain, full-scale output at 1 kHz		–65		dB
Mute attenuation	1 kHz output		107		dB

(3) Measurements performed with stereo signals out of phase.

4 TYPICAL CHARACTERISTICS

4.1 Typical Performance

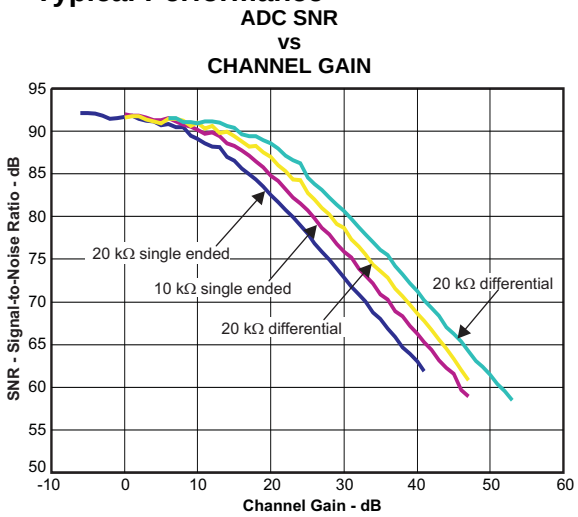


Figure 4-1.

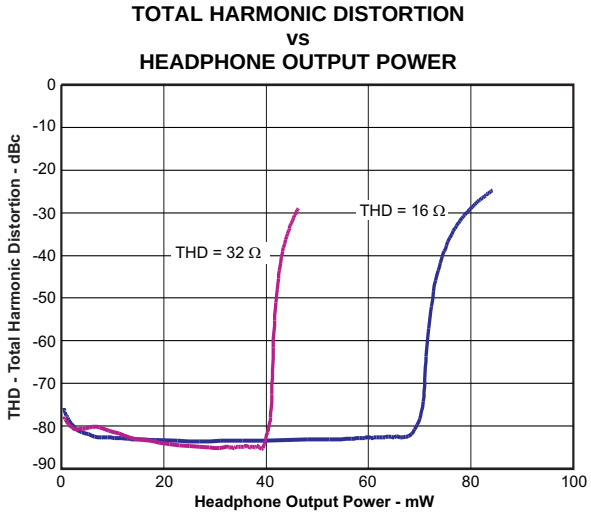


Figure 4-2.

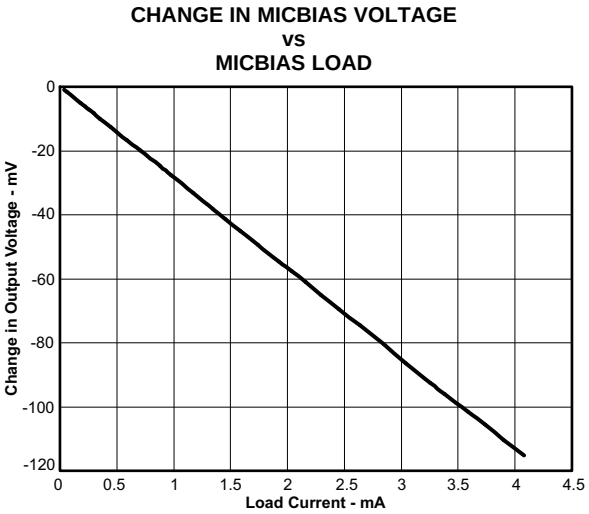


Figure 4-3.

4.2 FFT

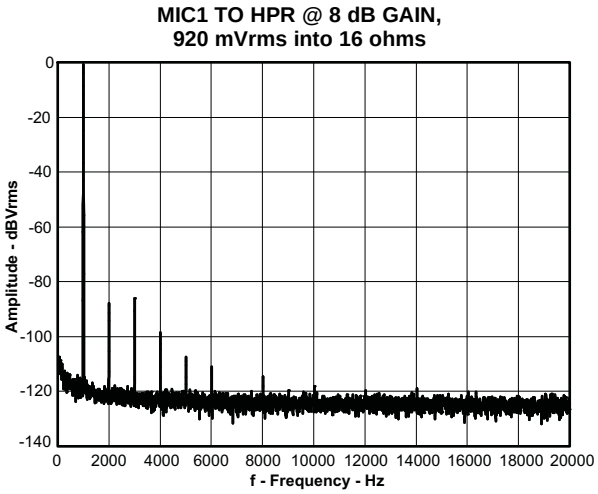


Figure 4-4.

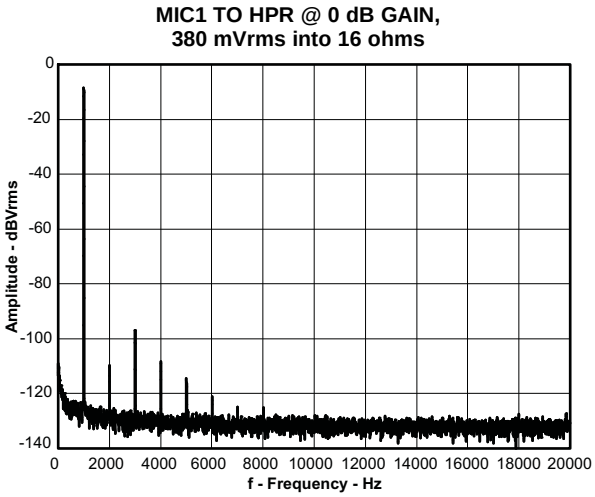


Figure 4-5.

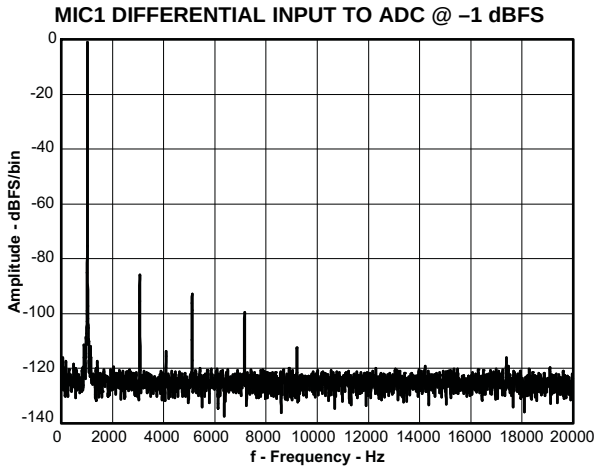


Figure 4-6.

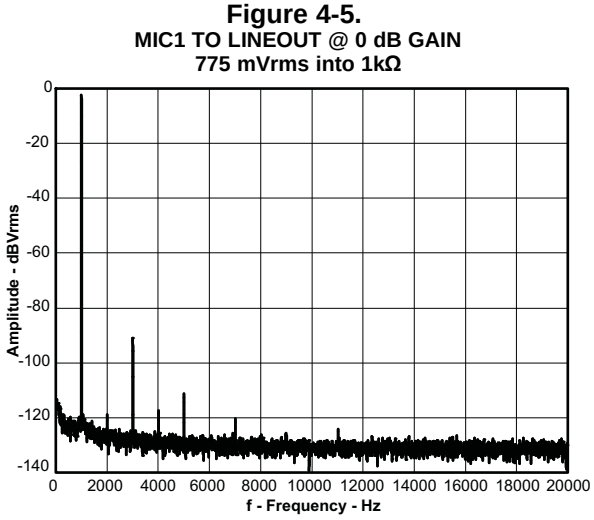


Figure 4-7.

MIC1 TO LINE OUT @ 6 dB GAIN,
1.5 Vrms into 1kΩ

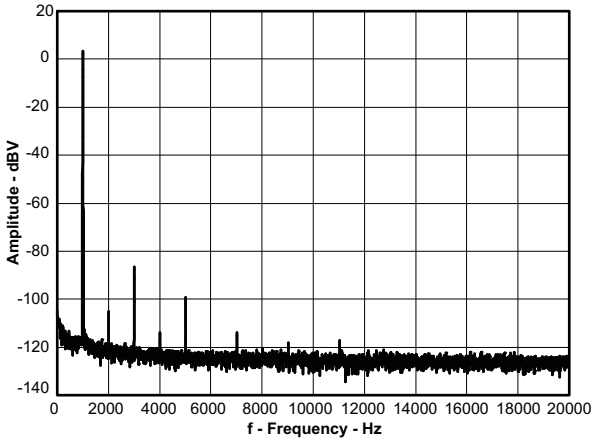


Figure 4-8.

DAC PLAYBACK TO HEADPHONE,
0 dB gain, 0.7 Vrms into 16Ω

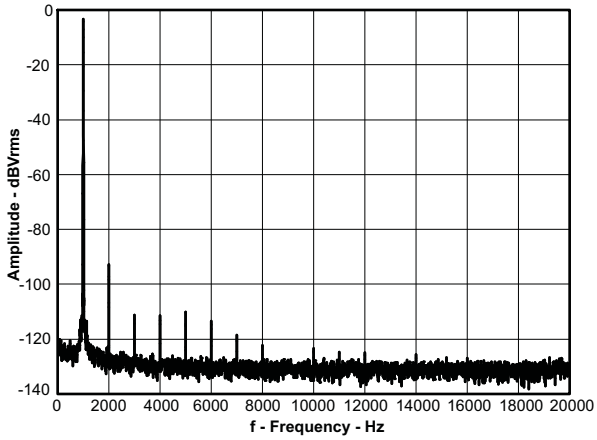


Figure 4-9.

DAC PLAYBACK TO LINE-OUT,
1.5 Vrms into 1kΩ

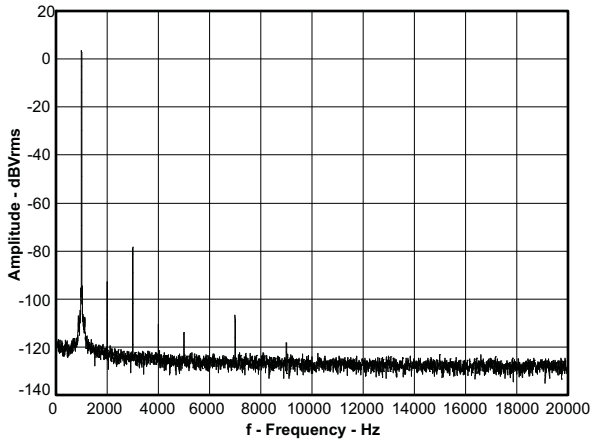


Figure 4-10.

CHANGE IN AVDD1 LDO VOLTAGE
vs
LDO LOAD

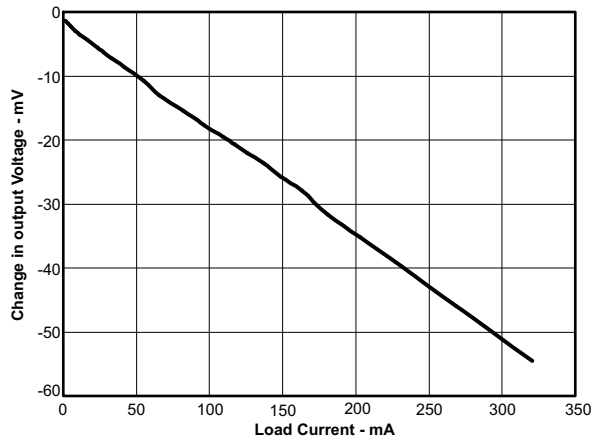


Figure 4-11.

AVDD1 LDO DROPOUT VOLTAGE
vs
LOAD CURRENT

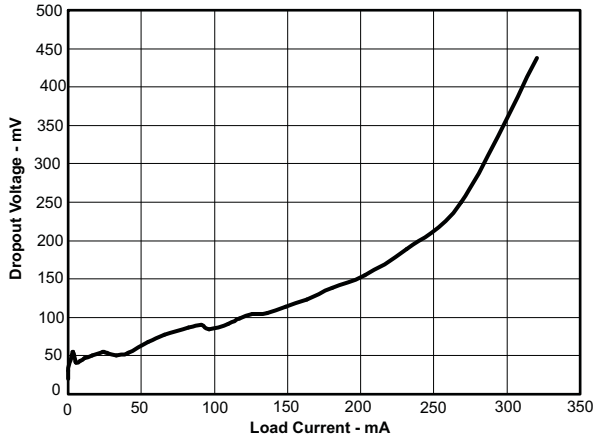


Figure 4-12.

5 APPLICATION INFORMATION

5.1 Typical Circuit Configuration

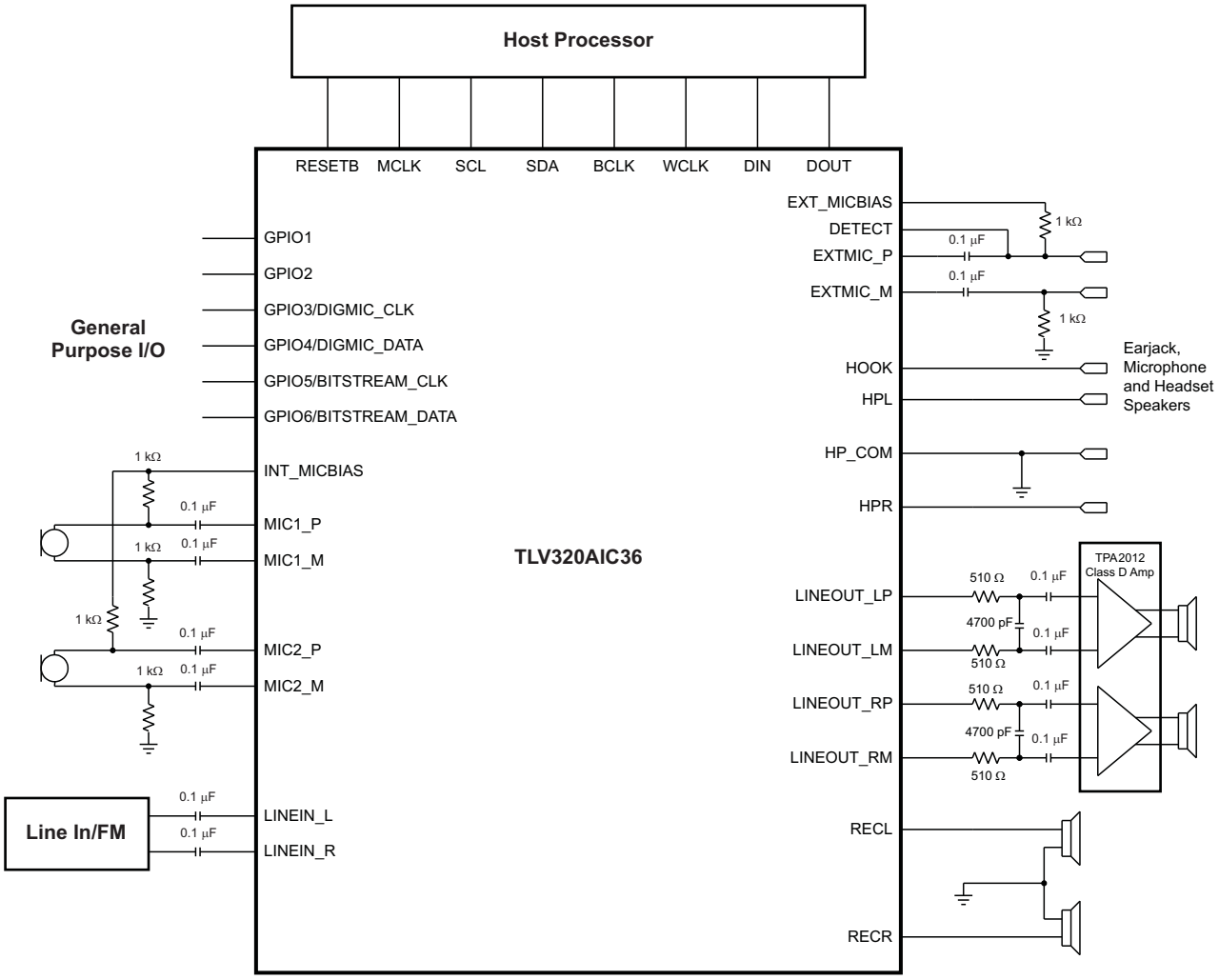


Figure 5-1. Typical Circuit Configuration

5.2 Overview

The TLV320AIC36 offers a wide range of configuration options. Figure 1-1 shows the basic functional blocks of the device.

5.2.1 Digital Pins

Only a small number of digital pins are dedicated to a single function; whenever possible, the digital pins have a default function, and also can be reprogrammed to cover alternative functions for various applications.

The fixed-function pins are RESETB, SDA, SCL, DIN, I2C_ADDR1, I2C_ADDR0, and MCLK. Other digital pins such as GPIO1–GPIO6, BCLK, WCLK, and DOUT, can be configured for various functions using register control.

5.2.2 Analog Pins

Analog functions can also be configured to a large degree. For minimum power consumption, analog blocks are powered down by default. The blocks can be powered up with fine granularity according to the application needs.

The possible analog routings of analog input pins to ADCs and output amplifiers as well as the routing from DACs to output amplifiers can be seen in Figure 5-2.

5.2.3 Power Supply

The TLV320AIC36 power management unit generates all of the analog supply voltages from a single nominal 2.5 V supply. The power management unit consists of two positive LDOs, one which generates a nominal +1.75 V supply for the input PGA and ADC section and another which generates a nominal +1.65 V for the DAC and audio amplifier section. A negative charge pump generates an unregulated negative voltage from the unregulated positive supply; a negative LDO generates a nominal –1.65 V supply for the DAC and audio amplifier section from this unregulated negative voltage. See Figure 5-48 for details on typical power supply connections.

5.2.4 Clocking

To minimize power consumption, the system ideally provides a master clock that is a suitable integer multiple of the desired sampling frequencies. In such cases, internal dividers can be programmed to set up the required internal clock signals at very low power consumption. For cases where such master clocks are not available, the built-in PLL can be used to generate a clock signal that serves as an internal master clock. In fact, this master clock can also be routed to an output pin and can be used elsewhere in the system. The clock system is flexible enough that it allows the internal clocks to be derived directly from an external clock source, while the PLL generates an other clock that is used only outside the TLV320AIC36.

5.3 miniDSP

The TLV320AIC36 features two miniDSP cores. The first miniDSP core is tightly coupled to the ADC, the second miniDSP core is tightly coupled to the DAC. The fully programmable algorithms for the miniDSP must be loaded into the device after power up. The miniDSPs have direct access to the digital stereo audio stream on the ADC and on the DAC side, offering the possibility for advanced, very low group delay DSP algorithms.

5.3.1 Software

Software development for the TLV320AIC36 is supported through TI's comprehensive PurePath Studio Development Environment. A powerful, easy-to-use tool designed specifically to simplify software development on the TI miniDSP audio platform. The Graphical Development Environment consists of a library of common audio functions that can be dragged-and-dropped into an audio signal flow and graphically connected together. The DSP code can then be assembled from the graphical signal flow with the click of a mouse.

Visit the TLV320AIC36 product folder on www.ti.com to learn more about PurePath Studio and the latest status on available, ready-to-use DSP algorithms.

5.4 Analog Routing

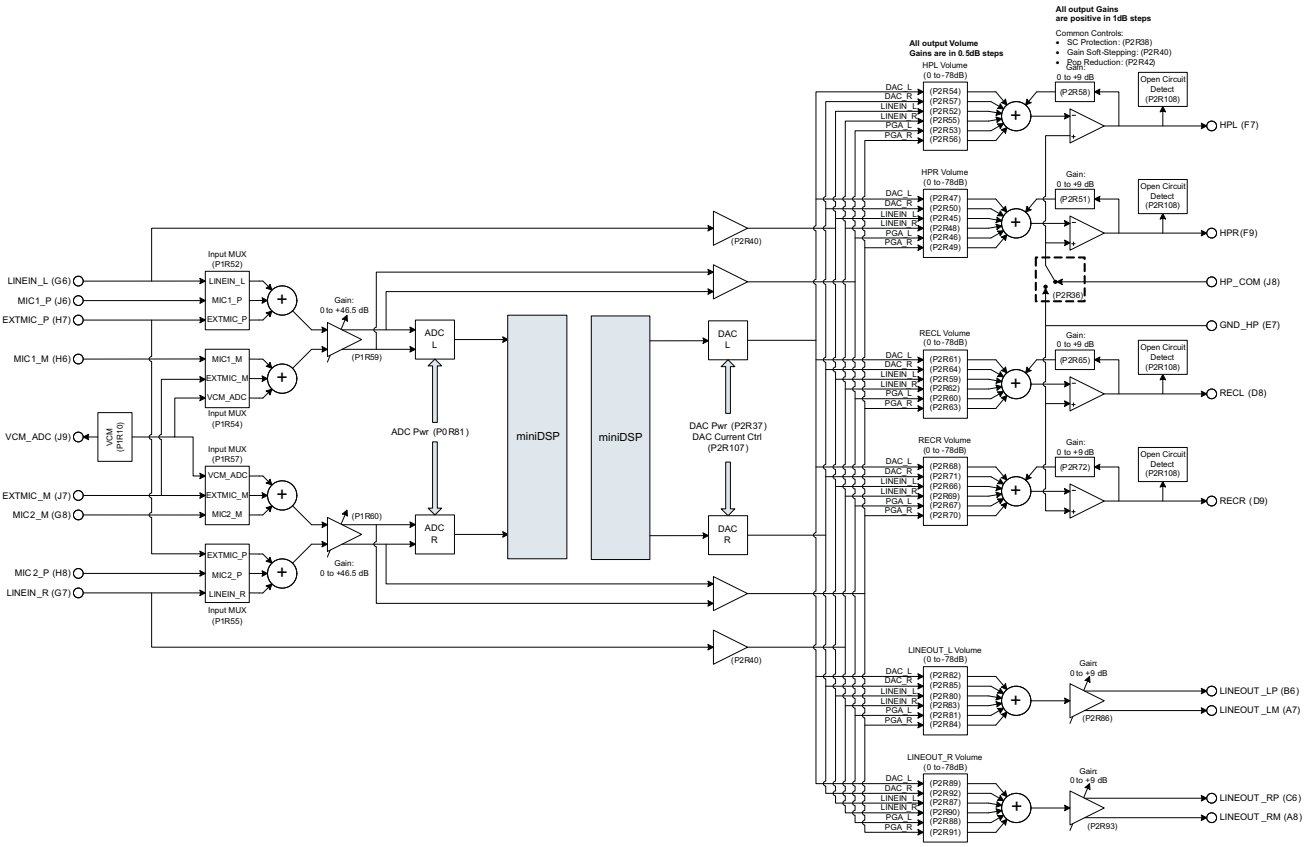


Figure 5-2. Analog Routing Diagram

5.4.1 Analog Bypass

The TLV320AIC36 offers two analog-bypass modes, line input bypass and PGA bypass mode. For these modes, all LDOs and the ADC must be enabled. The DAC does not need to be enabled to save power.

5.4.2 Line Input Bypass

This mode routes LINEINL/R to any of the output amplifiers by configuring Page 2, Register 40 and by programming the output amplifiers to select one or both line inputs. See Figure 5-2. Under normal bypass operation, the line inputs are AC-coupled to the LINEIN_L/LINEIN_R pins. The ADC generates an internal commode mode voltage for these signals before the bypass amplifiers. The bypass amplifiers have a fixed gain of 0 dB for single-ended output to HPL_R and RECL_R, and 6-dB gain for differential output to LINEOUT_L/LINEOUT_R.

To save power, the ADC can be disabled and an external common mode voltage can be generated for these pins. A simple 20kΩ/20kΩ resistor divider from AVDD_ADC to GND_ADC is sufficient with some compromise in performance.

5.4.3 PGA Bypass

In this mode, the mic or line input signals are amplified by the PGA and routed to the output amplifiers. See figure 5-2. This mode is enabled by selecting the input mux, setting the PGA gain, and programming the output amplifiers to select one or both PGA outputs.

The ADC must be enabled to supply biasing to the PGA. The bypass amplifiers have a fixed gain of –6 dB for single-ended output to HP_L/HP_R and REC_L/REC_R, and 0 dB gain for differential output to LINEOUT_L/LINEOUT_R

5.4.4 Line Input Routing

To avoid excessive internal DC offset, the line inputs should be routed to the Headphone Outputs whenever the line inputs are activated, even if the bypass paths to the Headphone Outputs are not needed. This can be accomplished by writing 1 to bit D7 of registers 45 and 55 in Page 2. If the line input-to-headphone output bypass paths are not needed, they can be muted in the same registers.

5.5 Device Initialization

5.5.1 Reset

The TLV320AIC36 internal logic must be initialized to a known condition for proper device function. To initialize the device in its default operating condition, the hardware reset pin (RESETB) must be pulled low for at least 100 ns. For this initialization to work, the IOVDD and DVdd supplies must be powered up. It is recommended that while the DVdd supply is being powered up, the RESETB pin be pulled low.

The device can also be reset through software by writing 1 into Page 0, Register 1 followed by writing 0 into Page 0, Register 1. After a device reset, all registers are initialized with default values as listed in the Register Map section.

5.5.2 Device Startup Lockout Times

After the is initialized through hardware reset at power-up or software reset, the internal memories are initialized to default values. This initialization occurs within 1 ms after pulling the RESETB signal high. During this initialization phase, no Register read or Register write operation should be performed on ADC or DAC coefficient buffers. Also, no block within the codec should be powered up during the initialization phase.

5.5.3 PLL Startup

Whenever the PLL is powered up, a startup delay of approximately of 10 ms is involved after the power up command of the PLL and before the clocks are available to the codec. This delay enables stable operation of PLL and clock-divider logic.

5.6 ADC

5.6.1 Concept

The TLV320AIC36 includes a stereo audio ADC, which uses a delta-sigma modulator with a programmable oversampling ratio, followed by a digital decimation filter. The ADC supports sampling rates from 8 to 192 kHz. To provide optimal system power management, the stereo ADC can be powered up one channel at a time, to support the case where only mono record capability is required. In addition, both channels can be fully powered or entirely powered down. Because of the oversampling nature of the audio ADC and the integrated digital decimation filtering, requirements for analog anti-aliasing filtering are very relaxed. The TLV320AIC36 integrates a second-order analog anti-aliasing filter with 28-dB attenuation at 6 MHz. This filter, combined with the digital decimation filter, provides sufficient anti-aliasing filtering without requiring additional external components.

5.6.2 Routing

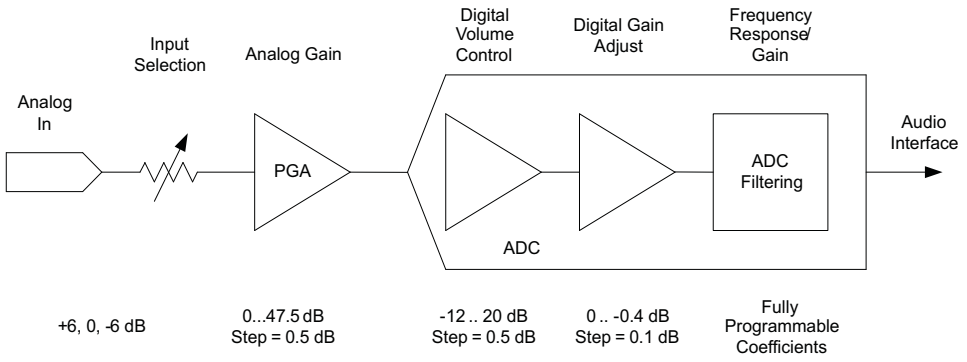
As shown in Figure 5-2, the TLV320AIC36 includes eight analog inputs that can be connected to two fully differential input amplifiers (one per ADC/PGA channel). By turning on only one set of switches per amplifier at a time, the inputs can be effectively multiplexed to each ADC/PGA channel. By turning on multiple sets of switches per amplifier at a time, audio sources can be mixed.

In most applications, high-input impedance is desired for analog inputs. However when used with high gain, as in the case of microphone inputs, the higher-input impedance results in higher noise or lower dynamic range. The TLV320AIC36 gives the user the flexibility of choosing the input impedance from 10kΩ, 20kΩ and 40kΩ. When multiple inputs are mixed together, by choosing different input impedances, level adjustment can be achieved. For example, if one input is selected with 10kΩ input impedance and the second input is selected with 20kΩ input impedance, then the second input is attenuated by half as compared to the first input. This input level control is intended to be a volume control, but instead used for level setting.

Mixing of multiple inputs can easily lead to PGA outputs that exceed the range of the internal amplifiers, resulting in saturation and clipping of the mixed output signal. Whenever mixing is being implemented, the system designer is advised to take adequate precautions to avoid such a saturation from occurring. In general, the mixed (summed) signal should not exceed 0 dB.

Typically, voice or audio signal inputs are capacitively coupled to the device. This allows the device to independently set the common mode of the input signals to values chosen by register control of Page 1, Register 10, D(6) to either 0.9 V or 0.75 V. The correct value maximizes the dynamic range across the entire analog-supply range. Failure to capacitively connect the input to the device can cause high offset due to mismatch in source common-mode and device common-mode setting. In extreme cases it could also saturate the analog channel, causing distortion.

5.7 ADC Gain Setting



When the gain of the ADC channel is kept at 6 dB and the common mode is set to 0.75 V, a single-ended input of 0.375 V_{RMS} results in a full-scale digital signal at the output of ADC channel. Similarly, when the gain is kept at 6 dB, and common mode is set to 0.9 V, a single-ended input of 0.5 V_{RMS} results in a full-scale digital signal at the output of the ADC channel. However various block functions control the gain through the channel. The gain applied by the PGA is described in Table 5-1. Additionally, the digital volume control adjusts the gain through the channel, as described in Section 5.7.2. A finer level of gain is controlled by fine gain control, as described in Section 5.7.3. The decimation filters A, B, and C along with the delta-sigma modulator contribute to a DC gain of 1.0 through the channel.

5.7.1 Analog PGA

The TLV320AIC36 features a built-in low-noise PGA for boosting low-level signals, such as direct microphone inputs, to full-scale to achieve high SNR. This PGA can provide a gain in the range of 0 dB to 47.5 dB for single-ended inputs or 6 dB to 53.5 dB for fully differential inputs (gain calculated with respect to input impedance setting of 10kΩ; 20kΩ input impedance will result in 6 dB lower and 40kΩ will result in 12 dB lower gain). This gain can be user controlled by writing to Page 1, Register 59 and Page 1, Register 60. In the AGC mode this gain can also be automatically controlled by the built-in hardware AGC.

Table 5-1. Analog PGA vs Input Configuration

Page 1, Register 59, D(6:0) Page 1, Register 60, D(6:0)	EFFECTIVE GAIN APPLIED BY PGA					
	SINGLE-ENDED			DIFFERENTIAL		
	R_{IN} = 10K	R_{IN} = 20K	R_{IN} = 40K	R_{IN} = 10K	R_{IN} = 20K	R_{IN} = 40K
000 0000	0 dB	–6 dB	–12 dB	6.0 dB	0 dB	–6.0 dB
000 0001	0.5 dB	–5.5 dB	–11.5 dB	6.5 dB	0.5 dB	–5.5 dB
000 0010	1.0 dB	–5.0 dB	–11.0 dB	7.0 dB	7.5 dB	–5.0 dB
…	…	…	…	…	…	…
101 1110	47.0 dB	41.0 dB	35.0 dB	53.0 dB	47.0 dB	41.0 dB
101 1111	47.5 dB	41.5 dB	35.5 dB	53.5 dB	47.5 dB	41.5 dB

The gain changes are implemented with an internal soft-stepping algorithm that only changes the actual volume level by one 0.5-dB step every one or two ADC output samples, depending on the register value (see registers Page 0, Reg 81, D(1:0)). This soft-stepping enables smooth volume-control changes with no audible artifacts. On reset, the PGA gain defaults to a mute condition, and at power down, the PGA soft-steps the volume to mute before shutting down. A read-only flag Page 0, Reg 36, D(7) and D(3) is set whenever the gain applied by the PGA equals the desired value set by the register. The soft-stepping control can also be disabled by programming Page 0, Reg 81, D(1:0).

5.7.2 Digital Volume Control

The TLV320AIC36 also has a digital volume-control block with a range from –12 dB to +20 dB in steps of 0.5-dB. It is set by programming Page 0, Register 83 and 84, respectively, for left and right channels.

Table 5-2. Digital Volume Control for ADC

Desired Gain (dB)	Left/Right Channel Page 1, Register 83/84, D(6:0)
–12.0	110 1000
–11.5	110 1001
–11.0	110 1010
..	
–0.5	111 1111
0.0	000 0000 (default)
+0.5	000 0001
..	
+19.5	010 0111
+20.0	010 1000

During volume control changes, the soft-stepping feature is used to avoid audible artifacts. The soft-stepping rate can be set to either 1 or 2 gain steps per sample. Soft-stepping can also be entirely disabled. This soft-stepping is configured using Page 1, Register 81, D(1:0), and is common to soft-stepping control for the analog PGA. During power-down of an ADC channel, this volume control soft-steps down to –12.0 dB before powering down. Due to the soft-stepping control, soon after changing the volume control setting or powering down the ADC channel, the actual applied gain may be different from the one programmed through the control register. The TLV320AIC36 gives feedback to the user, through read-only flags Page 1, Reg 36, D(7) for the Left Channel and Page 1, Reg 36, D(3) for the right channel.

5.7.3 Fine Digital Gain Adjustment

Additionally, the gains in each of the channels is finely adjustable in steps of 0.1 dB. This is useful when trying to match the gain between channels. By programming Page 0, Register 82 the gain can be adjusted from 0 dB to -0.4 dB in steps of 0.1 dB. This feature, in combination with the regular digital volume control allows the gains through the left and right channels be matched in the range of -0.5 dB to +0.5 dB with a resolution of 0.1 dB.

5.7.4 AGC

The TLV320AIC36 includes Automatic Gain Control (AGC) for ADC recording. AGC can be used to maintain a nominally-constant output level when recording speech. As opposed to manually setting the PGA gain, in the AGC mode, the circuitry automatically adjusts the PGA gain as the input signal becomes overly loud or very weak, such as when a person speaking into a microphone moves closer or farther from the microphone. The AGC algorithm has several programmable parameters, including target gain, attack and decay time constants, noise threshold, and max PGA applicable, that allow the algorithm to be fine tuned for any particular application. The algorithm uses the absolute average of the signal (which is the average of the absolute value of the signal) as a measure of the nominal amplitude of the output signal. Since the gain can be changed at the sample interval time, the AGC algorithm operates at the ADC sample rate.

- **Target level** represents the nominal output level at which the AGC attempts to hold the ADC output signal level. The TLV320AIC36 allows programming of eight different target levels, which can be programmed from –5.5 to –24 dB relative to a full-scale signal. Since the TLV320AIC36 reacts to the signal absolute average and not to peak levels, it is recommended that the target level be set with enough margin to avoid clipping at the occurrence of loud sounds.
- **Attack time** determines how quickly the AGC circuitry reduces the PGA gain when the output signal level exceeds the target level due to increase in input signal level. Wide range of attack time programmability is supported in terms of number of samples (i.e. number of ADC sample frequency clock cycles).
- **Decay time** determines how quickly the PGA gain is increased when the output signal level falls below the target level due to reduction in input signal level. Wide range of decay time programmability is supported in terms of number of samples (i.e., number of ADC sample frequency clock cycles).
- **Noise threshold** determines the level below which if the input signal level falls, the AGC considers it as silence, and thus brings down the gain to 0 dB in steps of 0.5 dB every FS and sets the noise threshold flag. The gain stays at 0 dB unless the input speech signal average rises above the noise threshold setting. This s that noise is not 'gained up' in the absence of speech. Noise threshold level in the AGC algorithm is programmable from -30 dB to -90 dB of full-scale. When AGC Noise Threshold is set to –70 dB, –80 dB, or –90 dB, the microphone input Max PGA applicable setting must be greater than or equal to 11.5 dB, 21.5 dB, or 31.5 dB respectively. This operation includes hysteresis and debounce to avoid the AGC gain from cycling between high gain and 0 dB when signals are near the noise threshold level. The noise (or silence) detection feature can be entirely disabled by the user.
- **Max PGA applicable** allows the designer to restrict the maximum gain applied by the AGC. This can be used for limiting PGA gain in situations where environmental noise is greater than the programmed noise threshold. Microphone input Max PGA can be programmed from 0 dB to 63.5 dB in steps of 0.5 dB.
- **Hysteresis**, as the name suggests, determines a window around the Noise Threshold which must be exceeded to either detect that the recorded signal is indeed noise or signal. If initially the energy of the recorded signal is greater than the Noise Threshold, then the AGC recognizes it as noise only when the energy of the recorded signal falls below the Noise Threshold by a value given by Hysteresis. Similarly, after the recorded signal is recognized as noise, for the AGC to recognize it as a signal, its energy must exceed the Noise Threshold by a value given by the Hysteresis setting. In order to prevent the AGC from jumping between noise and signal states, (which can happen when the energy of recorded signal is very close to the Noise threshold) a non-zero hysteresis value should be chosen. The Hysteresis feature can also be disabled.

- **Debounce time (noise and signal)** determines the hysteresis in time domain for noise detection. The AGC continuously calculates the energy of the recorded signal. If the calculated energy is less than the set Noise Threshold, then the AGC does not increase the input gain to achieve the Target Level. However, to handle audible artifacts which can occur when the energy of the input signal is very close to the Noise Threshold, the AGC checks if the energy of the recorded signal is less than the Noise Threshold for a time greater than the Noise Debounce Time. Similarly the AGC starts increasing the input-signal gain to reach the Target Level when the calculated energy of the input signal is greater than the Noise Threshold. Again, to avoid audible artifacts when the input-signal energy is very close to Noise Threshold, the energy of the input signal needs to continuously exceed the Noise Threshold value for the Signal Debounce Time. If the debounce times are kept very small, then audible artifacts can result by rapidly enabling and disabling the AGC function. At the same time, if the Debounce time is kept too large, then the AGC may take time to respond to changes in levels of input signals with respect to Noise Threshold. Both noise and signal debounce time can be disabled.
- The **AGC noise threshold flag** is a read-only flag indicating that the input signal has levels lower than the Noise Threshold, and thus is detected as noise (or silence). In such a condition the AGC applies a gain of 0 dB.
- **Gain applied by AGC** is a read-only register setting which gives a real-time feedback to the system on the gain applied by the AGC to the recorded signal. This, along with the Target Setting, can be used to determine the input signal level. In a steady state situation
  Target Level (dB) = Gain Applied by AGC (dB) + Input Signal Level (dB)
  When the AGC noise threshold flag is set, then the status of gain applied by AGC should be ignored.
- The **AGC saturation flag** is a read-only flag indicating that the ADC output signal has not reached its Target Level. However, the AGC is unable to increase the gain further because the required gain is higher than the Maximum Allowed PGA gain. Such a situation can happen when the input signal has very low energy and the Noise Threshold is also set very low. When the AGC noise threshold flag is set, the status of AGC saturation flag should be ignored.
- The **ADC saturation flag** is a read-only flag indicating an overflow condition in the ADC channel. On overflow, the signal is clipped and distortion results. This typically happens when the AGC Target Level is kept very high and the energy in the input signal increases faster than the Attack Time.
- An **AGC low-pass filter** is used to help determine the average level of the input signal. This average level is compared to the programmed detection levels in the AGC to provide the correct functionality. This low-pass filter is in the form of a first-order IIR filter. Two 8-bit registers are used to form the 16-bit digital coefficient as shown on the register map. In this way, a total of six registers are programmed to form the three IIR coefficients. The transfer function of the filter implemented for signal level detection is given by:

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{15} - D_1 z^{-1}} \quad (1)$$

Where:

Coefficient N0 can be programmed by writing into Page 4, Registers 2 and 3.
Coefficient N1 can be programmed by writing into Page 4, Registers 4 and 5.
Coefficient D1 can be programmed by writing into Page 4, Registers 6 and 7.
N0, N1, and D1 are 16-bit 2's complement numbers and their default values implement a low-pass filter with cut-off at 0.002735*ADC_FS.

See Table 5-3 for various AGC programming options. AGC can be used only if analog microphone input is routed to the ADC channel.

Table 5-3. AGC Parameter Settings

Function	Control Register Left ADC	Control Register Right ADC	Bit
AGC enable	Page 0, Register 86	Page 0, Register 94	D(7)
Target level	Page 0, Register 86	Page 0, Register 94	D(6:4)

Table 5-3. AGC Parameter Settings (continued)

Function	Control Register Left ADC	Control Register Right ADC	Bit
Hysteresis	Page 0, Register 87	Page 0, Register 95	D(7:6)
Noise threshold	Page 0, Register 87	Page 0, Register 95	D(5:1)
Max PGA applicable	Page 0, Register 88	Page 0, Register 96	D(6:0)
Time constants (attack time)	Page 0, Register 89	Page 0, Register 97	D(7:0)
Time constants(decay time)	Page 0, Register 90	Page 0, Register 98	D(7:0)
Debounce time (Noise)	Page 0, Register 91	Page 0, Register 99	D(4:0)
Debounce time (Signal)	Page 0, Register 92	Page 0, Register 100	D(3:0)
Gain applied by AGC	Page 0, Register 93	Page 0, Register 101	D(7:0) (Read Only)
AGC Noise Threshold Flag	Page 0, Register 42 (sticky flag), Page 0, Register 43 (nonsticky flag)	Page 0, Register 42 (sticky flag), Page 0, Register 43 (nonsticky flag)	D(3:2) (Read Only)
AGC Saturation flag	Page 0, Register 36 (sticky flag)	Page 0, Register 36 (sticky flag)	D(5), D(1) (Read Only)
ADC Saturation flag	Page 0, Register 38 (sticky flag), Page 0, Register 39 (nonsticky flag)	Page 0, Register 38 (sticky flag), Page 0, Register 39 (nonsticky flag)	D(4:3) (Read Only)

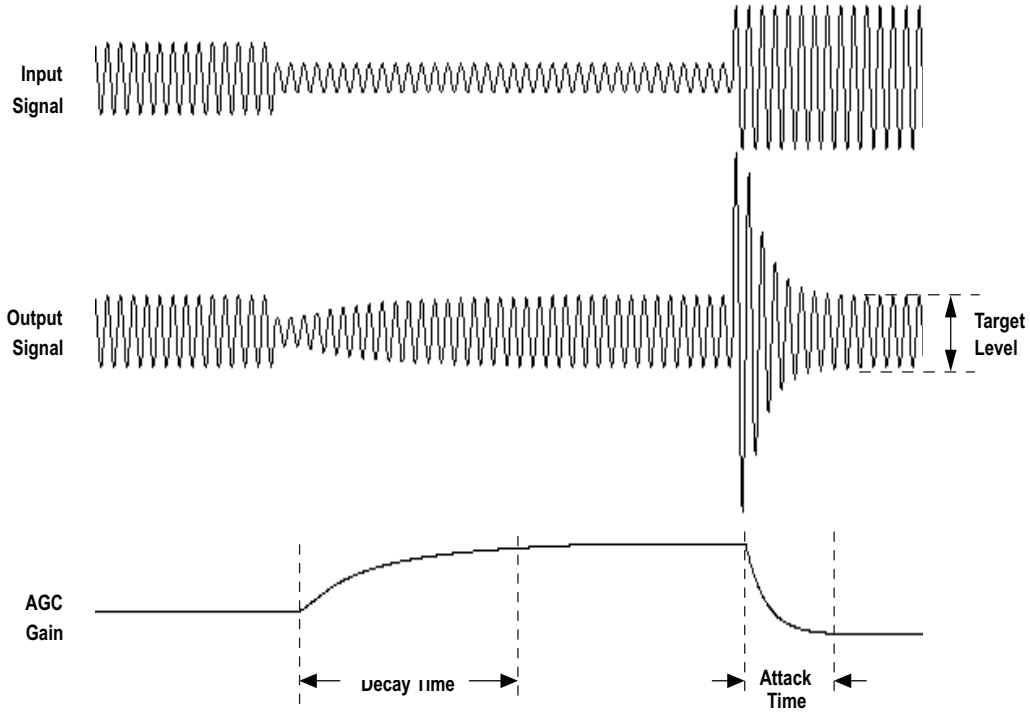


Figure 5-3. AGC Characteristics

5.8 ADC Decimation Filtering and Signal Processing

The TLV320AIC36 ADC channel includes a built-in digital decimation filter to process the oversampled data from the sigma-delta modulator to generate digital data at Nyquist sampling rate with high dynamic range. The decimation filter can be chosen from three different types, depending on the required frequency response, group delay and sampling rate.

5.8.1 Processing Blocks

The TLV320AIC36 offers a range of processing blocks which implement various signal processing capabilities along with decimation filtering. These processing blocks give users the choice of how much and what type of signal processing they may use and which decimation filter is applied.

The choice between these processing blocks is part of a strategy to balance power conservation and signal-processing flexibility. Less signal-processing capability reduces the power consumed by the device. Table 5-4 gives an overview of the available processing blocks of the ADC channel and their properties. The Resource Class (RC) Column gives an approximate indication of power consumption. Page 0, Register 61 is used to select one of the 18 processing blocks.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- Variable-tap FIR filter
- AGC

The processing blocks are tuned for common cases and can achieve high anti-alias filtering or low-group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first-order IIR, BiQuad, and FIR filters have fully user programmable coefficients.

Table 5-4. ADC Processing Blocks

Processing Blocks	Channel	Decimation Filter	First-Order IIR Available	Number BiQuads	FIR	Required AOSR Value	Resource Class
PRB_R1	Stereo	A	Yes	0	No	128,64	6
PRB_R2	Stereo	A	Yes	5	No	128,64	8
PRB_R3	Stereo	A	Yes	0	25-Tap	128,64	8
PRB_R4	Right	A	Yes	0	No	128,64	3
PRB_R5	Right	A	Yes	5	No	128,64	4
PRB_R6	Right	A	Yes	0	25-Tap	128,64	4
PRB_R7	Stereo	B	Yes	0	No	64	3
PRB_R8	Stereo	B	Yes	3	No	64	4
PRB_R9	Stereo	B	Yes	0	20-Tap	64	4
PRB_R10	Right	B	Yes	0	No	64	2
PRB_R11	Right	B	Yes	3	No	64	2
PRB_R12	Right	B	Yes	0	20-Tap	64	2
PRB_R13	Stereo	C	Yes	0	No	32	3
PRB_R14	Stereo	C	Yes	5	No	32	4
PRB_R15	Stereo	C	Yes	0	25-Tap	32	4
PRB_R16	Right	C	Yes	0	No	32	2
PRB_R17	Right	C	Yes	5	No	32	2
PRB_R18	Right	C	Yes	0	25-Tap	32	2

5.8.2 Processing Blocks – Details

5.8.2.1 First-Order IIR, AGC, Filter A

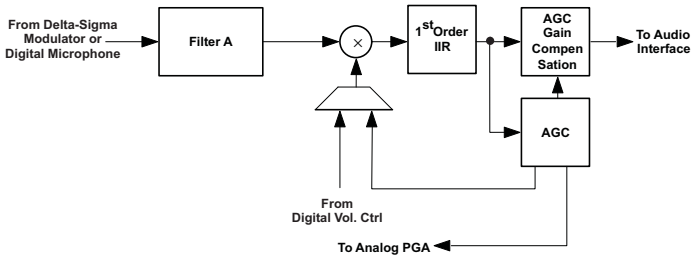


Figure 5-4. Signal Chain for PRB_R1 and PRB_R4

5.8.2.2 Five Biquads, First-Order IIR, AGC, Filter A

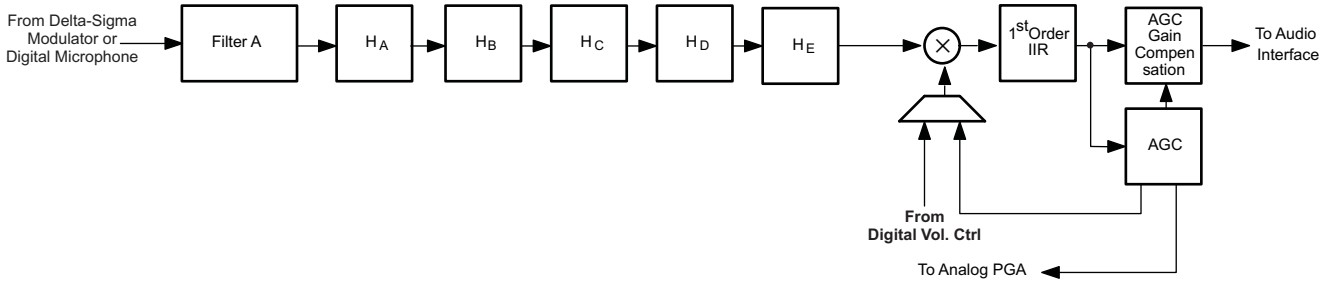


Figure 5-5. Signal Chain PRB_R2 and PRB_R5

5.8.2.3 25-Tap FIR, First-Order IIR, AGC, Filter A

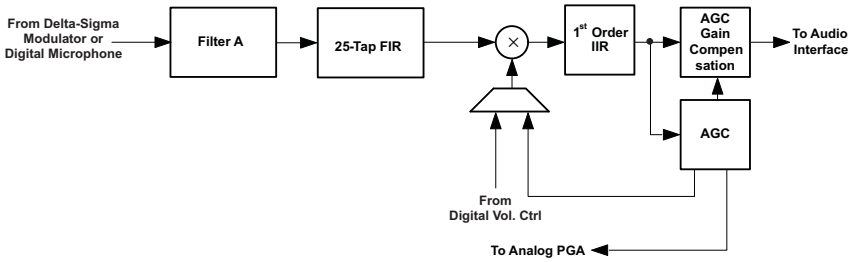


Figure 5-6. Signal Chain for PRB_R3 and PRB_R6

5.8.2.4 First-Order IIR, AGC, Filter B

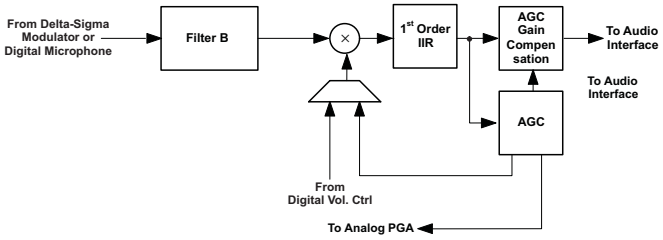


Figure 5-7. Signal Chain for PRB_R7 and PRB_R10

5.8.2.5 Three Biquads, First-Order IIR, AGC, Filter B

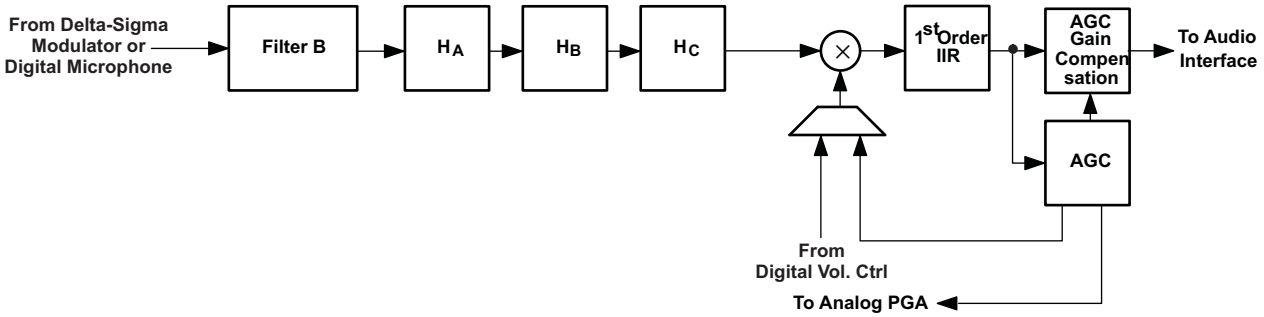


Figure 5-8. Signal Chain for PRB_R8 and PRB_R11

5.8.2.6 20-Tap FIR, First-Order IIR, AGC, Filter B

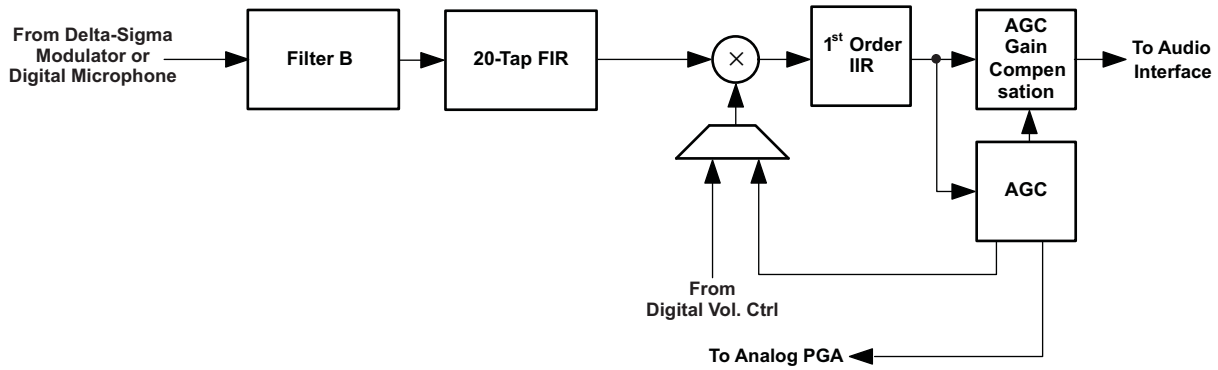


Figure 5-9. Signal Chain for PRB_R9 and PRB_R12

5.8.2.7 First-Order IIR, AGC, Filter C

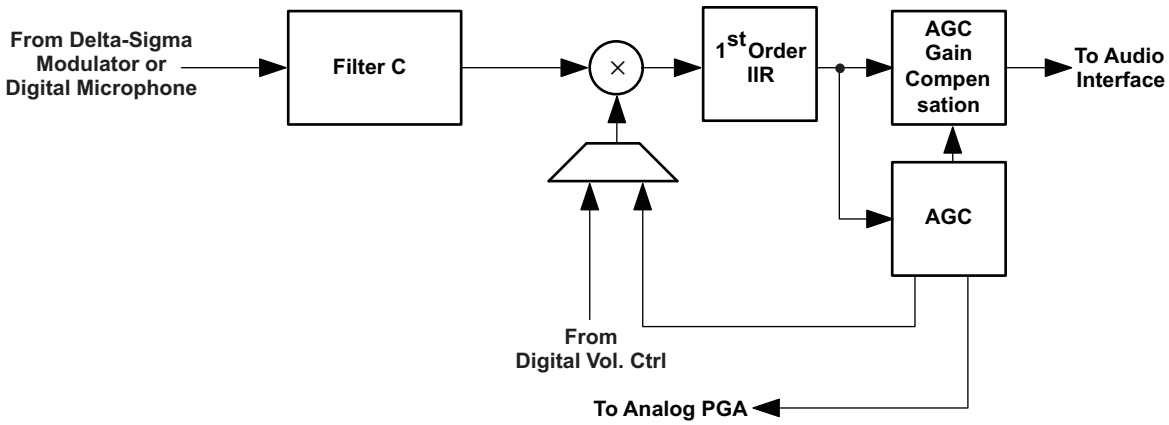


Figure 5-10. Signal Chain for PRB_R13 and PRB_R16

5.8.2.8 Five Biquads, First-Order IIR, AGC, Filter C

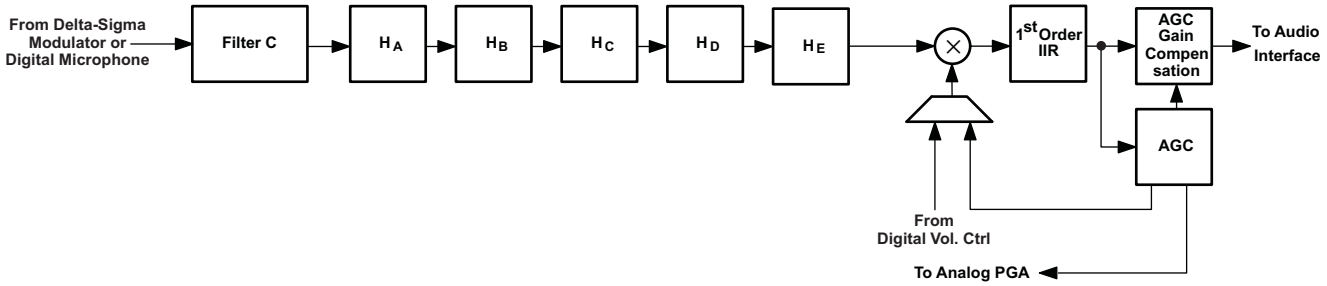


Figure 5-11. Signal Chain for PRB_R14 and PRB_R17

5.8.2.9 25-Tap FIR, First-Order IIR, AGC, Filter C

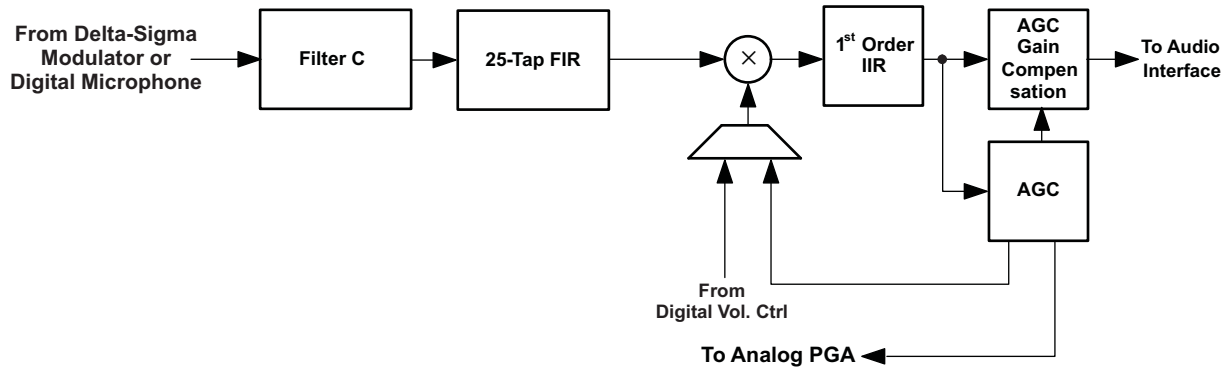


Figure 5-12. Signal for PRB_R15 and PRB_R18

5.8.3 User Programmable Filters

Depending on the selected processing block, different types and orders of digital filtering are available. A first-order IIR filter is always available, and is useful to efficiently filter out possible DC components of the signal. Up to 5 biquad section or alternatively up to 25-tap FIR filters are available for specific processing blocks. The coefficients of the available filters are arranged as sequentially indexed coefficients in Page 4.

The coefficients of these filters are each 16-bits wide, in twos complement and occupy 2 consecutive 8-bit registers in the register space. For default values please see the Register Map section.

5.8.3.1 First-Order IIR Section

The transfer function for the first-order IIR Filter is give by:

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{15} - D_1 z^{-1}} \quad (2)$$

The frequency response for the first-order IIR section with default coefficients is flat at a gain of 0 dB.

Table 5-5. ADC First-Order IIR Filter Coefficients

Filter	Filter Coefficient	ADC Coefficient Left Channel	ADC Coefficient Right Channel
First-Order IIR	N0	C4 (Pg 4, Reg 8 and 9)	C36 (Pg4, Reg 72 and 73)
	N1	C5 (Pg 4, Reg 10 and 11)	C37 (Pg4, Reg 74 and 75)
	D1	C6 (Pg 4, Reg 12 and 13)	C38 (Pg4, Reg 76 and 77)

5.8.3.2 Biquad Section

The transfer function of each of the biquad filters is given by

$$H(z) = \frac{N_0 + 2 * N_1 z^{-1} + N_2 z^{-2}}{2^{15} - 2 * D_1 z^{-1} - D_2 z^{-2}} \quad (3)$$

The frequency response for each of the biquad section with default coefficients is flat at a gain of 0 dB.

Table 5-6. ADC Biquad Filter Coefficients

Filter	Filter Coefficient	ADC Coefficient Left Channel	ADC Coefficient Right Channel
BIQUAD A	N0	C7 (Pg 4, Reg 14 and 15)	C39 (Pg 4, Reg 78 and 79)
	N1	C8 (Pg 4, Reg 16 and 17)	C40 (Pg 4, Reg 80 and 81)
	N2	C9 (Pg 4, Reg 18 and 19)	C41 (Pg 4, Reg 82 and 83)
	D1	C10 (Pg 4, Reg 20 and 21)	C42 (Pg 4, Reg 84 and 85)
	D2	C11 (Pg 4, Reg 22 and 23)	C43 (Pg 4, Reg 86 and 87)
BIQUAD B	N0	C12 (Pg 4, Reg 24 and 25)	C44 (Pg 4, Reg 88 and 89)
	N1	C13 (Pg 4, Reg 26 and 27)	C45 (Pg 4, Reg 90 and 91)
	N2	C14 (Pg 4, Reg 28 and 29)	C46 (Pg 4, Reg 92 and 93)
	D1	C15 (Pg 4, Reg 30 and 31)	C47 (Pg 4, Reg 94 and 95)
	D2	C16 (Pg 4, Reg 32 and 33)	C48 (Pg 4, Reg 96 and 97)
BIQUAD C	N0	C17 (Pg 4, Reg 34 and 35)	C49 (Pg 4, Reg 98 and 99)
	N1	C18 (Pg 4, Reg 36 and 37)	C50 (Pg 4, Reg 100 and 101)
	N2	C19 (Pg 4, Reg 38 and 39)	C51 (Pg 4, Reg 102 and 103)
	D1	C20 (Pg 4, Reg 40 and 41)	C52 (Pg 4, Reg 104 and 105)
	D2	C21 (Pg 4, Reg 42 and 43)	C53 (Pg 4, Reg 106 and 107)
BIQUAD D	N0	C22 (Pg 4, Reg 44 and 45)	C54 (Pg 4, Reg 108 and 109)
	N1	C23 (Pg 4, Reg 46 and 47)	C55 (Pg 4, Reg 110 and 111)
	N2	C24 (Pg 4, Reg 48 and 49)	C56 (Pg 4, Reg 112 and 113)
	D1	C25 (Pg 4, Reg 50 and 51)	C57 (Pg 4, Reg 114 and 115)
	D2	C26 (Pg 4, Reg 52 and 53)	C58 (Pg 4, Reg 116 and 117)
BIQUAD E	N0	C27 (Pg 4, Reg 54 and 55)	C59 (Pg 4, Reg 118 and 119)
	N1	C28 (Pg 4, Reg 56 and 57)	C60 (Pg 4, Reg 120 and 121)
	N2	C29 (Pg 4, Reg 58 and 59)	C61 (Pg 4, Reg 122 and 123)
	D1	C30 (Pg 4, Reg 60 and 61)	C62 (Pg 4, Reg 124 and 125)
	D2	C31 (Pg 4, Reg 62 and 63)	C63 (Pg 4, Reg 126 and 127)

5.8.3.3 FIR Section

Six of the available ADC processing blocks offer FIR filters for signal processing. Processing blocks PRB_R9 and PRB_R12 feature a 20-tap FIR filter, while PRB_R3, PRB_R6, PRB_R15, and PRB_R18 feature a 25-tap FIR filter.

$$H(z) = \sum_{n=0}^{M} Fir_n z^{-n}$$

$$M = 24, \text{for PRB\_R3, PRB\_R6, PRB\_R15 and PRB\_R18}$$

$$M = 19, \text{for PRB\_R9 and PRB\_R12} \quad (4)$$

The coefficients of the FIR filters are 16-bit twos complement format and correspond to the ADC coefficient space as listed below. There is no default transfer function for the FIR filter. When the FIR filter is used all applicable coefficients must be programmed.

Table 5-7. ADC FIR Filter Coefficients

Filter	ADC Coefficient Left Channel	ADC Coefficient Right Channel
Fir0	C7 (Pg 4, Reg 14 and 15)	C39 (Pg 4, Reg 78 and 79)
Fir1	C8 (Pg 4, Reg 16 and 17)	C40 (Pg 4, Reg 80 and 81)
Fir2	C9 (Pg 4, Reg 18 and 19)	C41 (Pg 4, Reg 82 and 83)
Fir3	C10 (Pg 4, Reg 20 and 21)	C42 (Pg 4, Reg 84 and 85)
Fir4	C11 (Pg 4, Reg 22 and 23)	C43 (Pg 4, Reg 86 and 87)
Fir5	C12 (Pg 4, Reg 24 and 25)	C44 (Pg 4, Reg 88 and 89)
Fir6	C13 (Pg 4, Reg 26 and 27)	C45 (Pg 4, Reg 90 and 91)
Fir7	C14 (Pg 4, Reg 28 and 29)	C46 (Pg 4, Reg 92 and 93)
Fir8	C15 (Pg 4, Reg 30 and 31)	C47 (Pg 4, Reg 94 and 95)
Fir9	C16 (Pg 4, Reg 32 and 33)	C48 (Pg 4, Reg 96 and 97)
Fir10	C17 (Pg 4, Reg 34 and 35)	C49 (Pg 4, Reg 98 and 99)
Fir11	C18 (Pg 4, Reg 36 and 37)	C50 (Pg 4, Reg 100 and 101)
Fir12	C19 (Pg 4, Reg 38 and 39)	C51 (Pg 4, Reg 102 and 103)
Fir13	C20 (Pg 4, Reg 40 and 41)	C52 (Pg 4, Reg 104 and 105)
Fir14	C21 (Pg 4, Reg 42 and 43)	C53 (Pg 4, Reg 106 and 107)
Fir15	C22 (Pg 4, Reg 44 and 45)	C54 (Pg 4, Reg 108 and 109)
Fir16	C23 (Pg 4, Reg 46 and 47)	C55 (Pg 4, Reg 110 and 111)
Fir17	C24 (Pg 4, Reg 48 and 49)	C56 (Pg 4, Reg 112 and 113)
Fir18	C25 (Pg 4, Reg 50 and 51)	C57 (Pg 4, Reg 114 and 115)
Fir19	C26 (Pg 4, Reg 52 and 53)	C58 (Pg 4, Reg 116 and 117)
Fir20	C27 (Pg 4, Reg 54 and 55)	C59 (Pg 4, Reg 118 and 119)
Fir21	C28 (Pg 4, Reg 56 and 57)	C60 (Pg 4, Reg 120 and 121)
Fir22	C29 (Pg 4, Reg 58 and 59)	C61 (Pg 4, Reg 122 and 123)
Fir23	C30 (Pg 4, Reg 60 and 61)	C62 (Pg 4, Reg 124 and 125)
Fir24	C31 (Pg 4, Reg 62 and 63)	C63 (Pg 4, Reg 126 and 127)

5.8.4 Decimation Filter

The TLV320AIC36 offers three different types of decimation filters. The integrated digital decimation filter removes high-frequency content and down samples the audio data from an initial sampling rate of AOSR*Fs to the final output sampling rate of Fs. The decimation filtering is achieved using a higher-order CIC filter followed by linear-phase FIR filters. The decimation filter cannot be chosen by itself, it is implicitly set through the chosen processing block.

The following subsections describe the properties of the available filters A, B, and C.

5.8.4.1 Decimation Filter A

This filter is intended for use at sampling rates up to 48 kHz. When configuring this filter, the oversampling ratio of the ADC can either be 128 or 64. For highest performance the oversampling ratio must be set to 128.

Filter A can also be used for 96 kHz at an AOSR of 64.

Table 5-8. ADC Decimation Filter A, Specification

Parameter	Condition	Value (Typical)	Units
AOSR = 128			
Filter Gain Pass Band	0…0.39 Fs	0.062	dB
Filter Gain Stop Band	0.55…64 Fs	–73	dB
Filter Group Delay		17/Fs	Sec.
Pass Band Ripple, 8 ksps	0…0.39 Fs	0.062	dB
Pass Band Ripple, 44.1 ksps	0…0.39 Fs	0.05	dB
Pass Band Ripple, 48 ksps	0…0.39 Fs	0.05	dB
AOSR = 64			
Filter Gain Pass Band	0…0.39 Fs	0.062	dB
Filter Gain Stop Band	0.55…32 Fs	–73	dB
Filter Group Delay		17/Fs	Sec.
Pass Band Ripple, 8 ksps	0…0.39 Fs	0.062	dB
Pass Band Ripple, 44.1 ksps	0…0.39 Fs	0.05	dB
Pass Band Ripple, 48 ksps	0…0.39 Fs	0.05	dB
Pass Band Ripple, 96 ksps	0…20 kHz	0.1	dB

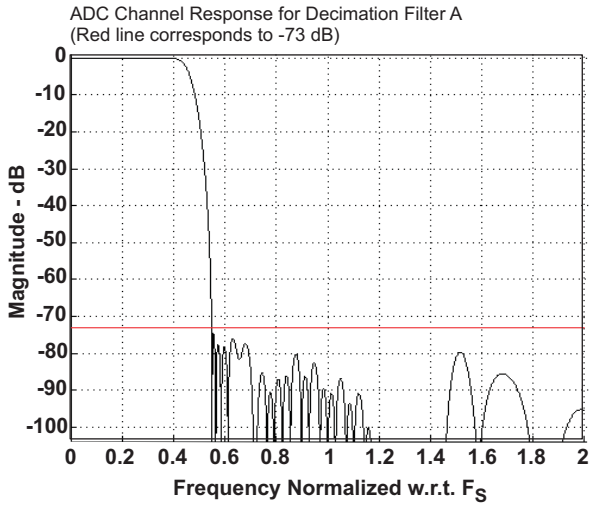


Figure 5-13. ADC Decimation Filter A, Frequency Response

5.8.4.2 Decimation Filter B

Filter B is intended to support sampling rates up to 96 kHz at a oversampling ratio of 64.

Table 5-9. ADC Decimation Filter B, Specifications

Parameter	Condition	Value (Typical)	Units
AOSR = 64			
Filter Gain Pass Band	0…0.39 Fs	±0.077	dB
Filter Gain Stop Band	0.60…32 Fs	–46	dB
Filter Group Delay		11/Fs	Sec.
Pass Band Ripple, 8 ksps	0…0.39 Fs	0.076	dB
Pass Band Ripple, 44.1 ksps	0…0.39 Fs	0.06	dB
Pass Band Ripple, 48 ksps	0…0.39 Fs	0.06	dB
Pass Band Ripple, 96 ksps	0…20 kHz	0.11	dB

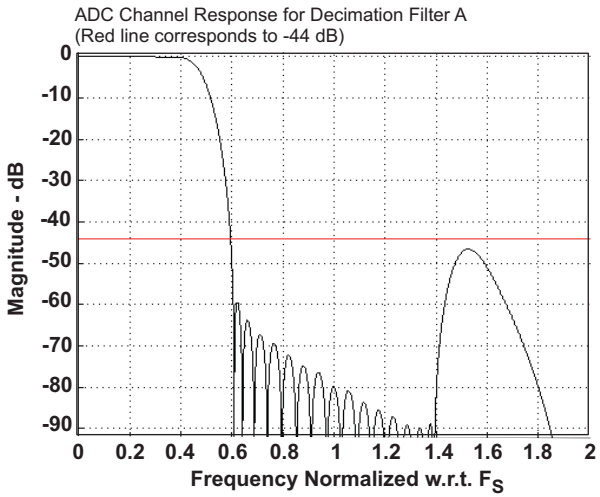


Figure 5-14. ADC Decimation Filter B, Frequency Response

5.8.4.3 Decimation Filter C

Filter C along with AOSR of 32 is specially designed for 192 kSPS operation for the ADC. The pass band which extends up to 0.11*Fs (corresponds to 21 kHz) is suited for audio applications.

Table 5-10. ADC Decimation Filter C, Specifications

Parameter	Condition	Value (Typical)	Units
Filter Gain from 0 to 0.11 Fs	0…0.11 Fs	±0.033	dB
Filter Gain from 0.28 Fs to 16 Fs	0.28 Fs…16 Fs	–60	dB
Filter Group Delay		11/Fs	Sec.
Pass Band Ripple, 8 ksps	0…0.11 Fs	0.033	dB
Pass Band Ripple, 44.1 ksps	0…0.11 Fs	0.033	dB
Pass Band Ripple, 48 ksps	0…0.11 Fs	0.032	dB
Pass Band Ripple, 96 ksps	0…0.11 Fs	0.032	dB
Pass Band Ripple, 192 ksps	0…20 kHz	0.086	dB

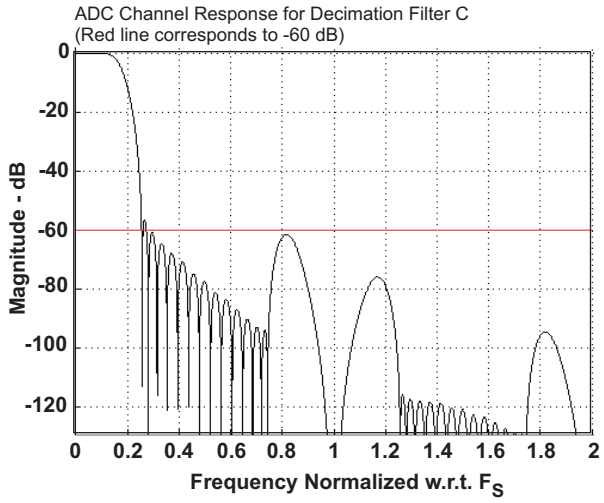


Figure 5-15. ADC Decimation Filter C, Frequency Response

5.8.5 ADC Data Interface

The decimation filter and signal processing block in the ADC channel passes 24-bit data words to the audio serial interface once every cycle of Fs,ADC. During each cycle of Fs,ADC, a pair of data words (for left and right channel) are passed. The audio serial interface rounds the data to the required word length of the interface before converting to serial data as per the different modes for audio serial interface.

5.9 ADC Special Functions

5.9.1 Digital Microphone Function

In addition to supporting analog microphones, the TLV320AIC36 also supports interfacing to a digital microphone. The internal ADC_MOD_CLK is available on pins selected with Page 0 Registers 120 – 125 as a digital microphone clock. The single-bit output of the external digital microphone can be connected to the GPIO1, DIGMIC_DATA, or the DIN pins as selected with Page 0 Register 81 as shown in Figure 5-16

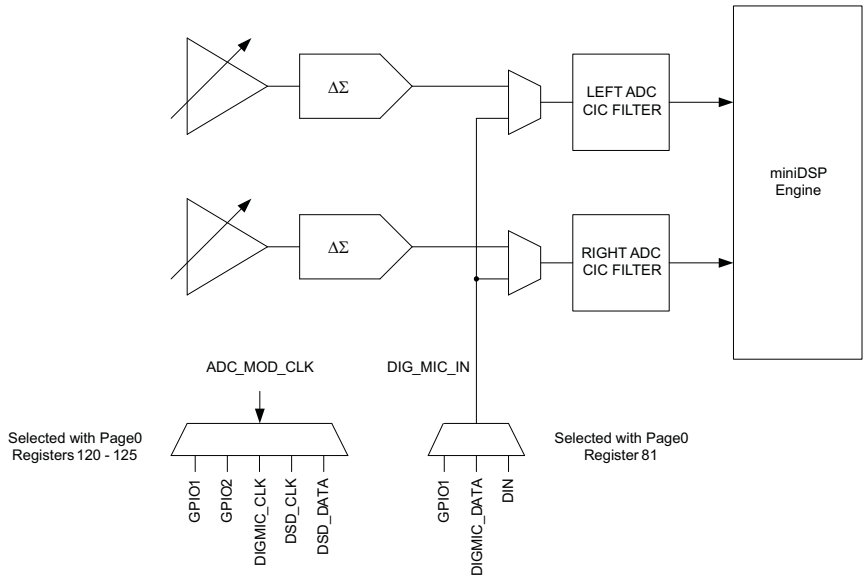


Figure 5-16. Digital Microphone in TLV320AIC36

Internally, the TLV320AIC36 samples the digital microphone left channel data using the rising edge of the microphone clock and the right channel data using the falling edge of the clock as shown in Figure 5-17.

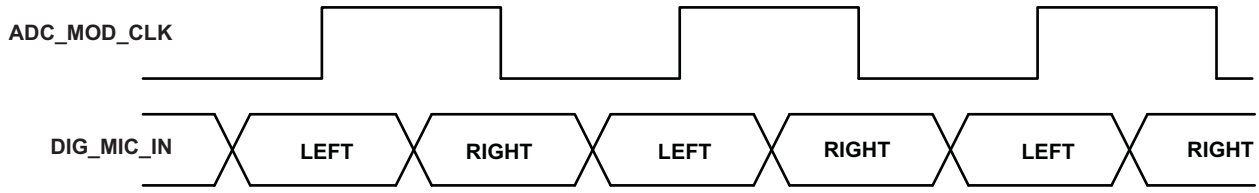


Figure 5-17. Timing Diagram for Digital Microphone Interface

The digital-microphone mode can be selectively enabled for only-left, only-right, or stereo channels. When the digital microphone mode is enabled, the analog section of the ADC can be powered down and bypassed for power efficiency. The AOSR value for the ADC channel must be configured to select the desired decimation ratio to be achieved based on the external digital microphone properties.

5.9.2 Channel-to-Channel Phase Adjustment

The TLV320AIC36 has a built-in feature to fine-adjust the phase between the stereo ADC record signals. The phase compensation is particularly helpful to adjust delays when using dual microphones for noise cancellation.

This delay can be controlled in fine amounts in the following fashion.

Delay(7:0) = Page 0/Register 85/D(7:0)

Where:

$$RIGHT\_ADC\_PHASE\_COMP(t) = RIGHT\_ADC\_OUT(t - t_{pr}) \quad (5)$$

Where:

$$t_{pr} = \frac{(Delay(4:0) + Delay(6:5) * AOSR * k_f)}{AOSR * ADC\_FS} \quad (6)$$

Where k_f is a function of the decimation filter:

Decimation Filter Type	k_f
A	0.25
B	0.5
C	1

and

$$LEFT\_ADC\_PHASE\_COMP(t) = LEFT\_ADC\_OUT(t - t_{pl}) \quad (7)$$

Where:

$$t_{pl} = \frac{Delay(7)}{AOSR * ADC\_FS} \quad (8)$$

5.9.3 DC Measurement

The TLV320AIC36 supports a highly flexible DC measurement feature using the high resolution oversampling and noise-shaping ADC. This mode can be used when the particular ADC channel is not used for the voice/audio record function. This mode can be enabled by programming Page 0, Register 102, D(7:6). The converted data is 24-bits, using 2.22 numbering format. The value of the converted data for the left-channel ADC can be read back from Page 0, Register 104–106 and for the right-channel ADC from Page 0, Register 107–109.

NOTE

Each group of three registers must be read in MSB-to-LSB order (ascending register numbers) to properly latch the converted data.

Mode A

In DC-measurement mode A, a variable-length averaging filter is used. The length of the averaging filter D, can be programmed from 1 to 20 by programming Page 0, Register 102, D(4:0). To choose mode A, Page 0, Register 102, D(5) must be programmed to 0.

Mode B

To choose mode B Page 0, Register 102, D(5) must be programmed to 1. In DC-measurement mode B, a first-order IIR filter is used. The coefficients of this filter are determined by D, Page 0, Register 102, D(4:0). The nature of the filter is given in Table 5-11.

Table 5-11. DC Measurement Bandwidth Settings

D:Page 0, Reg 102 , D(4:0)	–3 dB BW (kHz)	–0.5 dB BW (kHz)
1	688.44	236.5
2	275.97	96.334
3	127.4	44.579
4	61.505	21.532
5	30.248	10.59
6	15.004	5.253
7	7.472	2.616
8	3.729	1.305
9	1.862	652
10	931	326
11	465	163
12	232.6	81.5
13	116.3	40.7
14	58.1	20.3
15	29.1	10.2
16	14.54	5.09
17	7.25	2.54
18	3.63	1.27
19	1.8	0.635
20	0.908	0.3165

By programming Page 0, Reg 103, D(5) to 1, the averaging filter is periodically reset after 2^R number of ADC_MOD_CLK, where R is programmed in Page 0, Reg 103, D(4:0). When Page 0, Reg 103, D(5) is set to 1, the value of D should be less than the value of R. When Page 0, Reg 103, D(5) is programmed as 0 the averaging filter is never reset.

5.10 ADC Setup

The following discussion is intended to guide a system designer through the steps necessary to configure the TLV320AIC36 ADC.

Step 1

The system clock source (master clock) and the targeted ADC sampling frequency must be identified.

Depending on the targeted performance, the decimation filter type (A, B, or C) and OSR value can be determined.

- Filter A with AOSR of 128 or 64 should be used for 48-kHz (or below) high-performance operation. An AOSR of 64 can be also used for 96-kHz operation
- Filter B with AOSR of 64 should be used for 96-kHz operations.
- Filter C with AOSR of 32 should be used for 192-kHz operations

Based on the identified filter type and the required signal processing capabilities the appropriate processing block can be determined from the list of available processing blocks (PRB_R1 to PRB_R18) (see Table 5-4).

Based on the available master clock, the chosen OSR and the targeted sampling rate, the clock divider values NADC and MADC can be determined. If necessary the internal PLL will add a large degree of flexibility.

In summary, Codec_Clkin which is either derived directly from the system clock source or from the internal PLL, divided by MADC, NADC and AOSR, must be equal to the ADC sampling rate ADC_FS. The Clodec_Clkin clock signal is shared with the DAC clock generation block.

CODEC_CLKIN = NADC*MADC*AOSR*ADC_FS

To a large degree NADC and MADC can be chosen independently in the range of 1 to 128. In general NADC should be as large as possible as long as the following condition can still be met:

MADC*AOSR/32 ≥ RC

RC is a function of the chosen processing block and is listed in the Table 5-4.

At this point the following device specific parameters are known:

PRB_Rx, AOSR, NADC, MADC, common mode setting

Additionally if the PLL is used the PLL parameters P, J, D, and R are determined as well.

Step 2

Setting up the device through register programming:

The following list gives a sequence of items that must be executed between powering the device up and reading data from the device:

Define starting point:	Initiate SW Reset
Program PMU Settings:	Turn on charge pump Turn on ADC and DAC LDO with current limit
Program clock setting:s	Program PLL clock dividers P, J,D, R (if PLL is necessary) Power up PLL (if PLL is necessary) Program and power up NADC Program and power up MADC Program OSR value Program the processing block to be used
Program Codec Interface:	Set word length, BCLK, WCLK I/O, mode type, for example I^2S/DSP
Program Analog Blocks	Program common mode voltage Power up ADC Program common mode startup sequence Route inputs/common mode to ADC Unmute PGA and set gains Release LDO current limit Unmute digital volume control

See Section 5.20 for a detailed application example.

5.11 DAC

The TLV320AIC36 includes a stereo audio DAC supporting data rates from 8 to 192kHz. Each channel of the stereo audio DAC consists of a signal-processing engine with fixed processing blocks, a programmable miniDSP, a digital interpolation filter, multi-bit digital delta-sigma modulator, and an analog reconstruction filter. The DAC is designed to provide enhanced performance at low sampling rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and signal images strongly suppressed within the audio band to beyond 20kHz. To handle multiple input rates and optimize power dissipation and performance, the TLV320AIC36 allows the system designer to program the oversampling rates over a wide range from 1 to 1024 by configuring the Page 0, Reg 13, and Reg 14. The system designer can choose higher oversampling ratios for lower input data rates and lower oversampling ratios for higher input data rates.

The TLV320AIC36 DAC channel includes a built-in digital interpolation filter to generate oversampled data for the sigma delta modulator. The interpolation filter can be chosen from three different types depending on required frequency response, group delay and sampling rate.

5.11.1 Processing Blocks

The TLV320AIC36 implements signal processing capabilities and interpolation filtering using processing blocks. These fixed processing blocks give users the choice of how much and what type of signal processing they may use and which interpolation filter is applied.

The choice between these processing blocks is part of a strategy balancing power conservation and signal processing flexibility. Less signal processing capability will result in less power consumed by the device. The Table 5-12 gives an overview over all available processing blocks of the DAC channel and their properties. The Resource Class (RC) column gives an approximate indication of power consumption. Page 0, Register 60 is used to select one of the 25 processing blocks.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- 3D – Effect
- Beep Generator

The processing blocks are tuned for common cases and can achieve high image rejection or low group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first-order IIR and biquad filters have fully user-programmable coefficients.

Table 5-12. Overview – DAC Predefined Processing Blocks

Processing Block No.	Interpolation Filter	Channel	First-Order IIR Available	Number of Biquads	DRC	3D	Beep Generator	RC Class
PRB_P1	A	Stereo	No	3	No	No	No	8
PRB_P2	A	Stereo	Yes	6	Yes	No	No	12
PRB_P3	A	Stereo	Yes	6	No	No	No	10
PRB_P4	A	Left	No	3	No	No	No	4
PRB_P5	A	Left	Yes	6	Yes	No	No	6
PRB_P6	A	Left	Yes	6	No	No	No	6
PRB_P7	B	Stereo	Yes	0	No	No	No	6
PRB_P8	B	Stereo	No	4	Yes	No	No	8
PRB_P9	B	Stereo	No	4	No	No	No	8
PRB_P10	B	Stereo	Yes	6	Yes	No	No	10
PRB_P11	B	Stereo	Yes	6	No	No	No	8
PRB_P12	B	Left	Yes	0	No	No	No	3
PRB_P13	B	Left	No	4	Yes	No	No	4
PRB_P14	B	Left	No	4	No	No	No	4
PRB_P15	B	Left	Yes	6	Yes	No	No	6
PRB_P16	B	Left	Yes	6	No	No	No	4
PRB_P17	C	Stereo	Yes	0	No	No	No	3
PRB_P18	C	Stereo	Yes	4	Yes	No	No	6
PRB_P19	C	Stereo	Yes	4	No	No	No	4
PRB_P20	C	Left	Yes	0	No	No	No	2
PRB_P21	C	Left	Yes	4	Yes	No	No	3
PRB_P22	C	Left	Yes	4	No	No	No	2
PRB_P23	A	Stereo	No	2	No	Yes	No	8
PRB_P24	A	Stereo	Yes	5	Yes	Yes	No	12
PRB_P25	A	Stereo	Yes	5	Yes	Yes	Yes	12

5.11.2 Processing Blocks – Details

5.11.2.1 Three Biquads, Filter A

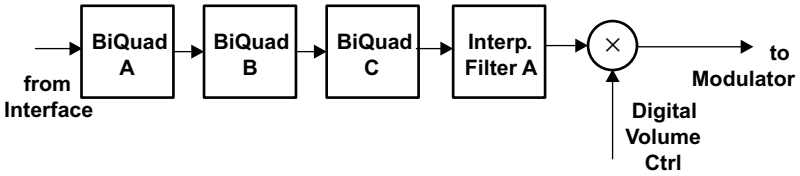


Figure 5-18. Signal Chain for PRB_P1 and PRB_P4

5.11.2.2 Six Biquads, First-Order IIR, DRC, Filter A or B

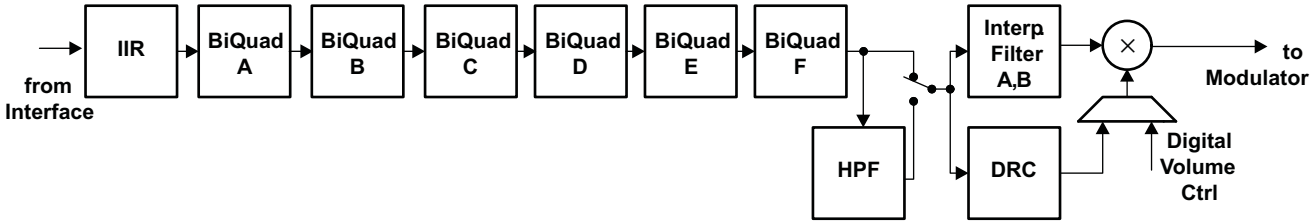


Figure 5-19. Signal Chain for PRB_P2, PRB_P5, PRB_P10, and PRB_P15

5.11.2.3 Six Biquads, First-Order IIR, Filter A or B

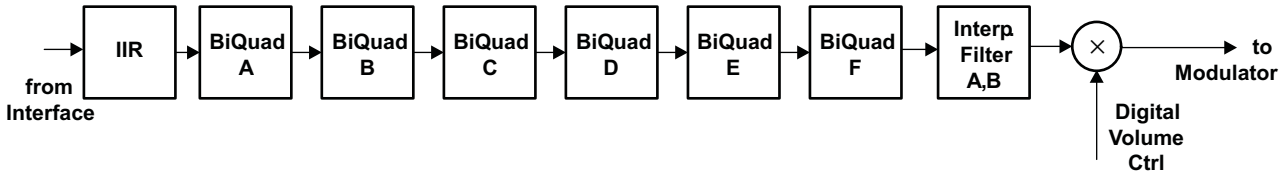


Figure 5-20. Signal Chain for PRB_P3, PRB_P6, PRB_P11, and PRB_P16

5.11.2.4 IIR, Filter B or C

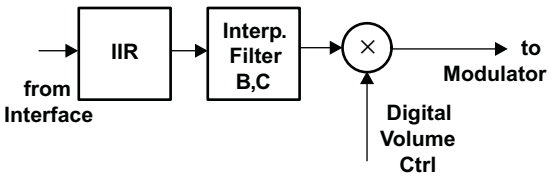


Figure 5-21. Signal Chain for PRB_P7, PRB_P12, PRB_P17, and PRB_P20

5.11.2.5 Four Biquads, DRC, Filter B

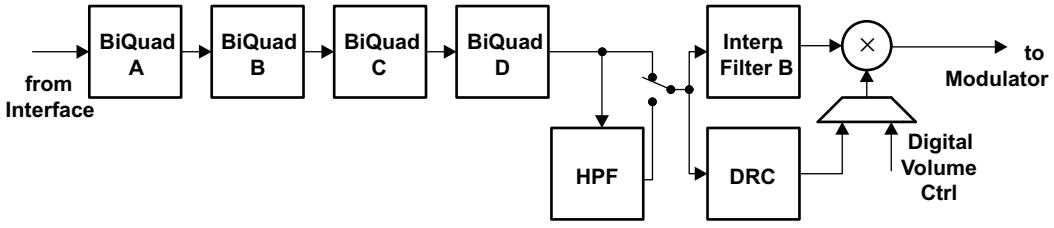


Figure 5-22. Signal Chain for PRB_P8 and PRB_P13

5.11.2.6 Four Biquads, Filter B

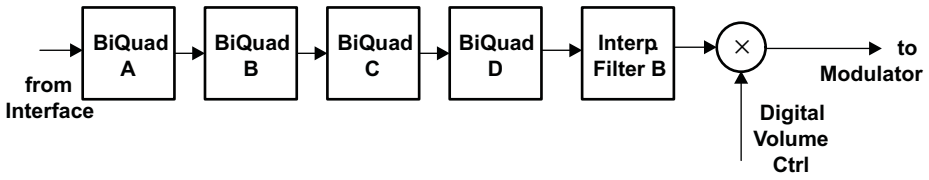


Figure 5-23. Signal Chain for PRB_P9 and PRB_P14

5.11.2.7 Four Biquads, First-Order IIR, DRC, Filter B

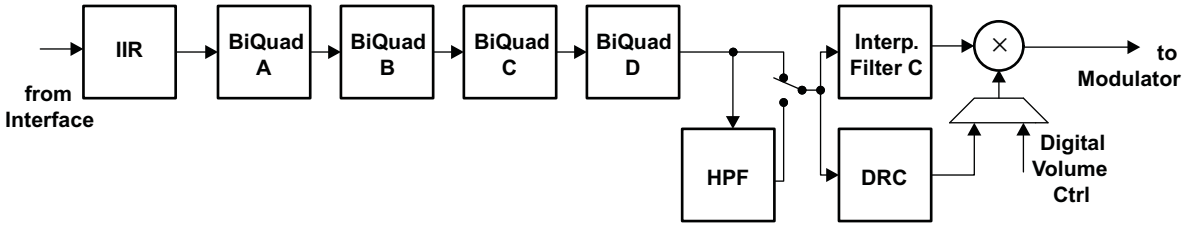


Figure 5-24. Signal Chain for PRB_P18 and PRB_P21

5.11.2.8 Four Biquads, First-Order IIR, Filter C

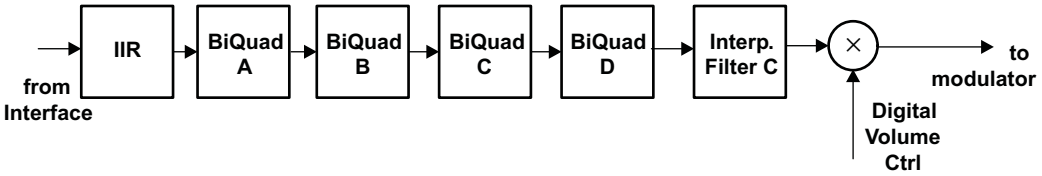


Figure 5-25. Signal Chain for PRB_P19 and PRB_P22

5.11.2.9 Two Biquads, 3D, Filter A

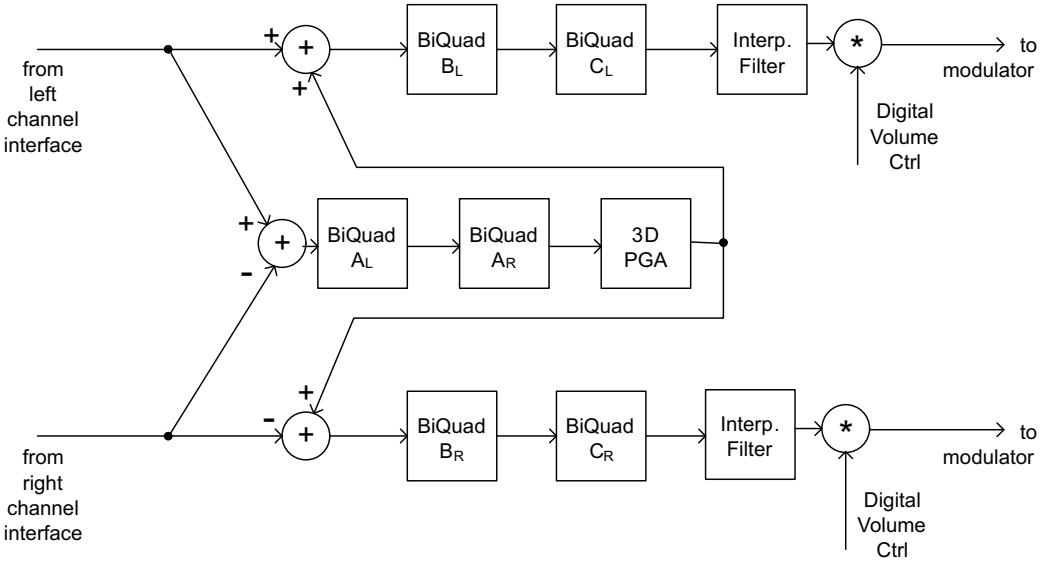


Figure 5-26. Signal Chain for PRB_P23

5.11.2.10 5 Biquads, DRC, 3D, Filter A

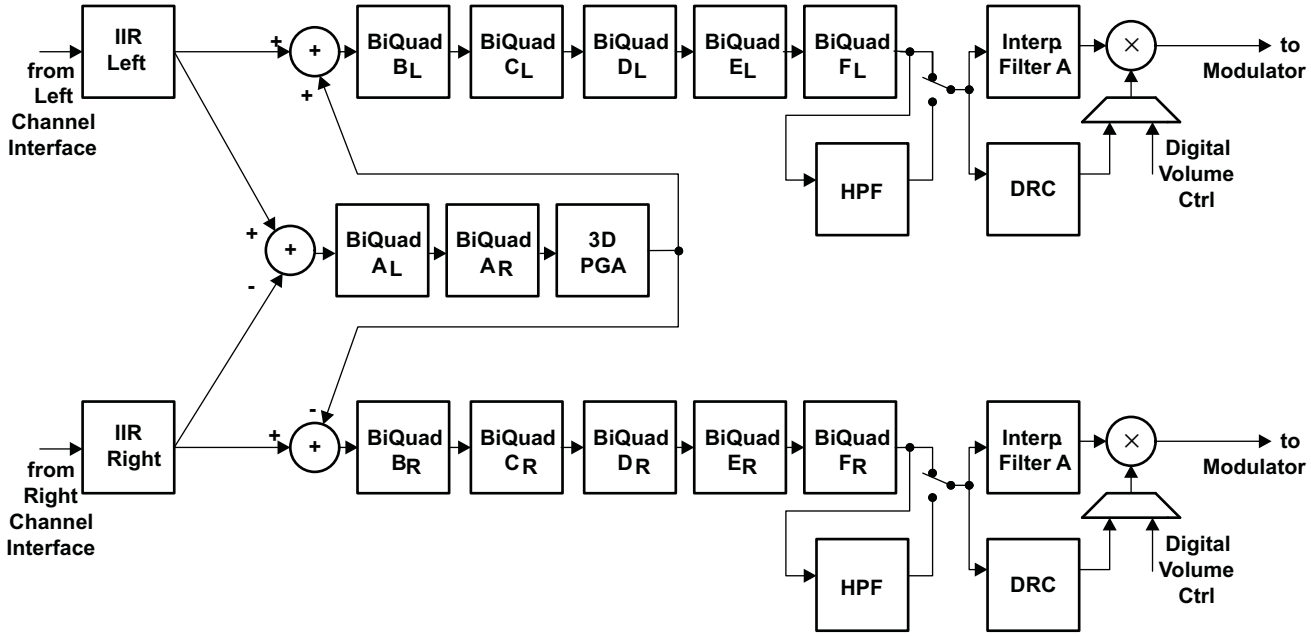


Figure 5-27. Signal Chain for PRB_P24

5.11.2.11 Five Biquads, DRC, 3D, Beep Generator, Filter A

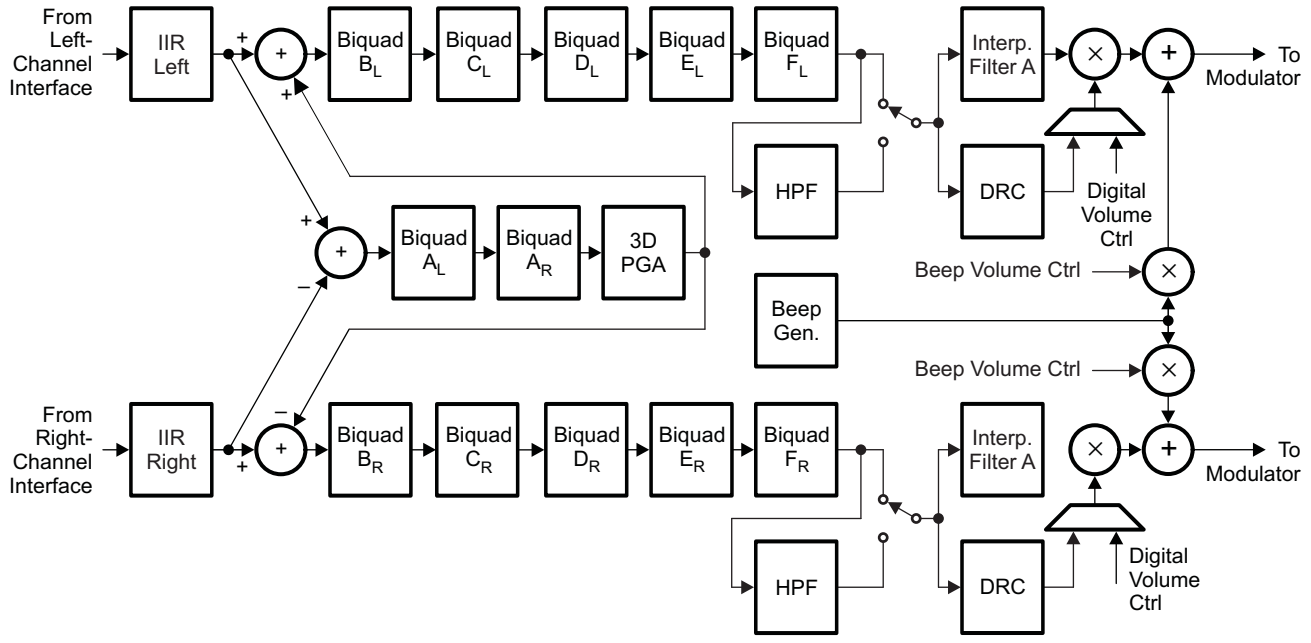


Figure 5-28. Signal Chain for PRB_P25

5.11.3 User Programmable Filters

Depending on the selected processing block, different types and orders of digital filtering are available. Up to six biquad sections are available for specific processing blocks.

The coefficients of the available filters are arranged as sequentially-indexed coefficients in two banks. If adaptive filtering is chosen, the coefficient banks can be switched on-the-fly. For more details on adaptive filtering please see Section 5.14.3.

The coefficients of these filters are each 16 bits wide, in twos complement, and occupy two consecutive 8-bit registers in the register space. For default values please see the *Register Map* section.

5.11.3.1 First-Order IIR Section

The IIR is of first-order and its transfer function is given by

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{15} - D_1 z^{-1}} \quad (9)$$

The frequency response for the first-order IIR Section with default coefficients is flat

Table 5-13. DAC IIR Filter Coefficients

Filter	Filter Coefficient	ADC Coefficient Left Channel	ADC Coefficient Right Channel
First-order IIR	N0	C65 (Pg 9, Reg 2 and 3)	C68 (Pg 9, Reg 8 and 9)
	N1	C66 (Pg 9, Reg 4 and 5)	C69 (Pg 9, Reg 10 and 11)
	D1	C67 (Pg 9, Reg 6 and 7)	C70 (Pg 9, Reg 12 and 13)

5.11.3.2 Biquad Section

The transfer function of each biquad filters is given by:

$$H(z) = \frac{N_0 + 2*N_1 z^{-1} + N_2 z^{-2}}{2^{15} - 2*D_1 z^{-1} - D_2 z^{-2}} \quad (10)$$

Table 5-14. DAC Biquad Filter Coefficients

Filter	Coefficient	Left DAC Channel	Right DAC Channel
BIQUAD A	N0	C1 (Pg 8, Reg 2 and 3)	C33 (Pg 8, Reg 66 and 67)
	N1	C2 (Pg 8, Reg 4 and 5)	C34 (Pg 8, Reg 68 and 69)
	N2	C3 (Pg 8, Reg 6 and 7)	C35 (Pg 8, Reg 70 and 71)
	D1	C4 (Pg 8, Reg 8 and 9)	C36 (Pg 8, Reg 72 and 73)
	D2	C5 (Pg 8, Reg 10 and 11)	C37 (Pg 8, Reg 74 and 75)
BIQUAD B	N0	C6 (Pg 8, Reg 12 and 13)	C38 (Pg 8, Reg 76 and 77)
	N1	C7 (Pg 8, Reg 14 and 15)	C39 (Pg 8, Reg 78 and 79)
	N2	C8 (Pg 8, Reg 16 and 172)	C40 (Pg 8, Reg 80 and 81)
	D1	C9 (Pg 8, Reg 18 and 19)	C41 (Pg 8, Reg 82 and 83)
	D2	C10 (Pg 8, Reg 20 and 21)	C42 (Pg 8, Reg 84 and 85)
BIQUAD C	N0	C11 (Pg 8, Reg 22 and 23)	C43 (Pg 8, Reg 86 and 87)
	N1	C12 (Pg 8, Reg 24 and 25)	C44 (Pg 8, Reg 88 and 89)
	N2	C13 (Pg 8, Reg 26 and 27)	C45 (Pg 8, Reg 90 and 91)
	D1	C14 (Pg 8, Reg 28 and 29)	C46 (Pg 8, Reg 92 and 93)
	D2	C15 (Pg 8, Reg 30 and 31)	C47 (Pg 8, Reg 94 and 95)
BIQUAD D	N0	C16 (Pg 8, Reg 32 and 33)	C48 (Pg 8, Reg 96 and 97)
	N1	C17 (Pg 8, Reg 34 and 35)	C49 (Pg 8, Reg 98 and 99)

Table 5-14. DAC Biquad Filter Coefficients (continued)

Filter	Coefficient	Left DAC Channel	Right DAC Channel
	N2	C18 (Pg 8, Reg 36 and 37)	C50 (Pg 8, Reg 100 and 101)
	D1	C19 (Pg 8, Reg 38 and 39)	C51 (Pg 8, Reg 102 and 103)
	D2	C20 (Pg 8, Reg 40 and 41)	C52 (Pg 8, Reg 104 and 105)
BIQUAD E	N0	C21 (Pg 8, Reg 42 and 43)	C53 (Pg 8, Reg 106 and 107)
	N1	C22 (Pg 8, Reg 44 and 45)	C54 (Pg 8, Reg 108 and 109)
	N2	C23 (Pg 8, Reg 46 and 47)	C55 (Pg 8, Reg 110 and 111)
	D1	C24 (Pg 8, Reg 48 and 49)	C56 (Pg 8, Reg 112 and 113)
	D2	C25 (Pg 8, Reg 50 and 51)	C57 (Pg 8, Reg 114 and 115)
BIQUAD F	N0	C26 (Pg 8, Reg 52 and 53)	C58 (Pg 8, Reg 116 and 117)
	N1	C27 (Pg 8, Reg 54 and 55)	C59 (Pg 8, Reg 118 and 119)
	N2	C28 (Pg 8, Reg 56 and 57)	C60 (Pg 8, Reg 120 and 121)
	D1	C29 (Pg 8, Reg 58 and 59)	C61 (Pg 8, Reg 122 and 123)
	D2	C30 (Pg 8, Reg 60 and 61)	C62 (Pg 8, Reg 124 and 125)

5.11.4 Interpolation Filter

5.11.4.1 Interpolation Filter A

Table 5-15. DAC Interpolation Filter A, Specification

Parameter	Condition	Value (Typical)	Units
Filter gain pass band	0 … 0.45 Fs	±0.015	dB
Filter gain stop band	0.55 Fs… 7.455 Fs	–65	dB
Filter group delay		21/Fs	s

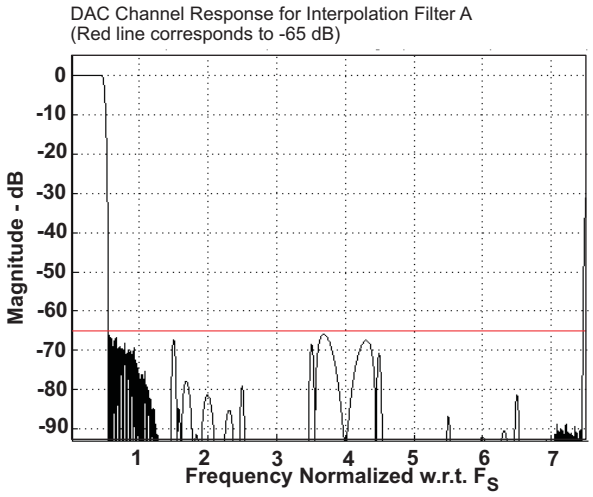


Figure 5-29. DAC Interpolation Filter A, Frequency Response

5.11.4.2 Interpolation Filter B

Filter B is specifically designed for an Fs above 96ksps. Thus, the flat passband region easily covers the required audio band of 0-20kHz.

Table 5-16. DAC Interpolation Filter B, Specification

Parameter	Condition	Value (Typical)	Units
Filter gain pass band	0 … 0.45 Fs	±0.015	dB
Filter gain stop band	0.55 … 3.45 Fs	–58	dB
Filter group delay		18/Fs	s

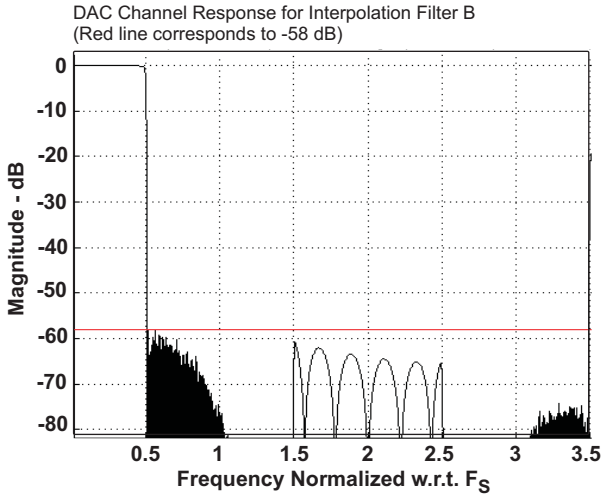


Figure 5-30. Channel Interpolation Filter B, Frequency Response

5.11.4.3 Interpolation Filter C

Filter C is specifically designed for the 192 ksps mode. The pass band extends up to 0.40*Fs (corresponds to 80 kHz), more than sufficient for audio applications.

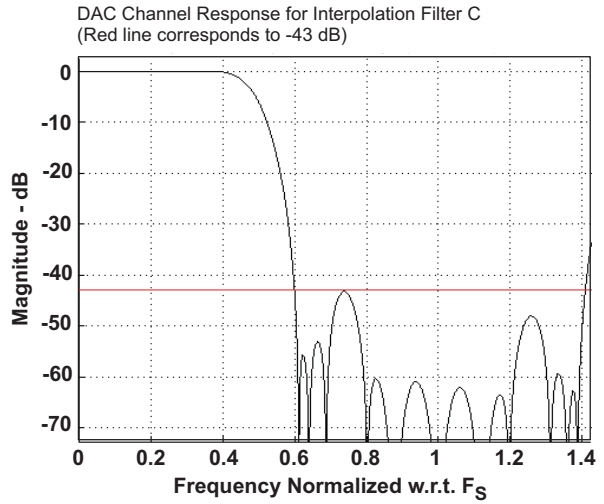


Figure 5-31. DAC Interpolation Filter C, Frequency Response

The basic filter characteristics for the Interpolation Filters A, B and C are as follows. These values are at 48 ksps with the droop of the analog reconstruction filters taken into account.

Table 5-17. DAC Interpolation Filter C, Specification

Parameter	Condition	Value (Typical)	Units
Filter gain pass band	0 … 0.35 Fs	±0.03	dB
Filter gain stop band	0.60 … 1.4 Fs	–43	dB
Filter group delay		13/Fs	s

5.12 DAC Output Drivers

5.12.1 Analog Fully Differential Line Output Drivers

The TLV320AIC36 has two fully differential line output drivers, each capable of driving a 10kΩ differential load. Each driver can connect to the left or the right DAC, the left or the right ADC PGA output, the left or right line input, or any combination of the six. The design includes extensive capability to adjust signal levels independently before any mixing occurs, beyond that already provided by the PGA gain and the DAC digital volume control. Note that since both left and right channel signals are routed to all output drivers, a mono mix of any of the stereo signals can easily be obtained by setting the volume controls of both left and right channel signals to –6 dB and mixing them. Undesired signals can also be disconnected from the mix as well through register control.

The TLV320AIC36 includes an output level control on each output driver with limited gain adjustment from 0 dB to +9 dB. The output driver circuitry in this device are designed to provide a low distortion output while playing full-scale stereo DAC signals at a 0 dB gain setting. However, a higher amplitude output can be obtained at the cost of increased signal distortion at the output. This output level control allows the user to make this tradeoff based on the requirements of the end equipment. Note that this output level control is not intended to be used as a standard output volume control. It is expected to be used only sparingly for level setting, that is, adjustment of the full-scale output range of the device.

Each differential line output driver can be powered down independently of the others when it is not needed in the system. When placed into powerdown through register programming, the driver output pins will be placed into a high-Z, high-impedance state.

The signal routing for the line level drivers is configured using Page 2, Registers 80 through 93

5.12.2 Analog High-Power Output Drivers

The TLV320AIC36 includes four single-ended high power output drivers arranged as two stereo pairs. These output drivers are capable of driving 0.89 Vrms each into a 16-Ω load if one pair is enabled or 0.5 Vrms each into 16-Ω if both pairs are enabled. The volume control and mixing blocks for the high-power output drivers are effectively identical to those of the line-level drivers. Note that each of these drivers have a output level control block like those included with the line output drivers, allowing gain adjustment up to +9 dB on the output signal. As in the previous case, this output level adjustment is not intended to be used as a standard volume control, but instead is included for additional full-scale output signal level control. In order to drive 0.89 Vrms for a full-scale DAC output into the load, the output level adjustment must be set to +2 dB.

The high power output drivers include additional circuitry to avoid artifacts on the audio output during power-on and power-off transient conditions. The power-up delay time for the high power output drivers is programmable over a wide range of time delays, from instantaneous up to 4-sec, using Page-2/Reg-42.

When these output drivers are powered down, they can be placed into a variety of output conditions based on register programming. If lowest power operation is desired, then the outputs can be placed into a tri-state condition, and all power to the output stage is removed. However, this generally results in the output nodes drifting to rest near the upper or lower analog supply, due to small leakage currents at the pins. This then results in a longer delay requirement to avoid output artifacts during driver power-on. In order to reduce this required power-on delay, the TLV320AIC36 includes an option for the output pins of the drivers to be weakly driven to the AGND level they would normally rest at when powered with no signal applied.

The high power output drivers can also be programmed to power up first with the output level control in a highly attenuated state, and then the output driver will automatically slowly reduce the output attenuation to reach the desired output level setting programmed.

The signal routing for the high power drivers is configured using Page 2, Registers 45 through 72.

5.12.3 Short-Circuit Output Protection

The TLV320AIC36 includes programmable short-circuit protection for the high power output drivers, for maximum flexibility in a given application. By default, if these output drivers are shorted, they will automatically limit the maximum amount of current that can be sourced to or sunk from a load, thereby protecting the device from an over-current condition. In this mode, the user can read Page-0/Reg-95 to determine whether the part is in short-circuit protection or not, and then decide whether to program the device to power down the output drivers. However, the device includes further capability to automatically power down an output driver whenever it does into short-circuit protection, without requiring intervention from the user. In this case, the output driver will stay in a power down condition until the user specifically programs it to power down and then power back up again, to clear the short-circuit flag.

5.13 DAC Gain Setting

5.13.1 Digital Volume Control

The TLV320AIC36 signal processing blocks incorporate a digital volume control block that can control the volume of the playback signal from +24 dB to –63.5 dB in steps of 0.5 dB. These can be controlled by writing to Page 0, Register 65 and 66. The volume control of left and right channels by default can be controlled independently, however by programming Page 0, Reg 64, D(1:0), they can be made interdependent. The volume changes are soft-stepped in steps of 0.5 dB to avoid audible artifacts during gain change. The rate of soft-stepping can be controlled by programming Page 0, Reg 63, D(1:0) to either one step per frame (DAC_FS) or one step per 2 frames. The soft-stepping feature can also be entirely disabled. During soft-stepping the value of the actual applied gain would differ from the programmed gain in register. The TLV320AIC36 gives a feedback to the user in form of register readable flag to indicate that soft-stepping is currently in progress. The flags for left and right channels can be read back by reading Page 0, Reg 37, D(2) and D(1) respectively. A value of 0 in these flags indicates a soft-stepping operation in progress, and a value of 1 indicates that soft-stepping has completed. A soft-stepping operation comes into effect during a) power-up, when the volume control soft-steps from –63.5 dB to programmed gain value b) volume change by user when DAC is powered up and c) power-down, when the volume control block soft-steps to –63.5 dB before powering down the channel.

5.13.2 Dynamic Range Compression

Typical music signals are characterized by crest factors, the ratio of peak signal power to average signal power, of 12 dB or more. In order to avoid audible distortions due to clipping of peak signals, the gain of the DAC channel must be adjusted so as not to cause hard clipping of peak signals. As a result, during nominal periods, the applied gain is low, causing the perception that the signal is not loud enough. To overcome this problem, the DRC in the TLV320AIC36 continuously monitors the output of the DAC Digital Volume control to detect its power level with respect to 0 dB FS. When the power level is low, it increases the input signal gain to make it sound louder. At the same time, if a peaking signal is detected, it autonomously reduces the applied gain to avoid hard clipping. This results in sounds more pleasing to the ear as well as sounding louder during nominal periods.

The DRC functionality in the TLV320AIC36 is implemented by a combination of Processing Blocks in the DAC channel as described in Section 5.11.2.

The DRC can be disabled by writing into Page 0, Reg 68, D(6:5).

The DRC typically works on the filtered version of the input signal. The input signals have no audio information at DC and extremely low frequencies; however they can significantly influence the energy estimation function in DRC. Also most of the information about signal energy is concentrated in the low frequency region of the input signal.

To estimate the energy of the input signal, the signal is first fed the DRC high-pass filter, and then fed to the DRC low-pass filter. These filters are implemented as first-order IIR filters given by

$$H_{HPF}(z) = \frac{N_0 + N_1 z^{-1}}{2^{15} - D_1 z^{-1}} \quad (11)$$

$$H_{LPF}(z) = \frac{N_0 + N_1 z^{-1}}{2^{15} - D_1 z^{-1}} \quad (12)$$

The coefficients for these filters are 16 bits wide in twos complement and are user programmable through register write as given in Table 5-18

Table 5-18. DRC HPF and LPF Coefficients

Coefficient	Location
HPF N0	C71 Page 9, Register 14 and 15
HPF N1	C72 Page 9, Register 16 and 17
HPF D1	C73 Page 9, Register 18 and 19
LPF N0	C74 Page 9, Register 20 and 21
LPF N1	C75 Page 9, Register 22 and 23
LPF D1	C76 Page 9, Register 24 and 25

The default values of these coefficients implement a high-pass filter with a cut-off at 0.00166*DAC_FS, and a low-pass filter with a cutoff at 0.00033 * DAC_FS.

The output of the DRC high-pass filter is fed to the Processing Block selected for the DAC Channel. The absolute value of the DRC-LPF filter is used for energy estimation within the DRC.

The gain in the DAC Digital Volume Control is controlled by Page 0, Register 65 and 66. When the DRC is enabled, the applied gain is a function of the Digital Volume Control register setting and the output of the DRC.

The DRC parameters are described in sections that follow.

5.13.2.1 DRC Threshold

The DRC Threshold represents the level of the DAC playback signal at which the gain compression becomes active. The output of the digital volume control in the DAC is compared with the set threshold. The threshold value is programmable by writing to register Page 0, Register 68, D(4:2). The Threshold value can be adjusted between –3 dBFS to –24 dBFS in steps of 3 dB. Keeping the DRC Threshold value too high may not leave enough time for the DRC block to detect peaking signals, and can cause excessive distortion at the outputs. Keeping the DRC Threshold value too low can limit the perceived loudness of the output signal.

The recommended DRC-Threshold value is –24 dB.

When the output signal exceeds the set DRC Threshold, the interrupt flag bits at Page 0, Register 44, D(3:2) are updated. These flag bits are 'sticky' in nature, and are reset only after they are read back by the user. The nonsticky versions of the interrupt flags are also available at Page 0, Register 46, D(3:2).

5.13.2.2 DRC Hysteresis

DRC Hysteresis is programmable by writing to Page 0, Register 68, D(1:0). It can be programmed to values between 0 dB and 3 dB in steps of 1 dB. It is a programmable window around the programmed DRC Threshold that must be exceeded for a disabled DRC to become enabled, or an enabled DRC to

become disabled. For example, if the DRC Threshold is set to –12 dBFS and DRC Hysteresis is set to 3 dB, then if the gain compressions in the DRC is inactive, the output of the DAC Digital Volume Control must exceed –9 dBFS before gain compression due to the DRC is activated. Similarly, when the gain compression in the DRC is active, the output of the DAC Digital Volume Control needs to fall below -15 dBFS for gain compression in the DRC to be deactivated. The DRC Hysteresis feature prevents the rapid activation and de-activation of gain compression in the DRC in cases when the output of DAC Digital Volume Control rapidly fluctuates in a narrow region around the programmed DRC Threshold. By programming the DRC Hysteresis as 0 dB, the hysteresis action is disabled.

The recommended value of DRC hysteresis is 3 dB.

5.13.2.3 DRC Hold

The DRC Hold is intended to slow the start of decay for a specified period of time in response to a decrease in energy level. To minimize audible artifacts, it is recommended to set the DRC Hold time to 0 through programming Page 0, Register 69, D(6:3) = 0000.

5.13.2.4 DRC Attack Rate

When the output of the DAC Digital Volume Control exceeds the programmed DRC Threshold, the gain applied in the DAC Digital Volume Control is progressively reduced to avoid the signal from saturating the channel. This process of reducing the applied gain is called Attack. To avoid audible artifacts, the gain is reduced slowly with a rate equaling the Attack Rate programmable using Page 0, Register 70, D(7:4). Attack Rates can be programmed from 4 dB gain change per 1/DAC_FS to 1.2207e-5 dB gain change per 1/DAC_FS.

Attack Rates should be programmed such that before the output of the DAC Digital Volume control can clip, the input signal should be sufficiently attenuated. High Attack Rates can cause audible artifacts, and too-slow Attack Rates may not be able to prevent the input signal from clipping.

The recommended value of DRC attack rate is 1.9531e-4 dB per 1/DAC_FS.

5.13.2.5 DRC Decay Rate

When the DRC detects a reduction in output signal swing beyond the programmed DRC Threshold, the DRC enters a Decay state, where the applied gain in Digital Volume Control is gradually increased to programmed values. To avoid audible artifacts, the gain is slowly increased with a rate equal to the Decay Rate programmed through Page 0, Register 70, D(3:0). The Decay Rates can be programmed from 1.5625e-3 dB per 1/DAC_FS to 4.7683e-7 dB per 1/DAC_FS. If the Decay Rates are programmed too high, then sudden gain changes can cause audible artifacts. However, if it is programmed too slow, then the output may be perceived as too low for a long time after the peak signal has passed.

The recommended Value of DRC Attack Rate is 2.4414e-5 dB per 1/DAC_FS.

5.13.2.6 Example Setup for DRC

- PGA Gain = 12 dB
- Threshold = –24 dB
- Hysteresis = 3 dB
- Hold time = 0 ms
- Attack Rate = 1.9531e-4 dB per 1/DAC_FS
- Decay Rate = 2.4414e-5 dB per 1/DAC_FS

Script

```
#Go to Page 0
w 30 00 00
#DAC => 12 db gain left
w 30 41 18
#DAC => 12 db gain right
w 30 42 18
#DAC => DRC Enabled for both channels, Threshold = -24 db, Hysteresis = 3 dB
w 30 44 7F
#DRC Hold = 0 ms, Rate of Changes of Gain = 0.5 dB/Fs'
w 30 45 00
#Attack Rate = 1.9531e-4 dB/Frame , DRC Decay Rate =2.4414e-5 dB/Frame
w 30 46 B6
#Go to Page 9
w 30 00 09
#DRC HPF
w 30 0E 7F AB 00 80 7F 56
#DRC LPF
W 30 14 00 11 00 11 7F DE
```

5.14 DAC Special Functions

5.14.1 Beep Generation

A special function has also been included in the processing block PRB_P25 for generating a digital sine-wave signal that is sent to the DAC. This is intended for generating key-click sounds for user feedback. A default value for the sine-wave frequency, sine burst length, and signal magnitude is kept in the Tone Generator Registers Page 0, Registers 71 through 79. The sine wave generator is very flexible, and is completely register programmable using nine registers of 8-bits each to provide many different sounds.

Two registers are used for programming the 16-bit, twos complement, sine-wave coefficient (Page 0, Registers 76 and 77). Two other registers program the 16-bit, twos complement, cosine-wave coefficient (Page 0, Registers 78 and 79). This coefficient resolution allows virtually any frequency of sine wave in the audio band to be generated up to DAC_FS/2.

Three registers are used to control the length of the sine burst waveform which are located on Page 0, Registers 73, 74, and 75. The resolution (bit) in the registers of the sine burst length is one sample period, so this allows great control on the overall time of the sine burst waveform. This 24-bit length timer supports 16,777,215 sample periods. (For example if DAC_FS is set at 48 kHz, and the registers combined value equals 96000d (01770h), then the sine burst would last exactly two seconds.)

Two registers are used to independently control the Left sine-wave volume and the Right sine-wave volume. The 6-bit digital volume control allows level control of 0 dB to –63 dB in one dB steps. The left-channel volume is controlled by writing to Page 0, Register 71, D(5:0). The right-channel volume is controlled by Page 0, Register 72, D(5:0). A master volume control for the left and right channel of the beep generator can be set up using Page 0, Register 72, D(7:6). The default volume control setting is 0 dB, the tone generator maximum-output level.

For playing back the sine wave, the DAC must be configured with regards to clock setup and routing. The sine wave gets started by setting the Beep Generator Enable Bit (Page 1, Register 71, D(7)=1)). After the sine wave has played for its predefined time period this bit will automatically set back to 0. While the sine wave is playing, the parameters of the beep generator cannot be changed. To stop the sine wave while it is playing set the Beep Generator Enable Bit to 0.

5.14.2 Digital Auto Mute

The TLV320AIC36 also incorporates a special feature, in which the DAC channel is auto-muted when a continuous stream of DC-input is detected. By default, this feature is disabled. It can be enabled by writing a non-000 value into Page 0, Register 64, D(6:4). The non-zero value controls the duration of continuous stream of DC-input before which the auto-mute feature takes effect. This feature is especially helpful for eliminating high-frequency-noise power being delivered into the load even during silent periods of speech or music.

5.14.3 Adaptive Filtering

When the DAC is running, the user-programmable filter coefficients are locked and cannot be accessed for either read or write.

However the TLV320AIC36 offers an adaptive filter mode as well. Setting Register Page 8, Reg 1, D(2)=1 will turn on double buffering of the coefficients. In this mode, filter coefficients can be updated through the host, and activated without stopping and restarting the DAC. This enables advanced adaptive filtering applications.

In the double-buffering scheme, all coefficients are stored in two buffers (Buffers A and B). When the DAC is running and adaptive filtering mode is turned on, setting the control bit Page 8, Register 1, D(0)=1 switches the coefficient buffers at the next start of a sampling period. This bit is set back to 0 after the switch occurs. At the same time, the flag Page 8, Reg 1, D(1) toggles.

The flag in Page 8, Register 1, D(1) indicates which of the two buffers is actually in use.

Page 8, Register 1, D(1)=0: Buffer A is in use by the DAC engine, D(1)=1: Buffer B is in use.

While the device is running, coefficient updates are always made to the buffer not in use by the DAC, regardless to which buffer the coefficients have been written.

DAC Running	Page 8, Reg 1, D(1)	Coefficient Buffer in Use	Writing To	Will Update
No	0	None	C1, Buffer A	C1, Buffer A
No	0	None	C1, Buffer B	C1, Buffer B
Yes	0	Buffer A	C1, Buffer A	C1, Buffer B
Yes	0	Buffer A	C1, Buffer B	C1, Buffer B
Yes	1	Buffer B	C1, Buffer A	C1, Buffer A
Yes	1	Buffer B	C1, Buffer B	C1, Buffer A

The user programmable coefficients C1 to C70 are defined on Pages 8 and 9 for Buffer A and Pages 12 and 13 for Buffer B.

5.15 DAC Setup

The following paragraphs are intended to guide a user through the steps necessary to configure the TLV320AIC36 DAC.

Step 1

The system clock source (master clock) and the targeted DAC sampling frequency must be identified.

Depending on the targeted performance the decimation filter type (A, B or C) and DOSR value can be determined.

-
- Filter A should be used for 48-kHz high-performance operation, DOSR must be a multiple of 8.
- Filter B should be used for up to 96k-Hz operations, DOSR must be a multiple of 4.
- Filter C should be used for up to 192-kHz operations, DOSR must be a multiple of 2.

In all cases the DOSR is limited in its range by the following condition:

2.8 MHz < DOSR * DAC_FS < 6.2 MHz

Based on the identified filter type and the required signal processing capabilities, the appropriate processing block can be determined from the list of available processing blocks (PRB_P1 to PRB_P25).

Based on the available master clock, the chosen DOSR and the targeted sampling rate, the clock divider values NDAC and MDAC can be determined. If necessary, the internal PLL can add a large degree of flexibility.

To a large degree, NDAC and MDAC can be chosen independently in the range of 1 to 128. In general, NDAC should be as large as possible as long as the following condition can still be met:

MADC*DOSR/32 ≥ RC

RC is a function of the chosen processing block and is listed in Table 5-12.

At this point the following device specific parameters are known:

PRB_Rx, DOSR, NADC, MADC, input and output common-mode values

If the PLL is used, the PLL parameters P, J, D and R are determined as well.

Step 2

Setting up the device through register programming:

The following list gives a sequence of items that must be executed in the time between powering the device up and reading data from the device:

Define starting point:	Initiate SW Reset
Program PMU settings:	Turn on charge pump Turn on ADC and DAC LDO with current limit
Program Clock Settings:	Program PLL clock dividers P, J, D, R (if PLL is necessary) Power up PLL (if PLL is necessary) Program and power up NADC Program and power up MADC Program OSR value Program the processing block to be used
Program Codec Interface:	Set word length, BCLK, WCLK I/O, mode type, for example, I^2S/DSP

Program Analog Blocks	Program headphone specific depop settings Power up DAC Modulator startup sequence Set Modulator taps for low noise Set Dac driver current control for low power Route DAC/PGA/LINEIN to outputs Release LDO current limit Unmute, set gain and power up outputs

To obtain optimum DAC audio quality, it is necessary to write the following sequence prior to enabling the DAC:

```
# Modulator startup sequence for optimum DAC audio quality
w 30 00 fd
w 30 0d 0d
w 30 04 20
w 30 0d 00
```

See Section 5.20 for a detailed application example.

5.16 Clock Generation and PLL

The TLV320AIC36 supports a wide range of options for generating clocks for the ADC and DAC sections as well as interface and other control blocks as shown in Figure 5-32. The clocks for ADC and DAC require a source reference clock. This clock can be provided on a variety of device pins such as MCLK, BCLK or GPI pins. The source reference clock for the codec can be chosen by programming the CODEC_CLKIN value on Page 0, Register 4, D(1:0). The CODEC_CLKIN can then be routed through highly-flexible clock dividers see Figure 5-32 to generate the various clocks required for ADC, DAC and the miniDSP sections. In the event that the desired audio or miniDSP clocks cannot be generated from the reference clocks on MCLK, BCLK or GPIO, the TLV320AIC36 also provides the option of using the on-chip PLL which supports a wide range of fractional multiplication values to generate the required clocks. Starting from CODEC_CLKIN the TLV320AIC36 provides several programmable clock dividers to help achieve a variety of sampling rates for ADC, DAC and clocks for the miniDSP.

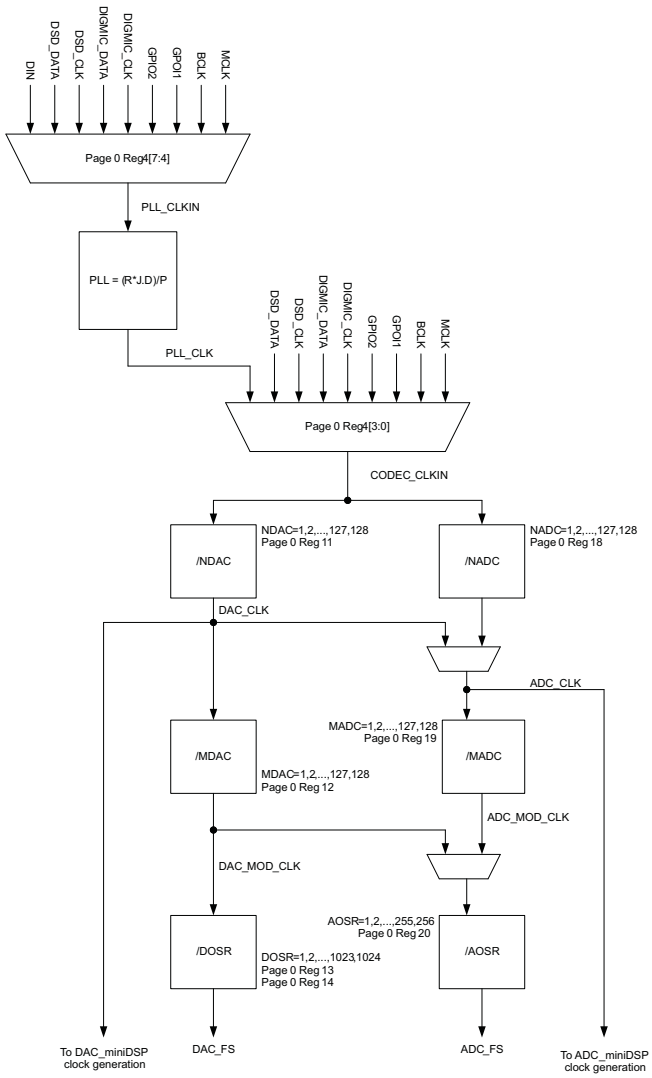


Figure 5-32. Clock Distribution Tree

$$ADC\_f_S = \frac{CODEC\_CLKIN}{NADC \times MADC \times AOSR} \quad (13)$$

$$ADC\_MOD\_CLK = \frac{CODEC\_CLKIN}{NADC \times MADC} \quad (14)$$

$$DAC\_f_S = \frac{CODEC\_CLKIN}{NDAC \times MDAC \times DOSR} \quad (15)$$

$$DAC\_MOD\_CLK = \frac{CODEC\_CLKIN}{NDAC \times MDAC} \quad (16)$$

Table 5-19. CODEC CLKIN Clock Dividers

Divider	Bits
NDAC	Page 0, Register 11, D(6:0)
MDAC	Page 0, Register 12, D(6:0)
DOSR	Page 0, Register 13, D(1:0) + Page 0, Register 14, D(7:0)
NADC	Page 0, Register 18, D(6:0)
MADC	Page 0, Register 19, D(6:0)

Table 5-19. CODEC CLKIN Clock Dividers (continued)

Divider	Bits
AOSR	Page 0, Register 20, D(7:0)

The DAC Modulator is clocked by DAC_MOD_CLK. For proper power-up operating of the DAC Channel, these clocks must be enabled by configuring the NDAC and MDAC clock dividers (Page 0, Register 11, D(7) =1 and Page 0, Register 12, D(7)=1). When the DAC channel is powered down, the device internally initiates a power-down sequence for proper shut-down. During this shut-down sequence, the NDAC and MDAC dividers must not be powered down, or else a proper low power shut-down may not take place. The user can read back the power-status flag Page 0, Register 37, D(7) and Page 0, Register 37, D(3). When both the flags indicate power-down, the MDAC divider may be powered down, followed by the NDAC divider.

The ADC modulator is clocked by ADC_MOD_CLK. For proper power-up of the ADC Channel, these clocks are enabled by the NADC and MADC clock dividers (Page 0, Register 18, D(7) =1 and Page 0, Register 19, D(7)=1). When the ADC channel is powered down, the device internally initiates a power-down sequence for proper shut-down. During this shut-down sequence, the NADC and MADC dividers must not be powered down, or else a proper low power shut-down may not take place. The user can read back the power-status flag Page 0, Register 36, D(6) and Page 0, Register 36, D(2). When both the flags indicate power-down, the MADC divider may be powered down, followed by NADC divider.

When ADC_CLK is derived from the NDAC divider output, the NDAC must be kept powered up till the power-down status flags for ADC do not indicate power-down. When the input to the AOSR clock divider is derived from DAC_MOD_CLK, then MDAC must be powered up when ADC_FS is needed (that is, when WCLK is generated by TLV320AIC36 or AGC is enabled) and can be powered down only after the ADC power-down flags indicate power-down status.

In general, all the root clock dividers should be powered down only after the child clock dividers have been powered down for proper operation.

The TLV320AIC36 also has options for routing some of the internal clocks to the output pins of the device to be used as general purpose clocks in the system. The feature is shown in Figure 5-33.

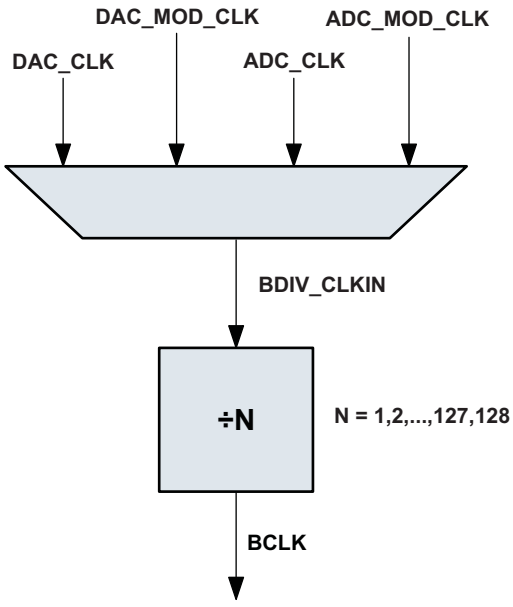


Figure 5-33. BCLK Output Options

In the mode when TLV320AIC36 is configured to drive the BCLK pin (Page 0, Register 25, D3='1') it can be driven as divided value of BDIV_CLKIN. The division value can be programmed in Page 0, Register 28, D(6:0) from 1 to 128. The BDIV_CLKIN can itself be configured to be one of DAC_CLK, DAC_MOD_CLK,

ADC_CLK or ADC_MOD_CLK by configuring the BDIV_CLKIN mux in Page 0, Register 27, D(1:0). Additionally a general purpose clock can be driven out on DOUT or a GPIO pin. This clock can be a divided down version of CDIV_CLKIN. The value of this clock divider can be programmed from 1 to 128 by writing to Page 0, Register 24, D(6:0). The CDIV_CLKIN can itself be programmed as one of the clocks among the list shown in Figure 5-34. This can be controlled by programming the mux in Page 0, Register 23, D(2:0).

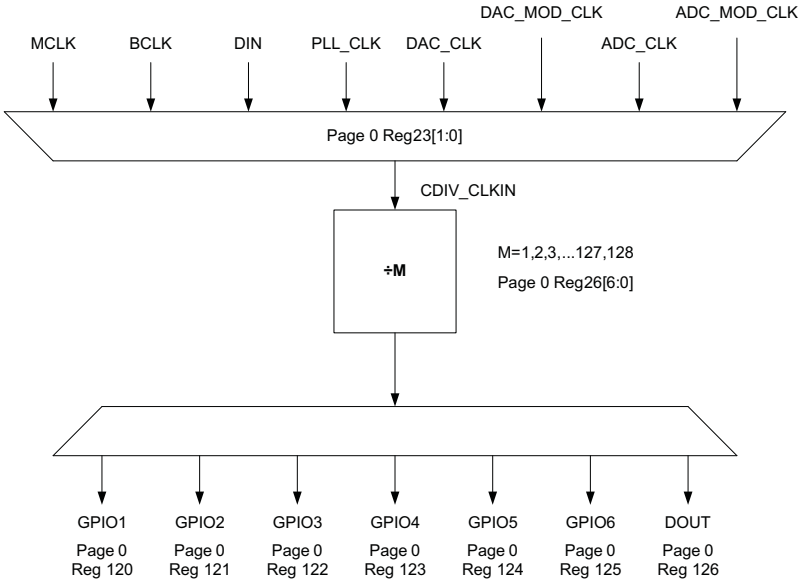


Figure 5-34. General-Purpose Clock Output Options

Table 5-20. Maximum TLV320AIC36 Clock Frequencies

Clock	Maximum Frequency (DVDD=1.8V)	Maximum Frequency (DVDD=1.5V)
CODEC_CLKIN	110MHz	104MHz
ADC_CLK	60MHz	34.6MHz
ADC_miniDSP_CLK	30MHz	17.3MHz
ADC_MOD_CLK	6.758MHz	5.77MHz
ADC_FS	0.192MHz	0.18MHz
DAC_CLK	60MHz	34.6MHz
DAC_miniDSP_CLK	60MHz	34.6MHz
DAC_MOD_CLK	6.758MHz	5.77MHz
DAC_FS	0.192MHz	0.18MHz
BDIV_CLKIN	50MHz	34.6MHz
CDIV_CLKIN	110MHz	104MHz

5.16.1 PLL

The TLV320AIC36 has an on chip PLL with fractional multiplication to generate the clock frequency needed by the audio ADC, DAC, and Digital Signal Processing blocks. The programmability of the PLL allows operation from a wide variety of clocks that may be available in the system.

The PLL input supports clocks varying from 512 kHz to 20 MHz and is register programmable to enable generation of required sampling rates with fine precision. The PLL can be turned on by writing to Page 0, Register 5, D(7). When the PLL is enabled, the PLL output clock PLL_CLK is given by the following equation:

$$PLL\_CLK = \frac{PLL\_CLKIN \times R \times J.D}{P} \quad (17)$$

Where:

R = 1, 2, 3, 4

J = 4, 5, 6,… 63, and D = 0, 1, 2… 9999

P = 1, 2, 3… 8

R, J, D, and P are register programmable.

The PLL can be programmed using Page 0, Registers 5 thru 8. The PLL can be turned on using Page 0, Register 5, D(7). The variable P can be programmed using Page 0, Register 5, D(6:4). The default register value for P is 2. The variable R can be programmed using Page 0, Register 5, D(3:0). The default register value for R is 1. The variable J can be programmed using Page 0, Register 6, D(5:0). The variable D is 12 bits and is programmed into two registers. The MSB portion can be programmed using Page 0, Register 7, D(5:0), and the LSB portion is programmed using Page 0, Register 8, D(5:0). The default register value for D is 0.

When the PLL is enabled the following conditions must be satisfied

- When the PLL is enabled and D = 0, the following conditions must be satisfied for PLL_CLKIN:

$$512kHz \le \frac{PLL\_CLKIN}{P} \le 20MHz \quad (18)$$

- When the PLL is enabled and D ≠ 0, the following conditions must be satisfied for PLL_CLKIN:

$$10MHz \le \frac{PLL\_CLKIN}{P} \le 20MHz \quad (19)$$

The PLL can be powered up independent of the ADC and DAC blocks, and can also be used as a general purpose PLL by routing its output to a GPIO output. After powering up the PLL, PLL_CLK is available typically after 10 ms. The PLL output frequency is controlled by J.D and R dividers

PLL Divider	Bits
J	Page 0, Register 6, D(5:0)
D	Page 0, Register 7, D(5:0) && Page 0, Register 8, D(7:0)
R	Page 0, Register 5, D(3:0)

The D-divider value is 14-bits wide and is controlled by two registers. For proper update of the D-divider value, Page 0, Register 7 must be programmed first followed immediately by Page 0, Register 8. Unless the write to Page 0, Register 8 is completed, the new value of D will not take effect.

The clocks for codec and various signal processing blocks, CODEC_CLKIN can be generated from MCLK input, BCLK input, GPIO inputs or PLL_CLK (Page 0/Register 4/D(1:0)).

If the CODEC_CLKIN is derived from the PLL, then the PLL must be powered up first and powered down last.

Table 5-21 lists several example cases of typical MCLK rates and how to program the PLL to achieve a sample rate Fs of either 44.1 or 48kHz.

Table 5-21. PLL Example Configurations

Fs = 44.1 kHz										
MCLK (MHz)	PLLP	PLLR	PLLJ	PLLD	MADC	NADC	AOSR	MDAC	NDAC	DOSR
2.8224	1	3	10	0	3	5	128	3	5	128
5.6448	1	3	5	0	3	5	128	3	5	128
12	1	1	7	560	3	5	128	3	5	128
13	1	2	4	2336	13	3	64	4	6	104

Table 5-21. PLL Example Configurations (continued)

Fs = 44.1 kHz										
MCLK (MHz)	**PLLP**	**PLLR**	**PLLJ**	**PLLD**	**MADC**	**NADC**	**AOSR**	**MDAC**	**NDAC**	**DOSR**
16	1	1	5	2920	3	5	128	3	5	128
19.2	1	1	4	4100	3	5	128	3	5	128
48	4	1	7	560	3	5	128	3	5	128
Fs = 48 kHz										
2.048	1	3	14	0	2	7	128	7	2	128
3.072	1	4	7	0	2	7	128	7	2	128
4.096	1	3	7	0	2	7	128	7	2	128
6.144	1	2	7	0	2	7	128	7	2	128
8.192	1	4	3	0	2	8	128	4	4	128
12	1	1	7	1680	2	7	128	7	2	128
16	1	1	5	3760	2	7	128	7	2	128
19.2	1	1	4	4800	2	7	128	7	2	128
48	4	1	7	1680	2	7	128	7	2	128

5.17 Interface

5.17.1 Audio Digital I/O Interface

Audio data is transferred between the host processor and the TLV320AIC36 through the digital audio data serial interface, or audio bus. The audio bus on this device is very flexible, including left or right-justified data options, support for I^2S or PCM protocols, programmable data length options, a TDM mode for multichannel operation, very flexible master/slave configurability for each bus clock line, and the ability to communicate with multiple devices within a system directly.

The audio bus of the TLV320AIC36 can be configured for left or right-justified, I^2S, DSP, or TDM modes of operation, where communication with standard telephony PCM interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits by configuring Page 0, Register 25, D(5:4). In addition, the word clock and bit clock can be independently configured in either Master or Slave mode, for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum of the selected ADC and DAC sampling frequencies.

The bit clock is used to clock in and clock out the digital audio data across the serial bus. When in Master mode, this signal can be programmed to generate variable clock pulses by controlling the bit-clock divider in Page 0, Register 28 (see Figure 5-32). The number of bit-clock pulses in a frame may need adjustment to accommodate various word-lengths as well as to support the case when multiple TLV320AIC36s may share the same audio bus.

The TLV320AIC36 also includes a feature to offset the position of start of data transfer with respect to the word-clock. This offset can be controlled in terms of number of bit-clocks and can be programmed in Page 0, Register 26.

The TLV320AIC36 also has the feature of inverting the polarity of the bit-clock used for transferring the audio data as compared to the default clock polarity used. This feature can be used independently of the mode of audio interface chosen. This can be configured using Page 0, Register 27, D(3).

The TLV320AIC36 further includes programmability (Page 0, Register 25, D0) to 3-state the DOUT line during all bit clocks when valid data is not being sent. By combining this capability with the ability to program at what bit clock in a frame the audio data begins, time-division multiplexing (TDM) can be accomplished, enabling the use of multiple codecs on a single audio serial data bus. When the audio serial data bus is powered down while configured in master mode, the pins associated with the interface are put into a 3-state output condition.

By default when the word-clocks and bit-clocks are generated by the TLV320AIC36, these clocks are active only when the codec (ADC, DAC or both) are powered up within the device. This is done to save power. However, it also supports a feature when both the word clocks and bit-clocks can be active even when the codec in the device is powered down. This is useful when using the TDM mode with multiple codecs on the same bus, or when word-clock or bit-clocks are used in the system as general-purpose clocks.

5.17.1.1 Right-Justified Mode

The Audio Interface of the TLV320AIC36 can be put into Right Justified Mode by programming Page 0, Register 25, D(7:6) = 10. In right-justified mode, the LSB of the left channel is valid on the rising edge of the bit clock preceding the falling edge of the word clock. Similarly, the LSB of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

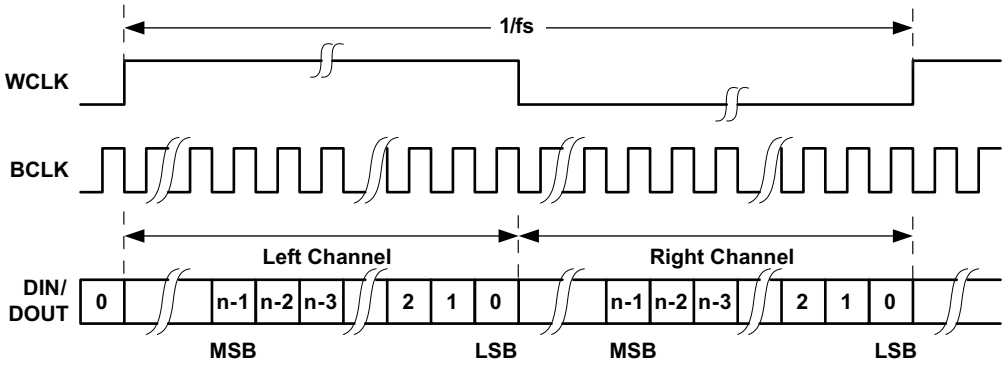


Figure 5-35. Timing Diagram for Right-Justified Mode

For Right-Justified mode, the number of bit-clocks per frame should be greater than twice the programmed word-length of the data.

5.17.1.2 Left-Justified Mode

The Audio Interface of the TLV320AIC36 can be put into Left Justified Mode by programming Page 0, Register 25, D(7:6) = 11. In left-justified mode, the MSB of the right channel is valid on the rising edge of the bit clock following the falling edge of the word clock. Similarly the MSB of the left channel is valid on the rising edge of the bit clock following the rising edge of the word clock.

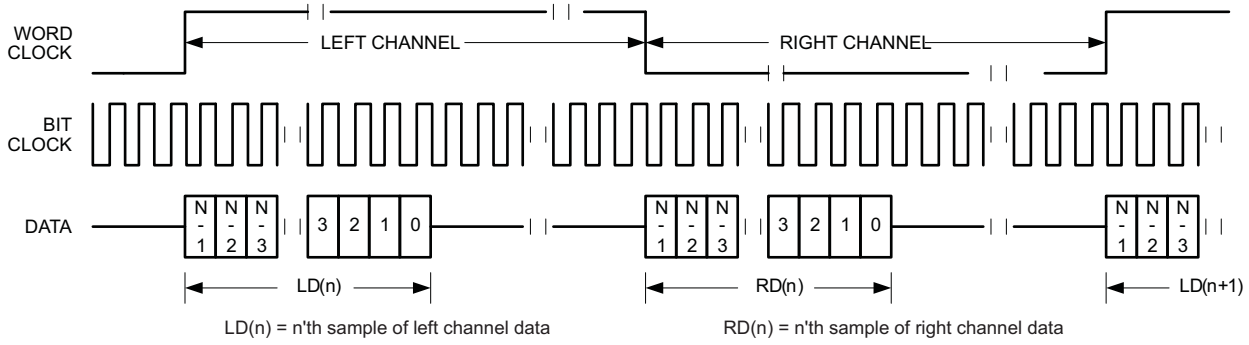


Figure 5-36. Timing Diagram for Left-Justified Mode

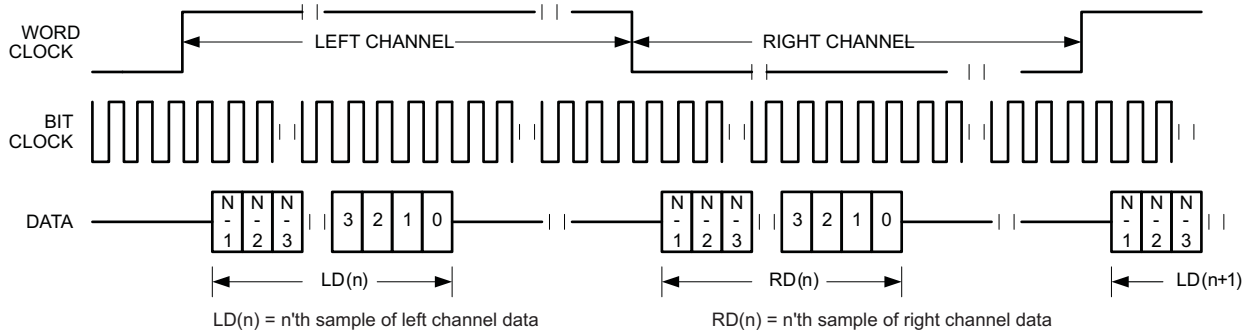


Figure 5-37. Timing Diagram for Left-Justified Mode with Offset=1

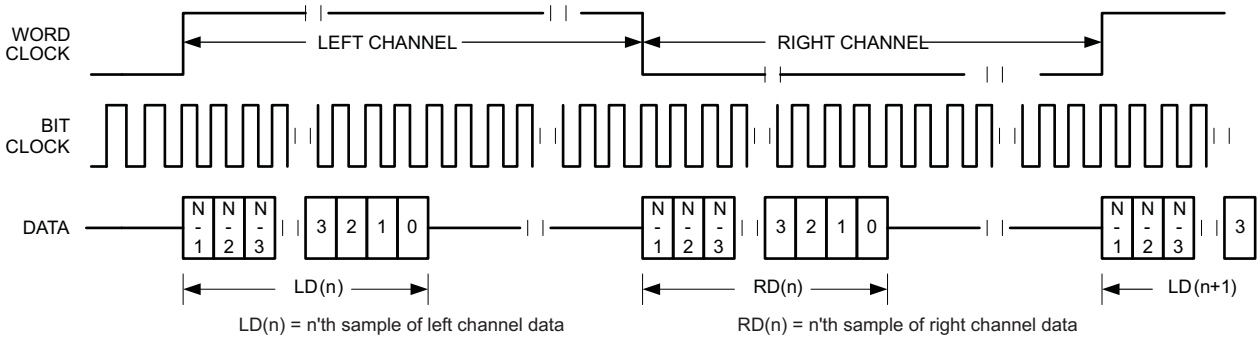


Figure 5-38. Timing Diagram for Left-Justified Mode with Offset = 0 and Inverted Bit Clock

For Left-Justified mode, the number of bit-clocks per frame should be greater than twice the programmed word-length of the data. Also, the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

5.17.1.3 I^2S Mode

The Audio Interface of the TLV320AIC36 can be put into Right Justified Mode by programming Page 0, Register 25, D(7:6) = to 00. In I^2S mode, the MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

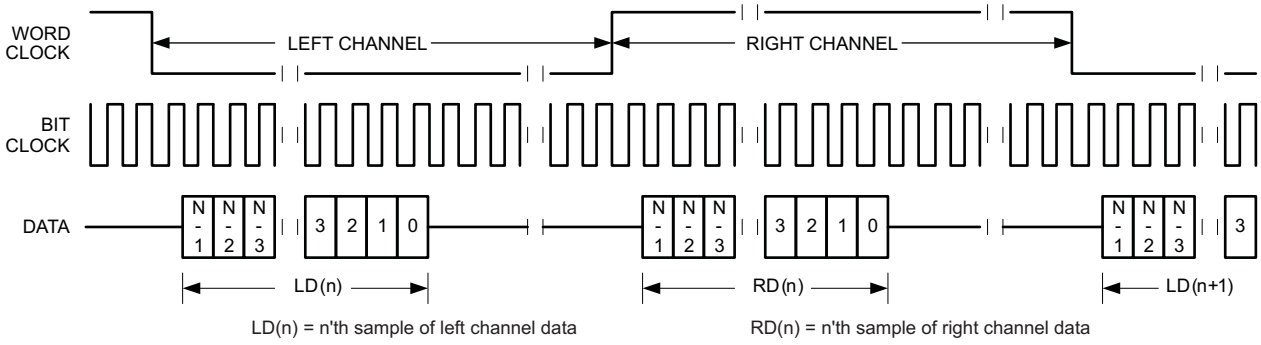


Figure 5-39. Timing Diagram for I^2S Mode

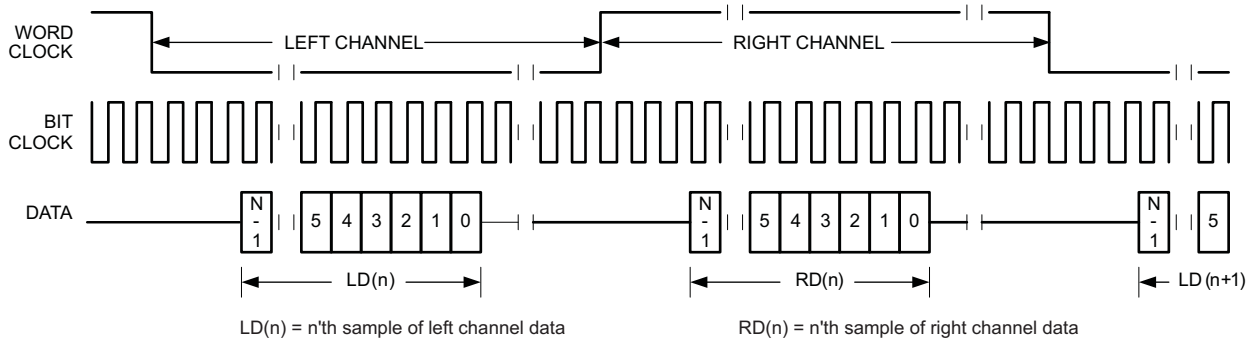


Figure 5-40. Timing Diagram for I²S Mode With Offset = 2

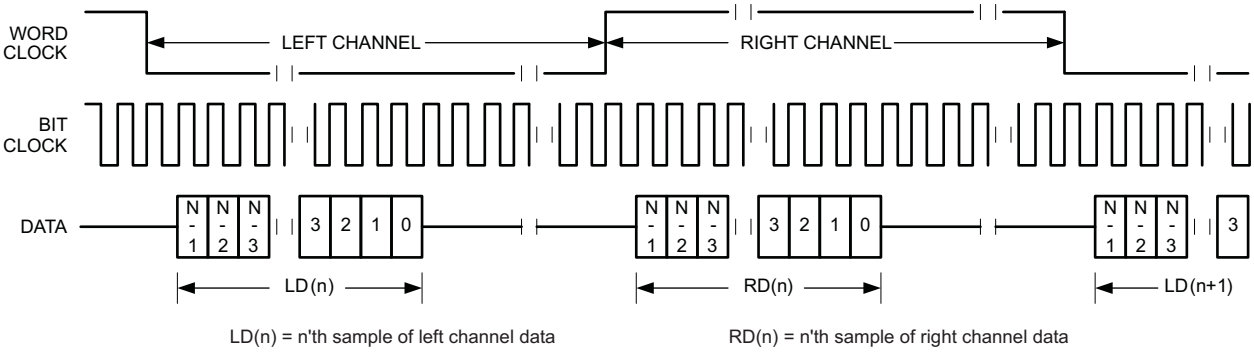


Figure 5-41. Timing Diagram for I²S Mode With Offset = 0 and Bit Clock Invert

For I²S mode, the number of bit-clocks per channel should be greater than or equal to the programmed word-length of the data. Also the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

5.17.1.4 DSP Mode

The Audio Interface of the TLV320AIC36 can be put into Right Justified Mode by programming Page 0, Register 25, D(7:6) = 01. In DSP mode, the falling edge of the word clock starts the data transfer with the left channel data first and immediately followed by the right channel data. Each data bit is valid on the falling edge of the bit clock.

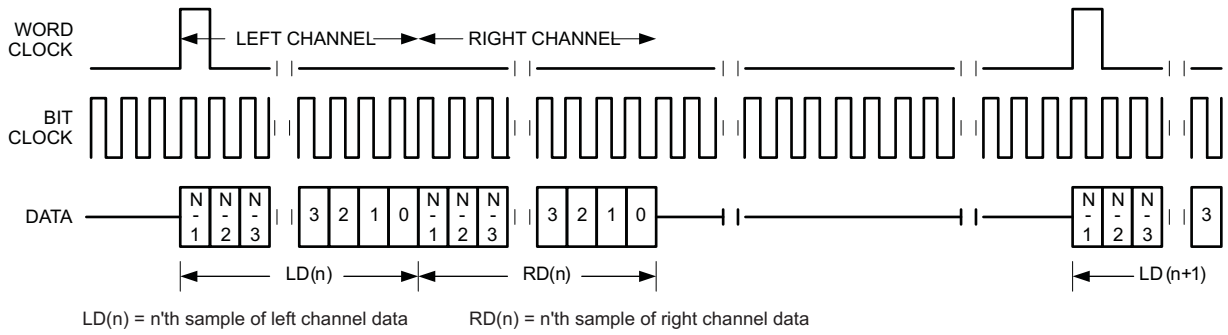


Figure 5-42. Timing Diagram for DSP Mode

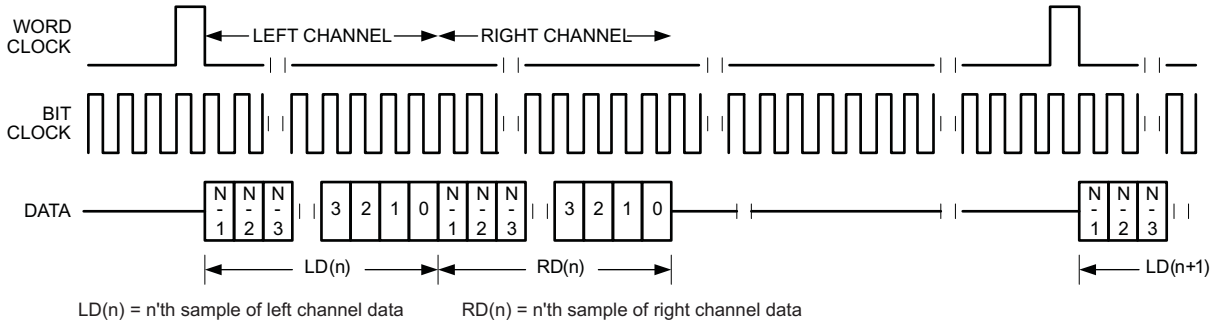


Figure 5-43. Timing Diagram for DSP Mode With Offset = 1

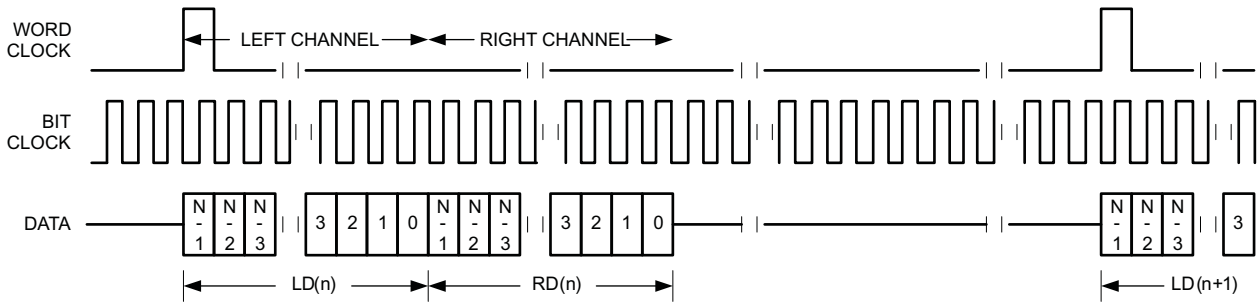


Figure 5-44. Timing Diagram for DSP Mode With Offset = 1 and Bit Clock Inverted

For DSP mode, the number of bit-clocks per frame should be greater than twice the programmed word-length of the data. Also the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

5.17.1.5 Secondary I^2S

The audio serial interface on the TLV320AIC36 has an extensive I/O control to allow communication with two independent processors for audio data. Each processor can communicate with the device one at a time. This feature is enabled by register programming of the various pin selections.

Figure 5-45 illustrates possible audio interface routing.

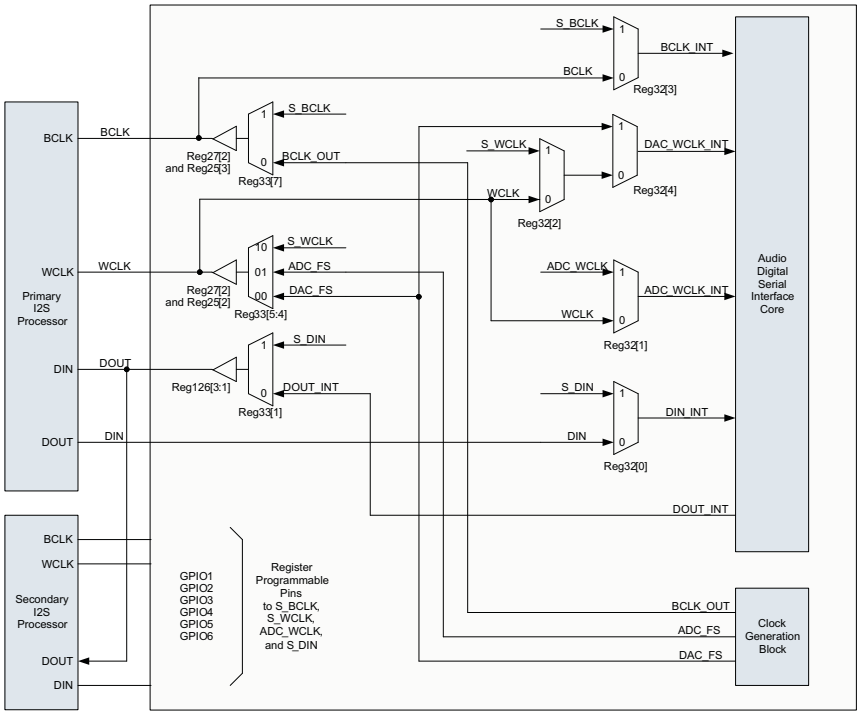


Figure 5-45. Audio Serial Interface Multiplexing

5.17.2 I²C Control InterFACE

The TLV320AIC36 supports the I²C control protocol, and will respond to the I²C address of 0011000. I²C is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the I²C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pullup resistors, so the bus wires are HIGH when no device is driving them LOW. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

Communication on the I²C bus always takes place between two devices, one acting as the master and the other acting as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I²C devices can act as masters or slaves, but the TLV320AIC36 can only act as a slave device.

An I²C bus consists of two lines, SDA and SCL. SDA carries data, and the SCL signal provides the clock. All data is transmitted across the I²C bus in groups of 8 bits. To send a bit on the I²C bus, the SDA line is driven to the appropriate level while SCL is LOW (a LOW on SDA indicates the bit is zero, while a HIGH indicates the bit is one).

Once the SDA line has settled, the SCL line is brought HIGH, then LOW. This pulse on the SCL line clocks the SDA bit into the receiver's shift register.

The I²C bus is bidirectional: the SDA line is used both for transmitting and receiving data. When a master reads from a slave, the slave drives the data line; when a master sends to a slave, the master drives the data line.

Most of the time the bus is idle, no communication is taking place, and both lines are HIGH. When communication is taking place, the bus is active. Only master devices can start communication on the bus. Normally, the data line is only allowed to change state while the clock line is LOW. If the data line changes state while the clock line is HIGH, it is either a START condition or its counterpart, a STOP condition. A START condition is when the clock line is HIGH and the data line goes from HIGH to LOW. A STOP condition is when the clock line is HIGH and the data line goes from LOW to HIGH.

After the master issues a START condition, it sends a byte that selects the slave device for communication. This byte is called the address byte. Each device on an I^2C bus has a unique 7-bit address to which it responds. (Slaves can also have 10-bit addresses; see the I^2C specification for details.) The master sends an address in the address byte, together with a bit that indicates whether it wishes to read from or write to the slave device.

Every byte transmitted on the I^2C bus, whether it is address or data, is acknowledged with an acknowledge bit. When a master has finished sending a byte (eight data bits) to a slave, it stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA LOW. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when a master has finished reading a byte, it pulls SDA LOW to acknowledge this to the slave. It then sends a clock pulse to clock the bit. (Remember that the master always drives the clock line.)

A not-acknowledge is performed by simply leaving SDA HIGH during an acknowledge cycle. If a device is not present on the bus, and the master attempts to address it, it will receive a not−acknowledge because no device is present at that address to pull the line LOW.

When a master has finished communicating with a slave, it may issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. A master may also issue another START condition. When a START condition is issued while the bus is active, it is called a repeated START condition.

The TLV320AIC36 can also respond to and acknowledge a General Call, which consists of the master issuing a command with a slave address byte of 00H. This feature is disabled by default, but can be enabled using Page 0, Register 34, Bit D(5).

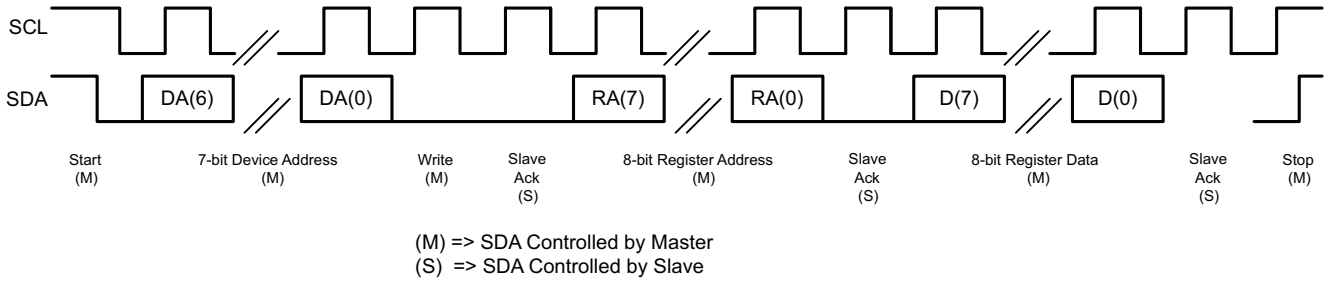


Figure 5-46. I^2C Write

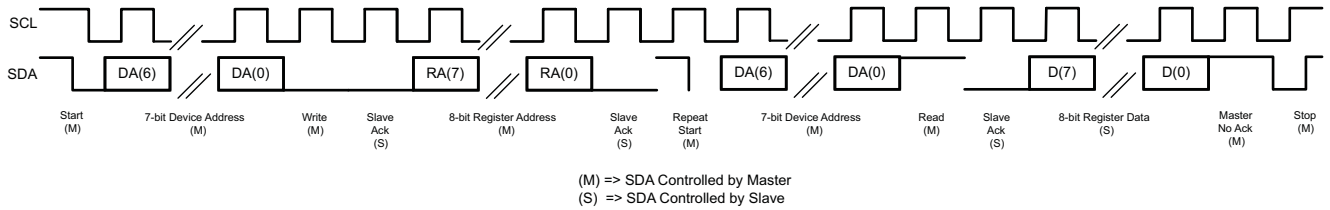


Figure 5-47. I^2C Read

In the case of an I^2C register write, if the master does not issue a STOP condition, then the device enters auto-increment mode. So in the next eight clocks, the data on SDA is treated as data for the next incremental register.

Similarly, in the case of an I^2C register read, after the device has sent out the 8-bit data from the addressed register, if the master issues a ACKNOWLEDGE, the slave takes over control of SDA bus and transmit for the next eight clocks the data of the next incremental register.

5.18 Power Management Unit

The allowed voltage supply ranges for the TLV320AIC36 analog blocks are 1.4 V to 1.8 V and –1.4 V to –1.8V. To ease system-level design, a charge pump and three low-dropout regulators (LDOs) are integrated to generate the appropriate analog voltage supplies from a single 2.1 to 2.8 V supply input. One positive LDO is used to generate a nominal +1.8 V supply for the input PGA and ADC section and another positive LDO generates a nominal +1.65 V for the DAC and audio amplifier sections. A negative charge pump generates a negative voltage which is then regulated to a nominal -1.65 V using a negative LDO. Figure 5-48 shows suggested hookup from the PMU to the analog core.

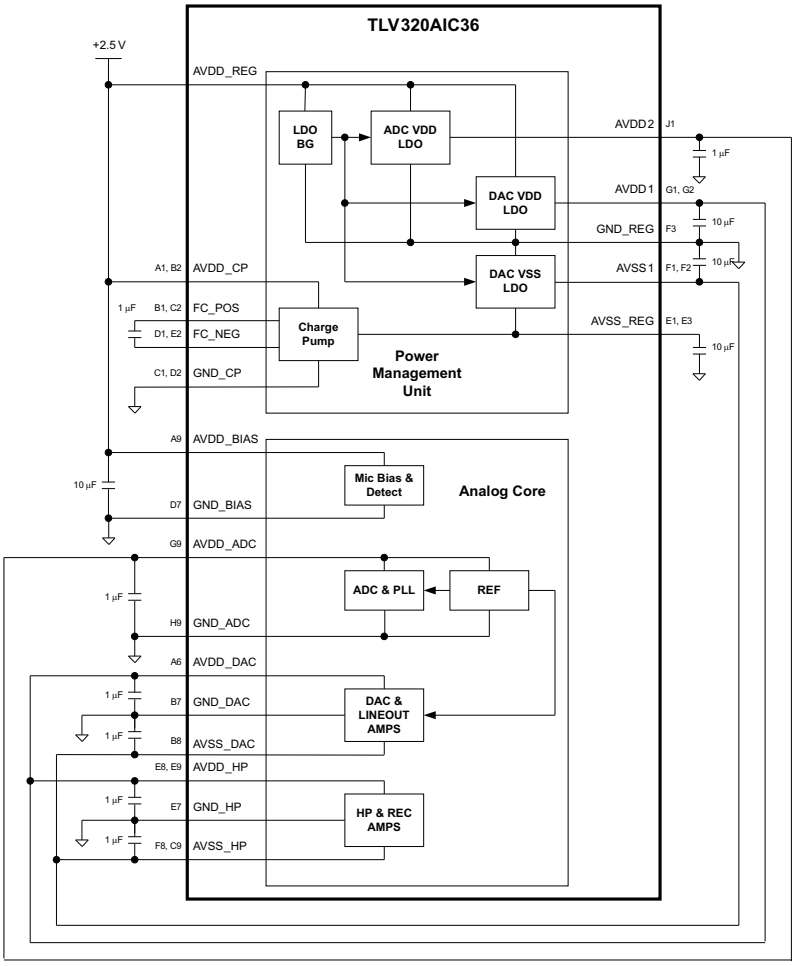


Figure 5-48. Recommended Analog Power Supply Connections

Internal voltage references for the analog core are derived from the AVDD_ADC supply inputs. Even in playback-only applications, the AVDD_ADC supply inputs must be powered to support the internal references.

5.18.1 Charge Pump

The charge pump uses a minimum 1-µF flying capacitor connected between FC_POS and FC_NEG. AVDD_CP is the positive (input) supply connection and AVSS_REG is the negative (output) connection. A 1-µF smoothing capacitor is recommended on the AVSS_REG node, although a smaller value can be used at the expense of increased ripple on the input to the negative regulator.

The charge pump is enabled by setting Page 2, Register 71, D0=1. By default the charge pump uses a divided version of BCLK as its clock, but setting Page 2, Register 71, D1=1 will cause it to use MCLK instead. The frequency division is controlled by two registers: Page 2, Register 72 contains the number of clock cycles that the charge pump clock is high (minus one), while Page 2, Register 73 contains the number of clock cycles the charge pump is low (minus one). As an example, if the default values of 11 are used in these two registers the charge pump clock frequency is BCLK/24.

The charge pump frequency should be programmed between 400 and 500 kHz. If no very high current loads are being driven from the amplifier section, this frequency can be reduced to save power. Care should be taken to keep the charge pump frequency above the audio range.

5.18.2 LDOs

The unregulated input for the two positive LDOs is AVDD_REG. AVDD1 is the output of the high-power regulator meant to drive the DAC and output amplifiers; a minimum of 10μF (maximum 100μF) capacitance is required on this pin for LDO stability. The capacitance can be split between AVDD1, AVDD_DAC, and AVDD_HP as long as the trace resistance plus the capacitor ESR is less than 400mΩ. Similarly a minimum of 1μF (maximum 10μF) is required on AVDD2, the output of the low-power regulator intended to supply the preamp and ADC section.

The input to the negative regulator is connected internally to the charge pump output. AVSS1 is the output of the high-power regulator meant to drive the DAC and output amplifiers; a minimum of 10μF (maximum 100μF) capacitance is required on this pin for LDO stability. The capacitance can be split between AVSS1, AVSS_DAC, and AVSS_HP as long as the trace resistance plus the capacitor ESR is less than 400mΩ.

The regulators are enabled by the lower 3 bits of Page 2, Register 74. The negative regulator should be enabled only after the charge pump is enabled, otherwise the charge pump may not start up properly.

By default, the regulators start up in a current-limited mode to prevent high inrush currents. The two high-power regulators (AVDD1 and AVSS1) are limited to 50 mA, while the low-power regulator (AVDD2) is limited to 5 mA. After the regulators have had time to power up, remove the current limit by clearing the least-significant 3 bits of Page 2, Register 76.

Short circuit protection for the regulators may be disabled through Page 2, Register 77. The nominal output level of the regulators can be programmed through Page 2, Register 78.

5.18.3 Low Power Mode

In addition to the standard configuration, the PMU can be used in two alternative configurations to further reduce power consumption. These low power modes sacrifice some performance for power savings. See sections 3.7 and 3.8 for typical performance electrical characteristics.

The first low power (LP) mode is capable of reducing power dissipation to 14mW for DAC to headphone playback. Max headphone output power is 20mW per channel. Referring to Figure 5-48, the changes are:

1. AVDD_REG supply should be reduced to 1.8V (1.65V min)
2. This 1.8V supply also drives AVDD_ADC. AVDD2 is not connected to AVDD_ADC, and the AVDD LDO is disabled.
3. Register settings (see Section 5.21): DAC VDD LDO=1.5V, DAC VSS LDO=1.5V, ADC VDD LDO = off, Bias current = low power setting, DACSP = PRB_P17, REC,LO,HP gain=-2dB.

The second ultra low power (ULP) mode is capable of reducing power dissipation to 10mW for DAC to headphone playback. Max output power is 10mW. Maximum input voltage for the ADC is reduced by 6dB.

Referring to Figure 5-48, the changes are

1. AVDD_REG supply should be reduced to 1.5V (1.4V min)
2. The 1.5V supply also drives AVDD_ADC, AVDD_DAC, AVDD_HP, DVDD.
3. AVSS_REG is directly connected to AVSS_DAC and AVSS_HP.
4. DAC VDD LDO, DAC VSS LDO, ADC VDD LDO are not used, powered down and disconnected.

5. 47 kΩ resistor is placed from FC_NEG to GND to speed charge pump startup.
6. Register settings (see Section 5.21): all LDOs=off, Bias current = low power setting. DACSP = PRB_P17, ADC CM=0.75V, ADC FS=0.83Vrms. REC,LO,HP gain=-5dB.

Referring to Table 5-20, adhere to the maximum clock frequencies listed for the ULP DVDD=1.5V mode.

5.19 Device Special Functions

5.19.1 Headset Detection

The DETECT input is used to monitor the external microphone bias for momentary connections to ground using an external resistor and pushbutton. Multiple pushbuttons and resistors may be placed in parallel to support detection of unique button presses as shown in Figure 5-49.

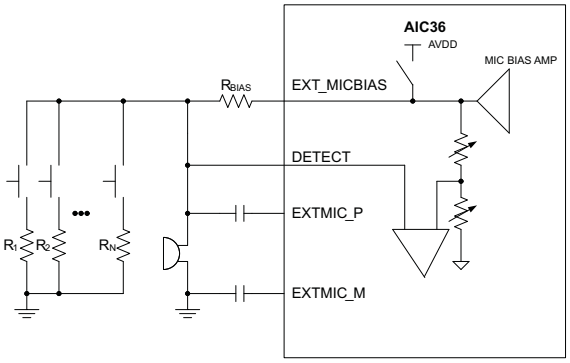


Figure 5-49. Microphone Bias Detection External Circuit

Unique values of R1, R2, through RN in series with RBIAS form a resistor voltage divider which can be sensed by the DETECT pin. This document details the AIC36 detect circuit and programming features.

5.19.1.1 Overview

Internally, the detect circuit consists of a low frequency oscillator, clock dividers, 5-bit SAR ADC, window comparator, and de-bounce functions as shown in Figure 5-50.

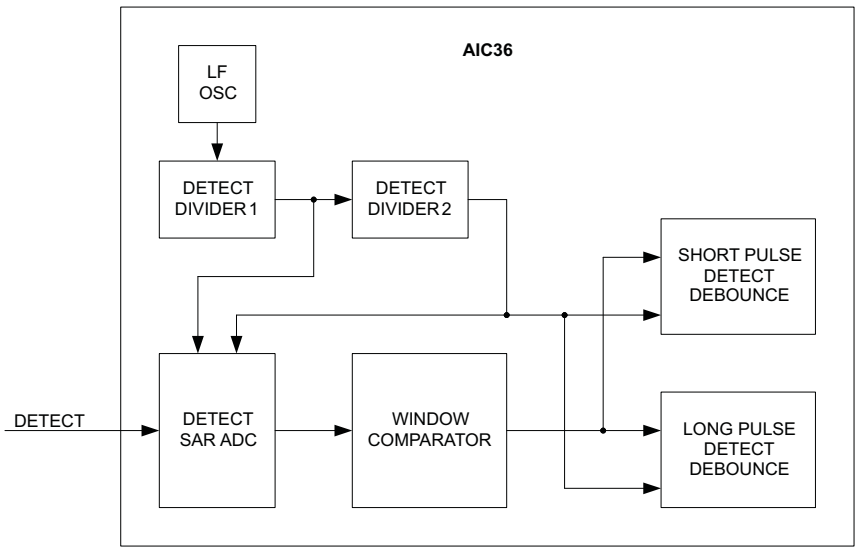


Figure 5-50. Detect Circuit Block Diagram

5.19.1.2 Basic Operational Description

The detect circuit, once programmed, can provide either on-demand sampling of the detect input or trigger an AIC36 interrupt when used in continuous detection mode. This section provides details for the main sub-sections of the detect circuit and provides programming examples to illustrate its operation.

First assume the EXT_MICBIAS circuit is enabled and programmed to the desired bias voltage. When no buttons are pressed, the voltage at the DETECT pin is determined by the bias current of the microphone and the bias resistor Rbias. If a button is pressed, the resistor associated with that button is put in parallel with the microphone, causing the voltage at the DETECT pin to drop. If the EXT_MICBIAS circuit is disabled, then the EXT_MICBIAS pin is temporarily connected to AVDD_BIAS for the duration of the ADC reading.

The 5-bit detect ADC has its input connected to the DETECT pin and its reference connected to the EXT_MICBIAS pin. Thus the output of the ADC is the DETECT pin voltage relative to the EXT_MICBIAS voltage. The state of the microphone and pushbuttons can be deduced from the ADC output. If the ADC output is zero, DETECT is shorted to ground; if it is full-scale then the microphone is unplugged. If the output is in between, then the microphone is plugged in and/or a button may be pressed, depending on the particular ADC output value.

The detect ADC can provide a raw value corresponding to the voltage at the detect pin but it's unsuitable as an interrupt source. To condition this raw detect value, an 8 window comparator is used to divide the 32-level ADC output into as many as eight mapped windows. Using seven programmable threshold registers, the edges of up to 8 windows are defined within the code values of 0–31 of the ADC. These threshold registers encode ranges of raw ADC values into a button press value which is then de-bounced for generating an interrupt.

As a windowing example, assume that three unique pushbuttons must be detected in an application. Based on resistor values selected for the voltage dividers, assume they correspond to raw ADC codes of ideally 4, 11, and 17. Thresholds 1, 2, and 3 can be set to 7, 14, and 23 as shown in Figure 5-51to window the three values. A fourth code range is defined to describe the ADC values returned when no button is pressed. To properly map ADC codes into windows, threshold 1 must correspond to the edge of the lowest window, threshold 2 is the next highest window, and so on. Detect threshold registers 4 through 7 should not be enabled in this case.

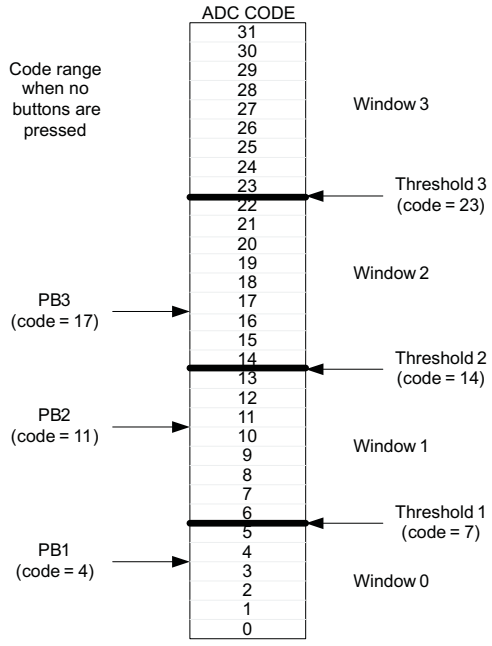


Figure 5-51. Example Threshold Settings

5.19.1.3 Sampling Rate and Debounce Period Control

The low frequency oscillator and detect dividers 1 and 2 provide clock generation for the circuit. When enabled, the LF oscillator provides a nominal frequency of 1MHz to detect divider 1, which in turn provides a clock source to detect divider 2. The detect divider 2 rate is the sampling rate of the ADC and the clock source for the detect debouncers. Detect divider 1 is the clock source for the SAR ADC.

The short and long detect debouncers are programmed separately and can generate an interrupt after detecting a stable window value (0–7) for a minimum number of divider 2 periods. Because one window will always correspond to a no-buttons pressed ADC value, interrupts generated from this window are useful for detecting button releases. The short and long debouncers are identical in function but can be programmed to different values.

5.19.1.4 Application Programming Example – Interrupt Driven

This example register initialization assumes four buttons with raw ADC values of 3, 9, 16, and 23 are required. Automatic button sampling will be enabled at a rate of 50 Hz and separate interrupts for short and long pulses of 400 and 800 ms will be generated on INT1 and INT2 respectively. INT1 and INT2 will be mapped to GPIO1 and GPIO2 respectively.

```
w 30 00 01 # Change to page 1
w 30 33 60 # Power up EXT_MICBIAS
w 30 00 02 # Change to page 2
w 30 70 00 # Enable LF oscillator (1MHz nominal)
w 30 15 C8 # Detect divider 1 set to 200 decimal (1MHz/200) = 5KHz
w 30 16 64 # Detect divider 2 set to 100 decimal (5KHz/100) = 50Hz
w 30 14 88 # Enable both detect dividers
w 30 17 80 # Enable continuous detection mode
w 30 1C 86 # Set and enable threshold 1 to 6 (between 3 and 9)
w 30 1D 8C # Set and enable threshold 2 to 12 (between 9 and 16)
w 30 1E 94 # Set and enable threshold 3 to 20 (between 16 and 23)
w 30 1F 99 # Set and enable threshold 4 to 25 (between 23 and open)
w 30 20 00 # Disable threshold 5
w 30 21 00 # Disable threshold 6
w 30 22 00 # Disable threshold 7
w 30 1A 14 # Set short pulse duration (1/50Hz) * 20 = 400ms
w 30 18 80 # Enable short pulse detection
w 30 1B 28 # Set long pulse duration (1/50Hz) * 40 = 800ms
w 30 19 80 # Enable long pulse detection
w 30 00 00 # Change to page 0
w 30 34 01 # Enable short detect interrupt to INT1
w 30 35 02 # Enable long detect interrupt to INT2
w 30 78 14 # Map INT1 to GPIO1 pin
w 30 79 20 # Map INT2 to GPIO2 pin
```

Upon GPIO1 interrupt, read Page 2, Register 0x18 for the short pushbutton value and write 0x01 to page 0 Reg 0x32 to clear the interrupt.

Upon GPIO2 interrupt, read Page 2, Register 0x19 for the long pushbutton value and write 0x02 to page 0 Reg 0x32 to clear the interrupt.

5.19.1.5 Application Programming Example – On-Demand Detect Sampling – Raw ADC

This example provides a fast, raw ADC sample of the detect pin. This feature is useful for determining the ADC code for a corresponding resistor value. No windowing or de-bouncing is performed in this mode.

```
w 30 00 01 # Change to page 1
w 30 33 60 # Power up EXT_MICBIAS
w 30 00 02 # Change to page 2
w 30 70 00 # Enable LF oscillator (1MHz nominal)
w 30 15 01 # Detect divider 1 set to 1 decimal (1MHz/1) = 1MHz
w 30 14 80 # Enable detect divider 1
w 30 17 20 # Initiate on-demand ADC sample
# Poll page 2 Reg 0x17, bit 5 for a 0 (1=in progress; 0=done)
# When done, read page 2 Reg 0x17, bits 4-0 for raw ADC code
w 30 70 01 # Disable LF oscillator
```

5.19.1.6 Application Programming Example – On-Demand Detect Sampling – Windowed

This example provides a fast, windowed ADC sample of the detect pin. This feature is useful for software initiated button detects. No de-bouncing is performed in this mode.

```
# Perform these steps only at system initialization

w 30 00 01 # Change to page 1
w 30 33 60 # Power up EXT_MICBIAS
w 30 00 02 # Change to page 2
w 30 15 01 # Detect divider 1 set to 1 decimal (1MHz/1) = 1MHz
w 30 16 01 # Detect divider 2 set to 1 decimal (1MHz/1) = 1MHz


      # (Using the window values from the previous example)
w 30 1C 86 # Set and enable threshold 1 to 6 (between 3 and 9)
w 30 1D 8C # Set and enable threshold 2 to 12 (between 9 and 16)
w 30 1E 94 # Set and enable threshold 3 to 20 (between 16 and 23)
w 30 1F 99 # Set and enable threshold 4 to 25 (between 23 and open)
w 30 20 00 # Disable threshold 5
w 30 21 00 # Disable threshold 6
w 30 22 00 # Disable threshold 7
w 30 18 00 # Disable short pulse detection

# Perform these steps only at on-demand time
w 30 70 00 # Enable LF oscillator (1MHz nominal)
w 30 14 88 # Enable detect divider 1 and 2
w 30 17 20 # Initiate on-demand ADC sample

# Poll page Reg 0x17, bit 5 for a 0 (1=in progress; 0=done)
# When done, read page 2 Reg 0x18, bits 6-4 for window number

w 30 70 01 # Disable LF oscillator
```

5.19.2 Low-Impedance Detection

The TLV320AIC36 supports detection of low impedance (<50 ohm) to ground on the HPL, HPR, RECL, RECR, and HOOK pins. Detection can either be performed manually using an I^2C register access or periodically sampled to generate an interrupt.

Manual detection is performed by enabling manual detection using Page 2, Register 108 and reading back the status register on Page 2, Register 109 on a per-pin basis. For power reasons, it is recommended that the enables for the manual detection in Register 108 are cleared after the status values are read from Register 108.

The periodic sampling rate uses the same LF oscillator and detect dividers as the headset detection see Figure 5-52.

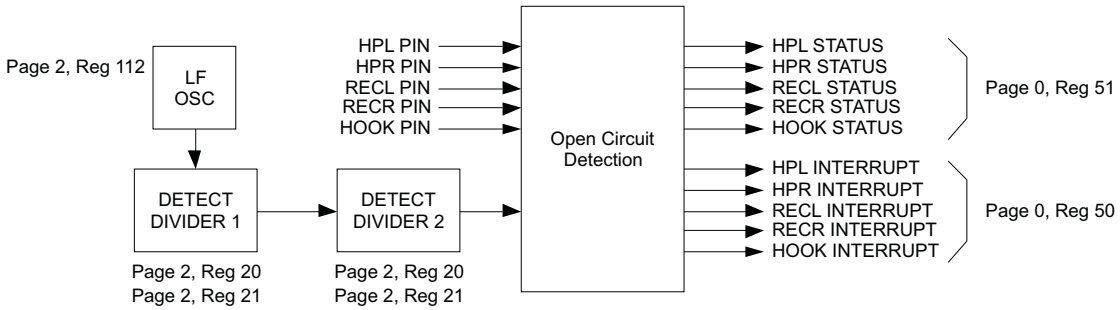


Figure 5-52. Periodic OC Detection Sampling

5.19.3 General-Purpose I/O

The TLV320AIC36 provides flexible I/O multiplexing to support digital microphone input, class-D amplifier output, interrupt output, and general purpose digital I/O options. Page 0 Registers 120 through 125 are used to control the GPIO1, GPIO2, GPIO4/DIGMIC_CLK, GPIO3/DIGMIC_DATA, GPIO6/BITSTREAM_CLK, and GPIO5/BITSTREAM_DATA pin functions.

5.19.4 Interrupts

The TLV320AIC36 can generate host interrupts originating from miniDSP, power threshold, LDO over current, detect, and hook sources. Each source can be individually enabled and associated with two separate interrupt groups (INT1 and INT2) and routed to device pins. Each pin provides active high, active low or open drain output capabilities.

The status of each interrupt source is available in a “sticky bit” and a real-time format. A sticky bit is a status bit that is set by the interrupting source and remains set until cleared using an I^2C register write. Real-time status bits provide a live read-back of the interrupting condition. Some interrupts can be programmed to assert based on rising, falling, or changes of state for additional user customization.

To associate an interrupt source with an interrupt group, the corresponding interrupt enable register bit must be set. Multiple interrupt sources may be used for one interrupt group. If multiple enabled interrupts are asserted in an interrupt group, all sticky bits must be cleared before the device pin is de-asserted. All interrupts listed in Table 5-22can be selectively assigned to the INT1 or INT2 group.

Table 5-22. Interrupt Sources

Interrupt Source	Type
Right DAC Signal Power is above Signal Threshold of DRC	DAC engine
Left DAC Signal Power is above Signal Threshold of DRC	DAC engine
ADC Barrel Shifter Output Overflow Flag	ADC engine
Right ADC Overflow Flag	ADC engine
Left ADC Overflow Flag	ADC engine
DAC Barrel Shifter Output Overflow	DAC engine
Right DAC Overflow	DAC engine
Left DAC Overflow	DAC engine
Right DAC Signal Power is above Signal Threshold of DRC	DAC engine
Left DAC Signal Power is above Signal Threshold of DRC	DAC engine
ADC MAC Engine Auxiliary Interrupt Port Output	ADC engine
ADC MAC Engine Standard Interrupt Port Output	ADC engine
Right ADC Signal Power Lesser than Noise Threshold for Right AGC.	ADC engine
Left ADC Signal Power Greater than Noise Threshold for Left AGC.	ADC engine
DAC MAC Engine Auxiliary Interrupt Port Output	DAC engine
DAC MAC Engine Standard Interrupt Port Output	DAC engine
Over current on VDD_ADC_LDO	Power Control
Over current on VSS_DAC_LDO	Power Control
Over current on VDD_DAC_LDO	Power Control
Power good on VDD_ADC_LDO	Power Control
Power good on VSS_DAC_LDO	Power Control
Power good on VDD_DAC_LDO	Power Control
Combined Rec amp/headphone short circuit	Short Circuit
Left headphone open circuit detect	Headphone detection
Right headphone open circuit detect	Headphone detection
Left receiver open circuit detect	Receiver detection
Right receiver open circuit detect	Receiver detection

Table 5-22. Interrupt Sources (continued)

Hook open circuit detect	Hook detection
Microphone bias detected long pulse	Headset Detection
Microphone bias detected short pulse	Headset Detection

INT1 and INT2 interrupt groups may be routed to the GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, or GPIO6 pins with the active-state formats as described in the Page 0 Control Registers 120 - 125.

Interrupt sources not enabled for either the INT1 or INT2 group will still provide sticky bit and real-time status information accessible using the I^2C interface but they will not assert device pins. This is useful for monitoring interrupt source status without using an actual interrupt pin.

5.20 Detailed Application Example

```
################################################
# Example script for the ADC and DAC data paths
# Assumes Mclk(input)=11.2896 MHz, Wclk(input) =fs=44.1kHz, Bclk(input)=2.8224 MHz
# I2S data, 24bits, BCLK, WCLk are inputs
# mic1 and mic2 are fully differential inputs
# HPR, HPL are single ended headphone outputs
# LOR,LOL are fully differential line outputs
#############################################################

# software reset
w 30 00 00
w 30 01 01
w 30 01 00

# PMU CODE
#############################################################
# charge pump on, cpclk=MCLK (71=01) , cpclk/12 (72=73=0b)
w 30 00 02
w 30 71 01
w 30 72 0b
w 30 73 0b

# turn on ADC ,DAC LDO (74=00), no current limit (76=00),
# short ckt protect, ADC=1.75V, LDO BGAP=on (77=00)
# DAC=+-1.75 (78=33), +-1.65 (78=22), +-1.5 (78=11), +-1.4 (78=00)
w 30 00 02
w 30 74 00
w 30 76 00
w 30 77 00
w 30 78 22

# CLOCK CODE
#############################################################
# clocking settup, see fig. 5-33 clock dist tree
# no pll: 04=00,05=00,0b=81,12=81
# pll: 04=08,05=91,0b=88,12=88
# CODEC_CLKIN=PLL_CLK, PLL_CLKIN=MCLK_PIN (04=08)
w 30 00 00
w 30 04 08

# PLL=R*J.D/P,
# PLL on, P=1,R=1, (05=91)
w 30 05 91

# PLL J.D (06=J, 07,08=D)
w 30 06 08
w 30 07 00
w 30 08 00

# DAC CLOCK CODE
#############################################################
# NDAC power up and div by 8 (0B=88), div by 16 (0B=90)
w 30 0B 88
# MDAC power up and div by 2 (0C=82)
w 30 0C 82
# DAC OSR=128 (0D, 0E=80), OSR=64 (0E=40)
```

```
w 30 0D 00
w 30 0E 80
# IDAC, DAC Mac instructions per FS, only used for custom filters
#w 30 0F 40
# DAC inter ratio for digital filters, only used for custom filters
#w 30 10 08

# ADC CLOCK CODE
############################################################
# NADC power up and div by 8 (12=88)
w 30 12 88
# MADC power up and div by 2 (13=82)
w 30 13 82
# ADC OSR=128 (14=80),
w 30 14 80
# IADC, ADC MAC instructions per FS, only used for custom filters
#w 30 15 5E
# ADC dec ratio for digital filter =4, only used for custom filters
#w 30 16 04

# CODEC INTERFACE, DIGITAL ADC,DAC CONTROLS, INCLUDES ANALOG DAC,ADC POWERUP
############################################################
# I2S, 24bit wordlength (19=2x) , 16bit (19=0x), BCLK, WCLK are outputs (19=xC), inputs (19=x0)
w 30 19 20

# DAC filter engine 1
w 30 3C 01
# ADC filter engine 1
w 30 3D 01

# Left, Right ADC not muted digital gain=0 dB (52=00), gain=-0.1 dB (52=11)
w 30 52 00
# ADCL, ADCR digital gain (7b signed 0.5 dB steps)
w 30 53 00
w 30 54 00

# L AGC, R AGC disabled, target=-5.5 dB
w 30 56 00
w 30 5E 00

# PRI_BCLK_OUT=internally generated BCLK, SEC_BCLK_OUT=Primary BCLK,
# PRI_WCLK_OUT= ADC_FS clock, SEC_WCLK=Primary WCLK, PRI_DOUT=DOUT from CODEC
w 30 21 10
# ADC filter output to I2S, I2S to DAC filter input, BCLK not inverted, BCLK WCLK active even
when CODEC is PD
w 30 1B 06

# LADC,RADC powerup, DIG_MIC_INP, LDIG_MIC,RDIG_MIC disabled, soft-step disabled
w 30 00 00
w 30 51 C2
# LDAC,RDAC powerup,soft-step disble, left data to LDAC, right data to RDAC (d6), L->R, R->L
(ea), L->L, L->R (da)
w 30 3F d6
# Dac auto-mute disable, left,right dac not muted, left,right dac volume control independent
w 30 40 00

# LDAC, RDAC digital gain 8 bit signed (0.5 dB steps) -6 dB (41=f4,42=f4)
w 30 41 00
w 30 42 00

# ANALOG ADC CODE
###################################
# Briefly connect internal CM to LEFT and RIGHT MIC PGA
# for CM startup in differential mode
w 30 00 01
w 30 34 00
w 30 36 80
w 30 37 00
w 30 39 80

# connect mic1p,1m to pga leftp (34=20) leftm (36=20) 20k
# connect mic2p,2m to pga rightp (37=20) rightm (39=20) 20k
# connect extmic_p,m to pga leftp (34=08) leftm (36=08) 20k
```

```
# connect lineinl to pgalp (34=80), cml to pgalm (36=80)
# connect lineinr to pgarp (37=80), cmr to pgarm (39=80)
w 30 00 01
w 30 34 20
w 30 36 20
w 30 37 20
w 30 39 20
# all inputs float if not used (3A=00), all inputs are connected to CM if not used (3A=FF)
w 30 3A 00
# LADC,RADC analog PGA gain=0 dB (0.5 dB steps),
w 30 3B 00
w 30 3C 00
# ADC CM=0.9V (0A=00), 0.75V (0A=40)
w 30 0A 00
# select LINE2L, LINE2R, 28=14 SE in bypass amp
w 30 00 02
w 30 28 14

# Modulator start-up sequence
w 30 00 fd
w 30 0d 0d
w 30 04 20
w 30 0d 00

# ANALOG DAC CODE
###################################
# dacl,dacr power up, short ckt protect output drivers enabled
# c0=both dacs, 80=ldac, 40=rdac
w 30 00 02
w 30 25 c0
w 30 26 02

# BCLK powerup, divide 4
w 30 00 00
w 30 1C 84

# pop reduction for DAC output drivers
w 30 00 02
w 30 2A 34

# enable outputs and set gains
# HPR 2D-33
# HPL 34-3a
# RECL 3b-41
# RECR 42-48
# LOL 50-56
# LOR 57-5D

# disable ground sense for hpr, hpl (24=00)
w 30 00 02
w 30 24 00

#enable HPR gain=0,
#connect to LINEL (2d) PGAL(2e) DACL (2f) LINER (30) PGAR (31) DACR (32), 80=0 dB f5=-78 dB,
f6=mute
w 30 00 02
w 30 2f 80
w 30 33 09

#enable HPL gain=0
# connect to LINEL (34) PGAL (35) DACL (36) LINER (37) PGAR (38) DACR (39), 0 dB
w 30 39 80
w 30 3a 09

# enable recl gain=0
# connect to LINE2L (3B) PGAL (3C) DACL (3D) LINE2R (3E) PGAR (3F) DACR (40)
# a.0 0d=03 a.1 (comment out)
w 30 00 02
w 30 3d 80
w 30 41 00
# enable recr gain=0
# connect to LINE2L (42) PGAL (43) DACL (44) LINE2R (45) PGAR (46) DACR (47)
w 30 47 80
```

```
w 30 48 00

#enable LOL (09) gain=0
#connect to LINE2L (50) PGAL (51) DACL (52) LINE2R (53) PGAR (54) DACR (55), 80=0 dB f5=-78 dB
w 30 00 02
w 30 52 80
w 30 56 09
#enable LOR gain=0
#connect to LINE2L (57) PGAL (58) DACL (59) LINE2R (5a) PGAR (5b) DACR (5c), att=0 dB
w 30 5c 80
w 30 5D 09

# reduce hp,dac,lo,rec currents to lowest power state
w 30 00 02
w 30 7a 55

# set modulator taps for best performance (0,2,4,6,8,a or 0,1,2,3,4,5 or 1,1,1,1,1 or
0,3,5,7,9,c)
w 30 00 00
w 30 72 30
w 30 73 75
w 30 74 c9

# dac current control 1.5x current (6B=40), 0.5x current (6B=80)
w 30 00 02
w 30 6B 00
```

5.21 Detailed Application Example – Low Power Modes

```
############################################################
# Example script for the ADC and DAC data paths - low and ultra low power modes
# dac to hp only for lowest power
# Assumes Mclk(input)=11.2896 MHz, Wclk(input) =fs=44.1kHz, Bclk(input)=2.8224 MHz
# I2S data, 24bits, BCLK, WCLk are inputs
# HPR, HPL are single ended headphone outputs
#
# ultra low power mode (search ulp:)
# low power (search lp:)
# adc on (search adc on:)
############################################################

# software reset
w 30 00 00
w 30 01 01
w 30 01 00

# PMU CODE
############################################################
# charge pump on with slow clocks(71=00 disabled, 71=01 clk=BCLK, 72=73=0b Bclk/6)
w 30 00 02
w 30 72 7f
w 30 73 7f
w 30 71 01

# turn on ADC ,DAC LDO (74=00), no current limit (76=00),
# short ckt protect, ADC=1.75V, LDO BGAP=on (77=00)
# DAC=+-1.75 (78=33), +-1.65 (78=22), +-1.5 (78=11), +-1.4 (78=00)
# ulp: 74=07 78=00, lp: 74=00 78=11, normal 74=00,78=22
w 30 00 02
w 30 74 00
w 30 76 00
w 30 77 00
w 30 78 11
# CLOCK CODE
############################################################
# clocking settup, see fig. 5-33 clock dist tree
# no pll: 04=00,05=00,0b=81,12=81
# pll: 04=08,05=91,0b=88,12=88
# CODEC_CLKIN=PLL_CLK, PLL_CLKIN=MCLK_PIN (04=08)
w 30 00 00
w 30 04 00
# PLL power up, P = 1 (divide), R=1 (mult)
# PLL off 05 =00
```

```
w 30 05 00

# PLL multiply 8.0000
w 30 06 08
w 30 07 00
w 30 08 00

# DAC CLOCK CODE
############################################################
# NDAC power up and div by 1 (88) (max divide 80 =128, a0=32)
w 30 0B 81
# MDAC power up and div by 2 (82) (max divide 80=128)
w 30 0C 82
# DAC OSR=128 (0E=80)
w 30 0D 00
w 30 0E 80
# DAC Mac instructions per FS=256 (40)
w 30 0F 40
# DAC inter ratio=8
w 30 10 08

# ADC CLOCK CODE
############################################################
# NADC power up and div by 1
w 30 12 81
# MADC power up and div by 2 (82)
w 30 13 82
# ADC OSR=128
w 30 14 80
# ADC MAC instructions per FS=94
w 30 15 5E
# ADC dec ratio=4
w 30 16 04

# CODEC INTERFACE, DIGITAL ADC,DAC CONTROLS, INCLUDES ANALOG DAC,ADC POWERUP
############################################################
# I2S, 24bit wordlength (2) , BCLK, WCLK are outputs (C), inputs (0)
w 30 19 20

# DAC filter engine 1, 8x inter, 3 biquads (3c=01),
# ulp: 3c=11, lp: 3c=11
w 30 3C 11
# ADC filter engine 1, 4x dec, 1st order IIR
w 30 3D 01

# Left, Right ADC not muted digital gain=0dB (-0.1dB steps)
# adc on: 52=00, adc off: 52=88
w 30 52 88
# ADCL, ADCR digital gain (7b signed 0.5dB steps)
w 30 53 00
w 30 54 00

# L AGC, R AGC disabled, target=-5.5dB
w 30 56 00
w 30 5E 00

# PRI_BCLK_OUT=internally generated BCLK, SEC_BCLK_OUT=Primary BCLK,
# PRI_WCLK_OUT= ADC_FS clock, SEC_WCLK=Primary WCLK, PRI_DOUT=DOUT from CODEC
w 30 21 10
# ADC filter output to I2S, I2S to DAC filter input, BCLK not inverted, BCLK WCLK active even
when CODEC is PD
w 30 1B 06

# reduce hp,dac,lo,rec currents on pg2p0
# ulp, lp: ( 7a=ff, reduce max, 7a=55, reduce by 1/2)
w 30 00 02
w 30 7a ff
# dac current control
w 30 6B 80

# charge pump on (71=00 disabled, 71=01 clk=BCLK, 72=73=0b Bclk/6)
w 30 00 02
w 30 72 0b
```

```
w 30 73 0b

# LADC,RADC powerup, DIG_MIC_INP, LDIG_MIC,RDIG_MIC disabled, soft-step disabled
# adc on: 51=c2, adc off: 51=02
w 30 00 00
w 30 51 02
# LDAC,RDAC powerup,left data to LDAC, right data to RDAC, soft-step disble (d6), L->R, R->L
(ea), L->L, L->R (da)
w 30 3F d6
# Dac auto-mute disable, left,right dac not muted, left,right dac volume control independent
w 30 40 00

# Modulator start-up sequence
w 30 00 fd
w 30 0d 0d
w 30 04 20
w 30 0d 00

# LDAC, RDAC digital gain 8 bit signed (0.5dB steps) f4=-6dB
# ulp 41=fc, f2=fc, lp: 41=00,42=00
w 30 00 00
w 30 41 fc
w 30 42 fc

# ANALOG ADC CODE
###################################
# Briefly connect internal CM to LEFT and RIGHT MIC PGA
# for CM startup in differential mode
w 30 00 01
w 30 34 00
w 30 36 80
w 30 37 00
w 30 39 80

# connect mic1p,1m to pga leftp (34=20) leftm (36=20) 20k
# connect mic2p,2m to pga rightp (37=20) rightm (39=20) 20k
# connect extmic_p,m to pga leftp (34=08) leftm (36=08) 20k
# connect lineinl to pgalp 34=80, cml to pgalm 36=80
# connect lineinr to pgarp 37=80, cmr to pgarm 39=80
w 30 00 01
w 30 34 20
w 30 36 20
w 30 37 20
w 30 39 20
# lineinr, lineinl (c0) to internal cm if adc is on (00) floating
w 30 3A 00
# LADC,RADC PGA gain=0dB (0.5dB steps), CM=0.9V
# ulp: 0A=40, lp: 0A=00
w 30 3B 00
w 30 3C 00
w 30 0A 40
w 30 00 02
# select LINE2LP, LINE2RP, 28=14 SE in bypass amp
w 30 00 02
w 30 28 14

# ANALOG DAC CODE
###################################
# dacl,dacr power up, short ckt protect output drivers enabled
# c0=both dacs, 80=ldac, 40=rdac
w 30 00 02
w 30 25 c0
w 30 26 04
# BCLK powerup, divide 4
w 30 00 00
w 30 1C 84

# pop reduction
w 30 00 02
w 30 2A 34

# modulator taps (2,4,6,8,a or 1,2,3,4,5 or 0,3,5,7,9,c)
w 30 00 00
```

```
w 30 72 30
w 30 73 75
w 30 74 c9

# dac to line out -3dB gain
w 30 00 02
#w 30 56 09
#w 30 52 86
#w 30 50 f6
#w 30 5d 09
#w 30 5c 86
#w 30 5a f6

#enable HPR gain=-3dB,
#connect to LINEL (2d) PGAL(2e) DACL (2f) LINER (30) PGAR (31) DACR (32), 80=0 dB f5=-78 dB,
f6=mute
# ulp 32=86, 36=86, lp: ,32=84, 36=84
w 30 00 02
w 30 24 00
w 30 32 86
w 30 33 09
#enable HPL gain=-3dB
# connect to LINEL (34) PGAL (35) DACL (36) LINER (37) PGAR (38) DACR (39), -3 dB
w 30 36 86
w 30 3a 09

#dac to rec amps
w 30 00 02
#w 30 3d 86
#w 30 41 09
#w 30 47 86
#w 30 48 09
```

6 REGISTER MAP

TLV320AIC36 contains 61 pages of 8-bit registers, each page can contain up to 128 registers. The register pages are divided up based on functional blocks for this device. Page 0 is the default “home” page after hardware reset.

6.1 Register Map Summary

Table 6-1. Summary of Register Map

PAGE NO.	DESCRIPTION
0	Configuration for Serial Interface, Digital IO, Clocking, ADC and DAC miniDSP configuration etc. See Table 6-2.
1	Configuration for Analog PGA’s, ADC, and Analog Inputs. See Table 6-2.
2	Configuration for Analog Outputs, DAC, Output Drivers. See Table 6-2.
3	Reserved.
4-5	ADC Coefficients (0:127). See Table 6-2 and Table 6-3.
6-7	Reserved.
8-11	DAC Coefficient Buffer A (0:255). See Table 6-4 and Table 6-5.
12-15	DAC Coefficient Buffer B (0:255). See Table 6-5 and Table 6-6.
16-31	Reserved.
32-47	ADC miniDSP Instructions (0:511). See Table 6-7.
48-63	Reserved.
64-95	DAC miniDSP Instructions (0:1024). See Table 6-8.
96-255	Reserved.

6.2 Register Descriptions

6.2.1 Page 0 / Register 0: Page Select Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

6.2.2 Page 0 / Register 1: Software Reset Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D1	R	0000 000	Reserved, Write only default values
D0	W	0	Asserts software reset - not self clearing. Must be re-written to 0 for normal operation.

6.2.3 Page 0 / Register 2: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0XXX 0XXX	Reserved, Write only default values

6.2.4 Page 0 / Register 3: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved, Write only default values to this register

6.2.5 Page 0 / Register 4: Clock Setting Register 1, Multiplexers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	Select PLL Input Clock 0000: MCLK pin is input to PLL 0001: BCLK pin is input to PLL 0010: GPIO1 pin is input to PLL 0011: GPIO2 pin is input to PLL 0100: DIGMIC_CLK pin is input to PLL 0101: DIGMIC_DATA pin is input to PLL 0110: DSD_CLK pin is input to PLL 0111: DSD_DATA pin is input to PLL 1000: DIN pin is input to PLL others: Reserved
D3–D0	R/W	0000	Select CODEC_CLKIN 0000: MCLK pin is input to CODEC_CLKIN 0001: BCLK pin is input to CODEC_CLKIN 0010: GPIO1 pin is input to CODEC_CLKIN 0011: GPIO2 pin is input to CODEC_CLKIN 0100: DIGMIC_CLK pin is input to CODEC_CLKIN 0101: DIGMIC_DATA pin is input to CODEC_CLKIN 0110: DSD_CLK pin is input to CODEC_CLKIN 0111: DSD_DATA pin is input to CODEC_CLKIN 1000: DIN pin is input to CODEC_CLKIN others: Reserved

6.2.6 Page 0 / Register 5: Clock Setting Register 2, PLL P&R Values

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PLL Power Up 0: PLL is powered down 1: PLL is powered up
D6–D4	R/W	001	PLL divider P Value 000: P=8 001: P=1 010: P=2 … 110: P=6 111: P=7
D3–D0	R/W	0001	PLL divider R Value 000: Reserved, do not use 001: R=1 010: R=2 011: R=3 100: R=4 101…111: Reserved, do not use

6.2.7 Page 0 / Register 6: Clock Setting Register 3, PLL J Values

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved. Write only default values any value other than default
D5–D0	R/W	00 0100	PLL divider J value 00 0000…00 0011: Do not use 00 0100: J=4 00 0101: J=5 … 11 1110: J=62 11 1111: J=63

6.2.8 Page 0 / Register 7: Clock Setting Register 4, PLL D Values (MSB)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved. Write only default values any value other than default
D5–D0	R/W	00 0000	PLL divider D value (MSB) PLL divider D value(MSB) & PLL divider D value(LSB) 00 0000 0000 0000: D=0000 00 0000 0000 0001: D=0001 … 10 0111 0000 1110: D=9998 10 0111 0000 1111: D=9999 10 0111 0001 0000…11 1111 1111 1111: Do not use Note: This register will be updated only when the Page-0, Reg-8 is written immediately after Page-0, Reg-7

6.2.9 Page 0 / Register 8: Clock Setting Register 5, PLL D Values (LSB)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	PLL divider D value (LSB) PLL divider D value(MSB) & PLL divider D value(LSB) 00 0000 0000 0000: D=0000 00 0000 0000 0001: D=0001 … 10 0111 0000 1110: D=9998 10 0111 0000 1111: D=9999 10 0111 0001 0000…11 1111 1111 1111: Do not use Note: Page-0, Reg-8 should be written immediately after Page-0, Reg-7

6.2.10 Page 0 / Register 9-10: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved, Write only default values.

6.2.11 Page 0 / Register 11: Clock Setting Register 6, NDAC Values

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	NDAC Divider Power Control 0: NDAC divider powered down 1: NDAC divider powered up
D6–D0	R/W	000 0001	NDAC Value 000 0000: NDAC=128 000 0001: NDAC=1 000 0010: NDAC=2 … 111 1110: NDAC=126 111 1111: NDAC=127 Note: Please check the clock frequency requirements in the Overview section

6.2.12 Page 0 / Register 12: Clock Setting Register 7, MDAC Values

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	MDAC Divider Power Control 0: MDAC divider powered down 1: MDAC divider powered up
D6–D0	R/W	000 0001	MDAC Value 000 0000: MDAC=128 000 0001: MDAC=1 000 0010: MDAC=2 … 111 1110: MDAC=126 111 1111: MDAC=127 Note: Please check the clock frequency requirements in the Overview section

6.2.13 Page 0 / Register 13: DAC OSR Setting Register 1, MSB Value

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D2	R	0000 00	Reserved. Write only default values
D1–D0	R/W	00	DAC OSR (DOSR) Setting DAC OSR(MSB) & DAC OSR(LSB) 00 0000 0000: DOSR=1024 00 0000 0001: DOSR=1 00 0000 0010: DOSR=2 … 11 1111 1110: DOSR=1022 11 1111 1111: DOSR=1023 Note: This register is updated when Page-0, Reg-14 is written to immediately after Page-0, Reg-13

6.2.14 Page 0 / Register 14: DAC OSR Setting Register 2, LSB Value

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0000	DAC OSR (DOSR) Setting DAC OSR(MSB) & DAC OSR(LSB) 00 0000 0000: DOSR=1024 00 0000 0001: DOSR=1 00 0000 0010: DOSR=2 … 11 1111 1110: DOSR=1022 11 1111 1111: DOSR=1023 Note: This register should be written immediately after Page-0, Reg-13

6.2.15 Page 0 / Register 15: DAC miniDSP Instruction Control Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0000	Use when DAC miniDSP is in use for signal processing (page 0,Reg 60) DAC miniDSP IDAC(7:0) 1000 0000: DAC miniDSP IDAC = 1024 0000 0001: DAC miniDSP IDAC = 4 0000 0010: DAC miniDSP IDAC = 8 … … 1111 1110: DAC miniDSP IDAC = 1012 1111 1111: DAC miniDSP IDAC = 1020 Note: IDAC should be a integral multiple of INTERP (Page-0, Reg-16)

6.2.16 Page 0 / Register 16: DAC miniDSP Interpolation Factor Setting Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R	0000	Reserved. Write only default values
D3–D0	R/W	1000	DAC miniDSP interpolation factor setting. Used when DAC miniDSP is in use for signal processing (page 0,Reg 60) 0000 : Interpolation factor in DAC miniDSP(INTERP) = 16 0001: Interpolation factor in DAC miniDSP(INTERP)= 1 0010: Interpolation factor in DAC miniDSP(INTERP) = 2 … 1110: Interpolation factor in DAC miniDSP(INTERP) = 14 1111: Interpolation factor in DAC miniDSP(INTERP) = 15

6.2.17 Page 0 / Register 17: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved, Write only default values to this register

6.2.18 Page 0 / Register 18: Clock Setting Register 8, NADC Values

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	NADC Clock Divider Power Control 0: NADC divider powered down, ADC_CLK is same as DAC_CLK 1: NADC divider powered up

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D0	R/W	000 0001	NADC Value 000 0000: NADC=128 000 0001: NADC=1 … 111 1110: NADC=126 111 1111: NADC=127

6.2.19 Page 0 / Register 19: Clock Setting Register 9, MADC Values

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	MADC Clock Divider Power Control 0: MADC divider powered down, ADC_MOD_CLK is same as DAC_MOD_CLK 1: MADC divider powered up
D6–D0	R/W	000 0001	MADC Value 000 0000: MADC=128 000 0001: MADC=1 … 111 1110: MADC=126 111 1111: MADC=127

6.2.20 Page 0 / Register 20: ADC Oversampling (AOSR) Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0000	ADC Oversampling Value 0000 0000: ADC AOSR = 256 0000 0001: ADC AOSR = 1 0000 0010: ADC AOSR = 2 ... 0010 0000: ADC AOSR=32 (Use with PRB_R13 to PRB_R18, ADC Filter Type C) ... 0100 0000: AOSR=64 (Use with PRB_R1 to PRB_R12, ADC Filter Type A or B) ... 1000 0000: AOSR=128 (Use with PRB_R1 to PRB_R6, ADC Filter Type A) ... 1111 1110: ADC AOSR = 254 1111 1111: ADC AOSR = 255 Note: If the ADC miniDSP will be used for signal processing ADC (Pg 0, Reg 61) AOSR should be an integral multiple of ADC DECIM factor.

6.2.21 Page 0 / Register 21: ADC miniDSP Instruction Control Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0000	ADC miniDSP IADC (7:0) setting. Use when ADC miniDSP is in use for signal processing (page 0,Reg 61) 0000 0000: Don't use (Reserved) 0000 0001: ADC miniDSP IADC = 2 0000 0010: ADC miniDSP IADC = 4 … … 1111 1110: ADC miniDSP IADC = 508 1111 1111: ADC miniDSP IADC = 510 Note: IADC should be a integral multiple of DECIM (Page-0, Reg-22)

6.2.22 Page 0 / Register 22: ADC miniDSP Decimation Factor Setting Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R	0000	Reserved. Write only default values
D3–D0	R/W	0100	ADC miniDSP Decimation factor setting. Use when ADC miniDSP is in use for signal processing (page 0,Reg 61) 0000: Decimation factor in ADC miniDSP = 16 0001: Decimation factor in ADC miniDSP = 1 0010: Decimation factor in ADC miniDSP = 2 … 1110: Decimation factor in ADC miniDSP = 14 1111: Decimation factor in ADC miniDSP = 15

6.2.23 Page 0 / Register 23: Clock Setting Register 9, Multiplexers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R	0000 0	Reserved. Write only default values
D2–D0	R/W	000	CDIV_CLKIN Clock Selection 000: CDIV_CLKIN= MCLK 001: CDIV_CLKIN= BCLK 010: CDIV_CLKIN=DIN 011: CDIV_CLKIN=PLL_CLK 100: CDIV_CLKIN=DAC_CLK 101: CDIV_CLKIN=DAC_MOD_CLK 110: CDIV_CLKIN=ADC_CLK 111: CDIV_CLKIN=ADC_MOD_CLK

6.2.24 Page 0 / Register 24: Clock Setting Register 10, CLKOUT M Divider Value

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	CLKOUT M divider power control 0: CLKOUT M divider powered down 1: CLKOUT M divider powered up
D6–D0	R/W	000 0001	CLKOUT M divider value 000 0000: CLKOUT M divider = 128 000 0001: CLKOUT M divider = 1 000 0010: CLKOUT M divider = 2 … 111 1110: CLKOUT M divider = 126 111 1111: CLKOUT M divider = 127

6.2.25 Page 0 / Register 25: Audio Interface Setting Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Audio Interface Selection 00: Audio Interface = I^2S 01: Audio Interface = DSP 10: Audio Interface = RJF 11: Audio Interface = LJF
D5–D4	R/W	00	Audio Data Word length 00: Data Word length = 16 bits 01: Data Word length = 20 bits 10: Data Word length = 24 bits 11: Data Word length = 32 bits

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3	R/W	0	BCLK Direction Control 0: BCLK is input to the device 1: BCLK is output from the device
D2	R/W	0	WCLK Direction Control 0: WCLK is input to the device 1: WCLK is output from the device
D1	R	0	Reserved. Write only default value
D0	R/W	0	DOUT High Impendance Output Control 0: DOUT will not be high impedance while Audio Interface is active 1: DOUT will be high impedance after data has been transferred

6.2.26 Page 0 / Register 26: Audio Interface Setting Register 2, Data offset setting

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Data Offset Value 0000 0000: Data Offset = 0 BCLK's 0000 0001: Data Offset = 1 BCLK's … 1111 1110: Data Offset = 254 BCLK's 1111 1111: Data Offset = 255 BCLK's

6.2.27 Page 0 / Register 27: Audio Interface Setting Register 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved. Write only default values
D5	R/W	0	Loopback control 0: No Loopback 1: Audio Data in is routed to Audio Data out
D4	R/W	0	Loopback control 0: No Loopback 1: Stereo ADC output is routed to Stereo DAC input
D3	R/W	0	Audio Bit Clock Polarity Control 0: Default Bit Clock polarity 1: Bit Clock is inverted with respect to default polarity
D2	R/W	0	Primary BCLK and Primary WCLK Power control 0: Primary BCLK and Primary WCLK buffers are powered up when they are used in clock generation even when the codec is powered down 1: Priamry BCLK and Primary WCLK buffers are powered down when the codec is powered down
D1–D0	R/W	00	BDIV_CLKIN Multiplexer Control 00: BDIV_CLKIN = DAC_CLK 01: BDIV_CLKIN = DAC_MOD_CLK 10: BDIV_CLKIN = ADC_CLK 11: BDIV_CLKIN = ADC_MOD_CLK

6.2.28 Page 0 / Register 28: Clock Setting Register 11, BCLK N Divider

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	BCLK N Divider Power Control 0: BCLK N divider powered down 1: BCLK N divider powered up

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D0	R/W	000 0001	BCLK N Divider value 0000 0000: BCLK N divider = 128 0000 0001: BCLK N divider = 1 … 1111 1110: BCLK N divider = 126 1111 1111: BCLK N divider = 127

6.2.29 Page 0 / Register 29: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved, Write only default values to this register

6.2.30 Page 0 / Register 30: Audio Interface Setting Register 4

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved. Write only default values
D5–D3	R/W	000	Secondary Bit Clock Multiplexer 000: Secondary Bit Clock = GPIO1 pin 001: Secondary Bit Clock = GPIO2 pin 010: Secondary Bit Clock = DIGMIC_CLK pin 011: Secondary Bit Clock = DIGMIC_DATA pin 100: Secondary Bit Clock = DSD_CLK pin 101: Secondary Bit Clock = DSD_DATA pin 110: Secondary Bit Clock = SDOUT pin 111: Reserved
D2–D0	R/W	000	Secondary Word Clock Multiplexer 000: Secondary Word Clock = GPIO1 pin 001: Secondary Word Clock = GPIO2 pin 010: Secondary Word Clock = DIGMIC_CLK pin 011: Secondary Word Clock = DIGMIC_DATA pin 100: Secondary Word Clock = DSD_CLK pin 101: Secondary Word Clock = DSD_DATA pin 110: Secondary Word Clock = SDOUT pin 111: Reserved

6.2.31 Page 0 / Register 31: Audio Interface Setting Register 5

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved. Write only default values
D5–D3	R/W	000	Secondary ADC_CLK Multiplexer 000: Secondary ADC_CLK = GPIO1 pin 001: Secondary ADC_CLK = GPIO2 pin 010: Secondary ADC_CLK = DIGMIC_CLK pin 011: Secondary ADC_CLK = DIGMIC_DATA pin 100: Secondary ADC_CLK = DSD_CLK pin 101: Secondary ADC_CLK = DSD_DATA pin 110: Secondary ADC_CLK = SDOUT pin 111: Reserved

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D2–D0	R/W	000	Secondary DIN Multiplexer 000: Secondary DIN = GPIO1 pin 001: Secondary DIN = GPIO2 pin 010: Secondary DIN = DIGMIC_CLK pin 011: Secondary DIN = DIGMIC_DATA pin 100: Secondary DIN = DSD_CLK pin 101: Secondary DIN = DSD_DATA pin 110: Secondary DIN = SDOUT pin 111: Reserved

6.2.32 Page 0 / Register 32: Audio Interface Setting Register 6

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R	000	Reserved. Write only default values
D4	R/W	0	Primary / Secondary Word Clock Control for DAC engine 0: DAC engine uses WCLK for Audio Interface 1: DAC engine uses internally generated DAC_CLK for Audio Interface
D3	R/W	0	Primary / Secondary Bit Clock Control Select 0: Primary Bit Clock(BCLK) is used for Audio Interface and Clocking 1: Secondary Bit Clock is used for Audio Interface and Clocking
D2	R/W	0	Primary / Secondary Word Clock Control 0: Primary Word Clock(WCLK) is used for Audio Interface 1: Secondary Word Clock is used for Audio Interface
D1	R/W	0	ADC Word Clock Control 0: ADC Word Clock is same as DAC Word Clock 1: ADC Word Clock is Secondary ADC Word Clock
D0	R/W	0	Audio Data In Control 0: DIN is used for Audio Data In 1: Secondary Data In is used for Audio Data In

6.2.33 Page 0 / Register 33: Audio Interface Setting Register 7

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	BCLK Output Control 0: BCLK Output = Generated Primary Bit Clock 1: BCLK Output = Secondary Bit Clock Input
D6	R/W	0	Secondary Bit Clock Output Control 0: Secondary Bit Clock = BCLK input 1: Secondary Bit Clock = Generated Primary Bit Clock
D5–D4	R/W	00	WCLK Output Control 00: WCLK Output = Generated DAC_FS 01: WCLK Output = Generated ADC_FS 10: WCLK Output = Secondary Word Clock Input 11: Do not use
D3–D2	R/W	00	Secondary Word Clock Output Control 00: Secondary Word Clock output = WCLK input 01: Secondary Word Clock output = Generated DAC_FS 10: Secondary Word Clock output = Generated ADC_FS 11: Do not use
D1	R/W	0	Primary Data Out output control 0: DOUT output = Data Output from Serial Interface 1: DOUT output = Secondary Data Input (Loopback)
D0	R/W	0	Secondary Data Out output control 0: Secondary Data Output = DIN input (Loopback) 1: Secondary Data Output = Data output from Serial Interface

6.2.34 Page 0 / Register 34 - 35: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved, Write only default values to this register

6.2.35 Page 0 / Register 36: ADC Flag Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left ADC PGA Status Flag 0: Gain Applied in Left ADC PGA is not equal to Programmed Gain in Control Register 1: Gain Applied in Left ADC PGA is equal to Programmed Gain in Control Register
D6	R	0	Left ADC Power Status Flag 0: Left ADC Powered Down 1: Left ADC Powered Up
D5	R	0	Left AGC Gain Status. This sticky flag will self clear on reading 0: Gain in Left AGC is not saturated 1: Gain in Left ADC is equal to maximum allowed gain in Left AGC
D4	R	0	Reserved. Write only default value
D3	R	0	Right ADC PGA Status Flag 0: Gain Applied in Right ADC PGA is not equal to Programmed Gain in Control Register 1: Gain Applied in Right ADC PGA is equal to Programmed Gain in Control Register
D2	R	0	Right ADC Power Status Flag 0: Right ADC Powered Down 1: Right ADC Powered Up
D1	R	0	Right AGC Gain Status. This sticky flag will self clear on reading 0: Gain in Right AGC is not saturated 1: Gain in Right ADC is equal to maximum allowed gain in Right AGC
D0	R	0	Reserved. Write only default value

6.2.36 Page 0 / Register 37: DAC Flag Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left DAC Power Status Flag 0: Left DAC Powered Down 1: Left DAC Powered Up
D6–D4	R	000	Reserved. Write only default values
D3	R	0	Right DAC Power Status Flag 0: Right DAC Powered Down 1: Right DAC Powered Up
D2	R	0	Left DAC PGA Status Flag 0: Gain applied in Left DAC PGA is not equal to Gain programmed in Control Register 1: Gain applied in Left DAC PGA is equal to Gain programmed in Control Register
D1	R	0	Right DAC PGA Status Flag 0: Gain applied in Right DAC PGA is not equal to Gain programmed in Control Register 1: Gain applied in Right DAC PGA is equal to Gain programmed in Control Register
D0	R	0	Reserved. Write only default values

6.2.37 Page 0 / Register 38: Sticky Flag Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Right Channel DRC, Signal Threshold Flag 0: Signal Power is below Signal Threshold 1: Signal Power exceeded Signal Threshold (will be cleared when the register is read)
D6	R/W	0	Left Channel DRC, Signal Threshold Flag 0: Signal Power is below Signal Threshold 1: Signal Power exceeded Signal Threshold (will be cleared when the register is read)
D5	R/W	0	ADC miniDSP Barrel Shifter Output Overflow Sticky Flag. Flag is reset on register reading
D4	R/W	0	Right ADC Overflow Status. This sticky flag will self clear on read 0: No overflow in Right ADC 1: Overflow has happened in Right ADC since last read of this register
D3	R/W	0	Left ADC Overflow Status. This sticky flag will self clear on read 0: No overflow in Left ADC 1: Overflow has happened in Left ADC since last read of this register
D2	R/W	0	DAC miniDSP Barrel Shifter Output Overflow Sticky Flag. Flag is reset on register reading
D1	R/W	0	Right DAC Overflow Status. This sticky flag will self clear on read 0: No overflow in Right DAC 1: Overflow has happened in Right DAC since last read of this register
D0	R/W	0	Left DAC Overflow Status. This sticky flag will self clear on read 0: No overflow in Left DAC 1: Overflow has happened in Left DAC since last read of this register

6.2.38 Page 0 / Register 39: Interrupt Flag Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Right Channel DRC, Signal Threshold Flag 0: Signal Power is below Signal Threshold 1: Signal Power exceeded Signal Threshold
D6	R	0	Left Channel DRC, Signal Threshold Flag 0: Signal Power is below Signal Threshold 1: Signal Power exceeded Signal Threshold
D5	R	0	ADC Barrel Shifter Output Overflow Flag 0: no overflow 1: overflow
D4	R	0	Right ADC Overflow Flag 0: no overflow 1: overflow
D3	R	0	Left ADC Overflow Flag 0: no overflow 1: overflow
D2	R	0	DAC Barrel Shifter Output Overflow Flag 0: no overflow 1: overflow
D1	R	0	Right DAC Overflow Flag 0: no overflow 1: overflow
D0	R	0	Left DAC Overflow Flag 0: no overflow 1: overflow

6.2.39 Page 0 / Register 40: Interrupt Enable Control Register 1 (INT1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Right DAC Signal Power is above Signal Threshold of DRC interrupt to INT1 0: disabled 1: enabled
D6	R/W	0	Left DAC Signal Power is above Signal Threshold of DRC interrupt to INT1 0: disabled 1: enabled
D5	R/W	0	ADC Barrel Shifter Output Overflow interrupt to INT1 0: disabled 1: enabled
D4	R/W	0	Right ADC Overflow interrupt to INT1 0: disabled 1: enabled
D3	R/W	0	Left ADC Overflow interrupt to INT1 0: disabled 1: enabled
D2	R/W	0	DAC Barrel Shifter Output Overflow interrupt to INT1 0: disabled 1: enabled
D1	R/W	0	Right DAC Overflow interrupt to INT1 0: disabled 1: enabled
D0	R/W	0	Left DAC Overflow interrupt to INT1 0: disabled 1: enabled

6.2.40 Page 0 / Register 41: Interrupt Enable Control Register 2 (INT2)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Right DAC Signal Power is above Signal Threshold of DRC interrupt to INT1 0: disabled 1: enabled
D6	R/W	0	Left DAC Signal Power is above Signal Threshold of DRC interrupt to INT2 0: disabled 1: enabled
D5	R/W	0	ADC Barrel Shifter Output Overflow interrupt to INT2 0: disabled 1: enabled
D4	R/W	0	Right ADC Overflow interrupt to INT2 0: disabled 1: enabled
D3	R/W	0	Left ADC Overflow interrupt to INT2 0: disabled 1: enabled
D2	R/W	0	DAC Barrel Shifter Output Overflow interrupt to INT2 0: disabled 1: enabled
D1	R/W	0	Right DAC Overflow interrupt to INT2 0: disabled 1: enabled
D0	R/W	0	Left DAC Overflow interrupt to INT2 0: disabled 1: enabled

6.2.41 Page 0 / Register 42: Sticky Flag Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Right ADC DC Measurement Data Available Flag 0: Data not available 1: Data available (will be cleared when the register is read)
D6	R	0	Left ADC DC Measurement Data Available Flag 0: Data not available 1: Data available (will be cleared when the register is read)
D5	R	0	ADC miniDSP Auxilliary Interrupt Port Output (will be cleaed when register is read)
D4	R	0	ADC miniDSP Standard Interrupt Port Output (will be cleaed when register is read)
D3	R	0	Right AGC Noise Threshold Flag 0: Signal Power is greater than Noise Threshold 1: Signal Power was lower than Noise Threshold (will be cleared when the register is read)
D2	R	0	Left AGC Noise Threshold Flag 0: Signal Power is greater than Noise Threshold 1: Signal Power was lower than Noise Threshold (will be cleared when the register is read)
D1	R	0	DAC miniDSP Auxilliary Interrupt Port Output (will be cleaed when register is read)
D0	R	0	DAC miniDSP Standard Interrupt Port Output (will be cleaed when register is read)

6.2.42 Page 0 / Register 43: Interrupt Flag Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	0	0	Right ADC DC Measurement Data Available Flag 0: Data not available 1: Data available
D6	R	0	Left ADC DC Measurement Data Available Flag 0: Data not available 1: Data available
D5	R	0	ADC miniDSP Auxilliary Interrupt Port Output
D4	R	0	ADC miniDSP Standard Interrupt Port Output
D3	R	0	Right AGC Noise Threshold Flag 0: Signal Power is greater than Noise Threshold 1: Signal Power was lower than Noise Threshold
D2	R	0	Left AGC Noise Threshold Flag 0: Signal Power is greater than Noise Threshold 1: Signal Power was lower than Noise Threshold
D1	R	0	DAC miniDSP Auxilliary Interrupt Port Output
D0	R	0	DAC miniDSP Standard Interrupt Port Output

6.2.43 Page 0 / Register 44: Interrupt Enable Control Register 3 (INT1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Right DAC Signal Power is above Signal Threshold of DRC to INT1 0: disabled 1: enabled
D6	R/W	0	Left DAC Signal Power is above Signal Threshold of DRC to INT1 0: disabled 1: enabled
D5	R/W	0	ADC MAC Engine Auxilliary Interrupt to INT1 0: disabled 1: enabled

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4	R/W	0	ADC MAC Engine Standard Interrupt to INT1 0: disabled 1: enabled
D3	R/W	0	Right ADC Signal Power Lesser than Noise Threshold for Right AGC to INT1 0: disabled 1: enabled
D2	R/W	0	Left ADC Signal Power Lesser than Noise Threshold for Left AGC to INT1 0: disabled 1: enabled
D1	R/W	0	DAC MAC Engine Auxilliary Interrupt to INT1 0: disabled 1: enabled
D0	R/W	0	DAC MAC Engine Standard Interrupt to INT1 0: disabled 1: enabled

6.2.44 Page 0 / Register 45: Interrupt Enable Control Register 4 (INT2)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Right DAC Signal Power is above Signal Threshold of DRC to INT2 0: disabled 1: enabled
D6	R/W	0	Left DAC Signal Power is above Signal Threshold of DRC to INT2 0: disabled 1: enabled
D5	R/W	0	ADC MAC Engine Auxilliary Interrupt to INT2 0: disabled 1: enabled
D4	R/W	0	ADC MAC Engine Standard Interrupt to INT2 0: disabled 1: enabled
D3	R/W	0	Right ADC Signal Power Lesser than Noise Threshold for Right AGC to INT2 0: disabled 1: enabled
D2	R/W	0	Left ADC Signal Power Lesser than Noise Threshold for Left AGC to INT2 0: disabled 1: enabled
D1	R/W	0	DAC MAC Engine Auxilliary Interrupt to INT2 0: disabled 1: enabled
D0	R/W	0	DAC MAC Engine Standard Interrupt to INT2 0: disabled 1: enabled

6.2.45 Page 0 / Register 46: Sticky Flag Register 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values
D6	R	0	Overcurrent on VDD_ADC_LDO interrupt 0: no overcurrent condition 1: overcurrent condition detected (will be cleared when the register is read)

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5	R	0	Overcurrent on VSS_DAC_LDO interrupt 0: no overcurrent condition 1: overcurrent condition detected (will be cleared when the register is read)
D4	R	0	Overcurrent on VDD_DAC_LDO interrupt 0: no overcurrent condition 1: overcurrent condition detected (will be cleared when the register is read)
D3	R	0	Reserved. Write only default values
D2	R	0	Power Good on VDD_ADC_LDO 0: power not good 1: power good (will be cleared when register is read)
D1	R	0	Power Good on VDD_DAC_LDO 0: power not good 1: power good (will be cleared when register is read)
D0	R	0	Power Good on VSS_DAC_LDO 0: power not good 1: power good (will be cleared when register is read)

6.2.46 Page 0 / Register 47: Interrupt Flag Register 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values
D6	R	0	Overcurrent on VDD_ADC_LDO 0: no overcurrent condition 1: overcurrent condition
D5	R	0	Overcurrent on VSS_DAC_LDO 0: no overcurrent condition 1: overcurrent condition
D4	R	0	Overcurrent on VDD_DAC_LDO 0: no overcurrent condition 1: overcurrent condition
D3	R	0	Reserved. Write only default values
D2	R	0	Power good on VDD_ADC_LDO 0: power not good 1: power good
D1	R	0	Power good on VSS_DAC_LDO 0: power not good 1: power good
D0	R	0	Power good on VDD_DAC_LDO 0: power not good 1: power good

6.2.47 Page 0 / Register 48: Interrupt Enable Control Register 5 (INT1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values
D6	R/W	0	Overcurrent on VDD_ADC_LDO to INT1 0: disabled 1: enabled
D5	R/W	0	Overcurrent on VSS_DAC_LDO to INT1 0: disabled 1: enabled

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4	R/W	0	Overcurrent on VDD_DAC_LDO to INT1 0: disabled 1: enabled
D3	R	0	Reserved. Write only default values
D2	R/W	0	Power good on VDD_ADC_LDO on INT1 0: disabled 1: enabled
D1	R/W	0	Power good on VSS_DAC_LDO on INT1 0: disabled 1: enabled
D0	R/W	0	Power good on VDD_DAC_LDO on INT1 0: disabled 1: enabled

6.2.48 Page 0 / Register 49: Interrupt Enable Control Register 6 (INT2)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values
D6	R/W	0	Overcurrent on VDD_ADC_LDO to INT2 0: disabled 1: enabled
D5	R/W	0	Overcurrent on VSS_DAC_LDO to INT2 0: disabled 1: enabled
D4	R/W	0	Overcurrent on VDD_DAC_LDO to INT2 0: disabled 1: enabled
D3	R	0	Reserved. Write only default values
D2	R/W	0	Power good on VDD_ADC_LDO on INT2 0: disabled 1: enabled
D1	R/W	0	Power good on VSS_DAC_LDO on INT2 0: disabled 1: enabled
D0	R/W	0	Power good on VDD_DAC_LDO on INT2 0: disabled 1: enabled

6.2.49 Page 0 / Register 50: Sticky Flag Register 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Combined headphone/rec amp short circuit interrupt. Cleared on register reading. 0: no short circuit 1: short circuit
D6	R	0	Headphone Left open circuit interrupt. Cleared on register reading. 0: no open circuit 1: open circuit
D5	R	0	Headphone Right open circuit interrupt. Cleared on register reading. 0: no open circuit 1: open circuit
D4	R	0	Rec Left open circuit interrupt. Cleared on register reading. 0: no open circuit 1: open circuit

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3	R	0	Rec Right open circuit interrupt. Cleared on register reading. 0: no open circuit 1: open circuit
D2	R	0	Hook Interrupt. Cleared on register reading. 0: no interrupt 1: interrupt
D1	R	0	Detect long pulse. Cleared on register reading. 0: no long pulse detect 1: long pulse detect
D0	R	0	Detect short pulse. Cleared on register reading. 0: no short pulse detect 1: short pulse detect

6.2.50 Page 0 / Register 51: Interrupt Flag Register 4

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Combined headphone/rec amp short circuit interrupt. 0: no short circuit 1: short circuit
D6	R	0	Headphone Left open circuit interrupt. 0: no open circuit 1: open circuit
D5	R	0	Headphone Right open circuit interrupt. 0: no open circuit 1: open circuit
D4	R	0	Rec Left open circuit interrupt. 0: no open circuit 1: open circuit
D3	R	0	Rec Right open circuit interrupt. 0: no open circuit 1: open circuit
D2	R	0	Hook Interrupt. 0: no interrupt 1: interrupt
D1	R	0	Detect long pulse. 0: no long pulse detect 1: long pulse detect
D0	R	0	Detect short pulse. 0: no short pulse detect 1: short pulse detect

6.2.51 Page 0 / Register 52: Interrupt Enable Control Register 7 (INT1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	0	0	Combined headphone/rec amp short circuit interrupt for INT1 0: disabled 1: enabled
D6	R/W	0	Headphone Left open circuit interrupt for INT1 0: disabled 1: enabled
D5	R/W	0	Headphone Right open circuit interrupt for INT1 0: disabled 1: enabled

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4	R/W	0	Rec Left open circuit interrupt for INT1 0: disabled 1: enabled
D3	R/W	0	Rec Right open circuit interrupt for INT1 0: disabled 1: enabled
D2	R/W	0	Hook Interrupt for INT1 0: disabled 1: enabled
D1	R/W	0	Detect long pulse for INT1 0: disabled 1: enabled
D0	R/W	0	Detect short pulse for INT1 0: disabled 1: enabled

6.2.52 Page 0 / Register 53: Interrupt Enable Control Register 8 (INT2)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Combined headphone/rec amp short circuit interrupt for INT2 0: disabled 1: enabled
D6	R/W	0	Headphone Left open circuit interrupt for INT2 0: disabled 1: enabled
D5	R/W	0	Headphone Right open circuit interrupt for INT2 0: disabled 1: enabled
D4	R/W	0	Rec Left open circuit interrupt for INT2 0: disabled 1: enabled
D3	R/W	0	Rec Right open circuit interrupt for INT2 0: disabled 1: enabled
D2	R/W	0	Hook Interrupt for INT2 0: disabled 1: enabled
D1	R/W	0	Detect long pulse for INT2 0: disabled 1: enabled
D0	R/W	0	Detect short pulse for INT2 0: disabled 1: enabled

6.2.53 Page 0 / Register 54: Interrupt Edge Select Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved. Write only default values
D5–D4	R/W	01	Power good on VDD_ADC_LDO 00: reserved 01: rising edge triggered 10: falling edge triggered 11: triggered on change

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3–D2	R/W	01	Power good on VSS_DAC_LDO 00: reserved 01: rising edge triggered 10: falling edge triggered 11: triggered on change
D1–D0	R/W	01	Power good on VDD_DAC_LDO 00: reserved 01: rising edge triggered 10: falling edge triggered 11: triggered on change

6.2.54 Page 0 / Register 55: Interrupt Edge Select Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	01	Left HP over current 00: reserved 01: rising edge triggered 10: falling edge triggered 11: triggered on change
D5–D4	R/W	01	VDD_ADC_LDO overcurrent 00: reserved 01: rising edge triggered 10: falling edge triggered 11: triggered on change
D3–D2	R/W	01	VSS_DAC_LDO overcurrent 00: reserved 01: rising edge triggered 10: falling edge triggered 11: triggered on change
D1–D0	R/W	01	VDD_DAC_LDO overcurrent 00: reserved 01: rising edge triggered 10: falling edge triggered 11: triggered on change

6.2.55 Page 0 / Register 56: Interrupt Edge Select Register 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	01	Right HP over current 00: reserved 01: rising edge triggered 10: falling edge triggered 11: triggered on change
D5–D4	R/W	01	Left REC over current 00: reserved 01: rising edge triggered 10: falling edge triggered 11: triggered on change
D3–D2	R/W	01	
D1–D0	R/W	01	Hook over current 00: reserved 01: rising edge triggered 10: falling edge triggered 11: triggered on change

6.2.56 Page 0 / Register 57-59: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved, Write only default values to this register

6.2.57 Page 0 / Register 60: DAC Signal Processing Block Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value
D6	R/W	0	DAC miniDSP Power Configuration 0: DAC miniDSP is powered down with DAC Channel Power Down 1: DAC miniDSP is powered up if ADC Channel is powered up
D5	R	0	Reserved. Write only default value
D4–D0	R/W	0 0001	0 0000: The DAC miniDSP will be used for signal processing 0 0001: DAC Signal Processing Block PRB_P1 0 0010: DAC Signal Processing Block PRB_P2 0 0011: DAC Signal Processing Block PRB_P3 0 0100: DAC Signal Processing Block PRB_P4 … 1 1000: DAC Signal Processing Block PRB_P24 1 1001: DAC Signal Processing Block PRB_P25 1 1010-1 1111: Reserved. Do not use

6.2.58 Page 0 / Register 61: ADC Signal Processing Block Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R	000	Reserved. Write only default values
D4–D0	R/W	0 0001	0 0000: The ADC miniDSP will be used for signal processing 0 0001: ADC Singal Processing Block PRB_R1 0 0010: ADC Signal Processing Block PRB_R2 0 0011: ADC Signal Processing Block PRB_R3 0 0100: ADC Signal Processing Block PRB_R4 … 1 0001: ADC Signal Processing Block PRB_R17 1 0010: ADC Signal Processing Block PRB_R18 1 0010-1 1111: Reserved. Do not use

6.2.59 Page 0 / Register 62: ADC and DAC miniDSP Configuration Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values
D6	R/W	0	ADC miniDSP Auxilliary Control Bit-A. Used for conditional instruction like JMP.
D5	R/W	0	ADC miniDSP Auxilliary Control Bit-B. Used for conditional instruction like JMP.
D4	R/W	0	0: Reset ADC miniDSP instruction counter at the start of new frame. 1: Do not reset ADC miniDSP instruction counter at the start of new frame. If ADC miniDSP is used for Signal Processing
D3	R	0	Reserved. Write only default values
D2	R/W	0	DAC miniDSP Auxilliary Control Bit-A. Used for conditional instruction like JMP.
D1	R/W	0	DAC miniDSP Auxilliary Control Bit-B. Used for conditional instruction like JMP.

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D0	R/W	0	0: Reset DAC miniDSP instruction counter at the start of new frame. 1: Do not reset DAC miniDSP instruction counter at the start of new frame. If DAC miniDSP is used for Signal Processing

6.2.60 Page 0 / Register 63: DAC Channel Setup Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left DAC Channel Power Control 0: Left DAC Channel Powered Down 1: Left DAC Channel Powered Up
D6	R/W	0	Right DAC Channel Power Control 0: Right DAC Channel Powered Down 1: Right DAC Channel Powered Up
D5–D4	R/W	01	Left DAC Data path Control 00: Left DAC data is disabled 01: Left DAC data Left Channel Audio Interface Data 10: Left DAC data is Right Channel Audio Interface Data 11: Left DAC data is Mono Mix of Left and Right Channel Audio Interface Data
D3–D2	R/W	01	Right DAC Data path Control 00: Right DAC data is disabled 01: Right DAC data Right Channel Audio Interface Data 10: Right DAC data is Left Channel Audio Interface Data 11: Right DAC data is Mono Mix of Left and Right Channel Audio Interface Data
D1–D0	R/W	00	DAC Channel Volume Control's Soft-Step control 00: Soft-Stepping is 1 step per 1 DAC Word Clock 01: Soft-Stepping is 1 step per 2 DAC Word Clocks 10: Soft-Stepping is disabled 11: Reserved. Do not use

6.2.61 Page 0 / Register 64: DAC Channel Setup Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values
D6–D4	R/W	000	DAC Auto Mute Control 000: Auto Mute disabled 001: DAC is auto muted if input data is DC for more than 100 consecutive inputs 010: DAC is auto muted if input data is DC for more than 200 consecutive inputs 011: DAC is auto muted if input data is DC for more than 400 consecutive inputs 100: DAC is auto muted if input data is DC for more than 800 consecutive inputs 101: DAC is auto muted if input data is DC for more than 1600 consecutive inputs 110: DAC is auto muted if input data is DC for more than 3200 consecutive inputs 111: DAC is auto muted if input data is DC for more than 6400 consecutive inputs
D3	R/W	1	Left DAC Channel Mute Control 0: Left DAC Channel not muted 1: Left DAC Channel muted
D2	R/W	1	Right DAC Channel Mute Control 0: Right DAC Channel not muted 1: Right DAC Channel muted
D1–D0	R/W	00	DAC Master Volume Control 00: Left and Right Channel have independent volume control 01: Left Channel Volume is controlled by Right Channel Volume Control setting 10: Right Channel Volume is controlled by Left Channel Volume Control setting 11: Reserved. Do not use

6.2.62 Page 0 / Register 65: Left DAC Channel Digital Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Left DAC Channel Digital Volume Control Setting 0111 1111-0011 0001: Reserved. Do not use 0011 0000: Digital Volume Control = +24 dB 0010 1111: Digital Volume Control = +23.5 dB … 0000 0001: Digital Volume Control = +0.5 dB 0000 0000: Digital Volume Control = 0.0 dB 1111 1111: Digital Volume Control = -0.5 dB ... 1000 0010: Digital Volume Control = -63 dB 1000 0001: Digital Volume Control = -63.5 dB 1000 0000: Reserved. Do not use

6.2.63 Page 0 / Register 66: Right DAC Channel Digital Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Right DAC Channel Digital Volume Control Setting 0111 1111-0011 0001: Reserved. Do not use 0011 0000: Digital Volume Control = +24 dB 0010 1111: Digital Volume Control = +23.5 dB … 0000 0001: Digital Volume Control = +0.5 dB 0000 0000: Digital Volume Control = 0.0 dB 1111 1111: Digital Volume Control = -0.5 dB ... 1000 0010: Digital Volume Control = -63 dB 1000 0001: Digital Volume Control = -63.5 dB 1000 0000: Reserved. Do not use

6.2.64 Page 0 / Register 67: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved, Write only default values to this register

6.2.65 Page 0 / Register 68: DRC Control Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value
D6	R/W	0	DRC Enable Control 0: Left Channel DRC disabled 1: Left Channel DRC enabled
D5	R/W	0	DRC Enable Control 0: Right Channel DRC disabled 1: Right Channel DRC enabled

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4–D2	R/W	011	DRC Threshold control 000: DRC Threshold = -3 dBFS 001: DRC Threshold = -6 dBFS 010: DRC Threshold = -9 dBFS 011: DRC Threshold = -12 dBFS 100: DRC Threshold = -15 dBFS 101: DRC Threshold = -18 dBFS 110: DRC Threshold = -21 dBFS 111: DRC Threshold = -24 dBFS
D1–D0	R/W	11	DRC Hysteresis Control 00: DRC Hysteresis = 0 dB 01: DRC Hysteresis = 1 dB 10: DRC Hysteresis = 2 dB 11: DRC Hysteresis = 3 dB

6.2.66 Page 0 / Register 69: DRC Control Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value.
D6–D3	R/W	0111	DRC Hold Programmability 0000: DRC Hold Disabled 0001: DRC Hold Time = 32 DAC Word Clocks 0010: DRC Hold Time = 64 DAC Word Clocks 0011: DRC Hold Time = 128 DAC Word Clocks 0100: DRC Hold Time = 256 DAC Word Clocks 0101: DRC Hold Time = 512 DAC Word Clocks ... 1110: DRC Hold Time = 4*32768 DAC Word Clocks 1111: DRC Hold Time = 5*32768 DAC Word Clocks
D2–D0	R/W	000	Reserved. Write only default values

6.2.67 Page 0 / Register 70: DRC Control Register 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	DRC Attack Rate control 0000: DRC Attack Rate = 4.0 dB per DAC Word Clock 0001: DRC Attack Rate = 2.0 dB per DAC Word Clock 0010: DRC Attack Rae = 1.0 dB per DAC Word Clock … 1110: DRC Attack Rate = 2.4414e-4 dB per DAC Word Clock 1111: DRC Attack Rate = 1.2207e-4 dB per DAC Word Clock
D3–D0	R/W	0000	DRC Decay Rate control 0000: DRC Decay Rate = 1.5625e-2 dB per DAC Word Clock 0001: DRC Decay Rate = 7.8125e-3 dB per DAC Word Clock 0010: DRC Decay Rae = 3.9062e-3 dB per DAC Word Clock … 1110: DRC Decay Rate = 9.5367e-7 dB per DAC Word Clock 1111: DRC Decay Rate = 4.7683e-7 dB per DAC Word Clock

6.2.68 Page 0 / Register 71: Beep Generator Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Beep Generator Disabled 1: Beep Generator Enabled. This bit will self clear after the beep has been generated.
D6	R	0	Reserved. Write only default value
D5–D0	R/W	00 0000	Left Channel Beep Volume Control 00 0000: Left Channel Beep Volume = 0 dB 00 0001: Left Channel Beep Volume = -1 dB … 11 1110: Left Channel Beep Volume = -62 dB 11 1111: Left Channel Beep Volume = -63 dB

6.2.69 Page 0 / Register 72: Beep Generator Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Beep Generator Master Volume Control Setting 00: Left and Right Channels have independent Volume Settings 01: Left Channel Beep Volume is the same as programmed for Right Channel 10: Right Channel Beep Volume is the same as programmed for Left Channel 11: Reserved. Do not use
D5–D0	R/W	00 0000	Right Channel Beep Volume Control 00 0000: Right Channel Beep Volume = 0 dB 00 0001: Right Channel Beep Volume = -1 dB … 11 1110: Right Channel Beep Volume = -62 dB 11 1111: Right Channel Beep Volume = -63 dB

6.2.70 Page 0 / Register 73: Beep Generator Register 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Programmed value is Beep Sample Length(23:16)

6.2.71 Page 0 / Register 74: Beep Generator Register 4

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Programmed value is Beep Sample Length(15:8)

6.2.72 Page 0 / Register 75: Beep Generator Register 5

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 1110	Programmed value is Beep Sample Length(7:0)

6.2.73 Page 0 / Register 76: Beep Generator Register 6

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0001 0000	Programmed Value is Beep Sin(x)(15:8), where Sin(x) = sin(2*pi*Fin/Fs), where Fin is desired beep frequency and Fs is DAC sample rate

6.2.74 Page 0 / Register 77: Beep Generator Register 7

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1101 1000	Programmed Value is Beep Sin(x)(7:0), where Sin(x) = sin(2*pi*Fin/Fs), where Fin is desired beep frequency and Fs is DAC sample rate

6.2.75 Page 0 / Register 78: Beep Generator Register 8

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1110	Programmed Value is Beep Cos(x)(15:8), where Cos(x) = cos(2*pi*Fin/Fs), where Fin is desired beep frequency and Fs is DAC sample rate

6.2.76 Page 0 / Register 79: Beep Generator Register 9

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 0011	Programmed Value is Beep Cos(x)(7:0), where Cos(x) = cos(2*pi*Fin/Fs), where Fin is desired beep frequency and Fs is DAC sample rate

6.2.77 Page 0 / Register 80: ADC Digital Mic Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D1	R	0000 000	Reserved. Write only default value.
D0	R/W	0	Digital Mic Input Control 0: Digital Mic Channel left/right not swapped 1: Digital Mic Channel left/right swapped

6.2.78 Page 0 / Register 81: ADC Channel Setup Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left Channel ADC Power Control 0: Left Channel ADC is powered down 1: Left Channel ADC is powered up
D6	R/W	0	Right Channel ADC Power Control 0: Right Channel ADC is powered down 1: Right Channel ADC is powered up

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5–D4	R/W	00	Digital Microphone Input Configuration 00: GPIO serves as Digital Microphone Input 01: GPIO1 serves as Digital Microphone Input 10: DIN serves as Digital Microphone Input 11: Reserved. Do not use
D3	R/W	0	Left Channel Digital Microphone Power Control 0: Left Channel ADC not configured for Digital Microphone 1: Left Channel ADC configured for Digital Microphone
D2	R/W	0	Right Channel Digital Microphone Power Control 0: Right Channel ADC not configured for Digital Microphone 1: Right Channel ADC configured for Digital Microphone
D1–D0	R/W	00	ADC Volume Control Soft-Stepping Control 00: ADC Volume Control changes by 1 gain step per ADC Word Clock 01: ADC Volume Control changes by 1 gain step per two ADC Word Clocks 10: ADC Volume Control Soft-Stepping disabled 11: Reserved. Do not use

6.2.79 Page 0 / Register 82: ADC Fine Gain Adjust Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Left ADC Channel Mute Control 0: Left ADC Channel Un-muted 1: Left ADC Channel Muted
D6–D4	R/W	000	Left ADC Channel Fine Gain Adjust 000: Left ADC Channel Fine Gain = 0 dB 001: Left ADC Channel Fine Gain = -0.1 dB 010: Left ADC Channel Fine Gain = -0.2 dB 011: Left ADC Channel Fine Gain = -0.3 dB 100: Left ADC Channel Fine Gain = -0.4 dB 101-111: Reserved. Do not use
D3	R/W	1	Right ADC Channel Mute Control 0: Right ADC Channel Un-muted 1: Right ADC Channel Muted
D2–D0	R/W	000	Right ADC Channel Fine Gain Adjust 000: Right ADC Channel Fine Gain = 0 dB 001: Right ADC Channel Fine Gain = -0.1 dB 010: Right ADC Channel Fine Gain = -0.2 dB 011: Right ADC Channel Fine Gain = -0.3 dB 100: Right ADC Channel Fine Gain = -0.4 dB 101-111: Reserved. Do not use

6.2.80 Page 0 / Register 83: Left ADC Channel Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D0	R/W	000 0000	Left ADC Channel Volume Control 100 0000-110 1000: Reserved. Do not use 110 0111: Left ADC Channel Volume = -12 dB 110 0110: Left ADC Channel Volume = -11.5 dB 110 0101: Left ADC Channel Volume = -11.0 dB … 111 1111: Left ADC Channel Volume = -0.5 dB 000 0000: Left ADC Channel Volume = 0.0 dB 000 0001: Left ADC Channel Volume = 0.5 dB ... 010 0110: Left ADC Channel Volume = 19.0 dB 010 0111: Left ADC Channel Volume = 19.5 dB 010 1000: Left ADC Channel Volume = 20.0 dB 010 1001-011 1111: Reserved. Do not use

6.2.81 Page 0 / Register 84: Right ADC Channel Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values
D6–D0	R/W	000 0000	Right ADC Channel Volume Control 100 0000-110 1000: Reserved. Do not use 110 0111: Right ADC Channel Volume = -12 dB 110 0110: Right ADC Channel Volume = -11.5 dB 110 0101: Right ADC Channel Volume = -11.0 dB … 111 1111: Right ADC Channel Volume = -0.5 dB 000 0000: Right ADC Channel Volume = 0.0 dB 000 0001: Right ADC Channel Volume = 0.5 dB ... 010 0110: Right ADC Channel Volume = 19.0 dB 010 0111: Right ADC Channel Volume = 19.5 dB 010 1000: Right ADC Channel Volume = 20.0 dB 010 1001-011 1111: Reserved. Do not use

6.2.82 Page 0 / Register 85: ADC Phase Adjust Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	ADC Phase Compensation Control 1000 0000-1111 1111: Left ADC Channel Data is delayed with respect to Right ADC Channel Data. For details of delayed amount please see the description of Phase Compensation in the Overview section. 0000 0000: Left and Right ADC Channel data are not delayed with respect to each other 0000 0001-0111 1111: Right ADC Channel Data is delayed with respect to Left ADC Channel Data. For details of delayed amount please see the description of Phase Compensation in the Overview section.

6.2.83 Page 0 / Register 86: Left Channel AGC Control Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Left Channel AGC Disabled 1: Left Channel AGC Enabled

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D4	R/W	000	Left Channel AGC Target Level Setting 000: Left Channel AGC Target Level = -5.5 dBFS 001: Left Channel AGC Target Level = -8.0 dBFS 010: Left Channel AGC Target Level = -10.0 dBFS 011: Left Channel AGC Target Level = -12.0 dBFS 100: Left Channel AGC Target Level = -14.0 dBFS 101: Left Channel AGC Target Level = -17.0 dBFS 110: Left Channel AGC Target Level = -20.0 dBFS 111: Left Channel AGC Target Level = -24.0 dBFS
D3–D0	R	0000	Reserved. Write only default values

6.2.84 Page 0 / Register 87: Left Channel AGC Control Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Left Channel AGC Hysteresis Setting 00: Left Channel AGC Hysteresis is 1.0 dB 01: Left Channel AGC Hysteresis is 2.0 dB 10: Left Channel AGC Hysteresis is 4.0 dB 11: Left Channel AGC Hysteresis is disabled
D5–D1	R/W	00 000	Left Channel AGC Noise Threshold 0 0000: Left Channel AGC Noise Gate disabled 0 0001: Left Channel AGC Noise Threshold is -30 dB 0 0010: Left Channel AGC Noise Threshold is -32 dB 0 0011: Left Channel AGC Noise Threshold is -34 dB … 1 1101: Left Channel AGC Noise Threshold is -86 dB 1 1110: Left Channel AGC Noise Threshold is -88 dB 1 1111: Left Channel AGC Noise Threshold is -90 dB
D0	R	0	Reserved. Write only default value

6.2.85 Page 0 / Register 88: Left Channel AGC Control Register 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value
D6–D0	R/W	111 1111	Left Channel AGC Maximum Gain Setting 000 0000: Left Channel AGC Maximum Gain = 0.0 dB 000 0001: Left Channel AGC Maximum Gain = 0.5 dB 000 0010: Left Channel AGC Maximum Gain = 1.0 dB … 111 0011: Left Channel AGC Maximum Gain = 57.5 dB 111 0100-111 1111: Left Channel AGC Maximum Gain = 58.0 dB

6.2.86 Page 0 / Register 89: Left Channel AGC Control Register 4

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R/W	0000 0	Left Channel AGC Attack Time Setting 0 0000: Left Channel AGC Attack Time = 1*32 ADC Word Clocks 0 0001: Left Channel AGC Attack Time = 3*32 ADC Word Clocks 0 0010: Left Channel AGC Attack Time = 5*32 ADC Word Clocks … 1 1101: Left Channel AGC Attack Time = 59*32 ADC Word Clocks 1 1110: Left Channel AGC Attack Time = 61*32 ADC Word Clocks 1 1111: Left Channel AGC Attack Time = 63*32 ADC Word Clocks

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D2–D0	R/W	000	Left Channel AGC Attack Time Scale Factor Setting 000: Scale Factor = 1 001: Scale Factor = 2 010: Scale Factor = 4 … 101: Scale Factor = 32 110: Scale Factor = 64 111: Scale Factor = 128

6.2.87 Page 0 / Register 90: Left Channel AGC Control Register 5

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R/W	0000 0	Left Channel AGC Decay Time Setting 0 0000: Left Channel AGC Decay Time = 1*512 ADC Word Clocks 0 0001: Left Channel AGC Decay Time = 3*512 ADC Word Clocks 0 0010: Left Channel AGC Decay Time = 5*512 ADC Word Clocks … 1 1101: Left Channel AGC Decay Time = 59*512 ADC Word Clocks 1 1110: Left Channel AGC Decay Time = 61*512 ADC Word Clocks 1 1111: Left Channel AGC Decay Time = 63*512 ADC Word Clocks
D2–D0	R/W	000	Left Channel AGC Decay Time Scale Factor Setting 000: Scale Factor = 1 001: Scale Factor = 2 010: Scale Factor = 4 … 101: Scale Factor = 32 110: Scale Factor = 64 111: Scale Factor = 128

6.2.88 Page 0 / Register 91: Left Channel AGC Control Register 6

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R	000	Reserved. Write only default values
D4–D0	R/W	0 0000	Left Channel AGC Noise Debounce Time Setting 0 0001: Left Channel AGC Noise Debounce Time = 0 0 0010: Left Channel AGC Noise Debounce Time = 4 ADC Word Clocks 0 0011: Left Channel AGC Noise Debounce Time = 8 ADC Word Clocks … 0 1010: Left Channel AGC Noise Debounce Time = 2048 ADC Word Clocks 0 1011: Left Channel AGC Noise Debounce Time = 4096 ADC Word Clocks 0 1100: Left Channel AGC Noise Debounce Time = 2*4096 ADC Word Clocks 0 1101: Left Channel AGC Noise Debounce Time = 3*4096 ADC Word Clocks ... 1 1101: Left Channel AGC Noise Debounce Time = 19*4096 ADC Word Clocks 1 1110: Left Channel AGC Noise Debounce Time = 20*4096 ADC Word Clocks 1 1111: Left Channel AGC Noise Debounce Time = 21*4096 ADC Word Clocks

6.2.89 Page 0 / Register 92: Left Channel AGC Control Register 7

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R	0000	Reserved. Write only default values

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3–D0	R/W	0000	Left Channel AGC Signal Debounce Time Setting 0001: Left Channel AGC Signal Debounce Time = 0 0010: Left Channel AGC Signal Debounce Time = 4 ADC Word Clocks 0011: Left Channel AGC Signal Debounce Time = 8 ADC Word Clocks … 1001: Left Channel AGC Signal Debounce Time = 1024 ADC Word Clocks 1010: Left Channel AGC Signal Debounce Time = 2048 ADC Word Clocks 1011: Left Channel AGC Signal Debounce Time = 2*2048 ADC Word Clocks 1100: Left Channel AGC Signal Debounce Time = 3*2048 ADC Word Clocks 1101: Left Channel AGC Signal Debounce Time = 4*2048 ADC Word Clocks 1110: Left Channel AGC Signal Debounce Time = 5*2048 ADC Word Clocks 1111: Left Channel AGC Signal Debounce Time = 6*2048 ADC Word Clocks

6.2.90 Page 0 / Register 93: Left Channel AGC Control Register 8

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Left Channel AGC Gain Flag 1111 0100: Left Channel AGC Gain = -12.0 dB 1111 0101: Left Channel AGC Gain = -11.5 dB 1111 0110: Left Channel AGC Gain = -11.0 dB … 0000 0000: Left Channel AGC Gain = 0.0 dB … 0111 0010: Left Channel AGC Gain = 57.0 dB 0111 0011: Left Channel AGC Gain = 57.5 dB 0111 0100: Left Channel AGC Gain = 58.0 dB

6.2.91 Page 0 / Register 94: Right Channel AGC Control Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Right Channel AGC Disabled 1: Right Channel AGC Enabled
D6–D4	R/W	000	Right Channel AGC Target Level Setting 000: Right Channel AGC Target Level = -5.5 dBFS 001: Right Channel AGC Target Level = -8.0 dBFS 010: Right Channel AGC Target Level = -10.0 dBFS 011: Right Channel AGC Target Level = -12.0 dBFS 100: Right Channel AGC Target Level = -14.0 dBFS 101: Right Channel AGC Target Level = -17.0 dBFS 110: Right Channel AGC Target Level = -20.0 dBFS 111: Right Channel AGC Target Level = -24.0 dBFS
D3–D0	R	0000	Reserved. Write only default values

6.2.92 Page 0 / Register 95: Right Channel AGC Control Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Right Channel AGC Hysteresis Setting 00: Right Channel AGC Hysteresis is 1.0 dB 01: Right Channel AGC Hysteresis is 2.0 dB 10: Right Channel AGC Hysteresis is 4.0 dB 11: Right Channel AGC Hysteresis is disabled

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5–D1	R/W	00 000	Right Channel AGC Noise Threshold 0 0000: Right Channel AGC Noise Gate disabled 0 0001: Right Channel AGC Noise Threshold is -30 dB 0 0010: Right Channel AGC Noise Threshold is -32 dB 0 0011: Right Channel AGC Noise Threshold is -34 dB … 1 1101: Right Channel AGC Noise Threshold is -86 dB 1 1110: Right Channel AGC Noise Threshold is -88 dB 1 1111: Right Channel AGC Noise Threshold is -90 dB
D0	R	0	Reserved. Write only default value

6.2.93 Page 0 / Register 96: Right Channel AGC Control Register 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value
D6–D0	R/W	111 1111	Right Channel AGC Maximum Gain Setting 000 0000: Right Channel AGC Maximum Gain = 0.0 dB 000 0001: Right Channel AGC Maximum Gain = 0.5 dB 000 0010: Right Channel AGC Maximum Gain = 1.0 dB … 111 0011: Right Channel AGC Maximum Gain = 57.5 dB 111 0100-111 1111: Right Channel AGC Maximum Gain = 58.0 dB

6.2.94 Page 0 / Register 97: Right Channel AGC Control Register 4

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R/W	00 000	Right Channel AGC Attack Time Setting 0 0000: Right Channel AGC Attack Time = 1*32 ADC Word Clocks 0 0001: Right Channel AGC Attack Time = 3*32 ADC Word Clocks 0 0010: Right Channel AGC Attack Time = 5*32 ADC Word Clocks … 1 1101: Right Channel AGC Attack Time = 59*32 ADC Word Clocks 1 1110: Right Channel AGC Attack Time = 61*32 ADC Word Clocks 1 1111: Right Channel AGC Attack Time = 63*32 ADC Word Clocks
D2–D0	R/W	000	Right Channel AGC Attack Time Scale Factor Setting 000: Scale Factor = 1 001: Scale Factor = 2 010: Scale Factor = 4 … 101: Scale Factor = 32 110: Scale Factor = 64 111: Scale Factor = 128

6.2.95 Page 0 / Register 98: Right Channel AGC Control Register 5

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R/W	0000 0	Right Channel AGC Decay Time Setting 0 0000: Right Channel AGC Decay Time = 1*512 ADC Word Clocks 0 0001: Right Channel AGC Decay Time = 3*512 ADC Word Clocks 0 0010: Right Channel AGC Decay Time = 5*512 ADC Word Clocks … 1 1101: Right Channel AGC Decay Time = 59*512 ADC Word Clocks 1 1110: Right Channel AGC Decay Time = 61*512 ADC Word Clocks 1 1111: Right Channel AGC Decay Time = 63*512 ADC Word Clocks
D2–D0	R/W	000	Right Channel AGC Decay Time Scale Factor Setting 000: Scale Factor = 1 001: Scale Factor = 2 010: Scale Factor = 4 … 101: Scale Factor = 32 110: Scale Factor = 64 111: Scale Factor = 128

6.2.96 Page 0 / Register 99: Right Channel AGC Control Register 6

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R	000	Reserved. Write only default values
D4–D0	R/W	0 0000	Right Channel AGC Noise Debounce Time Setting 0 0001: Right Channel AGC Noise Debounce Time = 0 0 0010: Right Channel AGC Noise Debounce Time = 4 ADC Word Clocks 0 0011: Right Channel AGC Noise Debounce Time = 8 ADC Word Clocks … 0 1010: Right Channel AGC Noise Debounce Time = 2048 ADC Word Clocks 0 1011: Right Channel AGC Noise Debounce Time = 4096 ADC Word Clocks 0 1100: Right Channel AGC Noise Debounce Time = 2*4096 ADC Word Clocks 0 1101: Right Channel AGC Noise Debounce Time = 3*4096 ADC Word Clocks ... 1 1101: Right Channel AGC Noise Debounce Time = 19*4096 ADC Word Clocks 1 1110: Right Channel AGC Noise Debounce Time = 20*4096 ADC Word Clocks 1 1111: Right Channel AGC Noise Debounce Time = 21*4096 ADC Word Clocks

6.2.97 Page 0 / Register 100: Right Channel AGC Control Register 7

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R	0000	Reserved. Write only default values
D3–D0	R/W	0000	Right Channel AGC Signal Debounce Time Setting 0001: Right Channel AGC Signal Debounce Time = 0 0010: Right Channel AGC Signal Debounce Time = 4 ADC Word Clocks 0011: Right Channel AGC Signal Debounce Time = 8 ADC Word Clocks … 1001: Right Channel AGC Signal Debounce Time = 1024 ADC Word Clocks 1010: Right Channel AGC Signal Debounce Time = 2048 ADC Word Clocks 1011: Right Channel AGC Signal Debounce Time = 2*2048 ADC Word Clocks 1100: Right Channel AGC Signal Debounce Time = 3*2048 ADC Word Clocks 1101: Right Channel AGC Signal Debounce Time = 4*2048 ADC Word Clocks 1110: Right Channel AGC Signal Debounce Time = 5*2048 ADC Word Clocks 1111: Right Channel AGC Signal Debounce Time = 6*2048 ADC Word Clocks

6.2.98 Page 0 / Register 101: Right Channel AGC Control Register 8

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Right Channel AGC Gain Flag 1111 0100: Right Channel AGC Gain = -12.0 dB 1111 0101: Right Channel AGC Gain = -11.5 dB 1111 0110: Right Channel AGC Gain = -11.0 dB … 0000 0000: Right Channel AGC Gain = 0.0 dB … 0111 0010: Right Channel AGC Gain = 57.0 dB 0111 0011: Right Channel AGC Gain = 57.5 dB 0111 0100: Right Channel AGC Gain = 58.0 dB

6.2.99 Page 0 / Register 102: DC Measurement Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: DC Measurement Mode disabled for Left ADC Channel 1: DC Measurement Mode enabled for Left ADC Channel
D6	R/W	0	0: DC Measurement Mode disabled for Right ADC Channel 1: DC Measurement Mode enabled for Right ADC Channel
D5	R/W	0	0: DC Measurement is done using First-Order moving average filter with averaging of 2^D 1: DC Measurement is done with 1sr order Low-pass IIR filter with coefficients as a function of D
D4–D0	R/W	0 0000	DC Measurement D setting 0 0000: Reserved. Do not use 0 0001: DC Measurement D parameter = 1 0 0010: DC Measurement D parameter = 2 .. 1 0011: DC Measurement D parameter = 19 1 0100: DC Measurement D parameter = 20 1 0101-1 1111: Reserved. Do not use

6.2.100 Page 0 / Register 103: DC Measurement Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved. Write only default values
D5	R/W	0	0: For IIR based DC measurement, measurement value is the instantaneous output of IIR filter 1: For IIR based DC measurement, the measurement value is updated before periodic clearing of IIR filter
D4–D0	R/W	0 0000	IIR based DC Measurement, averaging time setting 0 0000: Infinite average is used 0 0001: Averaging time is 2^1 ADC Modulator clocks 0 0010: Averaging time is 2^2 ADC Modulator clocks … 1 0011: Averaging time is 2^19 ADC Modulator clocks 1 0100: Averaging time is 2^20 ADC Modulator clocks 1 0101-1 1111: Reserved. Do not use

6.2.101 Page 0 / Register 104: Left Channel DC Measurement Output Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Left Channel DC Measurement Output (23:16)

6.2.102 Page 0 / Register 105: Left Channel DC Measurement Output Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Left Channel DC Measurement Output (15:8)

6.2.103 Page 0 / Register 106: Left Channel DC Measurement Output Register 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Left Channel DC Measurement Output (7:0)

6.2.104 Page 0 / Register 107: Right Channel DC Measurement Output Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Right Channel DC Measurement Output (23:16)

6.2.105 Page 0 / Register 108: Right Channel DC Measurement Output Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Right Channel DC Measurement Output (15:8)

6.2.106 Page 0 / Register 109: Right Channel DC Measurement Output Register 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Right Channel DC Measurement Output (7:0)

6.2.107 Page 0 / Register 110-113: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.108 Page 0 / Register 114: Analog FIR Control Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0001	Unit Delay Register for tap 1 in DAC AFIR.
D3–D0	R/W	0000	Unit Delay Register for tap 0 in DAC AFIR.

6.2.109 Page 0 / Register 115: Analog FIR Control Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0011	Unit Delay Register for tap 3 in DAC AFIR.
D3–D0	R/W	0010	Unit Delay Register for tap 2 in DAC AFIR.

6.2.110 Page 0 / Register 116: Analog FIR Control Register 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0101	Unit Delay Register for tap 5 in DAC AFIR.
D3–D0	R/W	0100	Unit Delay Register for tap 4 in DAC AFIR.

6.2.111 Page 0 / Register 117-119: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.112 Page 0 / Register 120: GPIO1 Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved. Write only default values
D5–D2	R/W	00 00	GPIO1 Control 0000: GPIO1 input/output disabled 0001: GPIO1 input is used for secondary BCLK, secondary WCLK, secondary DIN, secondary ADC_WCLK or seconday DIGMIC_DATA input 0010: GPIO1 is general purpose input (GPI) 0011: GPIO1 is general purpose output 0100: GPIO1 output is CLKOUT 0101: GPIO1 output is INT1 (active high) 0110: GPIO1 output is inverted INT1 (active low) 0111: GPIO1 output is INT1 (open drain) 1000: GPIO1 output is INT2 (active high) 1001: GPIO1 output is inverted INT2 (active low) 1010: GPIO1 output is INT2 (open drain) 1011: GPIO1 output is ADC_WCLK for Audio Interface 1100: GPIO1 output is secondary bit-clock for Audio Interface 1101: GPIO1 output is secondary word-clock for Audio Interface 1110: GPIO1 output is clock for the digital microphone 1111: Reserved
D1	R	X	GPIO1 Input Pin state as a GPI
D0	R/W	0	GPIO1 as general purpose output control 0: GPIO1 pin is driven to '0' in general purpose output mode 1: GPIO1 pin is driven to '1' in general purpose output mode

6.2.113 Page 0 / Register 121: GPIO2 Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved. Write only default values

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5–D2	R/W	00 00	GPIO2 Control 0000: GPIO2 input/output disabled 0001: GPIO2 input is used for secondary BCLK, secondary WCLK, secondary DIN or secondary ADC_WCLK input 0010: GPIO2 is general purpose input (GPI) 0011: GPIO2 is general purpose output 0100: GPIO2 output is CLKOUT 0101: GPIO2 output is INT1 (active high) 0110: GPIO2 output is inverted INT1 (active low) 0111: GPIO2 output is INT1 (open drain) 1000: GPIO2 output is INT2 (active high) 1001: GPIO2 output is inverted INT2 (active low) 1010: GPIO2 output is INT2 (open drain) 1011: GPIO2 output is ADC_WCLK for Audio Interface 1100: GPIO2 output is secondary bit-clock for Audio Interface 1101: GPIO2 output is secondary word-clock for Audio Interface 1110: GPIO2 output is clock for the digital microphone 1111: Reserved
D1	R	X	GPIO2 Input Pin state as a GPI
D0	R/W	0	GPIO2 as general purpose output control 0: GPIO2 pin is driven to '0' in general purpose output mode 1: GPIO2 pin is driven to '1' in general purpose output mode

6.2.114 Page 0 / Register 122: GPIO3/DIGMIC_CLK Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved. Write only default values
D5–D2	R/W	00 00	GPIO3/DIGMIC_CLK Control 0000: GPIO3/DIGMIC_CLK input/output disabled 0001: GPIO3/DIGMIC_CLK input is used for secondary BCLK, secondary WCLK, secondary DIN or secondary ADC_WCLK input 0010: GPIO3/DIGMIC_CLK is general purpose input (GPI) 0011: GPIO3/DIGMIC_CLK is general purpose output 0100: GPIO3/DIGMIC_CLK2 output is CLKOUT 0101: GPIO3/DIGMIC_CLK output is INT1 (active high) 0110: GPIO3/DIGMIC_CLK output is inverted INT1 (active low) 0111: GPIO3/DIGMIC_CLK output is INT1 (open drain) 1000: GPIO3/DIGMIC_CLK output is INT2 (active high) 1001: GPIO3/DIGMIC_CLK output is inverted INT2 (active low) 1010: GPIO3/DIGMIC_CLK output is INT2 (open drain) 1011: GPIO3/DIGMIC_CLK output is ADC_WCLK for Audio Interface 1100: GPIO3/DIGMIC_CLK output is secondary bit-clock for Audio Interface 1101: GPIO3/DIGMIC_CLK output is secondary word-clock for Audio Interface 1110: GPIO3/DIGMIC_CLK output is clock for the digital microphone 1111: GPIO3/DIGMIC_CLK output is clock for the digital microphon
D1	R	X	GPIO3/DIGMIC_CLK Input Pin state as a GPI
D0	R/W	0	GPIO3/DIGMIC_CLK as general purpose output control 0: GPIO3/DIGMIC_CLK pin is driven to '0' in general purpose output mode 1: GPIO3/DIGMIC_CLK pin is driven to '1' in general purpose output mode

6.2.115 Page 0 / Register 123: GPIO4/DIGMIC_DATA Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved. Write only default values

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5–D2	R/W	00 00	GPIO4/DIGMIC_DATA Control 0000: GPIO4/DIGMIC_DATA input/output disabled 0001: GPIO4/DIGMIC_DATA input is used for secondary BCLK, secondary WCLK, secondary DIN or secondary ADC_WCLK input 0010: GPIO4/DIGMIC_DATA is general purpose input (GPI) 0011: GPIO4/DIGMIC_DATA is general purpose output 0100: GPIO4/DIGMIC_DATA output is CLKOUT 0101: GPIO4/DIGMIC_DATA output is INT1 (active high) 0110: GPIO4/DIGMIC_DATA output is inverted INT1 (active low) 0111: GPIO4/DIGMIC_DATA output is INT1 (open drain) 1000: GPIO4/DIGMIC_DATA output is INT2 (active high) 1001: GPIO4/DIGMIC_DATA output is inverted INT2 (active low) 1010: GPIO4/DIGMIC_DATA output is INT2 (open drain) 1011: GPIO4/DIGMIC_DATA output is ADC_WCLK for Audio Interface 1100: GPIO4/DIGMIC_DATA output is secondary bit-clock for Audio Interface 1101: GPIO4/DIGMIC_DATA output is secondary word-clock for Audio Interface 1110: GPIO4/DIGMIC_DATA output is clock for the digital microphone 1111: Reserved
D1	R	X	GPIO4/DIGMIC_DATA Input Pin state as a GPI
D0	R/W	0	GPIO4/DIGMIC_DATA as general purpose output control 0: GPIO4/DIGMIC_DATA pin is driven to '0' in general purpose output mode 1: GPIO4/DIGMIC_DATA pin is driven to '1' in general purpose output mode

6.2.116 Page 0 / Register 124: GPIO5/DSD_CLK Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved. Write only default values
D5–D2	R/W	00 00	GPIO5/DSD_CLK Control 0000: GPIO5/DSD_CLK input/output disabled 0001: GPIO5/DSD_CLK input is used for secondary BCLK, secondary WCLK, secondary DIN or secondary ADC_WCLK input 0010: GPIO5/DSD_CLK is general purpose input (GPI) 0011: GPIO5/DSD_CLK is general purpose output 0100: GPIO5/DSD_CLK output is CLKOUT 0101: GPIO5/DSD_CLK output is INT1 (active high) 0110: GPIO5/DSD_CLK output is inverted INT1 (active low) 0111: GPIO5/DSD_CLK output is INT1 (open drain) 1000: GPIO5/DSD_CLK output is INT2 (active high) 1001: GPIO5/DSD_CLK output is inverted INT2 (active low) 1010: GPIO5/DSD_CLK output is INT2 (open drain) 1011: GPIO5/DSD_CLK output is ADC_WCLK for Audio Interface 1100: GPIO5/DSD_CLK output is secondary bit-clock for Audio Interface 1101: GPIO5/DSD_CLK output is secondary word-clock for Audio Interface 1110: GPIO5/DSD_CLK output is clock for the digital microphone 1111: GPIO5/DSD_CLK output is the DAC modulator clock (DSD_CLK)
D1	R	X	GPIO5/DSD_CLK Input Pin state as a GPI
D0	R/W	0	GPIO5/DSD_CLK as general purpose output control 0: GPIO5/DSD_CLK pin is driven to '0' in general purpose output mode 1: GPIO5/DSD_CLK pin is driven to '1' in general purpose output mode

6.2.117 Page 0 / Register 125: GPIO6/DSD_DATA Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved. Write only default values

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5–D2	R/W	00 00	GPIO6/DSD_DATA Control 0000: GPIO6/DSD_DATA input/output disabled 0001: GPIO6/DSD_DATA input is used for secondary BCLK, secondary WCLK, secondary DIN or secondary ADC_WCLK input 0010: GPIO6/DSD_DATA is general purpose input (GPI) 0011: GPIO6/DSD_DATA is general purpose output 0100: GPIO6/DSD_DATA output is CLKOUT 0101: GPIO6/DSD_DATA output is INT1 (active high) 0110: GPIO6/DSD_DATA output is inverted INT1 (active low) 0111: GPIO6/DSD_DATA output is INT1 (open drain) 1000: GPIO6/DSD_DATA output is INT2 (active high) 1001: GPIO6/DSD_DATA output is inverted INT2 (active low) 1010: GPIO6/DSD_DATA output is INT2 (open drain) 1011: GPIO6/DSD_DATA output is ADC_WCLK for Audio Interface 1100: GPIO6/DSD_DATA output is secondary bit-clock for Audio Interface 1101: GPIO6/DSD_DATA output is secondary word-clock for Audio Interface 1110: GPIO6/DSD_DATA output is clock for the digital microphone 1111: GPIO6/DSD_DATA output is Class D data output
D1	R	X	GPIO6/DSD_DATA Input Pin state as a GPI
D0	R/W	0	GPIO6/DSD_DATA as general purpose output control 0: GPIO6/DSD_DATA pin is driven to '0' in general purpose output mode 1: GPIO6/DSD_DATA pin is driven to '1' in general purpose output mode

6.2.118 Page 0 / Register 126: DOUT Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R	000	Reserved. Write only default values
D4	R/W	1	DOUT Bus Keep Control 0: DOUT bus keeper enabled 1: DOUT bus keeper disabled
D3–D1	R/W	001	DOUT Control 000: DOUT output disabled 001: DOUT is primary output for CODEC interface 010: DOUT is general purpose output 011: DOUT is CLKOUT divider output 100: DOUT output is INT1 (active high) 101: DOUT output is INT2 (active high) 110: DOUT output is secondary bit-clock for Audio Interface 111: DOUT output is secondary word-clock for Audio Interface
D0	R/W	0	DOUT as general purpose output control 0: DOUT pin is driven to '0' in general purpose output mode 1: DOUT pin is driven to '1' in general purpose output mode

6.2.119 Page 0 / Register 127: DIN Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R	0000 0	Reserved. Write only default values
D2–D1	R/W	01	
D0	R	X	DIN Control 00: DIN disabled (input buffer powered down) 01: DIN is used for DIN, secondary bit-clock, secondary word-clock or secondary DIG_MIC 10: DIN is general purpose input (GPI) 11: Reserved

6.2.120 Page 1 / Register 0: Page Select Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

6.2.121 Page 1 / Register 1-2: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved, Write only default values

6.2.122 Page 1 / Register 3: Left Bitstream Mode Enable

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left DAC Modulator Bitstream Mode Enable 0: Left DAC modulator in normal mode 1: Left DAC modulator in bitstream mode
D6–D0	R	000 0000	Reserved, Write only default values

6.2.123 Page 1 / Register 4: Right Bitstream Mode Enable

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Right DAC Modulator Bitstream Mode Enable 0: Right DAC modulator in normal mode 1: Right DAC modulator in bitstream mode
D6–D0	R	000 0000	Reserved, Write only default values

6.2.124 Page 1 / Register 5-9: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved, Write only default values

6.2.125 Page 1 / Register 10: ADC Channel Analog Configuration Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved, Write only default values
D6	R/W	0	ADC Input Common Mode Select 0: Set input common mode for ADC section to 0.9V 1: Set input common mode for ADC section to 0.75V
D5–D0	R	00 0000	Reserved, Write only default values

6.2.126 Page 1 / Register 11-50: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved, Write only default values

6.2.127 Page 1 / Register 51: ADC Channel Analog Configuration Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved, Write only default values
D6	R/W	0	EXT_MICBIAS control 0: EXT_MICBIAS powered down 1: EXT_MICBIAS powered up
D5–D4	R/W	00	EXT_MICBIAS Voltage Select Register 00: Set EXT_MICBIAS to 1.3V 01: Set EXT_MICBIAS to 1.5V 10: Set EXT_MICBIAS to 1.8V 11: Set EXT_MICBIAS to AVDD_BIAS voltage
D3	R	0	Reserved, Write only default values
D2	R/W	0	INT_MICBIAS control 0: INT_MICBIAS powered down 1: INT_MICBIAS powered up
D1–D0	R/W	00	INT_MICBIAS Voltage Select Register 00: Set INT_MICBIAS to 1.3V 01: Set INT_MICBIAS to 1.5V 10: Set INT_MICBIAS to 1.8V 11: Set INT_MICBIAS to AVDD_BIAS voltage

6.2.128 Page 1 / Register 52: Left MICPGA Positive Terminal Input Routing Configuration Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	LINEIN_L to Left MICPGA positive terminal selection 00: LINEIN_L is not routed to Left MICPGA 01: LINEIN_L is routed to Left MICPGA with 10K resistance 10: LINEIN_L is routed to Left MICPGA with 20K resistance 11: LINEIN_L is routed to Left MICPGA with 40K resistance
D5–D4	R/W	00	MIC1_P to Left MICPGA positive terminal selection 00: MIC1_P is not routed to Left MICPGA 01: MIC1_P is routed to Left MICPGA with 10K resistance 10: MIC1_P is routed to Left MICPGA with 20K resistance 11: MIC1_P is routed to Left MICPGA with 40K resistance
D3–D2	R/W	00	EXTMIC_P to Left MICPGA positive terminal selection 00: EXTMIC_P is not routed to Left MICPGA 01: EXTMIC_P is routed to Left MICPGA with 10K resistance 10: EXTMIC_P is routed to Left MICPGA with 20K resistance 11: EXTMIC_P is routed to Left MICPGA with 40K resistance
D1–D0	R	00	Reserved, Write only default values

6.2.129 Page 1 / Register 53: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved, Write only default values

6.2.130 Page 1 / Register 54: Left MICPGA Negative Terminal Input Routing Configuration Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	CM to Left MICPGA positive terminal selection 00: CM is not routed to Left MICPGA 01: CM is routed to Left MICPGA with 10K resistance 10: CM is routed to Left MICPGA with 20K resistance 11: CM is routed to Left MICPGA with 40K resistance
D5–D4	R/W	00	MIC1_M to Left MICPGA positive terminal selection 00: MIC1_M is not routed to Left MICPGA 01: MIC1_M is routed to Left MICPGA with 10K resistance 10: MIC1_M is routed to Left MICPGA with 20K resistance 11: MIC1_M is routed to Left MICPGA with 40K resistance
D3–D2	R/W	00	EXTMIC_M to Left MICPGA positive terminal selection 00: EXTMIC_M is not routed to Left MICPGA 01: EXTMIC_M is routed to Left MICPGA with 10K resistance 10: EXTMIC_M is routed to Left MICPGA with 20K resistance 11: EXTMIC_M is routed to Left MICPGA with 40K resistance
D1–D0	R	00	Reserved, Write only default values

6.2.131 Page 1 / Register 55: Right MICPGA Positive Terminal Input Routing Configuration Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	LINEIN_R to Right MICPGA positive terminal selection 00: LINEIN_R is not routed to Right MICPGA 01: LINEIN_R is routed to Right MICPGA with 10K resistance 10: LINEIN_R is routed to Right MICPGA with 20K resistance 11: LINEIN_R is routed to Right MICPGA with 40K resistance
D5–D4	R/W	00	MIC2_P to Right MICPGA positive terminal selection 00: MIC2_P is not routed to Right MICPGA 01: MIC2_P is routed to Right MICPGA with 10K resistance 10: MIC2_P is routed to Right MICPGA with 20K resistance 11: MIC2_P is routed to Right MICPGA with 40K resistance
D3–D2	R/W	00	EXTMIC_P to Right MICPGA positive terminal selection 00: EXTMIC_P is not routed to Right MICPGA 01: EXTMIC_P is routed to Right MICPGA with 10K resistance 10: EXTMIC_P is routed to Right MICPGA with 20K resistance 11: EXTMIC_P is routed to Right MICPGA with 40K resistance
D1–D0	R/W	00	Reserved, Write only default values

6.2.132 Page 1 / Register 56: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.133 Page 1 / Register 57: Right MICPGA Negative Terminal Input Routing Configuration Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	CM to Right MICPGA positive terminal selection 00: CM is not routed to Right MICPGA 01: CM is routed to Right MICPGA with 10K resistance 10: CM is routed to Right MICPGA with 20K resistance 11: CM is routed to Right MICPGA with 40K resistance
D5–D4	R/W	00	MIC2_M to Right MICPGA positive terminal selection 00: MIC2_M is not routed to Right MICPGA 01: MIC2_M is routed to Right MICPGA with 10K resistance 10: MIC2_M is routed to Right MICPGA with 20K resistance 11: MIC2_M is routed to Right MICPGA with 40K resistance
D3–D2	R/W	00	EXTMIC_M to Right MICPGA positive terminal selection 00: EXTMIC_M is not routed to Right MICPGA 01: EXTMIC_M is routed to Right MICPGA with 10K resistance 10: EXTMIC_M is routed to Right MICPGA with 20K resistance 11: EXTMIC_M is routed to Right MICPGA with 40K resistance
D1–D0	R/W	00	Reserved, Write only default values

6.2.134 Page 1 / Register 58: CM settings for unused inputs Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINEIN_L input setting when not used 0: LINEIN_L input is floating when not used 1: LINEIN_L input is weakly connected to CM when not used (if ADC L enabled)
D6	R/W	0	LINEIN_R input setting when not used 0: LINEIN_R input is floating when not used 1: LINEIN_R input is weakly connected to CM when not used (if ADC R is enabled)
D5	R/W	0	MIC1 input setting when not used 0: MIC1 input is floating when not used 1: MIC1 input is weakly connected to CM when not used (if ADC L is enabled)
D4	R/W	0	MIC2 input setting when not used 0: MIC2 input is floating when not used 1: MIC2 input is weakly connected to CM when not used (if ADC R is enabled)
D3	R/W	0	EXTMIC input setting when not used 0: EXTMIC input is floating when not used 1: EXTMIC input is weakly connected to CM when not used (if ADC L is enabled)
D2	R/W	0	EXTMIC input setting when not used Left ADC 0: EXTMIC input is floating when not used 1: EXTMIC input is weakly connected to CM when not used (if ADCR is enabled)
D1–D0	R	00	Reserved. Write only default values

6.2.135 Page 1 / Register 59: Left MICPGA Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	0: Left MICPGA Gain is enabled 1: Left MICPGA Gain is set to 0 dB

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D0	R/W	000 0000	Left MICPGA Volume Control 000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = 0.5 dB 000 0010: Volume Control = 1.0 dB … 101 1101: Volume Control = 46.5 dB 101 1110: Volume Control = 47.0 dB 101 1111: Volume Control = 47.5 dB 110 0000-111 1111: Reserved. Do not use

6.2.136 Page 1 / Register 60: Right MICPGA Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	0: Right MICPGA Gain is enabled 1: Right MICPGA Gain is set to 0 dB
D6–D0	R/W	000 0000	Right MICPGA Volume Control 000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = 0.5 dB 000 0010: Volume Control = 1.0 dB … 101 1101: Volume Control = 46.5 dB 101 1110: Volume Control = 47.0 dB 101 1111: Volume Control = 47.5 dB 110 0000-111 1111: Reserved. Do not use

6.2.137 Page 1 / Register 61: ADC Low Current Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	ADC ADMOD Driver Current Control 0: Normal Current Consumption Mode 1: Current consumption reduced by 40% 2: Current consumption reduced by 65% 3: Reserved
D5–D3	R/W	000	ADC ADMOD 0: Normal Current Consumption Mode Others: Current consumption reduced by TBD %
D2–D0	R/W	000	ADC REFBUF 0: Normal Current Consumption Mode Others: Current consumption reduced by TBD %

6.2.138 Page 1 / Register 62: ADC Analog Volume Control Flag Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D2	R	0000 00	Reserved. Write only default values
D1	R	0	Left Channel Analog Volume Control Flag 0: Applied Volume is not equal to Programmed Volume 1: Applied Volume is equal to Programmed Volume
D0	R	0	Right Channel Analog Volume Control Flag 0: Applied Volume is not equal to Programmed Volume 1: Applied Volume is equal to Programmed Volume

6.2.139 Page 1 / Register 63-127: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.140 Page 2 / Register 0: Page Select Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

6.2.141 Page 2 / Register 1-2: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved, Write only default values

6.2.142 Page 2 / Register 3: Power Control Overrides Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved, Write only default values
D5–D4	R/W	00	Oscillator Controls Override 00: Use oscillator automatic power controls (oscillator powers on only when needed) 01: Force oscillator to remain powered up (required when bits D1 or D0 in this register is set) 10: Force oscillator to remain off (ignore oscillator automatic power controls) 11: Reserved (do not use)
D3–D2	R	00	Reserved, Write only default values
D1	R/W	0	ADC automaic power sequencing clock control 0: Allow automatic ADC power sequencing 1: Force ADC power sequencing clock on (oscillator must also be running)
D0	R/W	0	DAC automaic power sequencing clock control 0: Allow automatic DAC power sequencing 1: Force DAC power sequencing clock on (oscillator must also be running)

6.2.143 Page 2 / Register 4-19: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved, Write only default values

6.2.144 Page 2 / Register 20: Detect Divider Enable Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Detect Divider 1 Enable Control First divider for the detect sampling rate. Uses the low power oscillator (nominal 1MHz). The output of this divider is cascaded to detect divider 2. 0: Disables detect divider 1 1: Enables detect divider 1
D6–D4	R	00	Reserved, Write only default values
D3	R/W	0	Detect Divider 2 Enable Control Second divider for the detect sampling rate. Uses the output of detect divider 1 as an input clock. Detect inputs are sampled based on the output of this divider. 0: Disables detect divider 2 1: Enables detect divider 2
D2–D0	R	000	Reserved, Write only default values

6.2.145 Page 2 / Register 21: Detect Divider 1 Count Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Detect Divider 1 count value 0: Divider 1 = 256 1: Divider 1 = 1 2: Divider 1 = 2 … 255: Divider 1 = 255

6.2.146 Page 2 / Register 22: Detect Divider 2 Count Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Detect Divider 2 count value 0: Divider 2 = 256 1: Divider 2 = 1 2: Divider 2 = 2 … 255: Divider 2 = 255

6.2.147 Page 2 / Register 23: Detect Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Continuous Detection Enable 0: disable continuous detection 1: enable continuous detection (used for interrupt driven detection)
D6	R	0	Reserved. Write only default values
D5	R/W	0	Software driven detect / detect status 0: read-back detection complete, OK to read detect value 1: read-back detection is in progress, detect value is not yet stable 1: write with self-clear: software initiated manual detect
D4–D0	R	0 0000	Output of detect SAR ADC prior to windowing. Useful for reading detect pin value.

6.2.148 Page 2 / Register 24: Short Pulse Detect Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Short Pulse Detect Enable 0: Short pulse detect disabled 1: Short pulse detect enabled
D6–D4	R	000	Stores the most recent debounced window number for the short pulse detect. The read value will change when the detect SAR value stablizes in a new window for a minimum period of (1uS * detect divider 1 * detect divider 2 * short pulse period) seconds (assuming a 1MHz nomimal LF oscillator rate)
D3	R	0	Reserved, Write only default values
D2–D0	R	000	Latched window value from bits D6-D4 of this register. The value is held when a short detect pulse interrupt is triggered and will remain held until the interrupt is cleared. It is useful for determing the window number that triggered the interrupt event.

6.2.149 Page 2 / Register 25: Long Pulse Detect Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Long Pulse Detect Enable 0: Long pulse detect disabled 1: Long pulse detect enabled
D6–D4	R	000	Stores the most recent debounced window number for the long pulse detect. The read value will change when the detect SAR value stablizes in a new window for a minimum period of (1uS * detect divider 1 * detect divider 2 * long pulse period) seconds (assuming a 1MHz nomimal LF oscillator rate)
D3	R	00	Reserved, Write only default values
D2–D0	R	000	Latched window value from bits D6-D4 of this register. The value is held when a long detect pulse interrupt is triggered and will remain held until the interrupt is cleared. It is useful for determing the window number that triggered the interrupt event.

6.2.150 Page 2 / Register 26: Short Pulse Period Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Used to calculate the minimum debounce period for the short pulse detect function. 1uS * detect divider 1 * detect divider 2 * this register determines the minimum pushbutton period that will be detected. Shorter button presses will be discarded and will not trigger an interrupt. Assumes a nominal LF oscillator rate.

6.2.151 Page 2 / Register 27: Log Pulse Period Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Used to calculate the minimum debounce period for the long pulse detect function. 1uS * detect divider 1 * detect divider 2 * this register determines the minimum pushbutton period that will be detected. Shorter button presses will be discarded and will not trigger an interrupt. Assumes a nominal LF oscillator rate.

6.2.152 Page 2 / Register 28: Detect Threshold 1 Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Detect Threshold Enable 0: disabled 1: enabled When enabled, the value in bits D4 - D0 of this register creates a window bounday for the raw 5-bit detect converter.
D6–D5	R	00	Reserved, Write only default values
D4–D0	R/W	0 0000	Window boundary value separating windows 0 and 1

6.2.153 Page 2 / Register 29: Detect Threshold 2 Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Detect Threshold Enable 0: disabled 1: enabled When enabled, the value in bits D4 - D0 of this register creates a window bounday for the raw 5-bit detect converter.
D6–D5	R	00	Reserved, Write only default values
D4–D0	R/W	0 0000	Window boundary value separating windows 1 and 2

6.2.154 Page 2 / Register 30: Detect Threshold 2 Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Detect Threshold Enable 0: disabled 1: enabled When enabled, the value in bits D4 - D0 of this register creates a window bounday for the raw 5-bit detect converter.
D6–D5	R	00	Reserved, Write only default values
D4–D0	R/W	0 0000	Window boundary value separating windows 2 and 3

6.2.155 Page 2 / Register 31: Detect Threshold 4 Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Detect Threshold Enable 0: disabled 1: enabled When enabled, the value in bits D4 - D0 of this register creates a window bounday for the raw 5-bit detect converter.
D6–D5	R	00	Reserved, Write only default values
D4–D0	R/W	0 0000	Window boundary value separating windows 3 and 4

6.2.156 Page 2 / Register 32: Detect Threshold 5 Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Detect Threshold Enable 0: disabled 1: enabled When enabled, the value in bits D4 - D0 of this register creates a window bounday for the raw 5-bit detect converter.
D6–D5	R	00	Reserved, Write only default values
D4–D0	R/W	0 0000	Window boundary value separating windows 4 and 5

6.2.157 Page 2 / Register 33: Detect Threshold 6 Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Detect Threshold Enable 0: disabled 1: enabled When enabled, the value in bits D4 - D0 of this register creates a window bounday for the raw 5-bit detect converter.
D6–D5	R	00	Reserved, Write only default values
D4–D0	R/W	0 0000	Window boundary value separating windows 5 and 6

6.2.158 Page 2 / Register 34: Detect Threshold 7 Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Detect Threshold Enable 0: disabled 1: enabled When enabled, the value in bits D4 - D0 of this register creates a window bounday for the raw 5-bit detect converter.
D6–D5	R	00	Reserved, Write only default values
D4–D0	R/W	0 0000	Window boundary value separating windows 6 and 7

6.2.159 Page 2 / Register 35: MIC Bias Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W		Mic Bias Control 0: Mic bias turned on only when detect is reading pin voltage 1: Mic bias always turned on
D6–D0	R	000 0000	Reserved, Write only default values

6.2.160 Page 2 / Register 36: HP Left/Right ground register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	HP Left/Right amp positive terminal ground register 0: Positive terminal of amp connected to GND_HP pin (must be tied to external ground) 1: Positive terminal of amp connected to HP_COM (can be tied to external resistor network for ground noise cancelation)

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D0	R	000 0000	Reserved. Write only default values

6.2.161 Page 2 / Register 37: DAC Power up Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left DAC Power Up register 0: Left Dac is not powered up 1: Left DAC is powered up
D6	R/W	0	Right DAC Power Up register 0: Right Dac is not powered up 1: Right DAC is powered up
D5–D0	R	00 0000	Reserved. Write only default values

6.2.162 Page 2 / Register 38: HP and REC output short circuit protection register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved, Write only default values
D5–D3	R/W	000	Reserved, Write only default values
D2	W	0	Short circuit enable register 0: Short circuit protection on HP and REC outputs is disabled 1: Short circuit protection on HP and REC outputs is enabled
D1	R/W	0	Short circuit control register 0: If short circuit protection is enabled, it will limit the max current to the load 1: If short circuit protection is enabled, it will power down the output when a short is dectected
D0	R/W	0	Reserved, Write only default values

6.2.163 Page 2 / Register 39: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	00	Reserved, Write only default values

6.2.164 Page 2 / Register 40: High Power Output Stage Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved, Write only default values
D5	R/W	0	LINEIN_L bypass control register 0: LINEIN_L bypass is disabled 1: LINEIN_L bypass is enabled
D4	R/W	0	Reserved, Write only default values
D3	R/W	0	LINEIN_R bypass control register 0: LINEIN_R bypass is disabled 1: LINEIN_R bypass is enabled
D2	R/W	0	Reserved, Write only default values

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D1–D0	R/W	00	Output soft-stepping control 00: ADC soft-stepping at one step per FS 01: ADC soft-stepping at one step per 2 Fs 10: ADC soft-stepping disabled 11: Reserved

6.2.165 Page 2 / Register 41: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved, Write only default values

6.2.166 Page 2 / Register 42: Output Driver Pop Reduction Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	Driver Power-on Time 0000: Driver power-on time = 0 usec 0001: Driver power-on time = 10 usec 0010: Driver power-on time = 100 usec 0011: Driver power-on time = 1 msec 0100: Driver power-on time = 10 msec 0101: Driver power-on time = 50 msec 0110: Driver power-on time = 100 msec 0111: Driver power-on time = 200 msec 1000: Driver power-on time = 400 msec 1001: Driver power-on time = 800 msec 1010: Driver power-on time = 2 sec 1011: Driver power-on time = 4 sec Others: Reserved
D3–D2	R/W	00	Driver Ramp-up Step Time 00: Driver Ramp-up step time = 0 msec 01: Driver Ramp-up step time = 1 msec 10: Driver Ramp-up step time = 2 msec 11: Driver Ramp-up step time = 4 msec
D1–D0	R	00	Reserved, Write only default values

6.2.167 Page 2 / Register 43-44: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved, Write only default values

6.2.168 Page 2 / Register 45: LINEIN_L to HPL Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINEIN_L to HPL Routing Control 0: LINEIN_L is not routed to HPL 1: LINEIN_L is routed to HPL

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB 000 0011: Volume Control = -1.5 dB 000 0100: Volume Control = -2.0 dB 000 0101: Volume Control = -2.5 dB 000 0110: Volume Control = -3.0 dB 000 0111: Volume Control = -3.5 dB 000 1000: Volume Control = -4.0 dB 000 1001: Volume Control = -4.5 dB 000 1010: Volume Control = -5.0 dB 000 1011: Volume Control = -5.5 dB 000 1100: Volume Control = -6.0 dB 000 1101: Volume Control = -6.5 dB 000 1110: Volume Control = -7.0 dB 000 1111: Volume Control = -7.5 dB 001 0000: Volume Control = -8.0 dB 001 0001: Volume Control = -8.5 dB 001 0010: Volume Control = -9.0 dB 001 0011: Volume Control = -9.5 dB 001 0100: Volume Control = -10.0 dB 001 0101: Volume Control = -10.5 dB 001 0110: Volume Control = -11.0 dB 001 0111: Volume Control = -11.5 dB 001 1000: Volume Control = -12.0 dB 001 1001: Volume Control = -12.5 dB 001 1010: Volume Control = -13.0 dB 001 1011: Volume Control = -13.5 dB 001 1100: Volume Control = -14.0 dB 001 1101: Volume Control = -14.5 dB 001 1110: Volume Control = -15.0 dB 001 1111: Volume Control = -15.5 dB 010 0000: Volume Control = -16.0 dB 010 0001: Volume Control = -16.5 dB 010 0010: Volume Control = -17.0 dB 010 0011: Volume Control = -17.5 dB 010 0100: Volume Control = -18.0 dB 010 0101: Volume Control = -18.6 dB 010 0110: Volume Control = -19.1 dB 010 0111: Volume Control = -19.6 dB 010 1000: Volume Control = -20.1 dB 010 1001: Volume Control = -20.6 dB 010 1010: Volume Control = -21.1 dB 010 1011: Volume Control = -21.6 dB 010 1100: Volume Control = -22.1 dB 010 1101: Volume Control = -22.6 dB 010 1110: Volume Control = -23.1 dB 010 1111: Volume Control = -23.6 dB 011 0000: Volume Control = -24.1 dB 011 0001: Volume Control = -24.6 dB 011 0010: Volume Control = -25.1 dB 011 0011: Volume Control = -25.6 dB 011 0100: Volume Control = -26.1 dB 011 0101: Volume Control = -26.6 dB 011 0110: Volume Control = -27.1 dB 011 0111: Volume Control = -27.6 dB 011 1000: Volume Control = -28.1 dB 011 1001: Volume Control = -28.6 dB 011 1010: Volume Control = -29.1 dB 011 1011: Volume Control = -29.6 dB 011 1100: Volume Control = -30.1 dB 011 1101: Volume Control = -30.6 dB 011 1110: Volume Control = -31.1 dB 011 1111: Volume Control = -31.6 dB 100 0000: Volume Control = -32.1 dB 100 0001: Volume Control = -32.6 dB 100 0010: Volume Control = -33.1 dB 100 0011: Volume Control = -33.6 dB

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
			100 0100: Volume Control = -34.1 dB 100 0101: Volume Control = -34.6 dB 100 0110: Volume Control = -35.1 dB 100 0111: Volume Control = -35.7 dB 100 1000: Volume Control = -36.1 dB 100 1001: Volume Control = -36.7 dB 100 1010: Volume Control = -37.1 dB 100 1011: Volume Control = -37.7 dB 100 1100: Volume Control = -38.2 dB 100 1101: Volume Control = -38.7 dB 100 1110: Volume Control = -39.2 dB 100 1111: Volume Control = -39.7 dB 101 0000: Volume Control = -40.2 dB 101 0001: Volume Control = -40.7 dB 101 0010: Volume Control = -41.2 dB 101 0011: Volume Control = -41.7 dB 101 0100: Volume Control = -42.2 dB 101 0101: Volume Control = -42.7 dB 101 0110: Volume Control = -43.2 dB 101 0111: Volume Control = -43.8 dB 101 1000: Volume Control = -44.3 dB 101 1001: Volume Control = -44.8 dB 101 1010: Volume Control = -45.2 dB 101 1011: Volume Control = -45.8 dB 101 1100: Volume Control = -46.2 dB 101 1101: Volume Control = -46.7 dB 101 1110: Volume Control = -47.4 dB 101 1111: Volume Control = -47.9 dB 110 0000: Volume Control = -48.2 dB 110 0001: Volume Control = -48.7 dB 110 0010: Volume Control = -49.3 dB 110 0011: Volume Control = -50.0 dB 110 0100: Volume Control = -50.3 dB 110 0101: Volume Control = -51.0 dB 110 0110: Volume Control = -51.4 dB 110 0111: Volume Control = -51.8 dB 110 1000: Volume Control = -52.2 dB 110 1001: Volume Control = -52.7 dB 110 1010: Volume Control = -53.7 dB 110 1011: Volume Control = -54.2 dB 110 1100: Volume Control = -55.3 dB 110 1101: Volume Control = -56.7 dB 110 1110: Volume Control = -58.3 dB 110 1111: Volume Control = -60.2 dB 111 0000: Volume Control = -62.7 dB 111 0001: Volume Control = -64.3 dB 111 0010: Volume Control = -66.2 dB 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.169 Page 2 / Register 46: PGA_L_L to HPL Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L to HPL Routing Control 0: PGA_L is not routed to HPL 1: PGA_L is routed to HPL
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.170 Page 2 / Register 47: DAC_L to HPL Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L to HPL Routing Control 0: DAC_L is not routed to HPL 1: DAC_L is routed to HPL
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.171 Page 2 / Register 48: LINEIN_R to HPL Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINEIN_R to HPL Routing Control 0: LINEIN_R is not routed to HPL 1: LINEIN_R is routed to HPL
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.172 Page 2 / Register 49: PGA_R to HPL Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R to HPL Routing Control 0: PGA_R is not routed to HPL 1: PGA_R is routed to HPL
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.173 Page 2 / Register 50: DAC_R to HPL Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R to HPL Routing Control 0: DAC_R is not routed to HPL 1: DAC_R is routed to HPL
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.174 Page 2 / Register 51: HPL Output Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	HPL Output Volume Control 0000: Volume = 0 dB 0001: Volume = 1 dB 0010: Volume = 2 dB 0011: Volume = 3 dB 0100: Volume = 4 dB 0101: Volume = 5 dB 0110: Volume = 6 dB 0111: Volume = 7 dB 1000: Volume = 8 dB 1001: Volume = 9 dB Others: Reserved
D3	R/W	0	HPL Mute Control 0: Muted 1: Not Muted
D2	R/W	1	HPL Power-down Mode 0: HPL is weakly driven to ground when powered down 1: HPL is high-Z when powered down

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D1	R/W	0	HPL Gain Status 0: Not all programmed gains to HPL have been applied yet 1: All programmed gains to HPL have been applied
D0	R/W	0	HPL Power Control 0: HPL is powered down 1: HPL is powered up

6.2.175 Page 2 / Register 52: LINEIN_L to HPR Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINEIN_L to HPR Routing Control 0: LINEIN_L is not routed to HPR 1: LINEIN_L is routed to HPR
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.176 Page 2 / Register 53: PGA_L_L to HPR Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L to HPR Routing Control 0: PGA_L is not routed to HPR 1: PGA_L is routed to HPR
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.177 Page 2 / Register 54: DAC_L to HPR Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L to HPR Routing Control 0: DAC_L is not routed to HPR 1: DAC_L is routed to HPR

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.178 Page 2 / Register 55: LINEIN_R to HPR Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINEIN_R to HPR Routing Control 0: LINEIN_R is not routed to HPR 1: LINEIN_R is routed to HPR
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.179 Page 2 / Register 56: PGA_R to HPR Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R to HPR Routing Control 0: PGA_R is not routed to HPR 1: PGA_R is routed to HPR
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.180 Page 2 / Register 57: DAC_R to HPR Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R to HPR Routing Control 0: DAC_R is not routed to HPR 1: DAC_R is routed to HPR

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.181 Page 2 / Register 58: HPR Output Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	HPR Output Volume Control 0000: Volume = 0 dB 0001: Volume = 1 dB 0010: Volume = 2 dB 0011: Volume = 3 dB 0100: Volume = 4 dB 0101: Volume = 5 dB 0110: Volume = 6 dB 0111: Volume = 7 dB 1000: Volume = 8 dB 1001: Volume = 9 dB Others: Reserved
D3	R/W	0	HPR Mute Control 0: Muted 1: Not Muted
D2	R/W	1	HPR Power-down Mode 0: HPR is weakly driven to ground when powered down 1: HPR is high-Z when powered down
D1	R	0	HPL Gain Status 0: Not all programmed gains to HPL have been applied yet 1: All programmed gains to HPL have been applied
D0	R/W	0	HPR Power Control 0: HPR is powered down 1: HPR is powered up

6.2.182 Page 2 / Register 59: LINEIN_L to RECL Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINEIN_L to RECL Routing Control 0: LINEIN_L is not routed to RECL 1: LINEIN_L is routed to RECL
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.183 Page 2 / Register 60: PGA_L to RECL Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L to RECL Routing Control 0: PGA_L is not routed to RECL 1: PGA_L is routed to RECL
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.184 Page 2 / Register 61: DAC_L to RECL Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L to RECL Routing Control 0: DAC_L is not routed to RECL 1: DAC_L is routed to RECL
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.185 Page 2 / Register 62: LINEIN_R to RECL Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINEIN_R to RECL Routing Control 0: LINEIN_R is not routed to RECL 1: LINEIN_R is routed to RECL
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.186 Page 2 / Register 63: PGA_R to RECL Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R to RECL Routing Control 0: PGA_R is not routed to RECL 1: PGA_R is routed to RECL
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.187 Page 2 / Register 64: DAC_R to RECL Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R to RECL Routing Control 0: DAC_R is not routed to RECL 1: DAC_R is routed to RECL
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.188 Page 2 / Register 65: RECL Output Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	RECL Output Volume Control 0000: Volume = 0 dB 0001: Volume = 1 dB 0010: Volume = 2 dB 0011: Volume = 3 dB 0100: Volume = 4 dB 0101: Volume = 5 dB 0110: Volume = 6 dB 0111: Volume = 7 dB 1000: Volume = 8 dB 1001: Volume = 9 dB Others: Reserved
D3	R/W	0	RECL Mute Control 0: Muted 1: Not Muted
D2	R/W	1	RECL Power-down Mode 0: RECL is weakly driven to ground when powered down 1: RECL is high-Z when powered down

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D1	R	0	RECL Gain Status 0: Not all programmed gains to RECL have been applied yet 1: All programmed gains to RECL have been applied
D0	R/W	0	RECL Power Control 0: RECL is powered down 1: RECL is powered up

6.2.189 Page 2 / Register 66: LINEIN_L to RECR Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINEIN_L to RECR Routing Control 0: LINEIN_L is not routed to RECR 1: LINEIN_L is routed to RECR
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.190 Page 2 / Register 67: PGA_L to RECR Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L to RECR Routing Control 0: PGA_L is not routed to RECR 1: PGA_L is routed to RECR
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.191 Page 2 / Register 68: DAC_L to RECR Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L to RECR Routing Control 0: DAC_L is not routed to RECR 1: DAC_L is routed to RECR

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.192 Page 2 / Register 69: LINEIN_R to RECR Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINEIN_R to RECR Routing Control 0: LINEIN_R is not routed to RECR 1: LINEIN_R is routed to RECR
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.193 Page 2 / Register 70: PGA_R to RECR Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R to RECR Routing Control 0: PGA_R is not routed to RECR 1: PGA_R is routed to RECR
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.194 Page 2 / Register 71: DAC_R to RECR Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R to RECR Routing Control 0: DAC_R is not routed to RECR 1: DAC_R is routed to RECR

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.195 Page 2 / Register 72: RECR Output Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	RECR Output Volume Control 0000: Volume = 0 dB 0001: Volume = 1 dB 0010: Volume = 2 dB 0011: Volume = 3 dB 0100: Volume = 4 dB 0101: Volume = 5 dB 0110: Volume = 6 dB 0111: Volume = 7 dB 1000: Volume = 8 dB 1001: Volume = 9 dB Others: Reserved
D3	R/W	0	RECR Mute Control 0: Muted 1: Not Muted
D2	R/W	1	RECR Power-down Mode 0: RECR is weakly driven to ground when powered down 1: RECR is high-Z when powered down
D1	R	0	RECR Gain Status 0: Not all programmed gains to RECR have been applied yet 1: All programmed gains to RECR have been applied
D0	R/W	0	RECR Power Control 0: RECR is powered down 1: RECR is powered up

6.2.196 Page 2 / Register 73-79: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	00	Reserved, Write only default values

6.2.197 Page 2 / Register 80: LINEIN_L to LINEOUT_LP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINEIN_L to LINEOUT_LP/M Routing Control 0: LINEIN_L is not routed to LINEOUT_LP/M 1: LINEIN_L is routed to LINEOUT_LP/M

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.198 Page 2 / Register 81: PGA_L to LINEOUT_LP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L to LINEOUT_LP/M Routing Control 0: PGA_L is not routed to LINEOUT_LP/M 1: PGA_L is routed to LINEOUT_LP/M
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.199 Page 2 / Register 82: DAC_L to LINEOUT_LP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L to LINEOUT_LP/M Routing Control 0: DAC_L is not routed to LINEOUT_LP/M 1: DAC_L is routed to LINEOUT_LP/M
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.200 Page 2 / Register 83: LINEIN_R to LINEOUT_LP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINEIN_R to LINEOUT_LP/M Routing Control 0: LINEIN_R is not routed to LINEOUT_LP/M 1: LINEIN_R is routed to LINEOUT_LP/M

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.201 Page 2 / Register 84: PGA_R to LINEOUT_LP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R to LINEOUT_LP/M Routing Control 0: PGA_R is not routed to LINEOUT_LP/M 1: PGA_R is routed to LINEOUT_LP/M
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.202 Page 2 / Register 85: DAC_R to LINEOUT_LP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R to LINEOUT_LP/M Routing Control 0: DAC_R is not routed to LINEOUT_LP/M 1: DAC_R is routed to LINEOUT_LP/M
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.203 Page 2 / Register 86: LINEOUT_LP/M Output Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	LINEOUT_LP/M Output Volume Control 0000: Volume = 0 dB 0001: Volume = 1 dB 0010: Volume = 2 dB 0011: Volume = 3 dB 0100: Volume = 4 dB 0101: Volume = 5 dB 0110: Volume = 6 dB 0111: Volume = 7 dB 1000: Volume = 8 dB 1001: Volume = 9 dB Others: Reserved
D3	R/W	0	LINEOUT_LP/M Mute Control 0: Muted 1: Not Muted
D2	R	0	Reserved, Write only default value
D1	R	0	LINEOUT_LP/M Gain Status 0: Not all programmed gains to LINEOUT_LP/M have been applied yet 1: All programmed gains to LINEOUT_LP/M have been applied
D0	R/W	0	LINEOUT_LP/M Power Control 0: LINEOUT_LP/M is powered down 1: LINEOUT_LP/M is powered up

6.2.204 Page 2 / Register 87: LINEIN_L to LINEOUT_RP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINEIN_L to LINEOUT_RP/M Routing Control 0: LINEIN_L is not routed to LINEOUT_RP/M 1: LINEIN_L is routed to LINEOUT_RP/M
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.205 Page 2 / Register 88: PGA_L to LINEOUT_RP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L to LINEOUT_RP/M Routing Control 0: PGA_L is not routed to LINEOUT_RP/M 1: PGA_L is routed to LINEOUT_RP/M

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.206 Page 2 / Register 89: DAC_L to LINEOUT_RP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L to LINEOUT_RP/M Routing Control 0: DAC_L is not routed to LINEOUT_RP/M 1: DAC_L is routed to LINEOUT_RP/M
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.207 Page 2 / Register 90: LINEIN_R to LINEOUT_RP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LINEIN_R to LINEOUT_RP/M Routing Control 0: LINEIN_R is not routed to LINEOUT_RP/M 1: LINEIN_R is routed to LINEOUT_RP/M
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.208 Page 2 / Register 91: PGA_R to LINEOUT_RP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R to LINEOUT_RP/M Routing Control 0: PGA_R is not routed to LINEOUT_RP/M 1: PGA_R is routed to LINEOUT_RP/M

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.209 Page 2 / Register 92: DAC_R to LINEOUT_RP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R to LINEOUT_RP/M Routing Control 0: DAC_R is not routed to LINEOUT_RP/M 1: DAC_R is routed to LINEOUT_RP/M
D6–D0	R/W	000 0000	000 0000: Volume Control = 0.0 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB … intermediate values identical to Page2/Register 45/D6-D0 … 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.2 dB 111 0101: Volume Control = -78.3 dB 111 0110: Volume Control = Mute Others: Reserved

6.2.210 Page 2 / Register 93: LINEOUT_RP/M Output Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	LINEOUT_RP/M Output Volume Control 0000: Volume = 0 dB 0001: Volume = 1 dB 0010: Volume = 2 dB 0011: Volume = 3 dB 0100: Volume = 4 dB 0101: Volume = 5 dB 0110: Volume = 6 dB 0111: Volume = 7 dB 1000: Volume = 8 dB 1001: Volume = 9 dB Others: Reserved
D3	R/W	0	LINEOUT_RP/M Mute Control 0: Muted 1: Not Muted
D2	R/W	1	Reserved, Write only default value
D1	R	0	LINEOUT_RP/M Gain Status 0: Not all programmed gains to LINEOUT_RP/M have been applied yet 1: All programmed gains to LINEOUT_RP/M have been applied
D0	R/W	0	LINEOUT_RP/M Power Control 0: LINEOUT_RP/M is powered down 1: LINEOUT_RP/M is powered up

6.2.211 Page 2 / Register 94: Module Power Status Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left DAC Power Status 0: Left DAC not fully powered up 1: Left DAC powered up
D6	R/W	0	Right DAC Power Status 0: Right DAC not fully powered up 1: Right DAC powered up
D5	R/W	0	Reserved
D4	R/W	0	LINEOUT_LP/M Power Status 0: LINEOUT_LP/M not fully powered up 1: LINEOUT_LP/M powered up
D3	R/W	0	LINEOUT_RP/M Power Status 0: LINEOUT_RP/MC not fully powered up 1: LINEOUT_RP/M powered up
D2	R/W	0	HPR Power Status 0: HPR not fully powered up 1: HPR powered up
D1	R/W	0	RECL Power Status 0: RECL not fully powered up 1: RECL powered up
D0	R	00	Reserved, Write only default values

6.2.212 Page 2 / Register 95-106: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	00	Reserved, Write only default values

6.2.213 Page 2 / Register 107: DAC Current Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	0	DAC Current Control Register 00: Nominal DAC Current 01: 1.5x Dac Current 10: 0.5x Dac current
D5–D0	R	00	Reserved, Write only default values

6.2.214 Page 2 / Register 108: Open Circuit Manual Read Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R	000	Reserved, Write only default values
D4	R/W	0	HPR Open Circuit Manual Read Control 0: Disabled 1: Enabled
D3	R/W	0	HPL Open Circuit Manual Read Control 0: Disabled 1: Enabled

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D2	R/W	0	RECL Open Circuit Manual Read Control 0: Disabled 1: Enabled
D1	R/W	0	RECL Open Circuit Manual Read Control 0: Disabled 1: Enabled
D0	R/W	0	Hook Open Circuit Manual Read Control 0: Disabled 1: Enabled

6.2.215 Page 2 / Register 109: Open Circuit Raw Status Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R	000	Reserved, Write only default values
D4	R	0	HPR Open Circuit Status 0: shorted 1: open
D3	R	0	HPL Open Circuit Status 0: shorted 1: open
D2	R	0	RECL Open Circuit Status 0: shorted 1: open
D1	R	0	RECR Open Circuit Status 0: shorted 1: open
D0	R	0	Hook Open Circuit Status 0: shorted 1: open

6.2.216 Page 2 / Register 110: Open Circuit Polling Enable Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R	000	Reserved, Write only default values
D4	R/W	0	HPR Open Circuit Polling Enable 0: disabled 1: enabled
D3	R/W	0	HPL Open Circuit Polling Enable 0: disabled 1: enabled
D2	R/W	0	RECL Open Circuit Polling Enable 0: disabled 1: enabled
D1	R/W	0	RECR Open Circuit Polling Enable 0: disabled 1: enabled
D0	R/W	0	Hook Open Circuit Polling Enable 0: disabled 1: enabled

6.2.217 Page 2 / Register 111: Open Circuit Interrupt Direction Status Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R	000	Reserved, Write only default values
D4	R	0	HPR Open Circuit Interrupt Direction A change in the HPR open circuit value can trigger a host interrupt on a rising or falling edge. Use this status bit to determine the direction of the interrupting event. 0: falling edge 1: rising edge
D3	R	0	HPL Open Circuit Interrupt Direction A change in the HPL open circuit value can trigger a host interrupt on a rising or falling edge. Use this status bit to determine the direction of the interrupting event. 0: falling edge 1: rising edge
D2	R	0	RECL Open Circuit Interrupt Direction A change in the RECL open circuit value can trigger a host interrupt on a rising or falling edge. Use this status bit to determine the direction of the interrupting event. 0: falling edge 1: rising edge
D1	R	0	RECR Open Circuit Interrupt Direction A change in the RECR open circuit value can trigger a host interrupt on a rising or falling edge. Use this status bit to determine the direction of the interrupting event. 0: falling edge 1: rising edge
D0	R	0	Hook Open Circuit Interrupt Direction A change in the Hook open circuit value can trigger a host interrupt on a rising or falling edge. Use this status bit to determine the direction of the interrupting event. 0: falling edge 1: rising edge

6.2.218 Page 2 / Register 112: Low Power Oscillator Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D1	R	0000 000	Reserved, Write only default values
D0	R/W	1	Low Power Oscillator Control 0: powered up 1: powered down

6.2.219 Page 2 / Register 113: PMU Configuration Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D2	R	0000 00	Reserved, Write only default values
D1	R/W	0	Charge Pump Clock Select 0: Charge pump uses MCLK 1: Charge pump uses BCLK
D0	R/W	0	Charge Pump Enable 0: Charge Pump Clock disabled 1: Charge Pump Clock enabled

6.2.220 Page 2 / Register 114: PMU Configuration Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 1011	Number of charge clock high cycles - 1 (used to set duty cycle on CP) 0000 0000: 1 cycle high 0000 0001: 2 cycles high … 1111 1111: 256 cycles high

6.2.221 Page 2 / Register 115: PMU Configuration Register 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 1011	Number of charge clock low cycles - 1 (used to set duty cycle on CP) 0000 0000: 1 cycle high 0000 0001: 2 cycles high … 1111 1111: 256 cycles high

6.2.222 Page 2 / Register 116: PMU Configuration Register 4

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R	0000 0	Reserved, Write only default values
D2	R/W	1	ADC VDD LDO Powerdown 0: ADC VDD LDO is in powerup 1: ADC VDO LDO is in powerdown
D1	R/W	1	DAC VSS LDO Powerdown 0: DAC VSS LDO is in powerup 1: DAC VSS LDO is in powerdown
D0	R/W	1	DAC VDD LDO Powerdown 0: DAC VDD LDO is in powerup 1: DAC VDD LDO is in powerdown

6.2.223 Page 2 / Register 117: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved, Write only default values

6.2.224 Page 2 / Register 118: PMU Configuration Register 5

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R	0000 0	Reserved, Write only default values
D2	R/W	1	ADC VDD LDO current limit 0: Don't current limit (set to Imax=30mA) 1: Current limit (set to Imax=5mA)
D1	R/W	1	DAC VSS LDO current limit 0: Don't current limit (set to Imax=-300mA) 1: Current limit (set to Imax=-50mA)

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D0	R/W	1	DAC VDD LDO current limit 0: Don't current limit (set to Imax=300mA) 1: Current limit (set to Imax=50mA)

6.2.225 Page 2 / Register 119: PMU Configuration Register 6

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	ADC VDD LDO open loop gain 0: Lower open loop gain LDO 1: High open loop gain LDO
D6–D4	R/W	000	ADC VDD LDO output voltage 000: Set ADC VDD LDO to 1.75V 001: Set ADC VDD LDO to 1.65V 010: Set ADC VDD LDO to 1.5V 011: Set ADC VDD LDO to 1.4V 1xx: Reserved
D3	R/W	0	LDO Bandgap powerdown 0: LDO Bandgap powered up 1: LDO Bandgap powered down
D2	R/W	0	Short circuit protection for DAC VDD LDO 0: Short circuit protection for DAC VDD LDO enabled 1: Short circuit protection for DAC VDD LDO disabled (current limit, reg 118 also disabled)
D1	R/W	0	Short circuit protection for DAC VSS LDO 0: Short circuit protection for DAC VSS LDO enabled 1: Short circuit protection for DAC VSS LDO disabled (current limit, reg 118 also disabled)
D0	R/W	0	Short circuit protection for ADC VDD LDO 0: Short circuit protection for ADC VDD LDO enabled 1: Short circuit protection for ADC VDD LDO disabled (current limit, reg 118 also disabled)

6.2.226 Page 2 / Register 120: PMU Configuration Register 7

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC VDD LDO open loop gain 0: Lower open loop gain LDO 1: High open loop gain LDO
D6–D4	R/W	000	DAC VDD LDO output voltage 000: Set DAC VDD LDO to 1.4V 001: Set DAC VDD LDO to 1.5V 010: Set DAC VDD LDO to 1.65V 011: Set DAC VDD LDO to 1.75V 1xx: Reserved
D3	R	0	Reserved, Write only default values
D2–D0	R/W	000	DAC VSS LDO output voltage 000: Set DAC VSS LDO to -1.4V 001: Set DAC VSS LDO to -1.5V 010: Set DAC VSS LDO to -1.65V 011: Set DAC VSS LDO to -1.75V 1xx: Reserved

6.2.227 Page 2 / Register 121: PMU Configuration Register 8

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R	0000	Reserved, Write only default values
D3–D0	R/W	0111	TRIMPMU bits 0000: Trim all LDO outputs +4.6% 0100: Trim all LDO outputs ..... 0101: Trim all LDO outputs +1.4% 0110: Trim all LDO outputs +0.7% 0111: Trim all LDO outputs +0% 1001: Trim all LDO outputs -0.8% 1010: Trim all LDO outputs .... 1111: Trim all LDO outputs -6.4%

6.2.228 Page 2 / Register 122: PMU Configuration Register 9

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Headphone nominal current settings 00: Nominal current 01: 1/2 Nominal current (recommended setting for low power) 10: 1/3 Nominal current 11: 1/4 Nominal current (recommended for ultimate low power, performance degraded)
D5–D4	R/W	00	Rec nominal current settings 00: Nominal current 01: 1/2 Nominal current (recommended setting for low power) 10: 1/3 Nominal current 11: 1/4 Nominal current (recommended for ultimate low power, performance degraded)
D3–D2	R/W	00	Line out nominal current settings 00: Nominal current 01: 1/2 Nominal current (recommended setting for low power) 10: 1/3 Nominal current 11: 1/4 Nominal current (recommended for ultimate low power, performance degraded)
D1–D0	R/W	00	IV amp nominal current settings 00: Nominal current 01: 1/2 Nominal current (recommended setting for low power) 10: 1/3 Nominal current 11: 1/4 Nominal current (recommended for ultimate low power, performance degraded)

6.2.229 Page 2 / Register 123: PMU Configuration Register 10

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D2	R	0000 00	Reserved, Write only default values
D1–D0	R/W	00	DAC Bias Voltage Register 00: Nominal Dac bias voltages 01: Reduced Dac bias voltages for use with very low DAC VDD 1x: Reserved

6.2.230 Page 2 / Register 124-127: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved, Write only default values

6.3 ADC Coefficients

Table 6-2. ADC Coefficients

Coef No	Page No	Base Register	Base Register + 0	Base Register + 1
C1	4	2	Coef(15:8)	Coef(7:0)
C2	4	4	Coef(15:8)	Coef(7:0)
…	…	…	…	…
C63	4	126	Coef(15:8)	Coef(7:0)
C65	5	2	Coef(15:8)	Coef(7:0)
…	…	…	…	…
C127	5	126	Coef(15:8)	Coef(7:0)

6.4 ADC Defaults

Table 6-3. Default Values of ADC Coefficients

ADC Coefficient	Default Value at Reset
C1	0117H
C2	0117H
C3	7DD3H
C4	7FFFH
C5-C6	0000H
C7	7FFFH
C8-C11	0000H
C12	7FFFH
C13-C16	0000H
C17	7FFFH
C18-C21	0000H
C22	7FFFH
C23-C26	0000H
C27	7FFFH
C28-C35	0000H
C36	7FFFH
C37-C38	0000H
C39	7FFFH
C40-C43	0000H
C44	7FFFH
C45-C48	0000H
C49	7FFFH
C50-C53	0000H
C54	7FFFH
C55-C58	0000H
C59	7FFFH
C60-C63	0000H
C65-C127	0000H

6.5 DAC Coefficients A+B

Table 6-4. DAC Coefficient Buffer-A Map

Coef No	Page No	Base Register	Base Register + 0	Base Register + 1
C1	8	2	Coef(15:8)	Coef(7:0)
C2	8	4	Coef(15:8)	Coef(7:0)
…	…	…	…	…
C63	8	126	Coef(15:8)	Coef(7:0)
C65	9	2	Coef(15:8)	Coef(7:0)
…	…	…	…	…
C127	9	126	Coef(15:8)	Coef(7:0)
C129	10	2	Coef(15:8)	Coef(7:0)
…	…	…	…	…
C191	10	126	Coef(15:8)	Coef(7:0)
C193	11	2	Coef(15:8)	Coef(7:0)
…	…	…	…	…
C255	11	126	Coef(15:8)	Coef(7:0)

Table 6-5. DAC Coefficient Buffer-B Map

Coef No	Page No	Base Register	Base Register + 0	Base Register + 1
C1	12	2	Coef(15:8)	Coef(7:0)
C2	12	4	Coef(15:8)	Coef(7:0)
…	…	…	…	…
C63	12	126	Coef(15:8)	Coef(7:0)
C65	13	2	Coef(15:8)	Coef(7:0)
…	…	…	…	…
C127	13	126	Coef(15:8)	Coef(7:0)
C129	14	2	Coef(15:8)	Coef(7:0)
…	…	…	…	…
C191	14	126	Coef(15:8)	Coef(7:0)
C193	15	2	Coef(15:8)	Coef(7:0)
…	…	…	…	…
C255	15	126	Coef(15:8)	Coef(7:0)

6.6 DAC Defaults

Table 6-6. Default Values of DAC Coefficients in Buffers A and B

DAC Coefficient	Default Value at Reset
C1	7FFFH
C2-C5	0000H
C6	7FFFH
C7-C10	0000H
C11	7FFFH
C12-C15	0000H
C16	7FFFH
C17-C20	0000H
C21	7FFFH
C22-C25	0000H

Table 6-6. Default Values of DAC Coefficients in Buffers A and B (continued)

C26	7FFFH
C27-C32	0000H
C33	7FFFH
C34-C37	0000H
C38	7FFFH
C39-C42	0000H
C43	7FFFH
C44-C47	0000H
C48	7FFFH
C49-C52	0000H
C53	7FFFH
C54-C57	0000H
C58	7FFFH
C59-C63	0000H
C65	7FFFH
C56-C67	0000H
C68	7FFFH
C69-C70	0000H
C71	7FF7H
C72	8009H
C73	7FEDH
C74-C75	0011H
C76	7FDEH
C77-C255	0000H

6.7 ADC miniDSP Instructions

Table 6-7. ADC miniDSP Instruction Map

Instr No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2
0	32	2	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
1	32	5	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
31	32	95	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
32	33	2	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
63	33	95	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
64	34	2	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
95	34	95	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
96	35	2	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
127	35	95	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
128	36	2	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
159	36	95	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
160	37	2	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
191	37	95	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)

Table 6-7. ADC miniDSP Instruction Map (continued)

192	38	2	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
223	38	95	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
224	39	2	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
255	39	95	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
256	40	2	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
287	40	95	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
288	41	2	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
319	41	95	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
320	42	2	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
351	42	95	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
352	43	2	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
383	43	95	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
384	44	2	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
415	44	95	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
416	45	2	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
447	45	95	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
448	46	2	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
479	46	95	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
480	47	2	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
510	47	92	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)
511	47	95	0000 : Instr(19:16)	Instr(15:8)	Instr(7:0)

6.8 DAC miniDSP Instructions

Table 6-8. DAC miniDSP Instruction Map

Instr No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2
0	64	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
1	64	5	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
31	64	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
32	65	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
63	65	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
64	66	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
95	66	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
96	67	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…

Table 6-8. DAC miniDSP Instruction Map (continued)

127	67	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
128	68	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
159	68	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
160	69	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
191	69	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
192	70	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
223	70	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
224	71	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
255	71	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
256	72	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
287	72	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
288	73	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
319	73	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
320	74	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
351	74	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
352	75	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
383	75	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
384	76	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
415	76	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
416	77	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
447	77	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
448	78	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
479	78	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
480	79	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
511	79	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
512	80	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
543	80	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
544	81	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
575	81	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
576	82	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
607	82	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
608	83	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…

Table 6-8. DAC miniDSP Instruction Map (continued)

639	83	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
640	84	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
671	84	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
672	85	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
703	85	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
704	86	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
735	86	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
736	87	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
767	87	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
768	88	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
799	88	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
800	89	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
831	89	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
832	90	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
863	90	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
864	91	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
895	91	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
896	92	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
927	92	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
928	93	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
959	93	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
960	94	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
991	94	95	Instr(23:16)	Instr(15:8)	Instr(7:0)
992	95	2	Instr(23:16)	Instr(15:8)	Instr(7:0)
…	…	…	…	…	…
1023	95	95	Instr(23:16)	Instr(15:8)	Instr(7:0)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May, 2009) to A Revision ..... **Page**

- Changed ESD rating for *HOOK* pin; moved from 1.5 kV to 1 kV 6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV320AIC36IZQER	NRND	BGA MICROSTAR JUNIOR	ZQE	80	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	AIC36	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

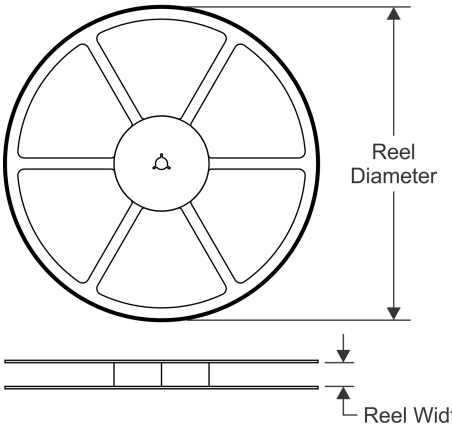
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

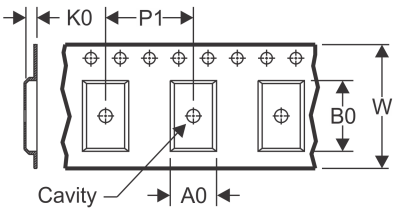
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

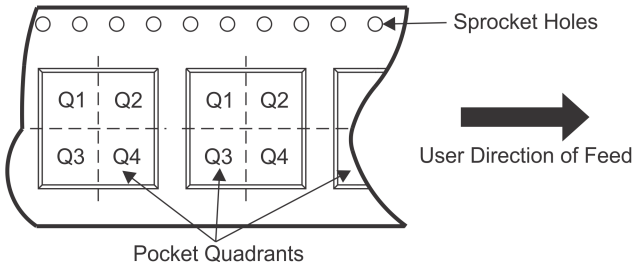


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

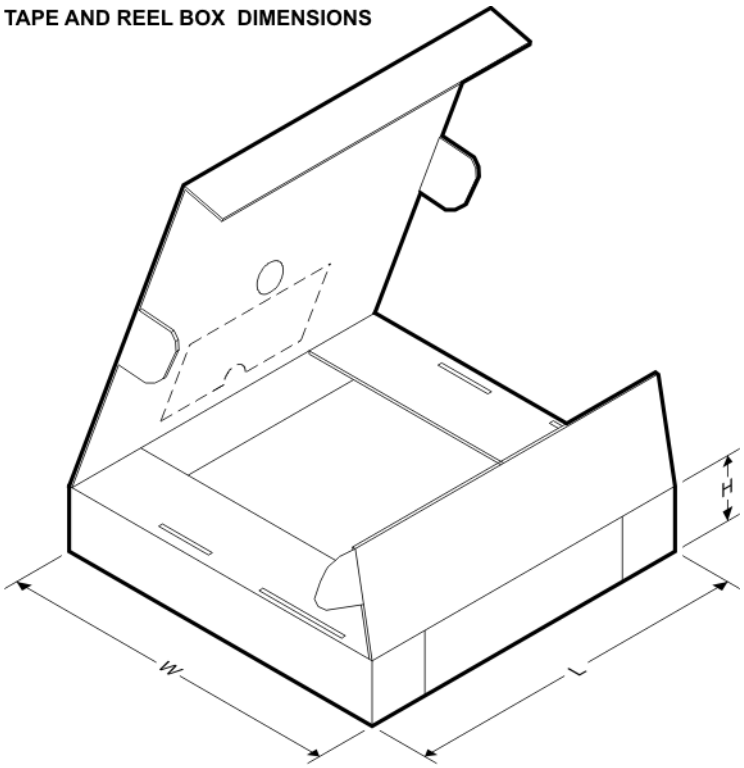
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV320AIC36IZQER	BGA MICROSTAR JUNIOR	ZQE	80	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1

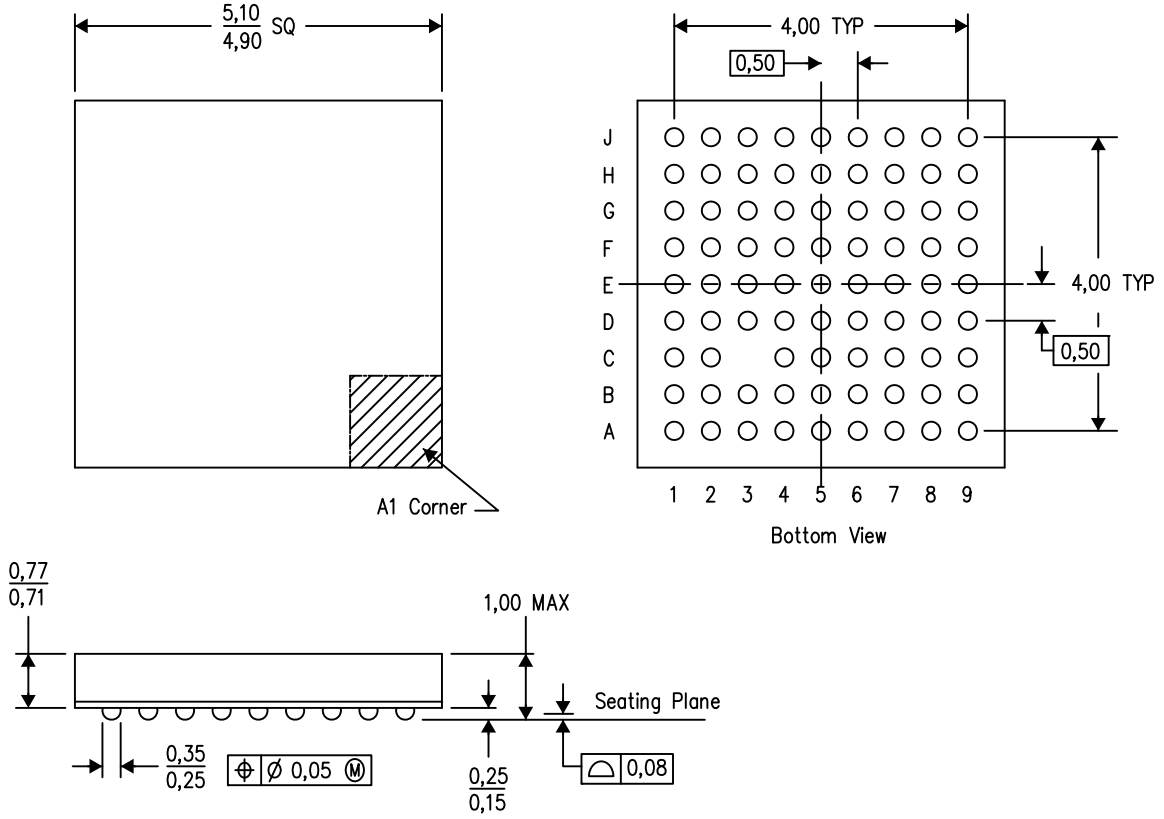
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV320AIC36IZQER	BGA MICROSTAR JUNIOR	ZQE	80	2500	350.0	350.0	43.0

ZQE (S–PBGA–N80) PLASTIC BALL GRID ARRAY



4204334-6/G 09/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This is a Pb–free solder ball design.

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