

Low-Voltage 1:10 LVPECL/HSTL With Selectable Input Clock Driver

Check for Samples: [CDCLVP110](#)

FEATURES

- Distributes One Differential Clock Input Pair LVPECL/HSTL to 10 Differential LVPECL Clock Outputs
- Fully Compatible With LVECL/LVPECL/HSTL
- Single Supply Voltage Required, $\pm 3.3\text{-V}$ or $\pm 2.5\text{-V}$ Supply
- Selectable Clock Input Through CLK_SEL
- Low-Output Skew (Typ 15 ps) for Clock-Distribution Applications
- VBB Reference Voltage Output for Single-Ended Clocking
- Available in a 32-Pin LQFP Package
- Frequency Range From DC to 3.5 GHz
- Pin-to-Pin Compatible With MC100 Series EP111, ES6111, LVEP111, PTN1111

DESCRIPTION

The CDCLVP110 clock driver distributes one differential clock pair of either LVPECL or HSTL (selectable) input, (CLK0, CLK1) to ten pairs of differential LVPECL clock (Q0, Q9) outputs with minimum skew for clock distribution. The CDCLVP110 can accept two clock sources into an input multiplexer. The CLK0 input accepts either LVECL/LVPECL input signals, while CLK1 accepts an HSTL input signal when operated under LVPECL conditions. The CDCLVP110 is specifically designed for driving 50- Ω transmission lines.

The VBB reference voltage output is used if single-ended input operation is required. In this case the VBB pin should be connected to $\overline{\text{CLK0}}$ and bypassed to GND via a 10-nF capacitor.

However, for high-speed performance up to 3.5 GHz, the differential mode is strongly recommended.

The CDCLVP110 is characterized for operation from -40°C to 85°C .

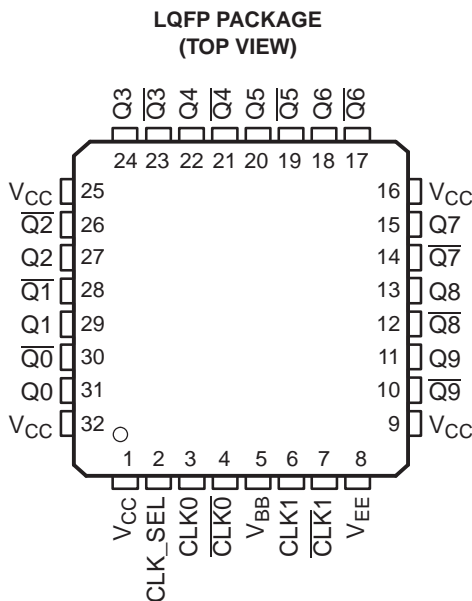


Table 1. FUNCTION TABLE

CLK_SEL	ACTIVE CLOCK INPUT
0	CLK0, $\overline{\text{CLK0}}$
1	CLK1, $\overline{\text{CLK1}}$



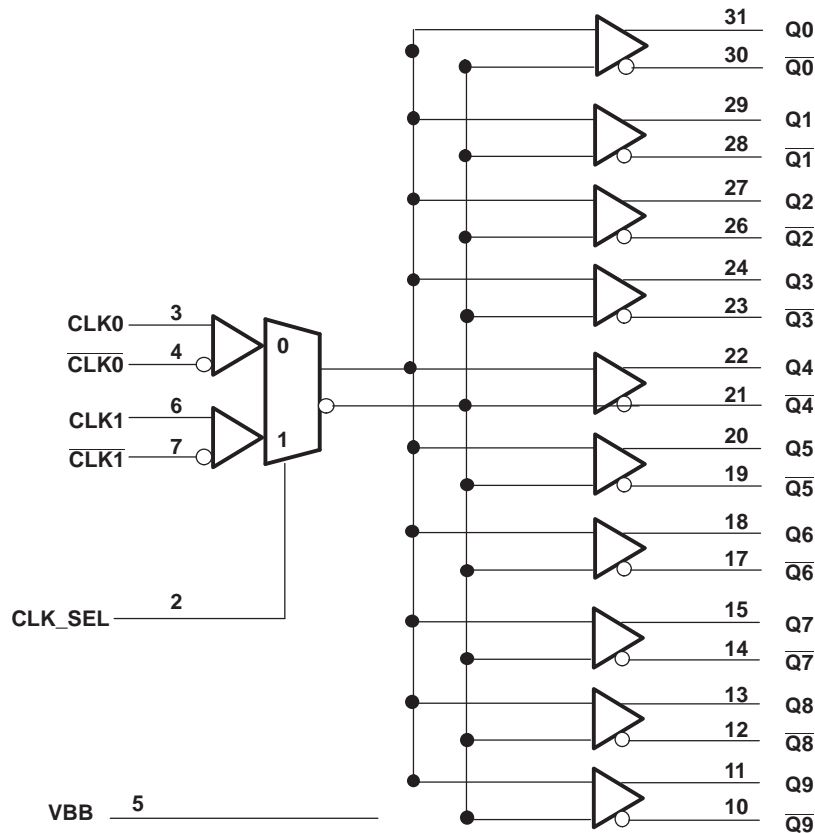
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

CDCLVP110

SCAS683D – JUNE 2002 – REVISED JANUARY 2011

www.ti.com


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
CLK_SEL	2	Clock select. Used to select between CLK0 and CLK1 input pairs.
CLK0, $\overline{\text{CLK0}}$	3, 4	Differential LVECL/LVPECL input pair
CLK1, $\overline{\text{CLK1}}$	6, 7	Differential HSTL input pair
Q [9:0]	11, 13, 15, 18, 20, 22, 24, 27, 29, 31	LVECL/LVPECL clock outputs, these outputs provide low-skew copies of CLKn.
$\overline{\text{Q}}$ [9:0]	10, 12, 14, 17, 19, 21, 23, 26, 28, 30	LVECL/LVPECL complementary clock outputs, these outputs provide copies of $\overline{\text{CLKn}}$.
V _{BB}	5	Reference voltage output for single-ended input operation
V _{CC}	1, 9, 16, 25, 32	Supply voltage
V _{EE}	8	Device ground or negative supply voltage in ECL mode

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

		VALUE	UNIT
V _{CC}	Supply voltage	–0.3 to 4.6	V
V _I	Input voltage	–0.3 to V _{CC} + 0.5	V
V _O	Output voltage	–0.3 to V _{CC} + 0.5	V
I _{IN}	Input current	±20	mA
V _{EE}	Negative supply voltage	–0.3 to 4.6	V
I _{BB}	Sink/source current	–1 to 1	mA
I _O	DC output current	–50	mA
T _{stg}	Storage temperature range	–65 to 150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage (relative to V _{EE})	2.375	2.5/3.3	3.8	V
T _A ⁽¹⁾	Operating free-air temperature	–40		85	°C

- (1) Operating junction temperature affects device lifetime. The continuous operation junction temperature is recommended to be at max 110°C. The device ac and dc parameters are specified up to 85°C ambient temperature. See the *PCB Layout Guidelines for CDCLVP110* application note, literature number SCAA057 for more details.

PACKAGE THERMAL IMPEDANCE

		TEST CONDITIONS	MIN	MAX	UNIT
Θ _{JA}	Thermal resistance junction to ambient ⁽¹⁾	0 LFM		74	°C/W
		150 LFM		66	°C/W
		250 LFM		64	°C/W
		500 LFM		61	°C/W
Θ _{JC}	Thermal resistance junction to case			39	°C/W

- (1) According to JESD 51-7 standard.

LVECL DC ELECTRICAL CHARACTERISTICS

V_{supply}: V_{CC} = 0 V, V_{EE} = –2.375 V to –3.8 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
I _{EE}	Supply internal current Absolute value of current	–40°C	40	78	mA		
		25°C	45	82			
		85°C	48	85			
I _{CC}	Output and internal supply current All outputs terminated 50 Ω to V _{CC} – 2 V	–40°C		343	mA		
		25°C		370			
		85°C		380			
I _{IN}	Input current	–40°C, 25°C, 85°C		150	μA		
V _{BB}	Internally generated bias voltage	For V _{EE} = –3 to –3.8 V, I _{BB} = –0.2 mA	–40°C, 25°C, 85°C	–1.45	–1.3	–1.15	V
		V _{EE} = –2.375 to –2.75 V, I _{BB} = –0.2 mA	–40°C, 25°C, 85°C	–1.4	–1.25	–1.1	
V _{IH}	High-level input voltage (CLK_SEL)	–40°C, 25°C, 85°C	–1.165	–0.88	V		
V _{IL}	Low-level input voltage (CLK_SEL)	–40°C, 25°C, 85°C	–1.81	–1.475	V		
V _{INPP}	Input amplitude (CLK0, CLK0)	Difference of input 9 V _{IH} –V _{IL} , See Note ⁽¹⁾	–40°C, 25°C, 85°C	0.5	1.3	V	
V _{CM}	Common-mode voltage (CLK0, CLK0)	Cross point of input 9 average (V _{IH} , V _{IL})	–40°C, 25°C, 85°C	V _{EE} + 0.975	–0.3	V	
V _{OH}	High-level output voltage	I _{OH} = –21 mA	–40°C	–1.26	–0.9	V	
		25°C	–1.2	–0.9			
		85°C	–1.15	–0.9			

- (1) V_{INPP} minimum and maximum is required to maintain ac specifications, actual device function tolerates a minimum V_{INPP} of 100 mV.

CDCLVP110

SCAS683D – JUNE 2002 – REVISED JANUARY 2011

www.ti.com

LVECL DC ELECTRICAL CHARACTERISTICS (continued)

Vsupply: $V_{CC} = 0\text{ V}$, $V_{EE} = -2.375\text{ V to } -3.8\text{ V}$

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	$I_{OL} = -5\text{ mA}$	-40°C	-1.85		-1.5	V	
			25°C	-1.85		-1.45		
			85°C	-1.85		-1.4		
V_{OD}	Differential output voltage swing	Terminated with 50 Ω to $V_{CC} - 2\text{ V}$, See Figure 3	-40°C, 25°C, 85°C	600			V	

LVPECL/HSTL DC ELECTRICAL CHARACTERISTICS

Vsupply: $V_{CC} = 2.375\text{ V to } 3.8\text{ V}$, $V_{EE} = 0\text{ V}$

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{EE}	Supply internal current	Absolute value of current	-40°C	40		78	mA	
			25°C	45		82		
			85°C	48		85		
I_{CC}	Output and internal supply current	All outputs terminated 50 Ω to $V_{CC} - 2\text{ V}$	-40°C			343	mA	
			25°C			370		
			85°C			380		
I_{IN}	Input current		-40°C, 25°C, 85°C			150	μA	
V_{BB}	Internally generated bias voltage	$V_{EE} = -3\text{ to } -3.8\text{ V}$, $I_{BB} = -0.2\text{ mA}$	-40°C, 25°C, 85°C	$V_{CC} - 1.45$	$V_{CC} - 1.3$	$V_{CC} - 1.15$	V	
		$V_{EE} = -2.375\text{ to } -2.75\text{ V}$, $I_{BB} = -0.2\text{ mA}$	-40°C, 25°C, 85°C	$V_{CC} - 1.4$	$V_{CC} - 1.25$	$V_{CC} - 1.1$		
V_{IH}	High-level input voltage (CLK_SEL)		-40°C, 25°C, 85°C	$V_{CC} - 1.165$		$V_{CC} - 0.88$	V	
V_{IL}	Low-level input voltage (CLK_SEL)		-40°C, 25°C, 85°C	$V_{CC} - 1.81$		$V_{CC} - 1.475$	V	
V_{INPP}	Input amplitude (CLK0, CLK0)	Difference of input 9 $V_{IH} - V_{IL}$, see Note (1)	-40°C, 25°C, 85°C	0.5		1.3	V	
V_{IC}	Common-mode voltage (CLK0, CLK0)	Cross point of input 9 average (V_{IH} , V_{IL})	-40°C, 25°C, 85°C	0.975		$V_{CC} - 0.3$	V	
V_{ID}	Differential input voltage (CLK1, CLK1)	Difference of input $V_{IH} - V_{IL}$, See Note (1)	-40°C, 25°C, 85°C	0.4		1.9	V	
$V_{I(x)}$	Input crossover voltage (CLK1, CLK1)	Cross point of input 9 average (V_{IH} , V_{IL})	-40°C, 25°C, 85°C	0.68		0.9	V	
V_{OH}	High-level output voltage	$I_{OH} = -21\text{ mA}$	-40°C	$V_{CC} - 1.26$		$V_{CC} - 0.9$	V	
			25°C	$V_{CC} - 1.2$		$V_{CC} - 0.9$		
			85°C	$V_{CC} - 1.15$		$V_{CC} - 0.9$		
V_{OL}	Low-level output voltage	$I_{OL} = -5\text{ mA}$	-40°C	$V_{CC} - 1.85$		$V_{CC} - 1.5$	V	
			25°C	$V_{CC} - 1.85$		$V_{CC} - 1.45$		
			85°C	$V_{CC} - 1.85$		$V_{CC} - 1.4$		
V_{OD}	Differential output voltage swing	Terminated with 50 Ω to $V_{CC} - 2\text{ V}$, See Figure 4	-40°C, 25°C, 85°C	600			mV	

(1) V_{INPP} minimum and maximum is required to maintain ac specifications, actual device function tolerates a minimum V_{INPP} of 100 mV.

AC ELECTRICAL CHARACTERISTICS

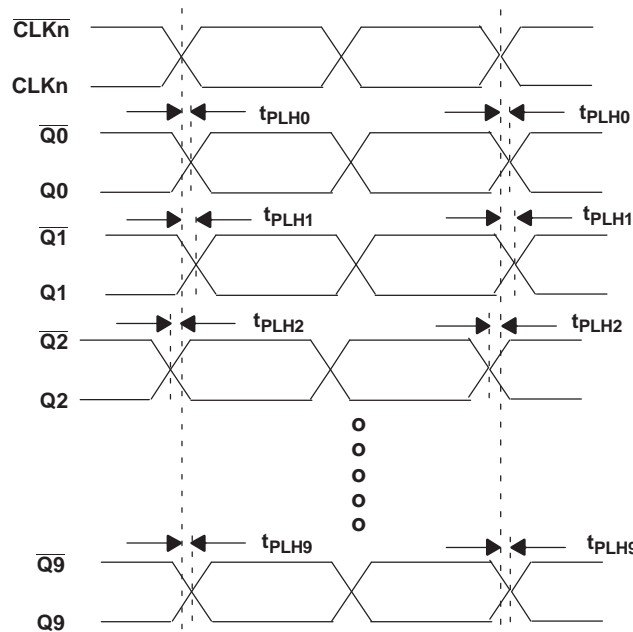
V_{supply}: V_{CC} = 2.375 V to 3.8 V, V_{EE} = 0 V or LVECL/LVPECL input V_{CC} = 0 V, V_{EE} = -2.375 V to -3.8 V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{pd}	Differential propagation delay CLK0, CLK0 to all Q0, Q0... Q9, Q9	Input condition: V _{CM} = 1 V, V _{PP} = 0.5 V	-40°C, 25°C, 85°C	230		350	ps
t _{sk(pp)}	Part-to-part skew	See Note B and Figure 1	-40°C, 25°C, 85°C			70	ps
t _{sk(o)}	Output-to-output skew	See Note A and Figure 1	-40°C, 25°C, 85°C		15	30	ps
t _(JITTER)	Cycle-to-cycle RMS jitter		-40°C, 25°C, 85°C			< 1	ps
f _(max)	Maximum frequency	Functional up to 3.5 GHz, timing specifications apply at 1 GHz, see Figure 3	-40°C, 25°C, 85°C			3500	MHz
t _r /t _f	Output rise and fall time (20%, 80%)		-40°C, 25°C, 85°C	100		200	ps

HSTL INPUT

V_{supply}: V_{CC} = 2.375 V to 3.8 V, V_{EE} = 0 V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{pd}	Differential propagation delay CLK0, CLK0 to all Q0, Q0... Q9, Q9	Input condition: V _x = 0.68 V, V _{diff} = 0.4 V	-40°C, 25°C, 85°C	290		370	ps
t _{sk(pp)}	Part-to-part skew	See Note B and Figure 1	-40°C, 25°C, 85°C			70	ps
t _{sk(o)}	Output to output skew	See Note A and Figure 1	-40°C, 25°C, 85°C		10	30	ps
t _(JITTER)	Cycle-to-cycle RMS jitter		-40°C, 25°C, 85°C			< 1	ps
f _(max)	Maximum frequency	Functional up to 3.5 GHz, timing specifications apply at 1 GHz, See Figure 4	-40°C, 25°C, 85°C			3500	MHz
t _r /t _f	Output rise and fall time (20%, 80%)		-40°C, 25°C, 85°C	100		200	ps



- A. Output skew is calculated as the greater of: The difference between the fastest and the slowest t_{PLHn} ($n = 0, 1, \dots, 9$) or the difference between the fastest and the slowest t_{pHLn} ($n = 0, 1, \dots, 9$).
- B. Part-to-part skew, is calculated as the greater of: The difference between the fastest and the slowest t_{PLHn} ($n = 0, 1, \dots, 9$) across multiple devices or the difference between the fastest and the slowest t_{pHLn} ($n = 0, 1, \dots, 9$) across multiple devices.

Figure 1. Waveform for Calculating Both Output and Part-to-Part Skew

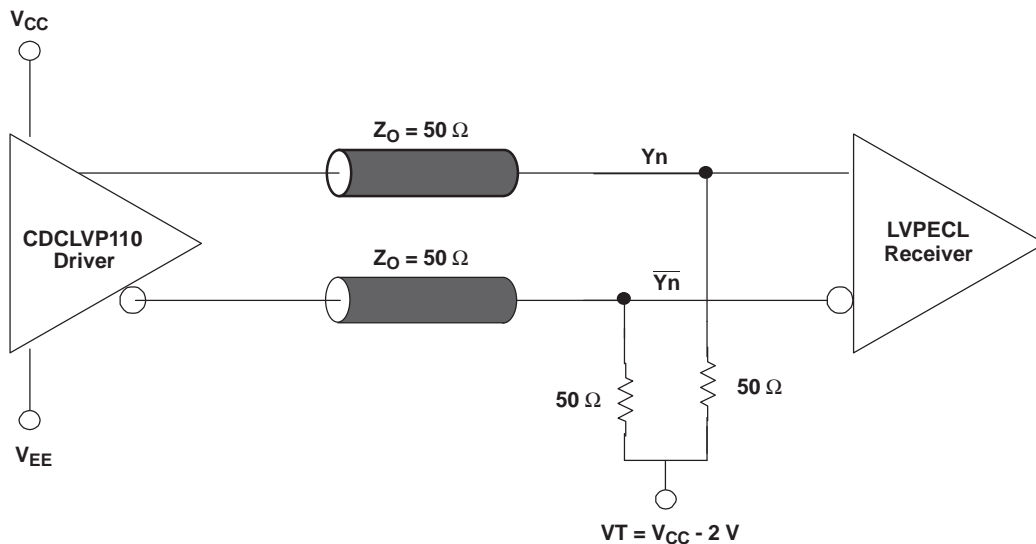


Figure 2. Typical Termination for Output Driver (See the Interfacing Between LVPECL, LVDS, and CML Application Note, Literature Number SCAA056)

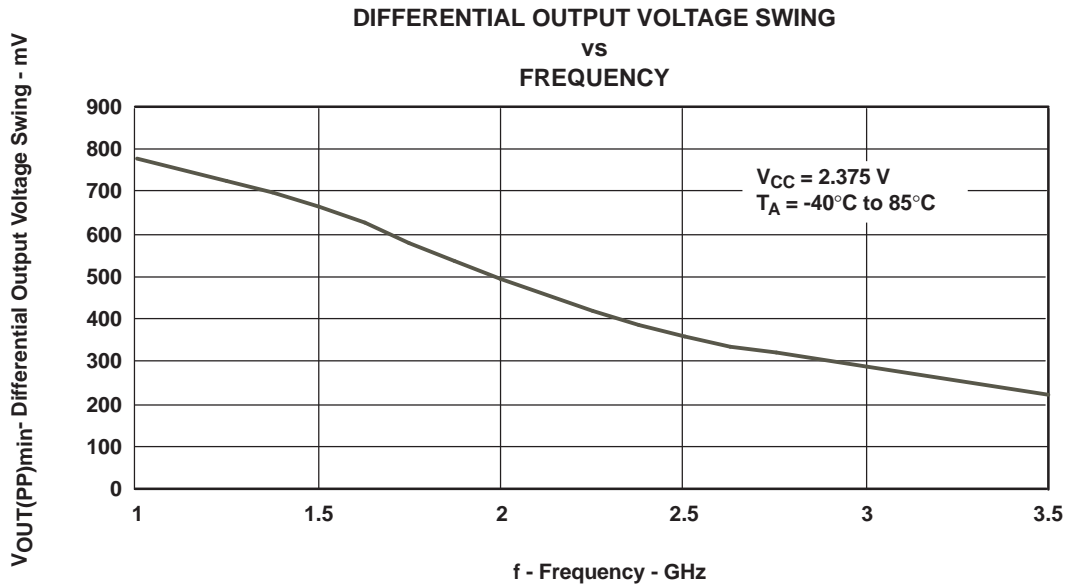


Figure 3. LVPECL Input Using CLK0 Pair, VCM = 1 V, VIN_{diff} = 0.5 V

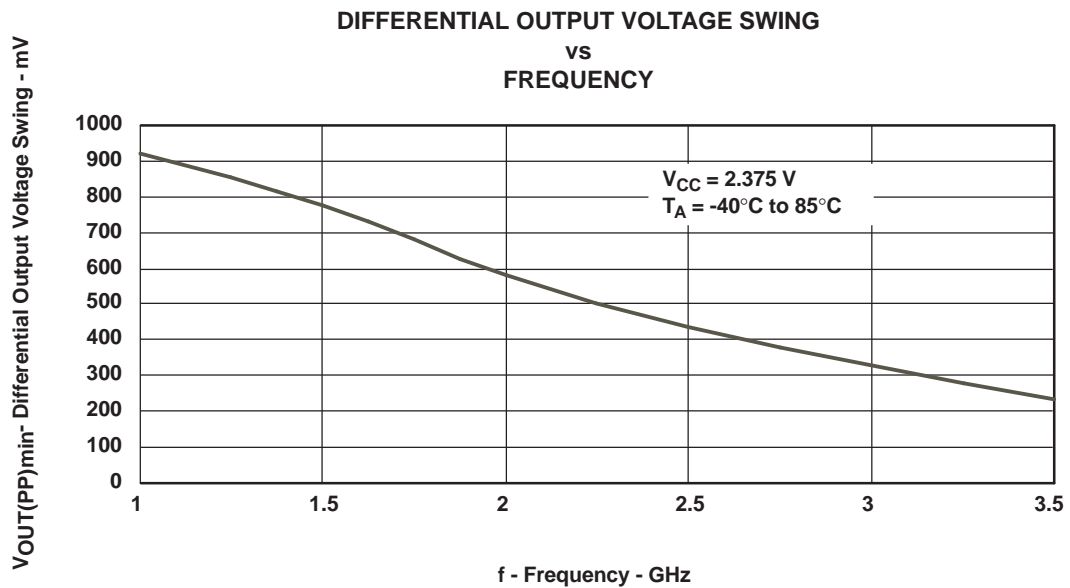


Figure 4. HSTL Input Using CLK1 Pair, VCM = 0.68 V, VIN_{diff} = 0.4 V

REVISION HISTORY

Changes from Revision A (August 2002) to Revision B	Page
• Changed PACKAGE THERMAL IMPEDANCE max values	3
• Deleted I_{IN} test condition	3
• Deleted I_{IN} test condition	4
<hr/>	
Changes from Revision B (January 2010) to Revision C	Page
• Changed LVECL DC spec for V_{BB} ($V_{EE} = -3$ to -3.8 V) from 3 rows to 1 row and added TYP value.	3
• Changed LVECL DC spec for V_{BB} ($V_{EE} = -2.375$ to -2.75 V); MIN value from -1.38 V to -1.4 V, MAX from -1.16 V to -1.1 V, and added TYP value of -1.25 V	3
• Changed LVECL/HSTL DC spec for V_{BB} ($V_{EE} = -3$ to -3.8 V) from 3 rows to 1 row and added TYP value.	4
• Changed LVECL/HSTL DC spec for V_{BB} ($V_{EE} = -2.375$ to -2.75 V); MIN value from $V_{CC} -1.38$ V to $V_{CC} -1.4$ V; MAX from $V_{CC} -1.16$ V to $V_{CC} -1.1$ V; and added TYP value of $V_{CC} -1.25$ V	4
<hr/>	
Changes from Revision C (January 2011) to Revision D	Page
• Changed V_{CM} spec from $V_{EE}+1$ to $V_{EE}+0.975$	3
• Changed V_{IC} spec from 1 to 0.975	4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCLVP110MVFR	ACTIVE	LQFP	VF	32	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCLVP110	Samples
CDCLVP110MVFRG4	ACTIVE	LQFP	VF	32	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCLVP110	Samples
CDCLVP110VF	ACTIVE	LQFP	VF	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCLVP110	Samples
CDCLVP110VFG4	ACTIVE	LQFP	VF	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCLVP110	Samples
CDCLVP110VFR	ACTIVE	LQFP	VF	32	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCLVP110	Samples
CDCLVP110VFRG4	ACTIVE	LQFP	VF	32	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCLVP110	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



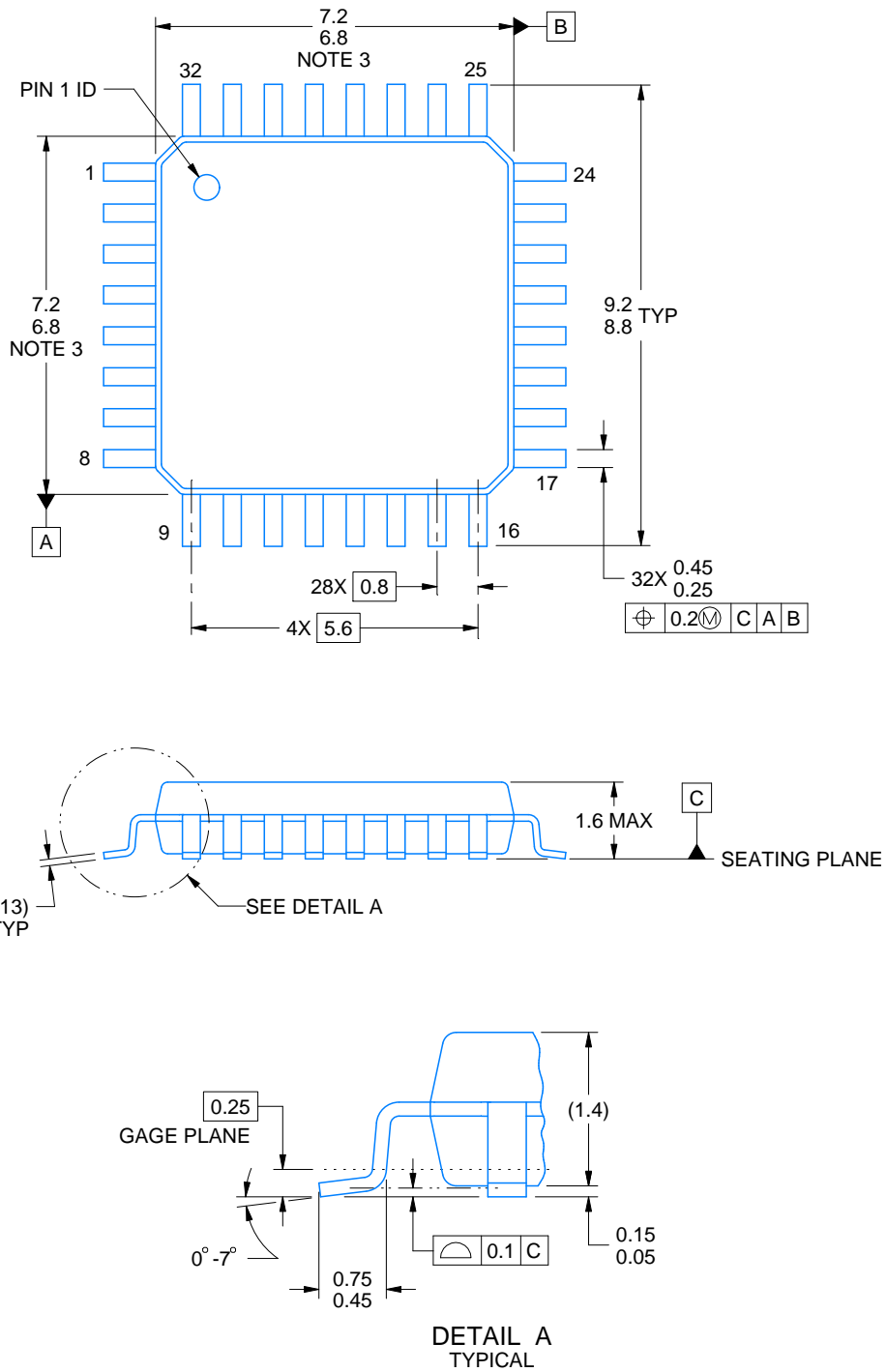
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVP110MVFR	LQFP	VF	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q1
CDCLVP110VFR	LQFP	VF	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVP110MVFR	LQFP	VF	32	1000	367.0	367.0	38.0
CDCLVP110VFR	LQFP	VF	32	1000	367.0	367.0	38.0



4219769/A 04/2019

NOTES:

PowerPAD is a trademark of Texas Instruments.

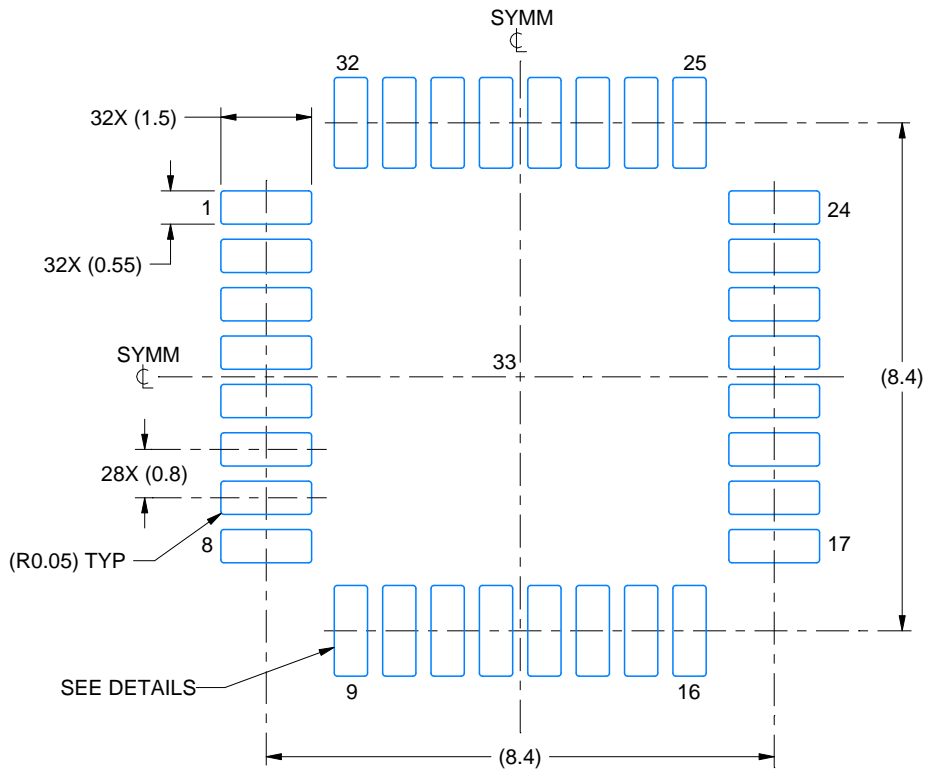
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

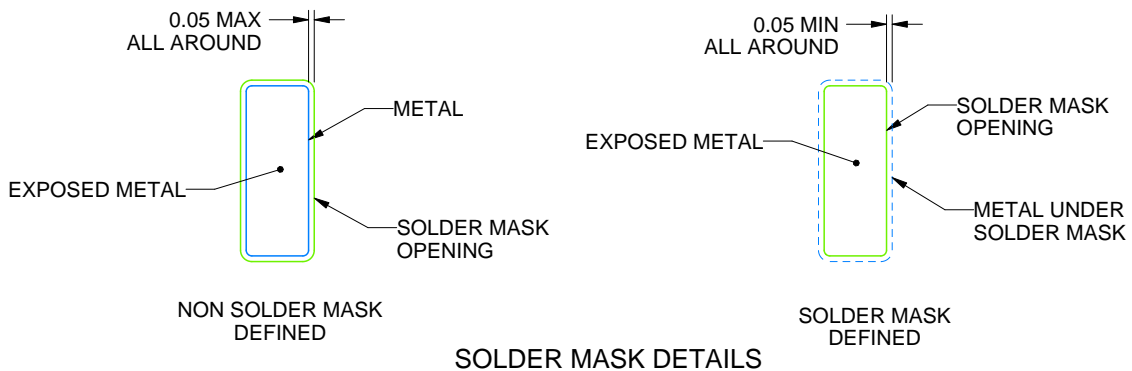
VF0032A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4219769/A 04/2019

NOTES: (continued)

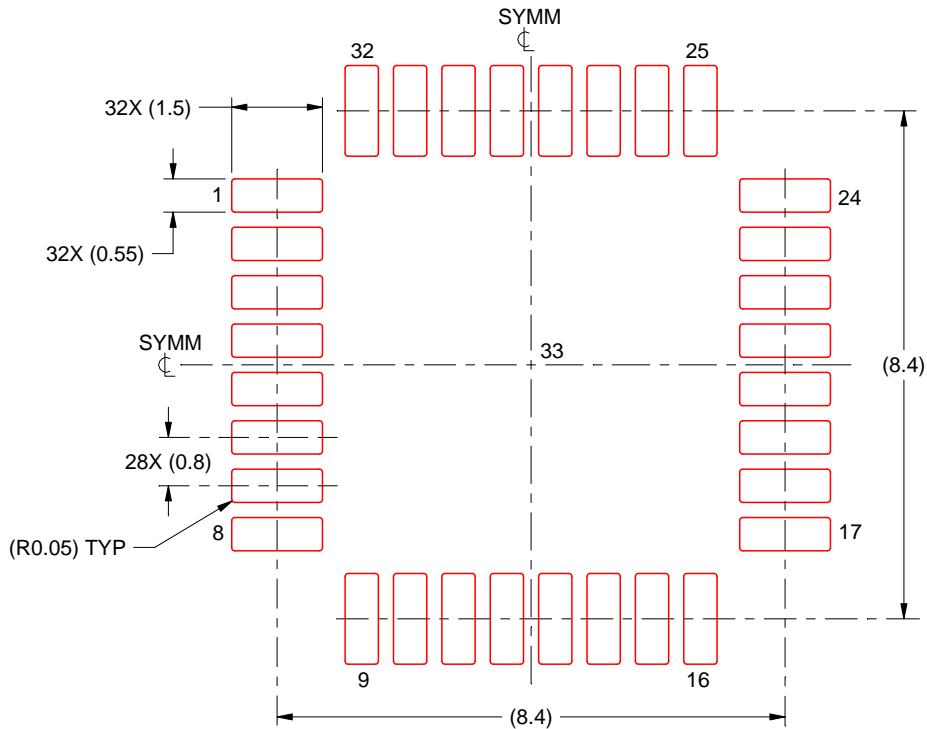
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

VF0032A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
SCALE:8X

4219769/A 04/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated