19-4439; Rev 0; 5/09

EVALUATION KIT AVAILABLE

Quad PCI Express Equalizer/Redriver

MAX4950

General Description

The MAX4950 PCI Express (PCIe®) quad equalizer/redriver operates from a single +3.3V supply. This device improves signal integrity at the receiver through programmable input equalization and programmable redrive circuitry. The output circuitry reestablishes de-emphasis lost on the board, compensating for circuit board loss. This device permits optimal placement of key PCIe components and longer runs of stripline, microstrip, or cable.

The MAX4950 contains four identical buffers capable of equalizing differential signals at data rates up to 5GT/s, and features electrical idle and receiver detection on each channel. The MAX4950 is ideal for use with PCIe Gen I (2.5GT/s) and Gen II (5.0GT/s) data rates and features a power-saving mode.

The MAX4950 is available in a small, lead-free, 42-pin (3.5mm x 9.0mm) TQFN package for optimal layout and minimal space requirements. The board traces are flow-through for ease of layout. The MAX4950 is specified over the 0°C to +70°C operating temperature range.

Applications

Servers

Industrial PCs

Test Equipment

Desktop Computers

Laptop Computers (for External Video Cards)

Communications Switchers

Storage Area Networks

PCIe is a registered trademark of PCI-SIG Corp.

Features

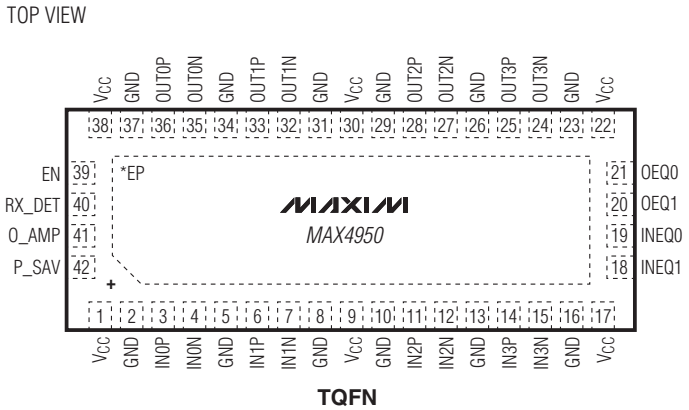
- **Single +3.3V Supply Operation**
- **Generation I (2.5GT/s) and Generation II (5.0GT/s) Capable**
- **Return Loss:**
  ≥ 10dB (f ≤ 1.25GHz)
  ≥ 8dB (f ≤ 2.5GHz)
- **Very Low Latency**
  280ps Propagation Delay
- **Individual Lane Detection**
- **Low Lane-to-Lane Skew: ±50ps**
- **Total Jitter ≤ 35psP-P at BER = 10^{-12}**
- **Three-Level-Programmable Input Equalization**
- **Three-Level-Programmable Output Deemphasis**
- **On-Chip 50Ω Input/Output Terminations**
- **±2kV Human Body Model (HBM) Protection on All Pins**
- **Space-Saving, 3.5mm x 9.0mm, TQFN Packaging**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4950CTO+	0°C to +70°C	42 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Pin Configuration



TQFN

*CONNECT EXPOSED PAD (EP) TO GND.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)
V_{CC} .....-0.3V to +4.0V
All Other Pins (Note 1).....-0.3V to (V_{CC} + 0.3V)
Continuous Current IN_P and IN_N.....±30mA
Peak Current IN_P and IN_N (pulsed for 1µs, 1% duty cycle).....±100mA
Continuous Power Dissipation (T_A = +70°C)
42-Pin TQFN (derate 34.5mW/°C above +70°C) 2759mW
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 2)
42-Pin TQFN.....2.0°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 2)
42-Pin TQFN.....29.0°C/W
Operating Temperature Range.....0°C to +70°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: All I/O pins are clamped by internal diodes.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, C_{CL} = 75nF coupling capacitor on each output, R_L = 50Ω resistor on each output, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC PERFORMANCE							
Power-Supply Range	V_{CC}			3.0		3.6	V
Supply Current	I_{CC}	O_AMP = GND, P_SAV = GND (Note 4)	EN = V_{CC}		262	328	mA
			EN = GND		100	125	
Differential Input Impedance	$Z_{RX-DIFF-DC}$	DC		80	100	120	Ω
Differential Output Impedance	$Z_{TX-DIFF-DC}$	DC		80	100	120	Ω
Common-Mode Resistance to GND	$Z_{RX-HIGH-IMP-DC-POS}$	V_{IN_P} = V_{IN_N} = 0 to +200mV, input terminations not powered		50			kΩ
Common-Mode Resistance to GND	$Z_{RX-HIGH-IMP-DC-NEG}$	V_{IN_P} = V_{IN_N} = -150mV to 0, input terminations not powered		1			kΩ
Common-Mode Resistance to GND, Input Terminations Powered	Z_{RX-DC}	DC		40	50	60	Ω
Output Short-Circuit Current	$I_{TX-SHORT}$	Single-ended				90	mA
Common-Mode Delta Between Active and Idle States	$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	O_AMP = GND				100	mV
DC Output Offset During Active State	$V_{TX-CM-DC-LINE-DELTA}$	$\lvert(V_{OUT_P} + V_{OUT_N})\rvert$				25	mV
DC Output Offset During Electrical Idle	$V_{TX-IDLE-DIFF-DC}$	$\lvert(V_{OUT_P} + V_{OUT_N})\rvert$				10	mV
AC PERFORMANCE (Note 5)							
Differential Input Return Loss	$RL_{RX-DIFF}$	f = 0.05GHz to 1.25GHz		10			dB
		f = 1.25GHz to 2.5GHz		8			
Common-Mode Input Return Loss	RL_{RX-CM}	f = 0.05GHz to 2.5GHz		6			dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, C_{CL} = 75nF coupling capacitor on each output, R_L = 50Ω resistor on each output, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Output Return Loss	$RL_{TX-DIFF}$	f = 0.05GHz to 1.25GHz	10			dB
		f = 1.25GHz to 2.5GHz	8			
Common-Mode Output Return Loss	RL_{TX-CM}	f = 0.05GHz to 2.5GHz	6			dB
Redriver Operation Differential Input Signal Range	$V_{RX-DIFF-PP}$	f = 0.05GHz to 2.5GHz	120		1200	mV_{P-P}
Full-Swing Differential Output Voltage (No Deemphasis)	$V_{TX-DIFF-PP}$	2 x l(V_{OUT_P} + V_{OUT_N})l, O_AMP = GND; f = 500MHz	800	1000	1200	mV_{P-P}
Differential Output Voltage (Low Swing, No Deemphasis)	$V_{TX-DIFF-PP-LOW}$	2 x l(V_{OUT_P} + V_{OUT_N})l, O_AMP = V_{CC}; f = 500MHz	600	750	900	mV_{P-P}
Output Deemphasis Ratio, 0dB	$V_{TX-DE-RATIO-0dB}$	f = 2.5GHz, OEQ1 = GND, OEQ0 = GND; see Table 3		0		dB
Output Deemphasis Ratio, 3.5dB	$V_{TX-DE-RATIO-3.5dB}$	f = 2.5GHz, OEQ1 = GND, OEQ0 = V_{CC}; see Table 3		3.5		dB
Output Deemphasis Ratio, 6dB	$V_{TX-DE-RATIO-6dB}$	f = 2.5GHz, OEQ1 = V_{CC}, OEQ0 = V_{CC} or GND; see Table 3		6		dB
Input Equalization, 0dB	$V_{RX-EQ-0dB}$	f = 2.5GHz, INEQ1 = GND, INEQ0 = GND; see Table 2 (Note 6)		0		dB
Input Equalization, 3.5dB	$V_{RX-EQ-3.5dB}$	f = 2.5GHz, INEQ1 = GND, INEQ0 = V_{CC}; see Table 2 (Note 6)		3.5		dB
Input Equalization, 6dB	$V_{RX-EQ-6dB}$	f = 2.5GHz, INEQ1 = V_{CC}, INEQ0 = V_{CC} or GND; see Table 2 (Note 6)		6		dB
Output Common-Mode Voltage Swing Peak-to-Peak	$V_{TX-CM-AC-PP}$	Max(V_{OUT_P} + V_{OUT_N})/2 – Min(V_{OUT_P} + V_{OUT_N})/2			100	mV_{P-P}
Propagation Delay	T_{PD}	f = 2.5GHz, K28.7 pattern	160	280	400	ps
Rise/Fall Time	$T_{TX-RISE-FALL}$	(Note 7)	30			ps
Rise/Fall Time Mismatch	$T_{TX-RF-MISMATCH}$	(Note 7)			20	ps
Output Skew Same Pair	T_{SK}	f = 2.5GHz		10	15	ps
Output Skew Lane to Lane	T_{SKL}	f = 2.5GHz	-50		50	ps
Deterministic Jitter	$T_{TX-DJ-DD}$	K28.5 pattern, 5.0GT/s, AC-coupled, R_L = 50Ω, effects of deemphasis deembedded			15	ps_{P-P}
Random Jitter	$T_{TX-RJ-DD}$	K28.7 pattern, f > 1.5MHz, BER = 10^{-12}			1.4	ps_{RMS}
Electrical Idle Entry Delay	$T_{TX-IDLE-SET-TO-IDLE}$	From input to output		15		ns
Electrical Idle Exit Delay	$T_{TX-IDLE-TO-DIFF-DATA}$	From input to output		8		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, C_{CL} = 75nF coupling capacitor on each output, R_L = 50Ω resistor on each output, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Electrical Idle Detect Threshold	$V_{TX-IDLE-THRESH}$	Squarewave input at 500MHz	65	85	120	mV_{P-P}
Output Voltage During Electrical Idle (AC)	$V_{TX-IDLE-DIFF-AC-P}$	$\|(V_{OUT_P} - V_{OUT_N})\|$, f = 2.5GHz			20	mV_{P-P}
Receiver Detect Pulse Amplitude	$V_{TX-RCV-DETECT}$	Voltage change in positive direction			600	mV
Receiver Detect Pulse Width				100		ns
Receiver Detect Retry Period				200		ns
CONTROL LOGIC (INEQ1, INEQ0, OEQ1, OEQ0, EN, RX_DET, O_AMP, P_SAV)						
Input Logic-Level Low	V_{IL}				0.6	V
Input Logic-Level High	V_{IH}		1.4			V
Input Logic Hysteresis	V_{HYST}			130		mV
Input Leakage Current	I_{IN}	$V_{CONTROL_LOGIC}$ = +0.5V or +1.5V	-50		+50	µA
ESD PROTECTION						
All Pins		Human Body Model (HBM)		±2		kV

Note 3: All devices are 100% production tested at T_A = +70°C. Specifications for all temperature limits are guaranteed by design.

Note 4: Currents are applicable for both PCIe Generation I and Generation II speeds. Power-saving mode (P_SAV), where electrical idle and receiver detection are only performed on channel 0 and reduced output swing (O_AMP) reduces this current. Table 5 summarizes the predicted power consumption.

Note 5: Guaranteed by design, unless otherwise noted.

Note 6: Equivalent to same amount of deemphasis driving the input.

Note 7: Rise and fall times are measured using 20% and 80% levels.

Timing Diagram

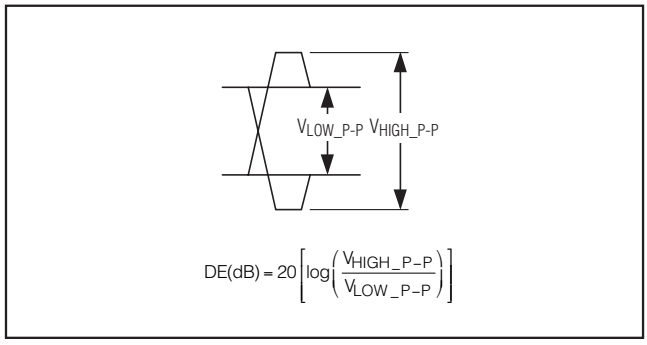
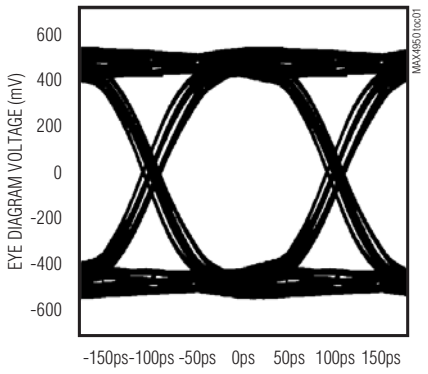


Figure 1. Illustration of Output Deemphasis

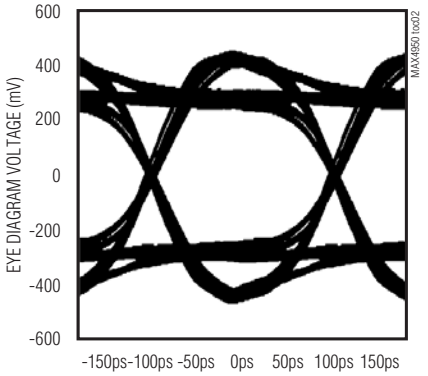
Typical Operating Characteristics

(V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted. All eye diagrams measured using K28.5 pattern.)

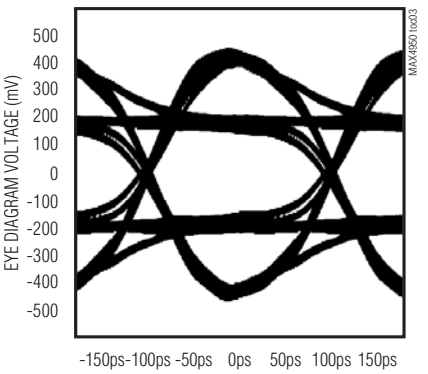
INEQ0 = INEQ1 = 0, O_AMP = 0, V_{IN} = 200mV_{P-P}, OEQ0 = 0, OEQ1 = 0



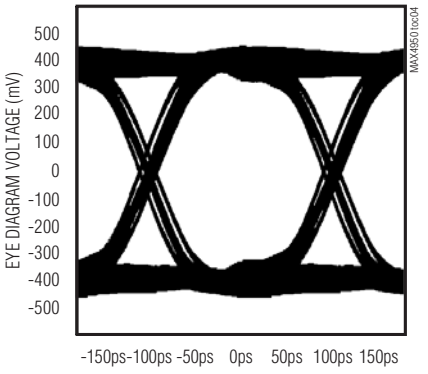
INEQ0 = INEQ1 = 0, O_AMP = 0, V_{IN} = 200mV_{P-P}, OEQ0 = 1, OEQ1 = 0



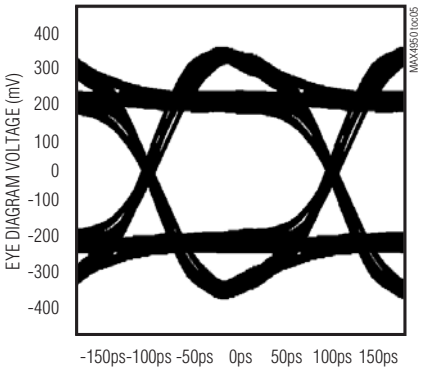
INEQ0 = INEQ1 = 0, O_AMP = 0, V_{IN} = 200mV_{P-P}, OEQ0 = 0, OEQ1 = 1



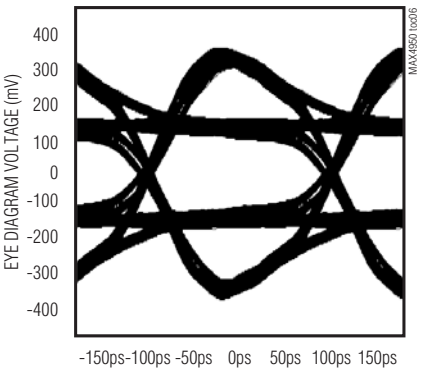
INEQ0 = INEQ1 = 0, O_AMP = 1, V_{IN} = 200mV_{P-P}, OEQ0 = 0, OEQ1 = 0



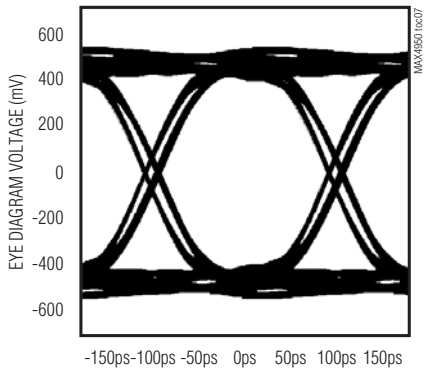
INEQ0 = INEQ1 = 0, O_AMP = 1, V_{IN} = 200mV_{P-P}, OEQ0 = 1, OEQ1 = 0



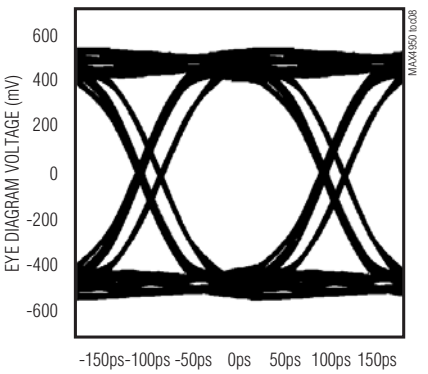
INEQ0 = INEQ1 = 0, O_AMP = 1, V_{IN} = 200mV_{P-P}, OEQ0 = 0, OEQ1 = 1



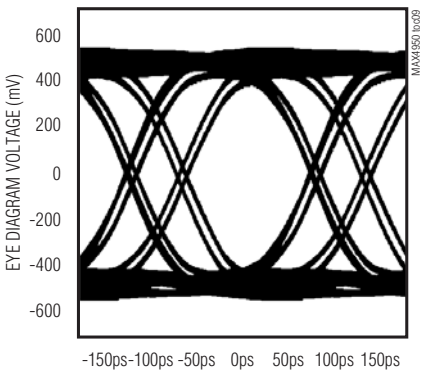
INEQ0 = 1, INEQ1 = 0, O_AMP = 0, V_{IN} = 500mV_{P-P}, WITH 6in. STRIPLINE OEQ0 = OEQ1 = 0



INEQ0 = 0, INEQ1 = 1, O_AMP = 0, V_{IN} = 500mV_{P-P}, WITH 19in. STRIPLINE OEQ0 = OEQ1 = 0



INEQ0 = 0, INEQ1 = 1, O_AMP = 0, V_{IN} = 500mV_{P-P}, WITH 19IN. STRIPLINE OEQ0 = OEQ1 = 0

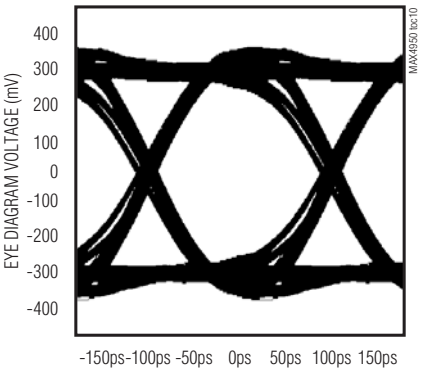


Quad PCI Express Equalizer/Redriver

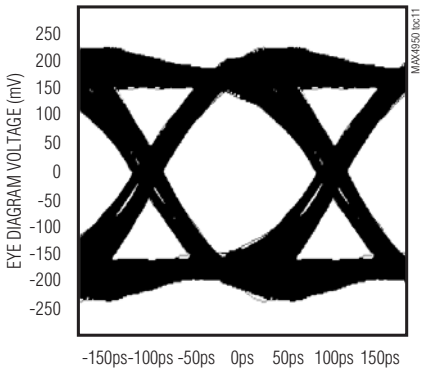
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted. All eye diagrams measured using K28.5 pattern.)

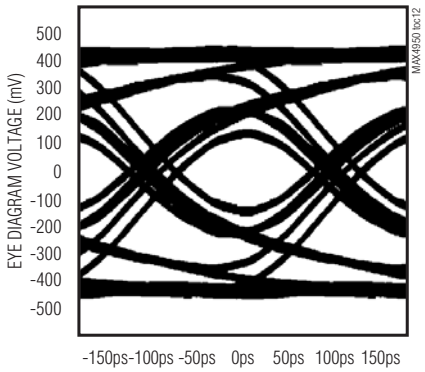
INEQ0 = INEQ1 = 0, O_AMP = 1, V_{IN} = 200mV$_{P-P}$, OEQ0 = 1, OEQ1 = 0, OUTPUT AFTER 6IN. STRIPLINE



INEQ0 = INEQ1 = 0, O_AMP = 0, V_{IN} = 200mV$_{P-P}$, OEQ0 = 0, OEQ1 = 1, OUTPUT AFTER 19IN. STRIPLINE



INEQ0 = INEQ1 = 0, O_AMP = 0, V_{IN} = 200mV$_{P-P}$, OEQ0 = 0, OEQ1 = 0, OUTPUT AFTER 19IN. STRIPLINE



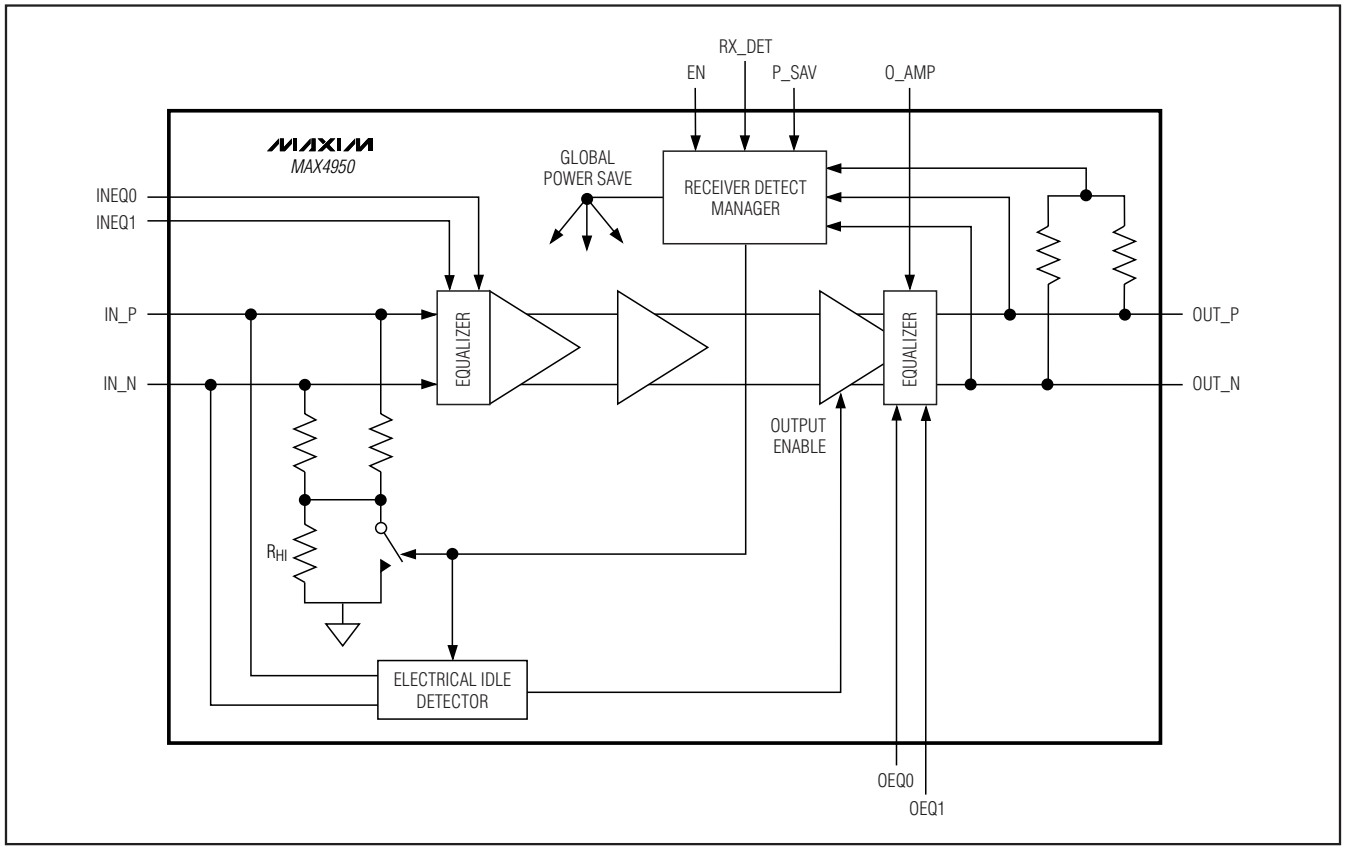
Pin Description

PIN	NAME	FUNCTION
1, 9, 17, 22, 30, 38	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with 1µF and .01µF capacitors in parallel as close to the device as possible.
2, 5, 8, 10,13, 16, 23, 26, 29, 31, 34, 37	GND	Ground
3	IN0P	Noninverting Input 0
4	IN0N	Inverting Input 0
6	IN1P	Noninverting Input 1
7	IN1N	Inverting Input 1
11	IN2P	Noninverting Input 2
12	IN2N	Inverting Input 2
14	IN3P	Noninverting Input 3
15	IN3N	Inverting Input 3
18	INEQ1	Input Equalization Control MSB. INEQ1 is internally pulled down by 60kΩ (typ) resistor. See Table 2.
19	INEQ0	Input Equalization Control LSB. INEQ0 is internally pulled down by 60kΩ (typ) resistor. See Table 2.
20	OEQ1	Output Deemphasis Control MSB. OEQ1 is internally pulled down by 60kΩ (typ) resistor. See Table 3.
21	OEQ0	Output Deemphasis Control LSB. OEQ0 is internally pulled down by 60kΩ (typ) resistor. See Table 3.
24	OUT3N	Inverting Output 3
25	OUT3P	Noninverting Output 3
27	OUT2N	Inverting Output 2
28	OUT2P	Noninverting Output 2

Pin Description (continued)

PIN	NAME	FUNCTION
32	OUT1N	Inverting Output 1
33	OUT1P	Noninverting Output 1
35	OUT0N	Inverting Output 0
36	OUT0P	Noninverting Output 0
39	EN	Enable Input. Drive EN low for standby mode. Drive EN high for normal mode. EN is internally pulled down by 60kΩ (typ) resistor.
40	RX_DET	Receiver Detection Control Bit. Drive RX_DET high to initiate receiver detection. Drive RX_DET low for normal mode. RX_DET is internally pulled down by 60kΩ (typ) resistor.
41	O_AMP	Output Redrive Selection Input. O_AMP is internally pulled down by 60kΩ (typ) resistor.
42	P_SAV	Power-Save Mode Input. P_SAV is internally pulled down by 60kΩ (typ) resistor. See Table 6.
—	EP	Exposed Pad. Internally connected to GND. Connect EP to a large ground plane to maximize thermal performance. EP is not intended as an electrical connection point.

Functional Diagram



Quad PCI Express Equalizer/Redriver

Detailed Description

The MAX4950 quad equalizer/redriver is designed to support both Gen I (2.5GT/s) and Gen II (5.0GT/s) PCIe data rates. The device contains four identical drivers with idle/receive detect on each lane and equalization to compensate for circuit-board loss. Signal integrity at the receiver is improved by the use of programmable input equalization circuitry. The MAX4950 output features a redrive output swing selection input, O_AMP (Table 1), and programmable output deemphasis, permitting optimal placement of key PCIe components and longer runs of stripline, microstrip, or cable.

Programmable Input Equalization

The MAX4950 features a programmable input equalizer capable of providing 0dB, 3.5dB, or 6dB of high-frequency boost by setting 2 control bits, INEQ1 and INEQ0 (see Table 2).

Programmable Output Deemphasis

The MAX4950 features programmable output deemphasis by setting two control bits, OEQ1 and OEQ0, for deemphasis ratios of 0dB, 3.5dB, and 6dB (see Table 3).

Receiver Detection

The MAX4950 features receiver detection on each channel. Upon initial power-up, if EN is high, receiver detection initializes. Receiver detection can also be initiated on a rising edge of the RX_DET input when EN is high. During this time, the part remains in low-power standby mode and the outputs are disabled, despite the logic-high state of EN. Until a channel has detected a receiver, receiver detection repeats indefinitely on each channel. If a channel detects a receiver, the other channels are limited to three retries. Upon receiver detection, channel output and electrical idle detection are enabled.

Note: *With a slowly rising power supply, it is recommended to toggle EN to avoid potential receiver detection timeout conditions.*

Electrical Idle Detection

The MAX4950 features electrical idle detection to prevent unwanted noise from being redriven at the output. If the MAX4950 detects that the differential input has fallen below $V_{TX-IDLE-THRESH}$, the MAX4950 squelches the output. For differential input signals that are above $V_{TX-IDLE-THRESH}$, the MAX4950 turns on the output and redrives the signal. There is little variation in output common-mode voltage between electrical idle and redrive modes.

Power-Saving Features

The MAX4950 features a power-save mode to reduce quiescent supply current. In power-save mode, electrical idle and receiver detection circuitry for channels 1, 2, and 3 are turned off, and all channel operation is slaved to channel 0. This feature is useful for reducing power consumption in applications where all channels operate simultaneously. During normal operation, all channels have independent electrical idle and receiver detection. Drive P_SAV high to activate power-save mode; drive P_SAV low for normal operation. To further reduce power consumption, the MAX4950 features a standby input (EN) when the device is not needed. To place the device in standby mode, drive EN low. To enable the device, drive EN high. Table 5 shows typical power consumption differences between normal mode, power-save mode, and standby mode with different output redrive strengths.

Table 1. Output Redrive Swing

O_AMP	DIFFERENTIAL OUTPUT VOLTAGE (mV_{P-P})
0	1000 (typ)
1	750 (typ)

Table 2. Input Equalization

INEQ1	INEQ0	INPUT EQUALIZATION (dB)
0	0	0 at 5.0GT/s
0	1	3.5 (typ) at 5.0GT/s
1	X	6 (typ) at 5.0GT/s

X = Don't Care.

Table 3. Output Deemphasis

OEQ1	OEQ0	OUTPUT DEEMPHASIS RATIO (dB)
0	0	0 at 5.0GT/s
0	1	3.5 (typ) at 5.0GT/s
1	X	6 (typ) at 5.0GT/s

X = Don't Care.

Table 4. Receiver Detection Input Function

RX_DET	EN	DESCRIPTION
X	0	Receiver Detection Inactive
0	1	Receiver Detection Inactive
Rising Edge	1	Initiate Receiver Detection
1	1	Following a Rising Edge, Indefinite Retry Until Receiver Detected

X = Don't Care.

Table 5. Power-Save Mode Quiescent Power Dissipation

EN	P_SAV	O_AMP	QUIESCENT POWER SUPPLY CURRENT (typ) (mA)	QUIESCENT POWER SUPPLY CURRENT (max) (mA)	QUIESCENT POWER DISSIPATION (3.3V, typ) (mW)	QUIESCENT POWER DISSIPATION (3.6V, max) (mW)
0	0	0	100	125	330	450
0	0	1	80	100	264	360
0	1	0	100	125	330	450
0	1	1	80	100	264	360
1	0	0	262	328	865	1181
1	0	1	242	303	799	1091
1	1	0	214	268	706	965
1	1	1	194	243	640	875

Applications Information

Figure 2 shows a typical application with two MAX4950s, both residing on the main board, with input and output equalization set individually for optimal performance. The receive equalizer is set to receive a degraded signal coming from a remote board through two sets of connectors, and a midplane stripline transmission. The output of the Rx section has little or no output equalization. The Tx section takes a high-quality signal, and provides boost to the output (deemphasis).

Layout

Circuit-board layout and design can significantly affect the performance of the MAX4950. Use good high-frequency design techniques, including minimizing ground inductance and using controlled-impedance transmission lines on data signals. Power-supply decoupling should also be placed as close to V_{CC} as possible. Always connect V_{CC} to a power plane. It is recommended to run receive and transmit on different layers to minimize crosstalk.

Exposed-Pad Package

The exposed-pad, 42-pin TQFN package incorporates features that provide a very low thermal-resistance path for heat removal from the IC. The exposed pad on the MAX4950 must be soldered to the circuit-board ground plane for proper thermal performance. For more information on exposed-pad packages, refer to Maxim Application Note HFAN-08.1: *Thermal Considerations of QFN and Other Exposed-Paddle Packages*.

Power-Supply Sequencing

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all devices. Always apply GND then V_{CC} before applying signals, especially if the signal is not current limited.

Chip Information

PROCESS: BiCMOS

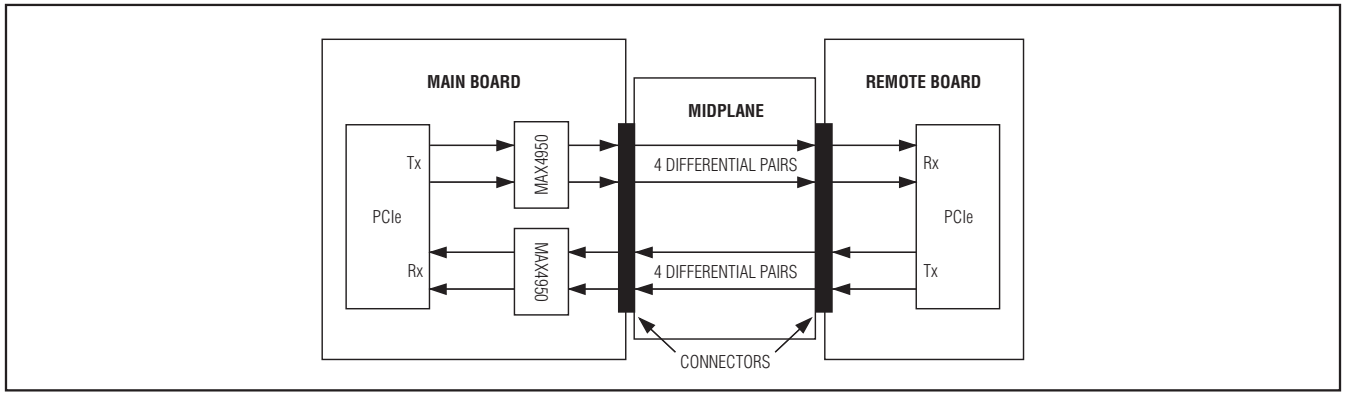


Figure 2. Typical Application Diagram

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
42 TQFN-EP	T423590+1	**21-0181**

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