

### **DUAL N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR**

### **Features**

- Dual N-Channel MOSFET
- Low On-Resistance
- Very Low Gate Threshold Voltage, 1.2V max
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- ESD Protected Gate
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)

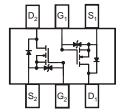
### **Mechanical Data**

- Case: SOT563
- Case Material: Molded Plastic, "Green" Molding Compound.
   UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish Matte Tin Annealed over Copper Leadframe.
   Solderable per MIL-STD-202, Method 208 (§3)
- Weight: 0.006 grams (Approximate)

#### **SOT563**







Top View Schematic and Transistor Diagram

### **Ordering Information** (Note 4)

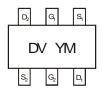
Part Number	Case	Packaging
DMN32D2LV-7	SOT563	3,000/Tape & Reel

Notes:

- $1.\ No\ purposely\ added\ lead.\ Fully\ EU\ Directive\ 2002/95/EC\ (RoHS)\ \&\ 2011/65/EU\ (RoHS\ 2)\ compliant.$
- See http://www.diodes.com/quality/lead\_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html

### **Marking Information**

### **SOT563**



DV = Product Type Marking Code YM = Date Code Marking Y = Year (ex: U = 2007) M = Month (ex: 9 = September)

#### Date Code Kev

Year	2007		20	14	2015	2016	2017	2018	3 20	19	2020	2021
Code	U		[	3	С	D	E	F	(	3	Н	ı
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D



## **Maximum Ratings** $(@T_A = +25^{\circ}C, \text{ unless otherwise specified.})$

Characteristic	Symbol	Value	Unit
Drain Source Voltage	$V_{DSS}$	30	V
Gate-Source Voltage	$V_{GSS}$	±10	V
Drain Current (Note 5)	I <sub>D</sub>	400	mA

### **Thermal Characteristics**

Total Power Dissipation (Note 5)	$P_{D}$	450	mW
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	313	°C/W
Operating and Storage Temperature Range	$T_{J}, T_{STG}$	-55 to +150	°C

## **Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

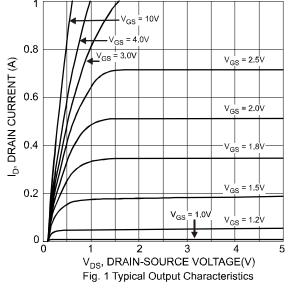
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition		
OFF CHARACTERISTICS (Note 6)					•			
Drain-Source Breakdown Voltage		BV <sub>DSS</sub>	30	_	_	V	$V_{GS} = 0V, I_D = 250\mu A$	
Zero Gate Voltage Drain Current	@T <sub>J</sub> = +25°C	I <sub>DSS</sub>	_	_	1	μΑ	$V_{DS} = 30V, V_{GS} = 0V$	
				_	±10	μΑ	$V_{GS} = \pm 10V$ , $V_{DS} = 0V$	
Gate-Body Leakage	$@T_J = +25^{\circ}C$	$I_{GSS}$	_	_	±500	nA	$V_{GS} = \pm 5V$ , $V_{DS} = 0V$	
				±1	±100	nA	$V_{GS} = \pm 2.5V, V_{DS} = 0V$	
Gate-Body Leakage (Note 7)	$@T_J = +105^{\circ}C$	1		±8	±100	nA nA	\/ 12 <b>E</b> \/ \/ = 0\/	
	$@T_J = +125^{\circ}C$	I <sub>GSS</sub>	_	±15	±100		$V_{GS} = \pm 2.5 V, V_{DS} = 0 V$	
ON CHARACTERISTICS (Note 6)								
Gate Threshold Voltage		V <sub>GS(TH)</sub>	0.6	_	1.2	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$	
		R <sub>DS(ON)</sub>	_	_	2.2 1.5		$V_{GS} = 1.8V, I_D = 20mA$	
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>		_	_		Ω	$V_{GS} = 2.5V, I_D = 20mA$	
		—	_	1.2		$V_{GS} = 4.0V, I_D = 100mA$		
Forward Transconductance		Y <sub>FS</sub>	100	_	_	mS	$V_{DS} = 10V, I_D = 0.1A$	
Source-Drain Diode Forward Voltage		V <sub>SD</sub>	0.5	_	1.4	V	$V_{GS} = 0V, I_{S} = 115mA$	
DYNAMIC CHARACTERISTICS (Note 7)								
Input Capacitance		C <sub>ISS</sub>	_	39	_	pF	., ., ., .,	
Output Capacitance		Coss	_	10	_	pF	$V_{DS} = 3V, V_{GS} = 0V$ f = 1.0MHz	
Reverse Transfer Capacitance			_	3.6	_	pF	1 = 1.0IVIDZ	
Switching Time	Turn-On Time	t <sub>ON</sub>	_	11	_	ns	$V_{DD} = 5V, I_D = 10 \text{ mA},$	
Switching time	Turn-Off Time	toff	_	51	_	ns	$V_{GS} = 5V$	

Notes:

<sup>5.</sup> Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch; pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found at http://www.diodes.com/datasheets/ap02001.pdf.

Short duration pulse test used to minimize self-heating effect.
 Guaranteed by design. Not subject to production testing.





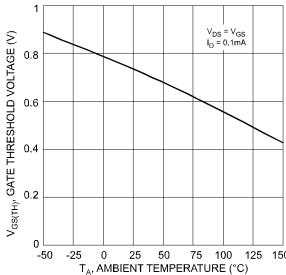


Fig. 3 Gate Threshold Voltage vs. Ambient Temperature

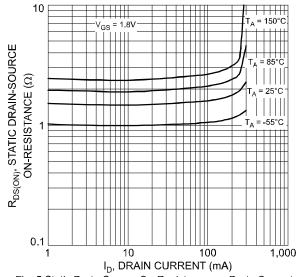
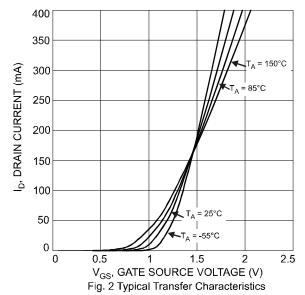


Fig. 5 Static Drain-Source On-Resistance vs. Drain Current



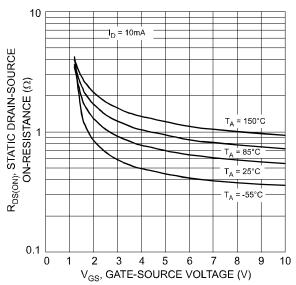


Fig. 4 Static Drain-Source On-Resistance vs. Gate-Source Voltage

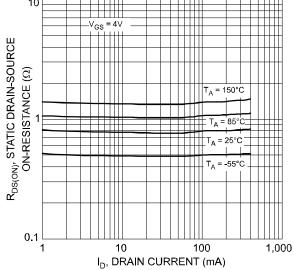
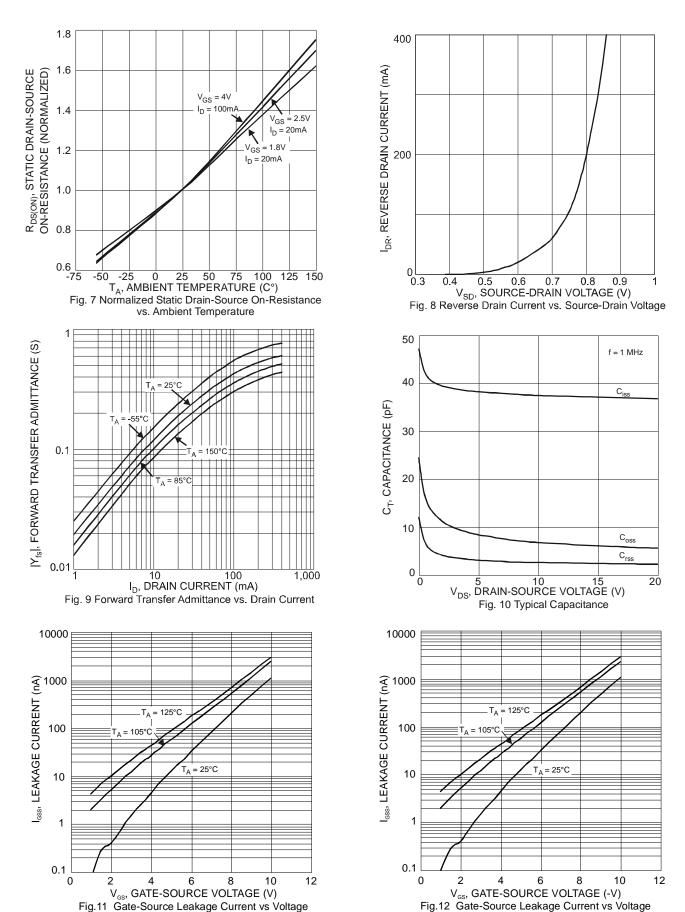


Fig. 6 Static Drain-Source On-Resistance vs. Drain Current



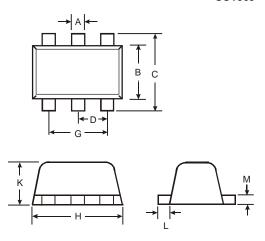




## **Package Outline Dimensions**

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

#### **SOT563**

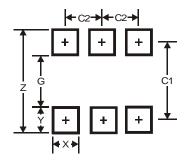


SOT-563						
Dim	Min	Max	Тур			
Α	0.15	0.30	0.20			
В	1.10	1.25	1.20			
С	1.55	1.70	1.60			
D	_	_	0.50			
G	0.90	1.10	1.00			
Н	1.50	1.70	1.60			
K	0.55	0.60	0.60			
L	0.10	0.30	0.20			
М	0.10	0.18	0.11			
All Dimensions in mm						

### **Suggested Pad Layout**

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

### SOT563



Dimensions	Value (in mm)
Z	2.2
G	1.2
Х	0.375
Υ	0.5
C1	1.7
C2	0.5



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