OPA1632 High-Performance, Fully-Differential Audio Operational Amplifier

1 Features

- Superior Sound Quality
- Ultra Low Distortion: 0.000022%
- Low Noise: 1.3 nV/√Hz
- High Speed:
  - Slew Rate: 50 V/µs
  - Gain Bandwidth: 180 MHz
- Fully Differential Architecture:
  - Balanced Input and Output Converts Single-Ended Input to Balanced Differential Output
- Wide Supply Range: ±2.5 V to ±16 V
- Shutdown to Conserve Power

2 Applications

- Audio ADC Driver
- Balanced Line Driver
- Balanced Receiver
- Active Filter
- Preamplifier

3 Description

The OPA1632 is a fully-differential amplifier designed for driving high-performance audio analog-to-digital converters (ADCs). It provides the highest audio quality, with very low noise and output drive characteristics optimized for this application. The OPA1632's excellent gain bandwidth of 180 MHz and very fast slew rate of 50 V/µs produce exceptionally low distortion. Very low input noise of 1.3 nV/√Hz further ensures maximum signal-to-noise ratio and dynamic range.

The flexibility of the fully differential architecture allows for easy implementation of a single-ended to fully-differential output conversion. Differential output reduces even-order harmonics and minimizes common-mode noise interference. The OPA1632 provides excellent performance when used to drive high-performance audio ADCs such as the PCM1804. A shutdown feature also enhances the flexibility of this amplifier.

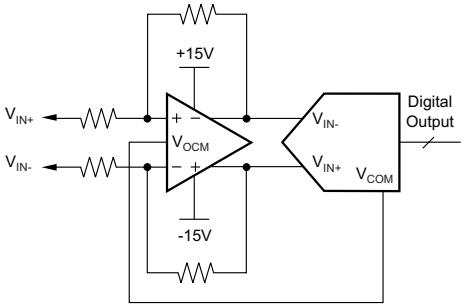
The OPA1632 is available in an SO-8 package and a thermally-enhanced MSOP-8 PowerPAD™ package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA1632	SOIC (8)	6.00 mm × 4.90 mm
	MSOP-PowerPAD (8)	5.00 mm × 3.00 mm

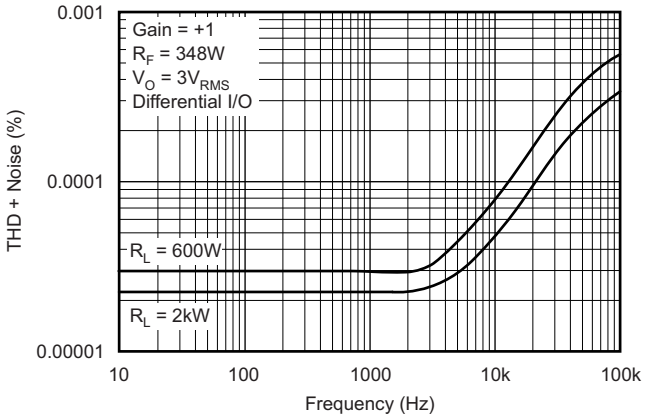
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Diagram



Typical ADC Circuit

THD + Noise vs Frequency



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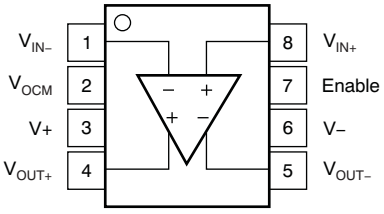
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (January 2010) to Revision C	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

5 Pin Configuration and Functions

D or DGN Package
8-Pin SOIC or MSOP-PowerPAD
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
Enable	7	I	Active high enable pin
V+	3	I/O	Positive supply voltage pin
V-	6	I/O	Negative supply voltage pin
V_{IN+}	8	I	Positive input voltage pin
V_{IN-}	1	I	Negative input voltage pin
V_{OCM}	2	I	Output common-mode control voltage pin
V_{OUT+}	4	O	Positive output voltage pin
V_{OUT-}	5	O	Negative output voltage pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
$\pm V_S$	Supply Voltage		±16.5	V
V_I	Input Voltage		$\pm V_S$	V
I_O	Output Current		150	mA
V_{ID}	Differential Input Voltage		±3	V
T_J	Maximum Junction Temperature		150	°C
	Operating Free-Air Temperature Range	–40	85	°C
T_{STG}	Storage Temperature Range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The OPA1632 MSOP-8 package version incorporates a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally-dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature, which can permanently damage the device. See TI technical brief SLMA002 for more information about using the PowerPAD thermally-enhanced package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	V
		Machine Model	±200	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage (V+ – V-)	Dual	±2.5	±15	V
	Single	5	30	
T_A	C-suffic	-0	70	°C
	I-suffic	.40	85	

6.4 Thermal Information

THERMAL METRIC(1)		OPA1632 D (SOIC) 8 PINS	OPA1632 RGN (MSOP-PowerPAD) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.5	59.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.3	57.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.8	38.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14	2.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.3	38.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	8.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_S = ±15 V; R_F = 390 Ω, R_L = 800 Ω, and G = +1 (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
Offset Voltage								
Input Offset Voltage						±0.5	±3	mV
	vs Power Supply, dc	dV_{OS}/dT				±5		µV°C
	vs Power Supply, dc	PSRR			316	13		µV/V
Input Bias Current								
Input Bias Current	I_B					2	6	µA
Input Offset Current	I_{OS}					±100	±500	nA
Noise								
Input Voltage Noise			f = 10 kHz			1.3		nV/√Hz
Input Current Noise			f = 10 kHz			0.4		pA/√Hz
Input Voltage								
Common-Mode Input Range					(V−) + 1.5		(V+) − 1	V
Common-Mode Rejection Ratio, dc					74	90		dB
Input Impedance								
Input Impedance (each input pin)						34 || 4		MΩ || pF
Open-Loop Gain								
Open-Loop Gain, dc					66	78		dB
Frequency Response								
Small-Signal Bandwidth			G = +1, R_F= 348 Ω			180		MHz
	(V_O = 100mV$_{PP}$, Peaking < 0.5 dB)		G = +2, R_F = 602 Ω			90		MHz
			G = +5, R_F = 1.5 kΩ			36		MHz
			G = +10, R_F = 3.01 kΩ			18		MHz
Bandwidth for 0.1dB Flatness			G = +1, V_O = 100 mV$_{PP}$			40		MHz
Peaking at a Gain of 1			V_O = 100 mV$_{PP}$			0.5		dB
Large-Signal Bandwidth			G = +2, V_O = 20 V$_{PP}$			800		kHz
Slew Rate (25% to 75%)			G = +1			50		V/µs
Rise and Fall Time			G = +1, V_O = 5-V Step			100		ns
Settling Time to	0.1%		G = +1, V_O = 2-V Step			75		ns
	0.01%		G = +1, V_O = 2-V Step			200		ns
Total Harmonic Distortion + Noise	Differential Input/Output		G = +1, f = 1 kHz, V_O = 3 V_{RMS}	R_L = 600 Ω		0.0003%		
	Differential Input/Output			R_L = 2 kΩ		0.000022%		
	Single-Ended In/Differential Out			R_L = 600 Ω		0.000059%		
	Single-Ended In/Differential Out			R_L = 2 kΩ		0.000043%		
Intermodulation Distortion	Differential Input/Output		G = +1, SMPTE/DIN, V_O = 2 V_{PP}	R_L = 600 Ω		0.00008%		
	Differential Input/Output			R_L = 2 kΩ		0.00005%		
	Single-Ended In/Differential Out			R_L = 600 Ω		0.0001%		
	Single-Ended In/Differential Out			R_L = 2 kΩ		0.0007%		
Headroom			THD < 0.01%, R_L = 2 kΩ			20.0		V_{PP}
Output								
Voltage Output Swing			R_L = 2 kΩ		(V+) − 1.9		(V−) + 1.9	V
			R_L = 800 Ω		(V+) − 4.5		(V−) + 4.5	V
Short-Circuit Current	I_{SC}		Sourcing		+50	85		mA
			Sinking		−60	85		
Closed-Loop Output Impedance			G = +1, f = 100 kHz			0.3		Ω

Electrical Characteristics (continued)

V_S = ±15 V; R_F = 390 Ω, R_L = 800 Ω, and G = +1 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power-Down(1)					
Enable Voltage Threshold			(V−) + 2		V
Disable Voltage Threshold			(V−) + 0.8		V
Shutdown Current	V_{ENABLE} = −15 V		0.85		mA
Turn-On Delay	Time for I_Q to Reach 50%		2		µs
Turn-Off Delay	Time for I_Q to Reach 50%		2		µs
Power Supply					
Specified Operating Voltage			±15	±16	V
Operating Voltage		±2.5			V
Quiescent Current I_Q	Per Channel		14	17.1	mA
Temperature Range					
Specified Range		–40		+85	°C
Operating Range		–40		+125	°C
Storage Range		–65		+150	°C

(1) Amplifier has internal 50-kΩ pull-up resistor to V_{CC}+ pin. This enables the amplifier with no connection to shutdown pin.

6.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ (unless otherwise noted)

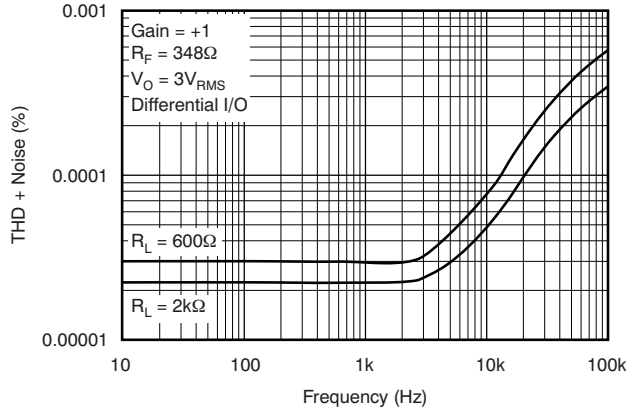


Figure 1. THD + Noise vs Frequency

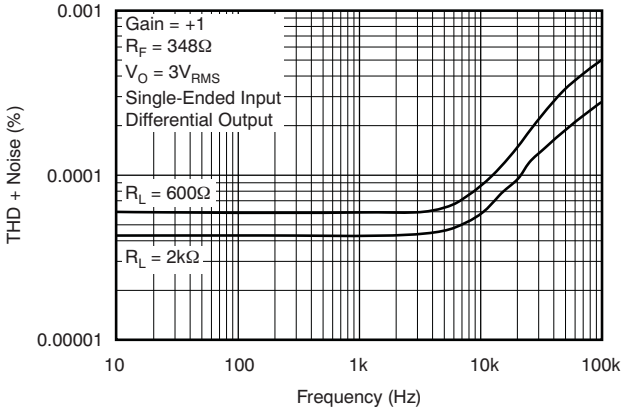


Figure 2. THD + Noise vs Frequency

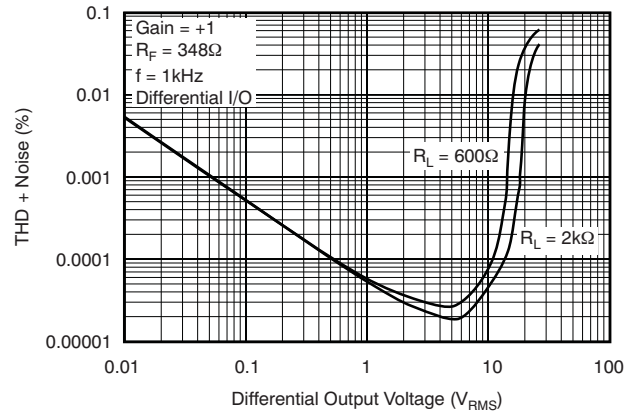


Figure 3. THD + Noise vs Output Voltage

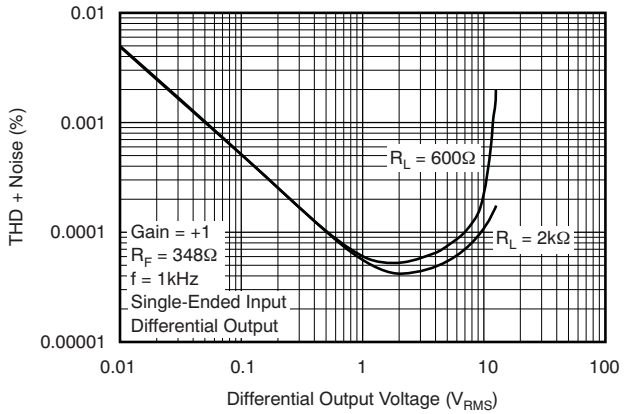


Figure 4. THD + Noise vs Output Voltage

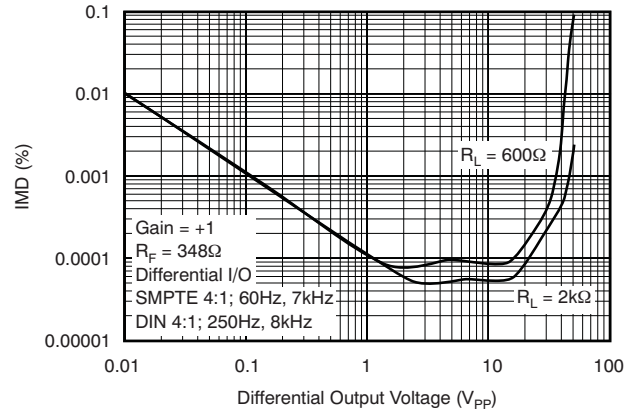


Figure 5. Intermodulation Distortion vs Output Voltage

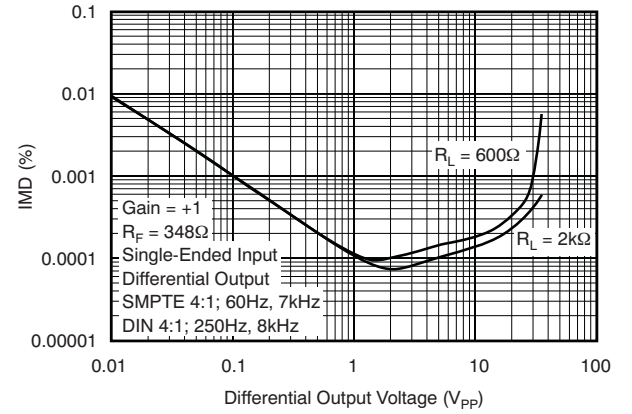


Figure 6. Intermodulation Distortion vs Output Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ (unless otherwise noted)

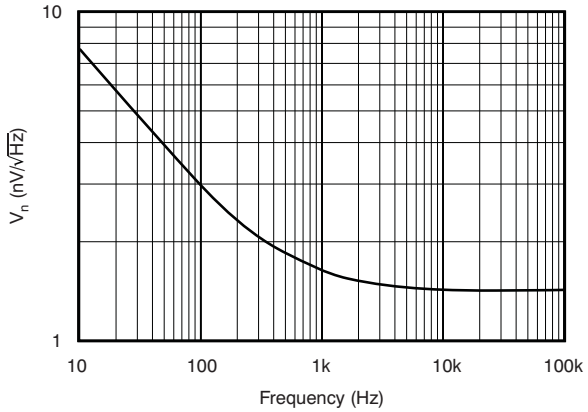


Figure 7. Voltage Noise vs Frequency

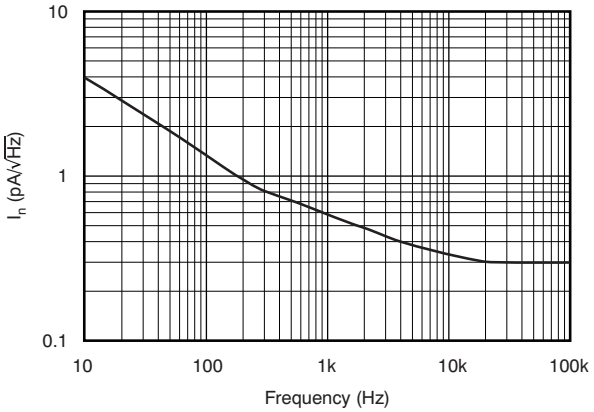


Figure 8. Current Noise vs Frequency

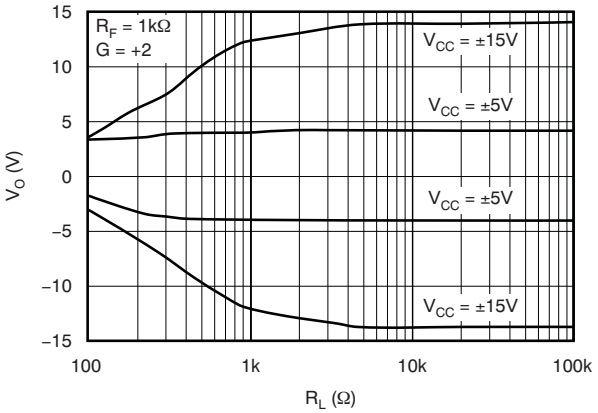


Figure 9. Output Voltage vs Differential Load Resistance

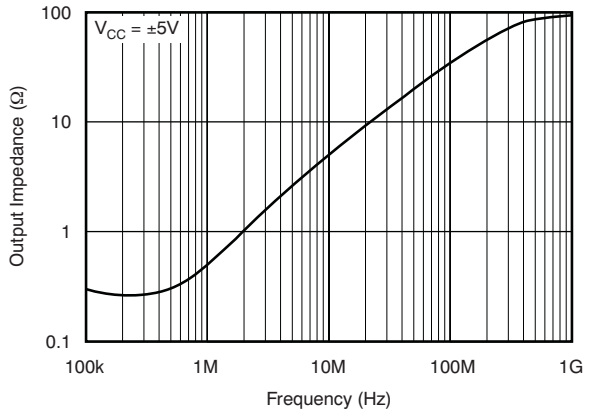


Figure 10. Output Impedance vs Frequency

7 Detailed Description

7.1 Overview

7.1.1 Fully-Differential Amplifiers

The OPA1632 is a fully differential amplifier. Differential signal processing offers a number of performance advantages in high-speed analog signal processing systems, including immunity to external common-mode noise, suppression of even-order nonlinearities, and increased dynamic range. Fully-differential amplifiers not only serve as the primary means of providing gain to a differential signal chain, but also provide a monolithic solution for converting single-ended signals into differential signals allowing for easy, high-performance processing.

A standard configuration for the device is shown in Figure 11. The functionality of a fully differential amplifier can be imagined as two inverting amplifiers that share a common noninverting terminal (though the voltage is not necessarily fixed). For more information on the basic theory of operation for fully differential amplifiers, refer to the Texas Instruments *Fully Differential Amplifiers* application note (SLOA054), available for download from the TI web site (www.ti.com).

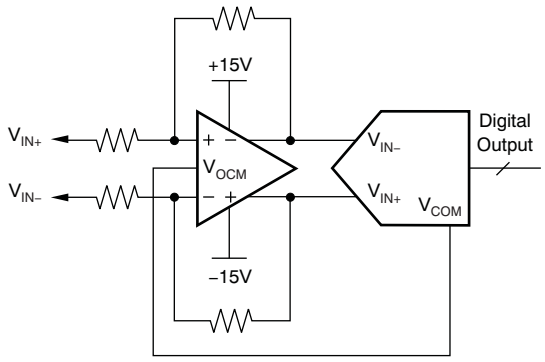
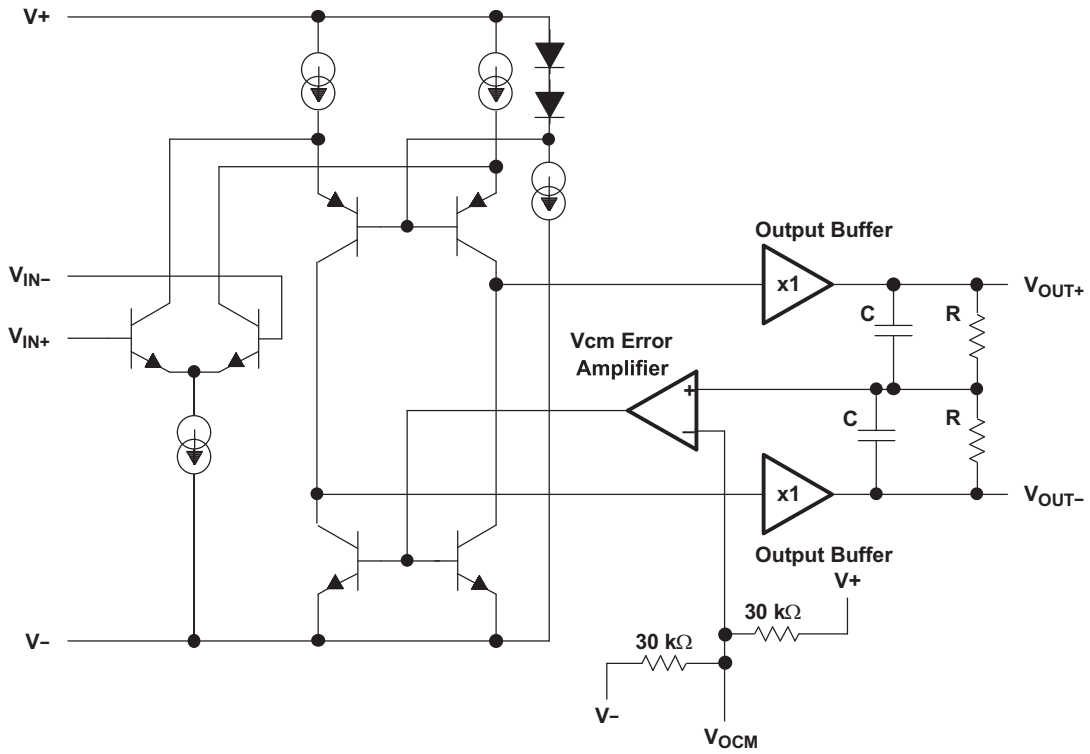


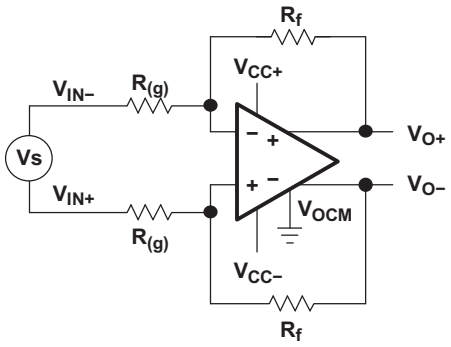
Figure 11. Typical ADC Circuit

7.2 Functional Block Diagram



7.3 Feature Description

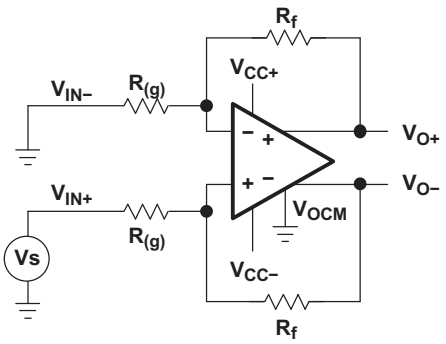
Figure 12 and Figure 13 depict the differences between the operation of the OPA1632 fully-differential amplifier in two different modes. Fully-differential amplifiers can work with differential input or can be implemented as single in/differential out.



Note: For proper operation, maintain symmetry by setting $R_f1 = R_f2 = R_f$ and $R_{(g)}1 = R_{(g)}2 = R_{(g)} \Rightarrow A = R_f/R_{(g)}$

Figure 12. Amplifying Differential Signals

Feature Description (continued)



RECOMMENDED RESISTOR VALUES

GAIN	$R_{(g)}$ Ω	R_f Ω
1	390	390
2	374	750
5	402	2010
10	402	4020

Figure 13. Single In With Differential Out

7.4 Device Functional Modes

7.4.1 Shutdown Function

The shutdown (enable) function of the OPA1632 is referenced to the negative supply of the operational amplifier. A valid logic low (< 0.8 V above negative supply) applied to the enable pin (pin 7) disables the amplifier output. Voltages applied to pin 7 that are greater than 2 V above the negative supply place the amplifier output in an active state, and the device is enabled. If pin 7 is left disconnected, an internal pull-up resistor enables the device. Turn-on and turn-off times are approximately 2 µs each.

Quiescent current is reduced to approximately 0.85 mA when the amplifier is disabled. When disabled, the output stage is *not* in a high-impedance state. Thus, the shutdown function cannot be used to create a multiplexed switching function in series with multiple amplifiers.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Output Common-Mode Voltage

The output common-mode voltage pin sets the dc output voltage of the OPA1632. A voltage applied to the V_{OCM} pin from a low-impedance source can be used to directly set the output common-mode voltage. For a V_{OCM} voltage at mid-supply, make no connection to the V_{OCM} pin.

Depending on the intended application, a decoupling capacitor is recommended on the V_{OCM} node to filter any high-frequency noise that could couple into the signal path through the V_{OCM} circuitry. A 0.1-µF or 1-µF capacitor is generally adequate.

Output common-mode voltage causes additional current to flow in the feedback resistor network. Since this current is supplied by the output stage of the amplifier, this creates additional power dissipation. For commonly-used feedback resistance values, this current is easily supplied by the amplifier. The additional internal power dissipation created by this current may be significant in some applications and may dictate use of the MSOP PowerPAD package to effectively control self-heating.

8.1.1.1 Resistor Matching

Resistor matching is important in fully-differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistor. CMRR, PSRR, and cancellation of the second-harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized.

V_{OCM} sets the dc level of the output signals. If no voltage is applied to the V_{OCM} pin, it is set to the midrail voltage internally defined as:

$$\frac{(V_{CC+}) + (V_{CC-})}{2} \quad (1)$$

In the differential mode, the V_{OCM} on the two outputs cancel each other. Therefore, the output in the differential mode is the same as the input in the gain of 1. V_{OCM} has a high bandwidth capability up to the typical operation range of the amplifier. For the prevention of noise going through the device, use a 0.1-µF capacitor on the V_{OCM} pin as a bypass capacitor. The *Functional Block Diagram* shows the simplified diagram of the OPA1632.

8.2 Typical Application

Figure 14 shows the OPA1632 used as a differential-output driver for the PCM1804 high-performance audio ADC.

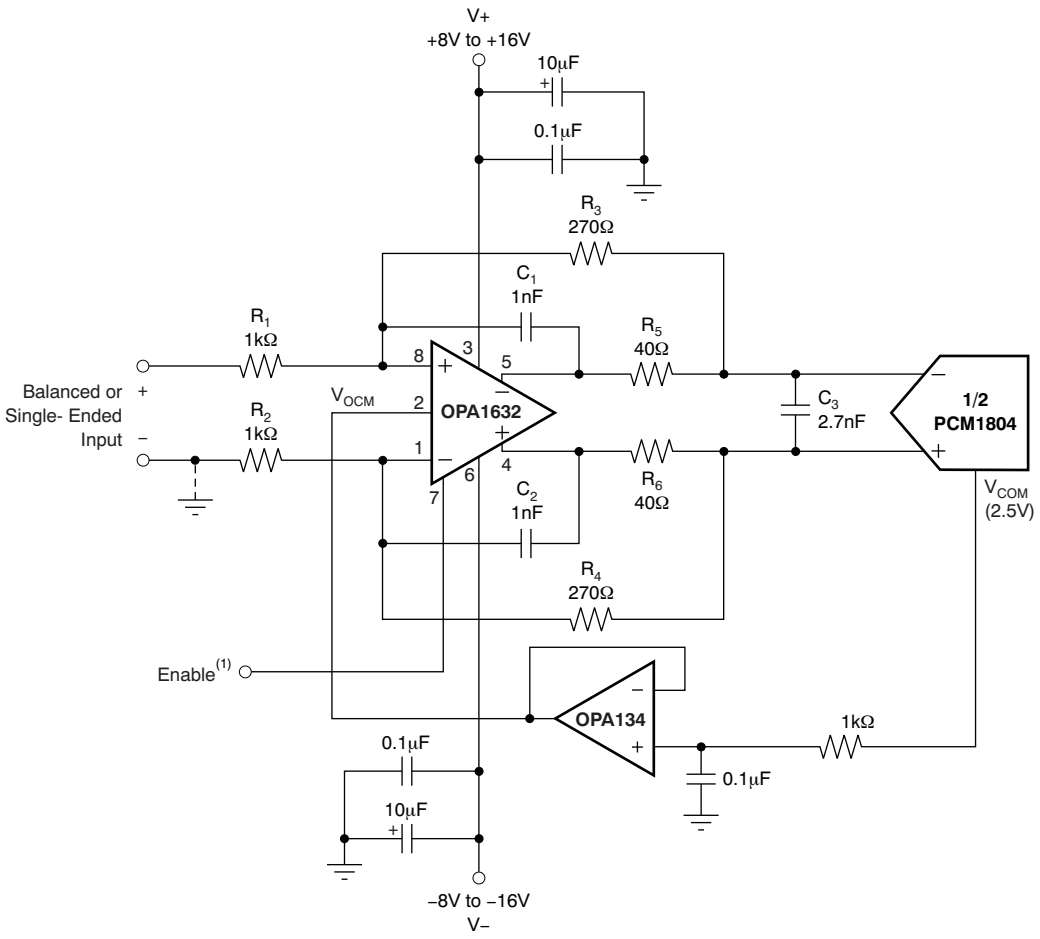


Figure 14. ADC Driver for Professional Audio

8.2.1 Design Requirements

Table 1 shows example design parameters and values for the typical application design example in Figure 12.

Table 1. Design Parameters

DESIGN PARAMETERS	VALUE
Supply voltage	±2.5 V to ±15 V
Amplifier topology	Voltage feedback
Output control	DC coupled with output common mode control capability
Filter requirement	500 kHz, Multiple feedback low pass filter

8.2.2 Detailed Design Procedure

Supply voltages of ±15 V are commonly used for the OPA1632. The relatively low input voltage swing required by the ADC allows use of lower power-supply voltage, if desired. Power supplies as low as ±8 V can be used in this application with excellent performance. This reduces power dissipation and heat rise. Power supplies should be bypassed with 10-µF tantalum capacitors in parallel with 0.1-µF ceramic capacitors to avoid possible oscillations and instability.

The V_{COM} reference voltage output on the PCM1804 ADC provides the proper input common-mode reference voltage (2.5 V). This V_{COM} voltage is buffered with op amp A_2 and drives the output common-mode voltage pin of the OPA1632. This biases the average output voltage of the OPA1632 to 2.5 V.

The signal gain of the circuit is generally set to approximately 0.25 to be compatible with commonly-used audio line levels. Gain can be adjusted, if necessary, by changing the values of R_1 and R_2. The feedback resistor values (R_3 and R_4) should be kept relatively low, as indicated, for best noise performance.

R_5, R_6, and C_3 provide an input filter and charge glitch reservoir for the ADC. The values shown are generally satisfactory. Some adjustment of the values may help optimize performance with different ADCs.

It is important to maintain accurate resistor matching on R_1/R_2 and R_3/R_4 to achieve good differential signal balance. Use 1% resistors for highest performance. When connected for single-ended inputs (inverting input grounded, as shown in Figure 14), the source impedance must be low. Differential input sources must have well-balanced or low source impedance.

Capacitors C_1, C_2, and C_3 should be chosen carefully for good distortion performance. Polystyrene, polypropylene, NPO ceramic, and mica types are generally excellent. Polyester and high-K ceramic types such as Z5U can create distortion.

8.2.3 Application Curves

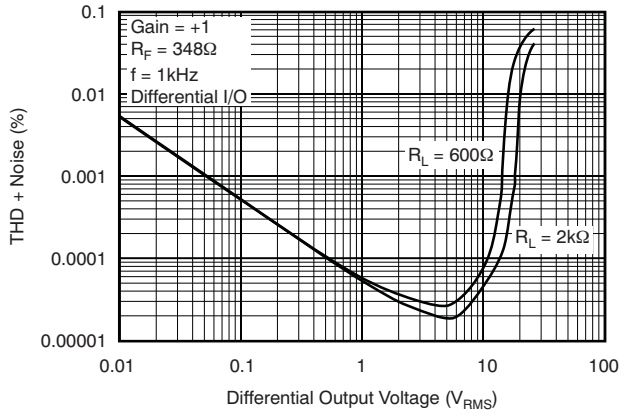


Figure 15. THD + Noise vs Output Voltage

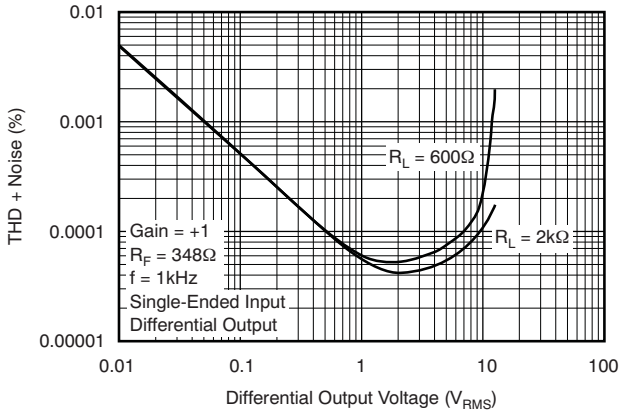


Figure 16. THD + Noise vs Output Voltage

9 Power Supply Recommendations

The OPA1632 device was designed to be operated on power supplies ranging from ±2.5 V to ±15 V. Single power supplies ranging from 5 V to 30 V can also be used. TI recommends using power-supply accuracy of 5%, or better. When operated on a board with high-speed digital signals, it is important to provide isolation between digital signal noise and the analog input pins. The OPA1632 is connected to power supplies through pin 3 (V_{CC+}) and pin 6 (V_{CC-}). Each supply pin should be decoupled to GND as close to the device as possible with a low-inductance, surface-mount ceramic capacitor of approximately 10 nF. When vias are used to connect the bypass capacitors to a ground plane the vias should be configured for minimal parasitic inductance. One method of reducing via inductance is to use multiple vias. For broadband systems, two capacitors per supply pin are advised.

To avoid undesirable signal transients, the OPA1632 device should not be powered on with large inputs signals present. Careful planning of system power on sequencing is especially important to avoid damage to ADC inputs when an ADC is used in the application.

10 Layout

10.1 Layout Guidelines

1. The PowerPAD is electrically isolated from the silicon and all leads. Connecting the PowerPAD to any potential voltage between the power-supply voltages is acceptable, but it is recommended to tie to ground because it is generally the largest conductive plane.
2. Prepare the PCB with a top-side etch pattern, as shown in Figure 17. There should be etch for the leads as well as etch for the thermal pad.
3. Place five holes in the area of the thermal pad. These holes should be 13 mils (0,03302 cm) in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
4. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. These vias help dissipate the heat generated by the OPA1632 IC, and may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
5. Connect all holes to the internal ground plane.
6. When connecting these holes to the plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the OPA1632 PowerPAD package should make their connection to the internal plane with a complete connection around the entire circumference of the plated-through hole.
7. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
8. Apply solder paste to the exposed thermal pad area and all of the IC terminals.

   With these preparatory steps in place, the IC is simply placed in position and runs through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

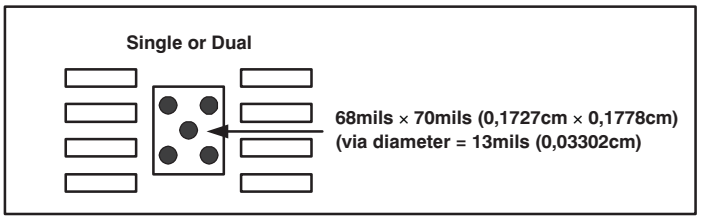


Figure 17. PowerPAD PCB Etch and Via Pattern

10.1.1 PowerPAD Design Considerations

The OPA1632 is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted (see Figure 18(a) and Figure 18(b)). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package (see Figure 18(c)). Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

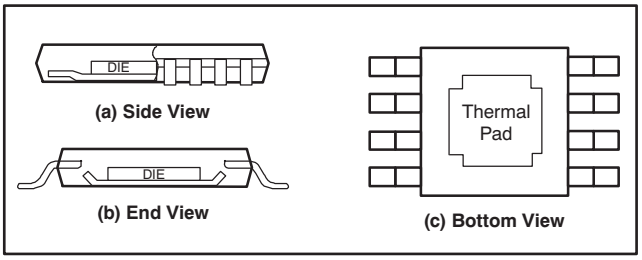


Figure 18. Views of the Thermally-Enhanced Package

Layout Guidelines (continued)

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. Soldering the PowerPAD to the printed circuit board (PCB) is always required, even with applications that have low power dissipation. It provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

10.1.2 Power Dissipation And Thermal Considerations

The OPA1632 does not have thermal shutdown protection. Take care to assure that the maximum junction temperature is not exceeded. Excessive junction temperature can degrade performance or cause permanent damage. For best performance and reliability, assure that the junction temperature does not exceed 125°C.

The thermal characteristics of the device are dictated by the package and the circuit board. Maximum power dissipation for a given package can be calculated using the following formula:

$$P_{DMax} = \frac{T_{Max} - T_A}{\theta_{JA}}$$

where:

- P_{DMax} is the maximum power dissipation in the amplifier (W)
- T_{Max} is the absolute maximum junction temperature (°C)
- T_A is the ambient temperature (°C)
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W)
- θ_{CA} is the thermal coefficient from the case to ambient air (°C/W)

For systems where heat dissipation is more critical, the OPA1632 is offered in an MSOP-8 with PowerPAD. The thermal coefficient for the MSOP PowerPAD (DGN) package is substantially improved over the traditional SO package. Maximum power dissipation levels are depicted in Figure 19 for the two packages. The data for the DGN package assume a board layout that follows the PowerPAD layout guidelines.

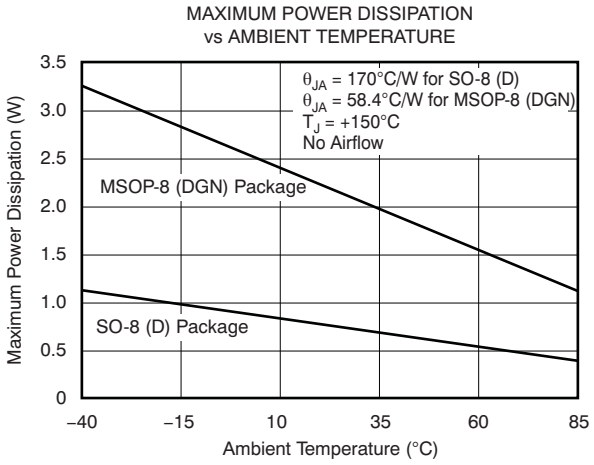


Figure 19. Maximum Power Dissipation vs Ambient Temperature

10.2 Layout Example

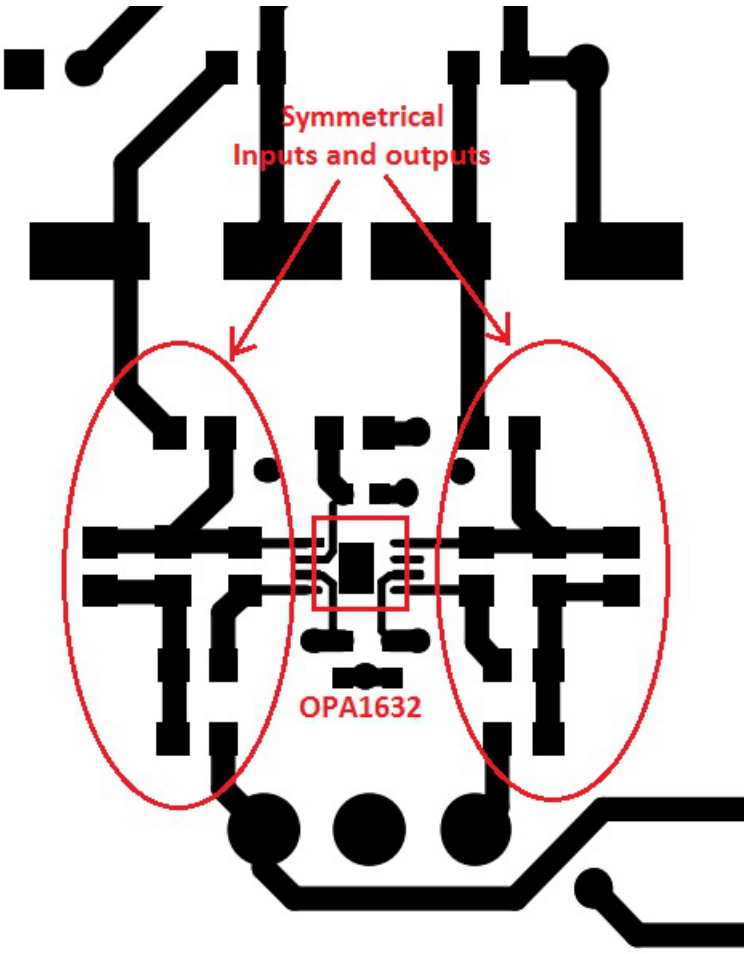


Figure 20. Example Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

Related Products

PRODUCT	DESCRIPTION
OPAx134	High-Performance Audio Amplifiers
OPA627/OPA637	Precision High-Speed DiFET Amplifiers
OPAx227/OPAx228	Low-Noise Bipolar Amplifiers

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA1632D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 1632	Samples
OPA1632DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 1632	Samples
OPA1632DGN	ACTIVE	HVSSOP	DGN	8	80	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	1632	Samples
OPA1632DGNG4	ACTIVE	HVSSOP	DGN	8	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1632	Samples
OPA1632DGNR	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	1632	Samples
OPA1632DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 1632	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

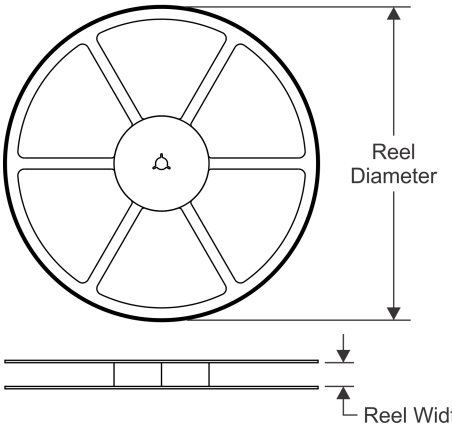
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

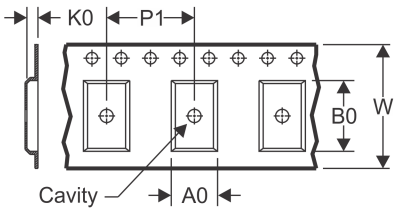
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

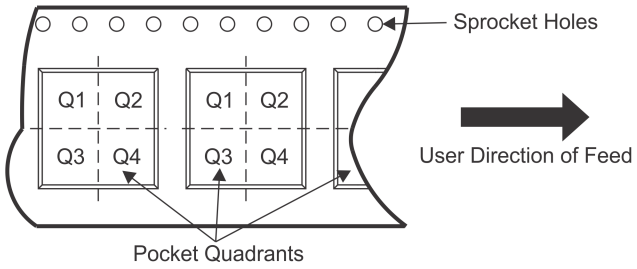


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

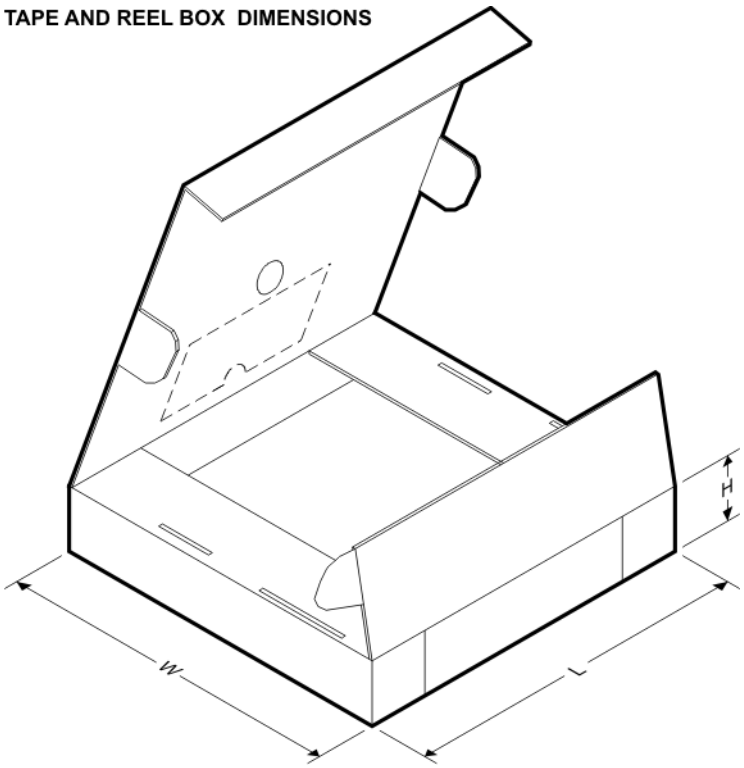
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

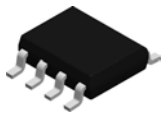
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1632DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1632DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1632DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
OPA1632DR	SOIC	D	8	2500	350.0	350.0	43.0

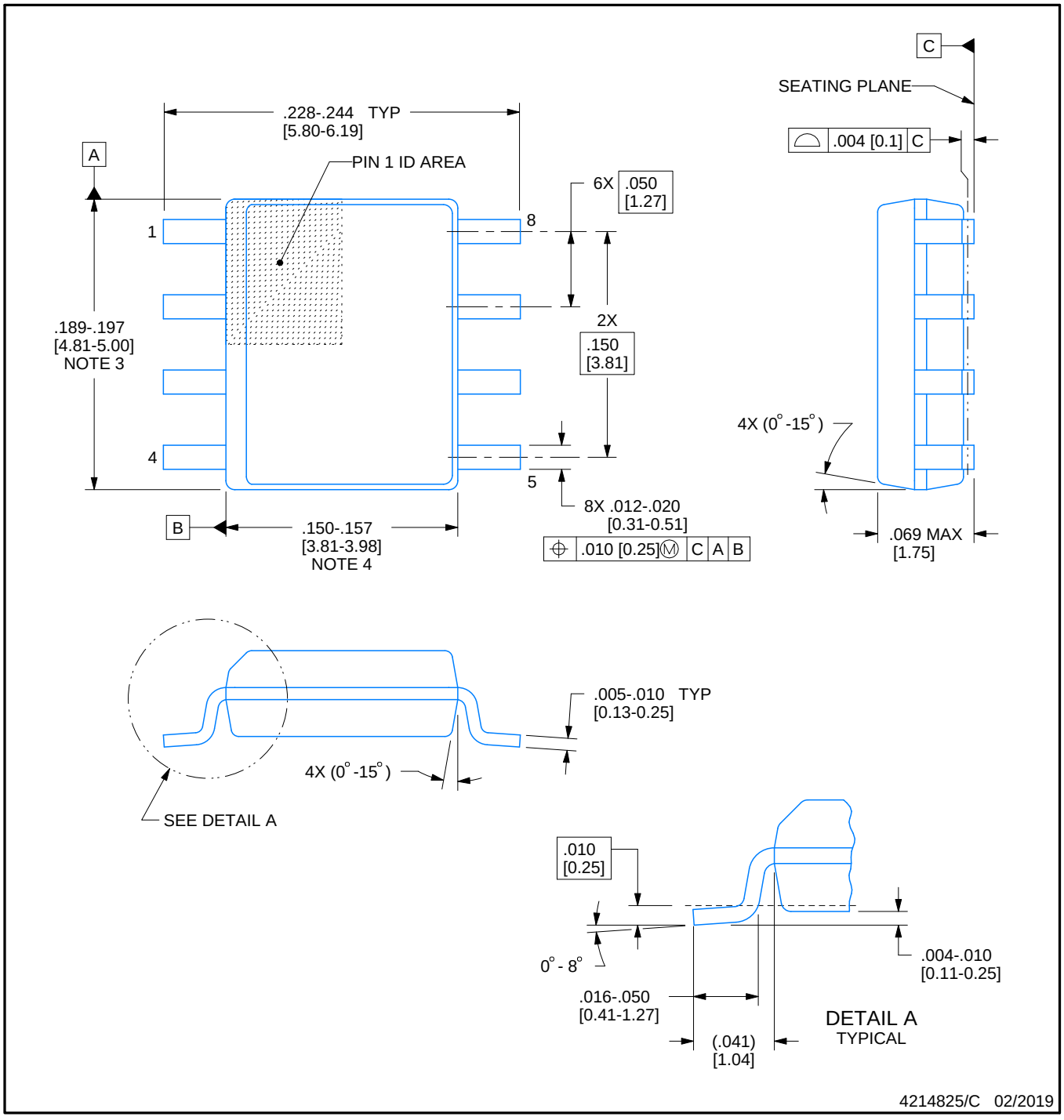


PACKAGE OUTLINE

D0008A

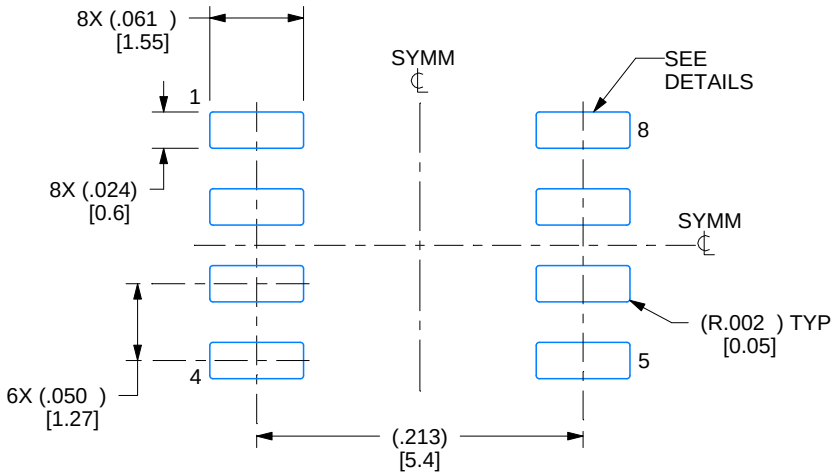
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

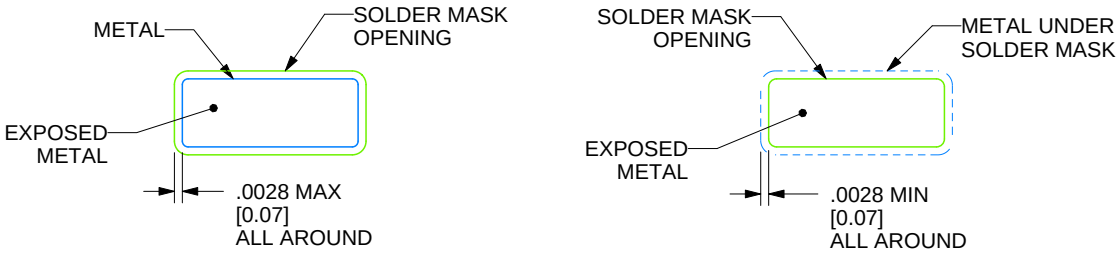


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

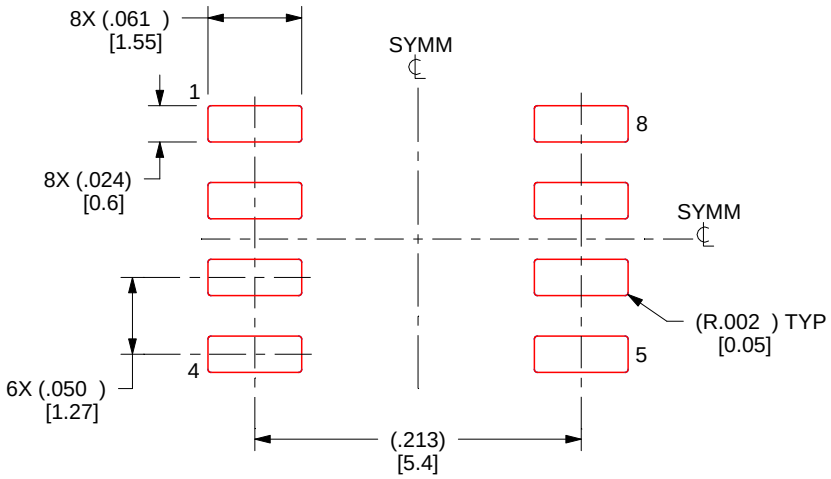
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



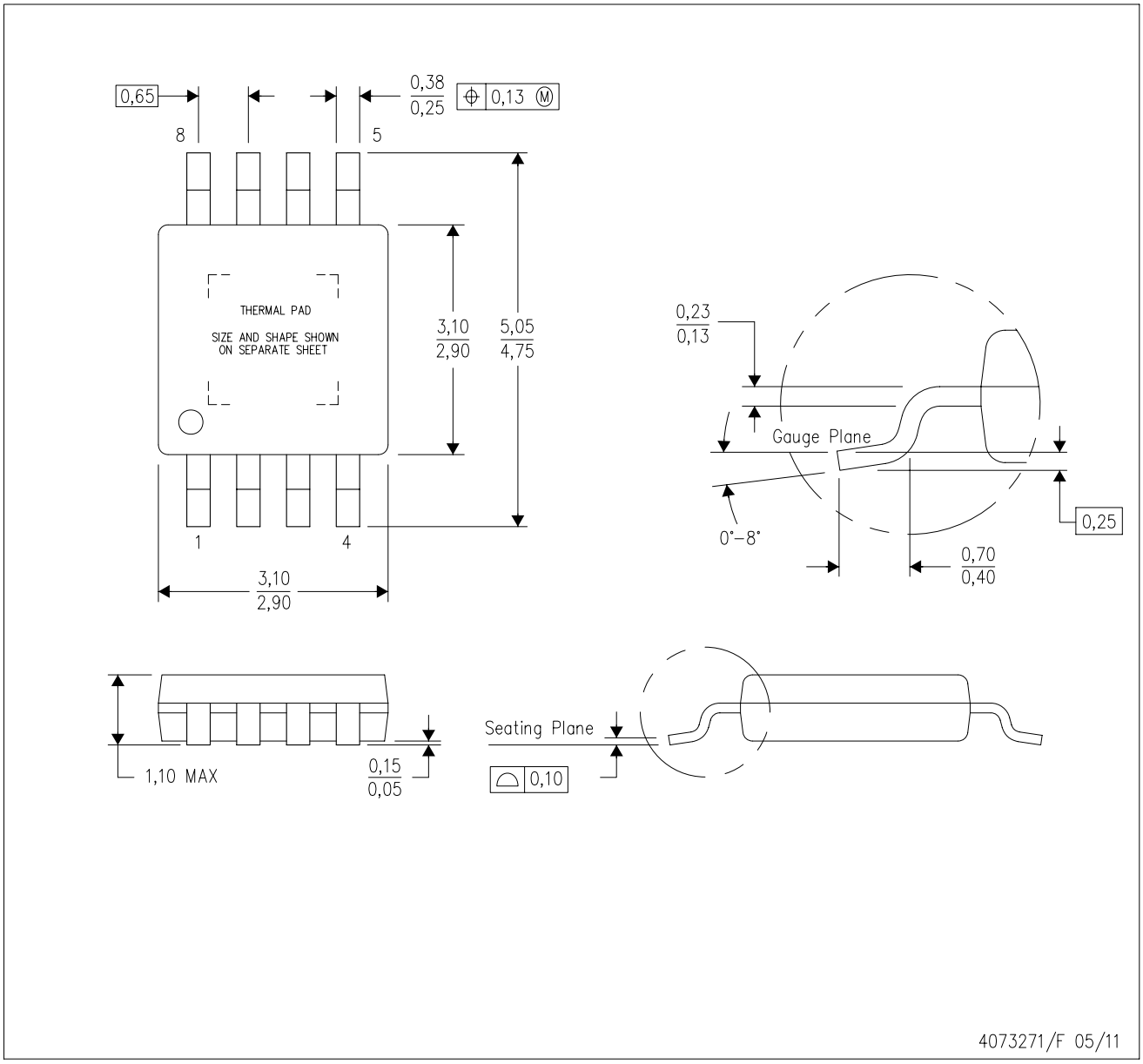
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

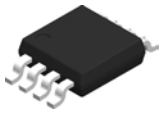


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

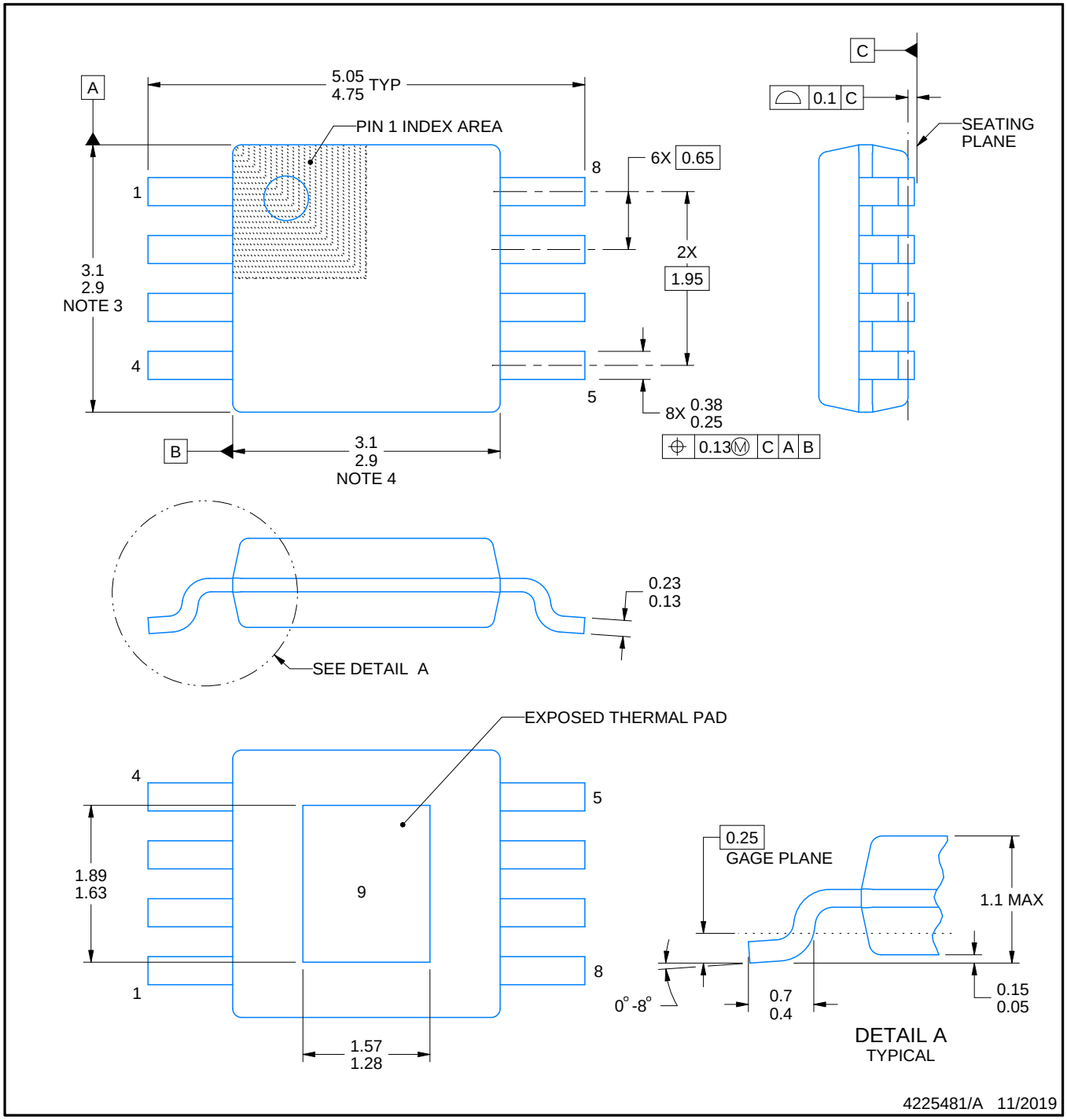
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

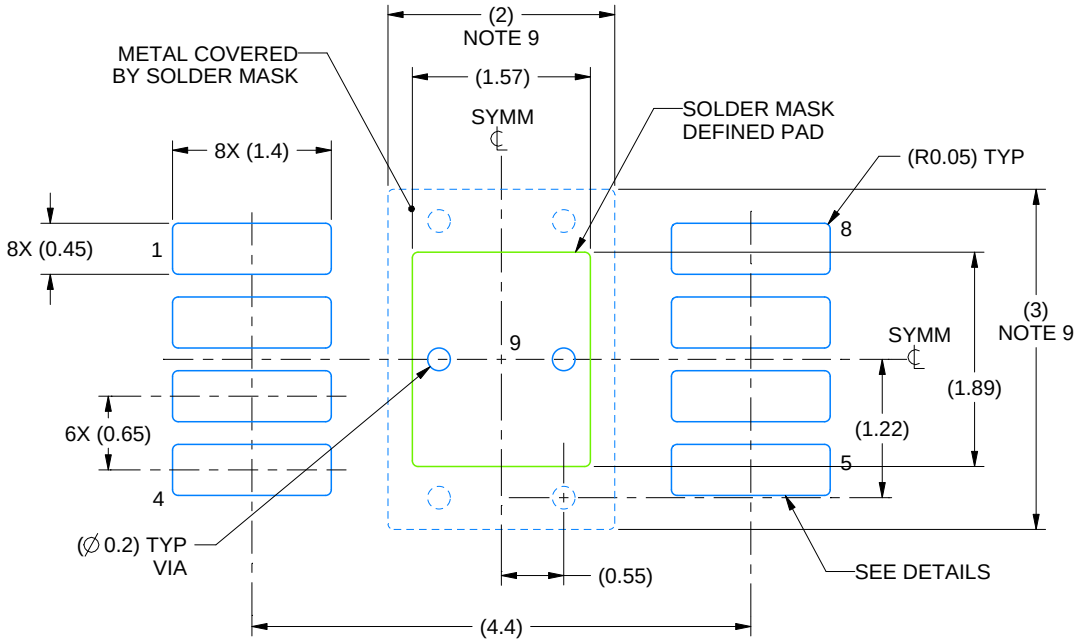
SMALL OUTLINE PACKAGE



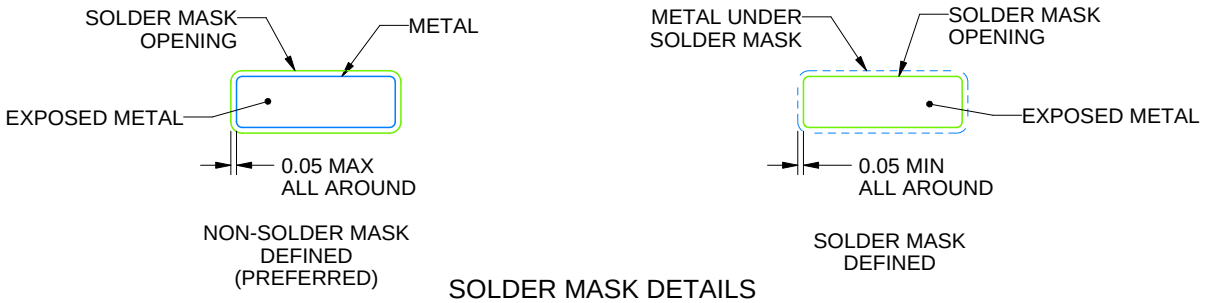
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

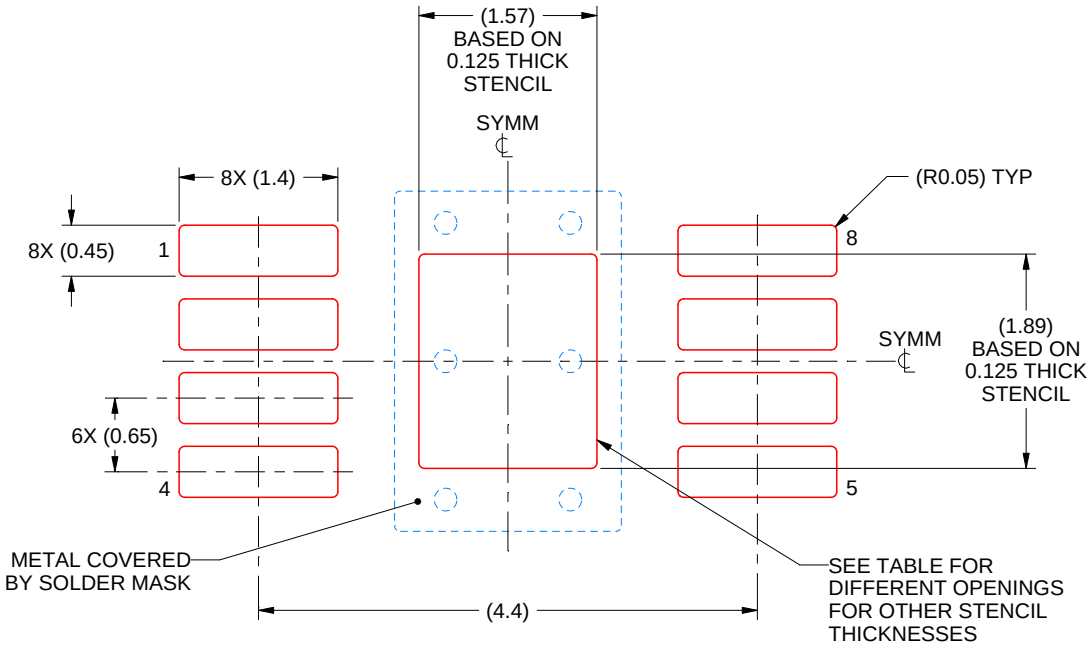


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

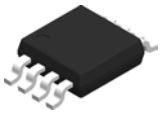
4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

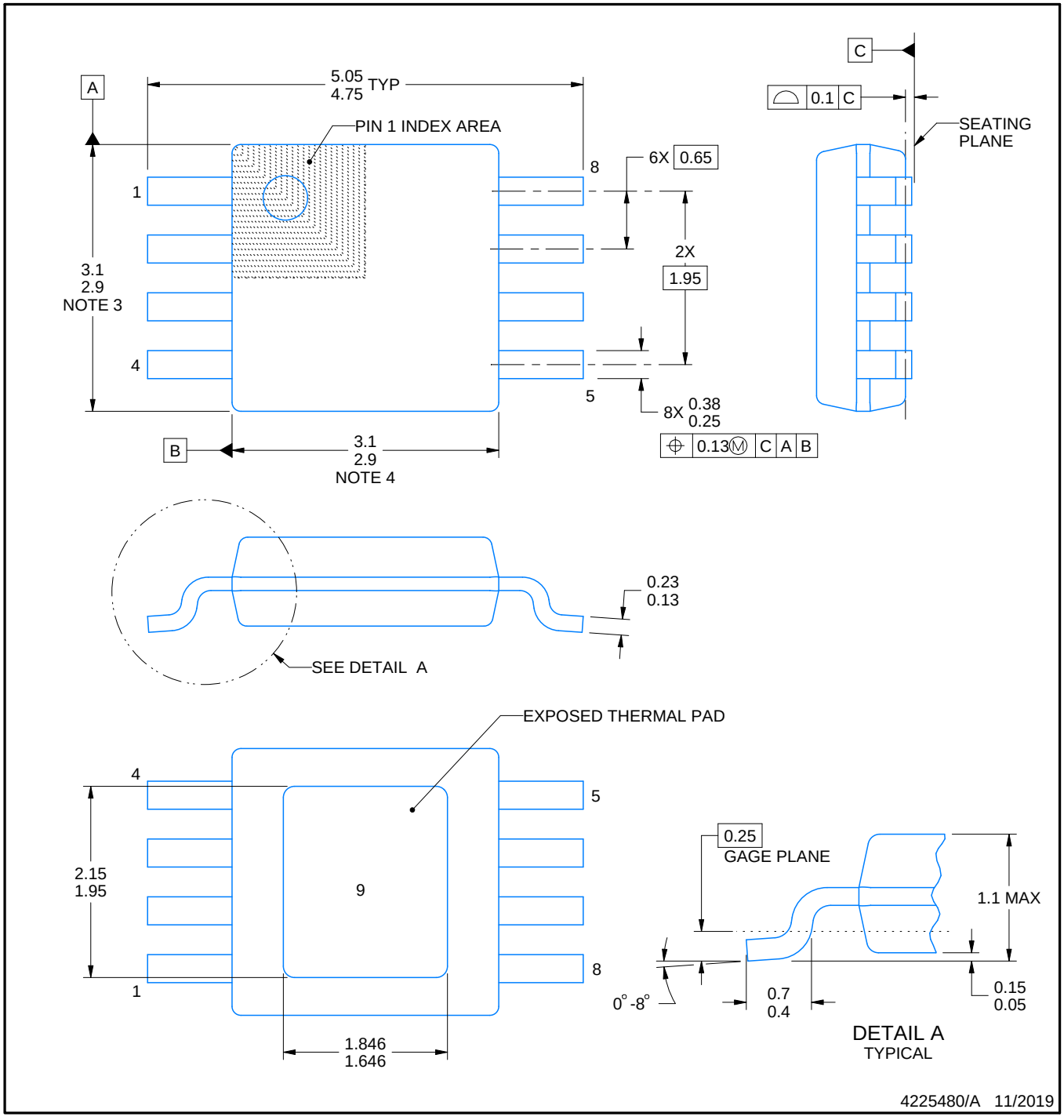
PACKAGE OUTLINE

DGN0008G



PowerPAD™ VSSOP - 1.1 mm max height

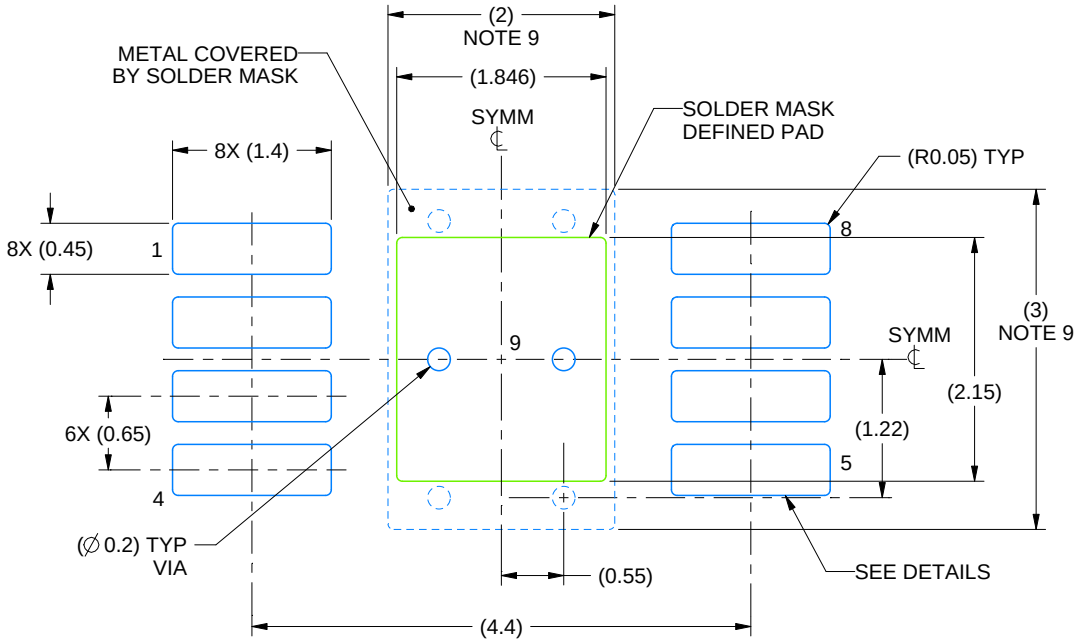
SMALL OUTLINE PACKAGE



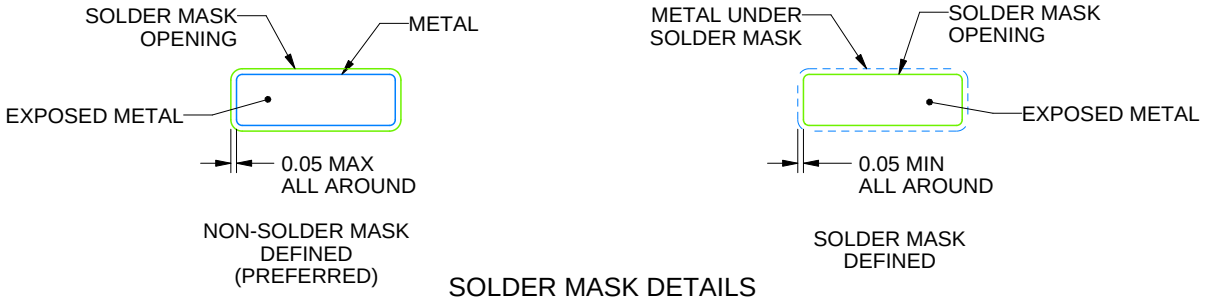
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

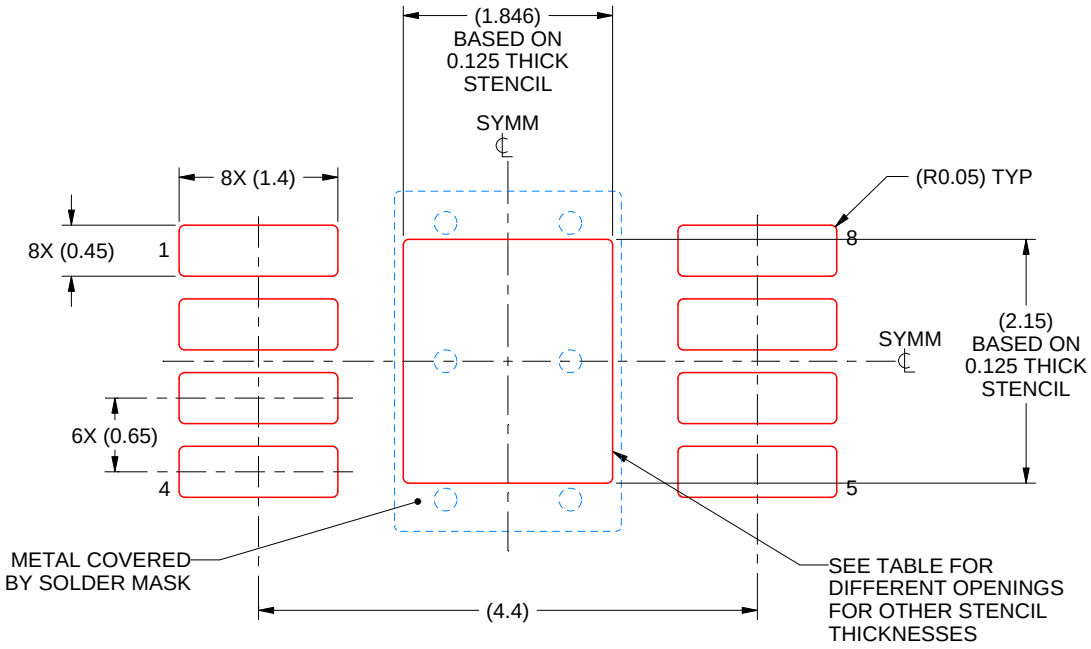


SOLDER MASK DETAILS

4225480/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.06 X 2.40
0.125	1.846 X 2.15 (SHOWN)
0.15	1.69 X 1.96
0.175	1.56 X 1.82

4225480/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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