MCP3421

18-Bit Analog-to-Digital Converter with I²C Interface and On-Board Reference

Features

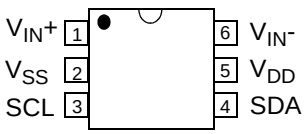
- 18-bit ΔΣ ADC in a SOT-23-6 package
- Differential input operation
- Self calibration of Internal Offset and Gain per each conversion
- On-board Voltage Reference:
  - Accuracy: 2.048V ± 0.05%
  - Drift: 15 ppm/°C
- On-board Programmable Gain Amplifier (PGA):
  - Gains of 1,2, 4 or 8
- On-board Oscillator
- INL: 10 ppm of FSR (FSR = 4.096V/PGA)
- Programmable Data Rate Options:
  - 3.75 SPS (18 bits)
  - 15 SPS (16 bits)
  - 60 SPS (14 bits)
  - 240 SPS (12 bits)
- One-Shot or Continuous Conversion Options
- Low current consumption:
  - 145 µA typical (V_{DD}= 3V, Continuous Conversion)
  - 39 µA typical (V_{DD}= 3V, One-Shot Conversion with 1 SPS)
- Supports I²C Serial Interface:
  - Standard, Fast and High Speed Modes
- Single Supply Operation: 2.7V to 5.5V
- Extended Temperature Range: -40°C to 125°C

Typical Applications

- Portable Instrumentation
- Weigh Scales and Fuel Gauges
- Temperature Sensing with RTD, Thermistor, and Thermocouple
- Bridge Sensing for Pressure, Strain, and Force.

Package Types

SOT-23-6 **Top View**



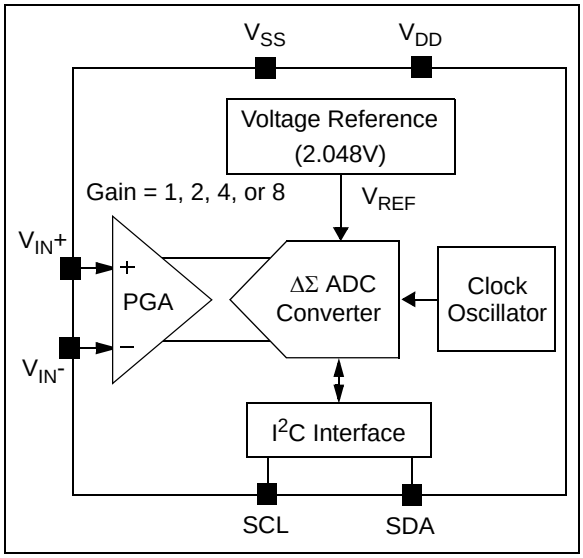
Description

The MCP3421 is a single channel low-noise, high accuracy ΔΣ A/D converter with differential inputs and up to 18 bits of resolution in a small SOT-23-6 package. The on-board precision 2.048V reference voltage enables an input range of ±2.048V differentially (Δ voltage = 4.096V). The device uses a two-wire I²C compatible serial interface and operates from a single 2.7V to 5.5V power supply.

The MCP3421 device performs conversion at rates of 3.75, 15, 60, or 240 samples per second (SPS) depending on the user controllable configuration bit settings using the two-wire I²C serial interface. This device has an on-board programmable gain amplifier (PGA). The user can select the PGA gain of x1, x2, x4, or x8 before the analog-to-digital conversion takes place. This allows the MCP3421 device to convert a smaller input signal with high resolution. The device has two conversion modes: (a) Continuous mode and (b) One-Shot mode. In One-Shot mode, the device enters a low current standby mode automatically after one conversion. This reduces current consumption greatly during idle periods.

The MCP3421 device can be used for various high accuracy analog-to-digital data conversion applications where design simplicity, low power, and small footprint are major considerations.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings†

V_{DD}.....7.0V
All inputs and outputs w.r.t V_{SS} ..... –0.3V to V_{DD}+0.3V
Differential Input Voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current .....Continuous
Current at Input Pins .....±2 mA
Current at Output and Supply Pins .....±10 mA
Storage Temperature.....-65°C to +150°C
Ambient Temp. with power applied .....-55°C to +125°C
ESD protection on all pins ..... ≥ 6 kV HBM, ≥ 400V MM
Maximum Junction Temperature (T_J).....+150°C

†Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.2 Electrical Specifications

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, V_{DD} = +5.0V, V_{SS} = 0V, $V_{IN}+ = V_{IN}- = V_{REF}/2$. All ppm units use $2*V_{REF}$ as full-scale range.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Analog Inputs						
Differential Input Range		—	±2.048/PGA	—	V	$V_{IN} = V_{IN}+ - V_{IN}-$
Common-Mode Voltage Range (absolute) **(Note 1)**		V_{SS}-0.3	—	V_{DD}+0.3	V	
Differential Input Impedance **(Note 2)**	Z_{IND} (f)	—	2.25/PGA	—	MΩ	During normal mode operation
Common Mode input Impedance	Z_{INC} (f)	—	25	—	MΩ	PGA = 1, 2, 4, 8
System Performance						
Resolution and No Missing Codes **(Note 8)**		12	—	—	Bits	DR = 240 SPS
		14	—	—	Bits	DR = 60 SPS
		16	—	—	Bits	DR = 15 SPS
		18	—	—	Bits	DR = 3.75 SPS
Data Rate **(Note 3)**	DR	176	240	328	SPS	S1,S0 = ‘00’, (12 bits mode)
		44	60	82	SPS	S1,S0 = ‘01’, (14 bits mode)
		11	15	20.5	SPS	S1,S0 = ‘10’, (16 bits mode)
		2.75	3.75	5.1	SPS	S1,S0 = ‘11’, (18 bits mode)
Output Noise		—	1.5	—	μV_{RMS}	T_A = 25°C, DR = 3.75 SPS, PGA = 1, V_{IN} = 0
Integral Nonlinearity **(Note 4)**	INL	—	10	35	ppm of FSR	DR = 3.75 SPS **(Note 6)**
Internal Reference Voltage	V_{REF}	—	2.048	—	V	
Gain Error **(Note 5)**		—	0.05	0.35	%	PGA = 1, DR = 3.75 SPS

Note 1: Any input voltage below or greater than this voltage causes leakage current through the ESD diodes at the input pins. This parameter is ensured by characterization and not 100% tested.
2: This input impedance is due to 3.2 pF internal input sampling capacitor.
3: The total conversion speed includes auto-calibration of offset and gain.
4: INL is the difference between the endpoints line and the measured code at the center of the quantization band.
5: Includes all errors from on-board PGA and V_{REF}.
6: Full Scale Range (FSR) = 2 x 2.048/PGA = 4.096/PGA.
7: This parameter is ensured by characterization and not 100% tested.
8: This parameter is ensured by design and not 100% tested.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, V_{DD} = +5.0V, V_{SS} = 0V, $V_{IN}+ = V_{IN}- = V_{REF}/2$. All ppm units use $2*V_{REF}$ as full-scale range.

Parameters	Sym	Min	Typ	Max	Units	Conditions
PGA Gain Error Match (Note 5)		—	0.1	—	%	Between any 2 PGA gains
Gain Error Drift (Note 5)		—	15	—	ppm/°C	PGA=1, DR=3.75 SPS
Offset Error	V_{OS}	—	15	40	µV	Tested at PGA = 1 V_{DD} = 5.0V and DR = 3.75 SPS
Offset Drift vs. Temperature		—	50	—	nV/°C	V_{DD} = 5.0V
Common-Mode Rejection		—	105	—	dB	at DC and PGA =1,
		—	110	—	dB	at DC and PGA =8, T_A = +25°C
Gain vs. V_{DD}		—	5	—	ppm/V	T_A = +25°C, V_{DD} = 2.7V to 5.5V, PGA = 1
Power Supply Rejection at DC		—	100	—	dB	T_A = +25°C, V_{DD} = 2.7V to 5.5V, PGA = 1
Power Requirements						
Voltage Range	V_{DD}	2.7	—	5.5	V	
Supply Current during Conversion	I_{DDA}	—	155	190	µA	V_{DD} = 5.0V
		—	145	—	µA	V_{DD} = 3.0V
Supply Current during Standby Mode	I_{DDS}	—	0.1	0.5	µA	
I^2C Digital Inputs and Digital Outputs						
High level input voltage	V_{IH}	0.7 V_{DD}	—	V_{DD}	V	
Low level input voltage	V_{IL}	—	—	$0.3V_{DD}$	V	
Low level output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 3 mA, V_{DD} = +5.0V
Hysteresis of Schmitt Trigger for inputs (Note 7)	V_{HYST}	$0.05V_{DD}$	—	—	V	f_{SCL} = 100 kHz
Supply Current when I^2C bus line is active	I_{DDB}	—	—	10	µA	
Input Leakage Current	I_{ILH}	—	—	1	µA	V_{IH} = 5.5V
	I_{ILL}	-1	—	—	µA	V_{IL} = GND
Pin Capacitance and I^2C Bus Capacitance						
Pin capacitance	C_{PIN}	—	—	10	pF	
I^2C Bus Capacitance	C_b	—	—	400	pF	
Thermal Characteristics						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	

Note 1: Any input voltage below or greater than this voltage causes leakage current through the ESD diodes at the input pins. This parameter is ensured by characterization and not 100% tested.

2: This input impedance is due to 3.2 pF internal input sampling capacitor.

3: The total conversion speed includes auto-calibration of offset and gain.

4: INL is the difference between the endpoints line and the measured code at the center of the quantization band.

5: Includes all errors from on-board PGA and V_{REF}.

6: Full Scale Range (FSR) = 2 x 2.048/PGA = 4.096/PGA.

7: This parameter is ensured by characterization and not 100% tested.

8: This parameter is ensured by design and not 100% tested.

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = -40°C to +85°C, V_{DD} = +5.0V, V_{SS} = 0V, $V_{IN}+ = V_{IN}- = V_{REF}/2$.

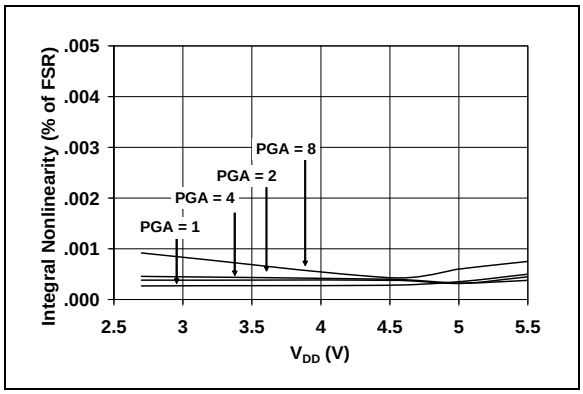


FIGURE 2-1: *INL vs. Supply Voltage (V_{DD}).*

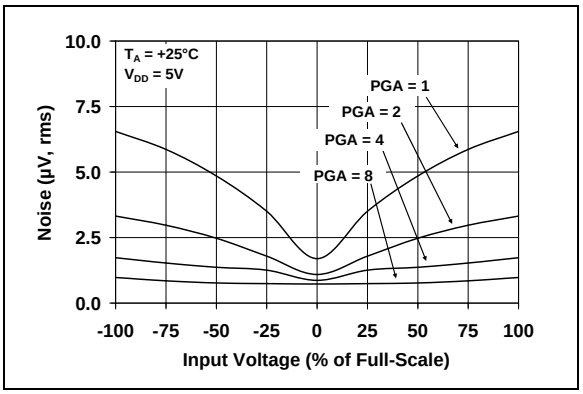


FIGURE 2-4: *Noise vs. Input Voltage.*

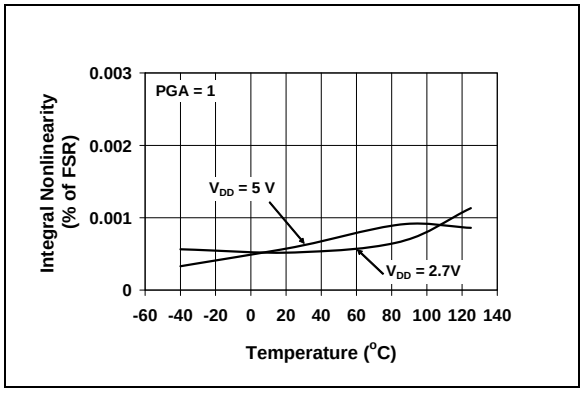


FIGURE 2-2: *INL vs. Temperature.*

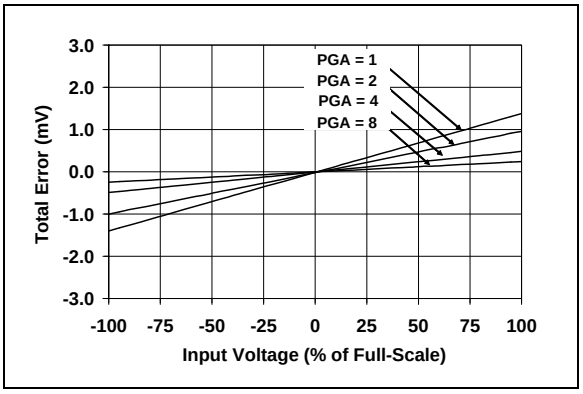


FIGURE 2-5: *Total Error vs. Input Voltage.*

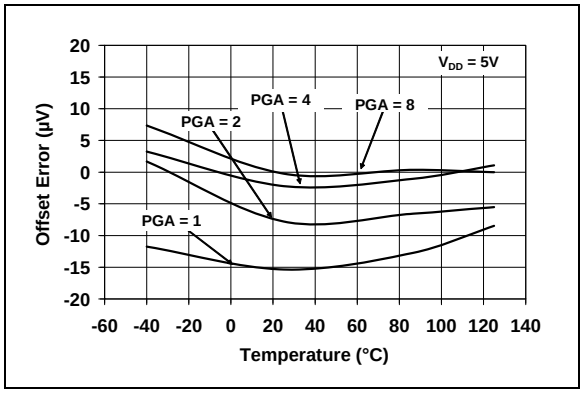


FIGURE 2-3: *Offset Error vs. Temperature.*

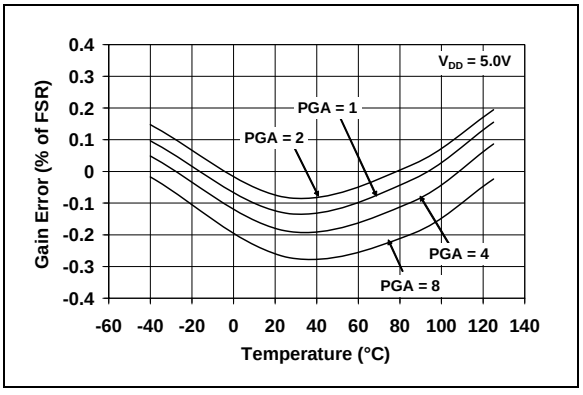


FIGURE 2-6: *Gain Error vs. Temperature.*

Note: Unless otherwise indicated, T_A = -40°C to +85°C, V_{DD} = +5.0V, V_{SS} = 0V, $V_{IN}+ = V_{IN}- = V_{REF}/2$.

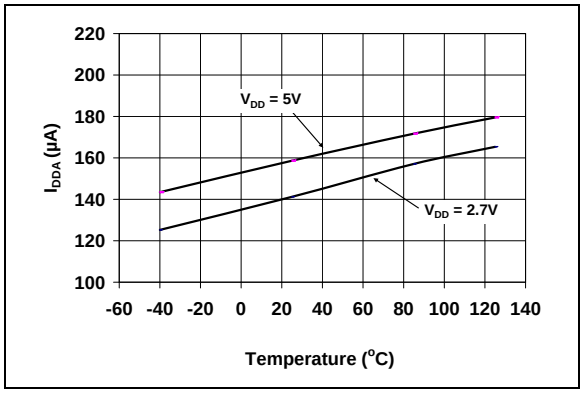


FIGURE 2-7: *I_{DDA} vs. Temperature.*

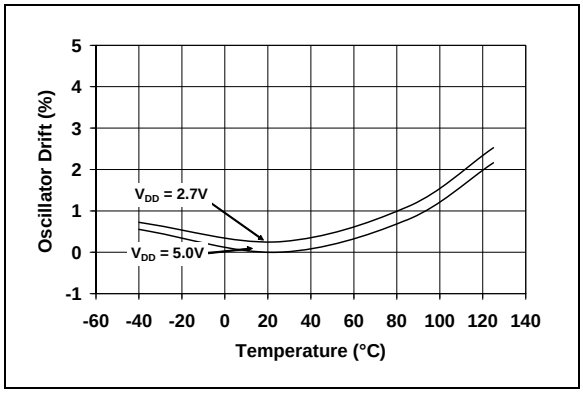


FIGURE 2-10: *OSC Drift vs. Temperature.*

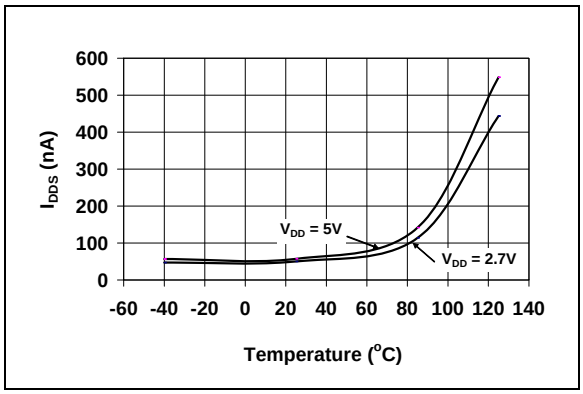


FIGURE 2-8: *I_{DDS} vs. Temperature.*

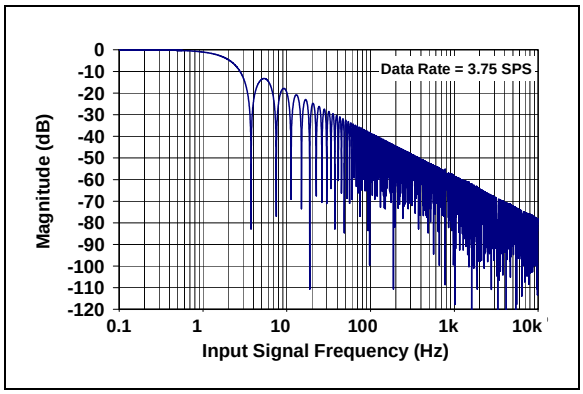


FIGURE 2-11: *Frequency Response.*

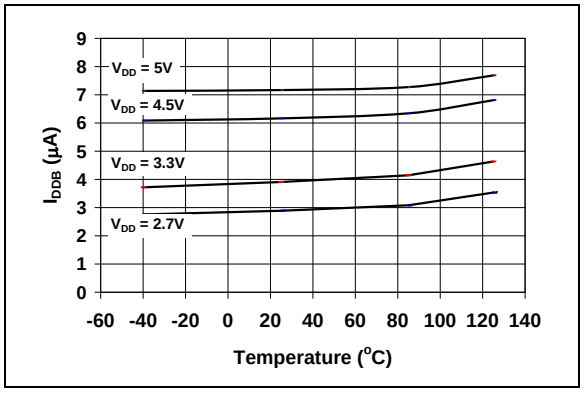


FIGURE 2-9: *I_{DDB} vs. Temperature.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No	Sym	Function
1	$V_{IN}+$	Non-Inverting Analog Input Pin
2	V_{SS}	Ground Pin
3	SCL	Serial Clock Input Pin of the I^2C Interface
4	SDA	Bidirectional Serial Data Pin of the I^2C Interface
5	V_{DD}	Positive Supply Voltage Pin
6	$V_{IN}-$	Inverting Analog Input Pin

3.1 Analog Inputs ($V_{IN}+$, $V_{IN}-$)

$V_{IN}+$ and $V_{IN}-$ are differential signal input pins. The MCP3421 device accepts a fully differential analog input signal which is connected on the $V_{IN}+$ and $V_{IN}-$ input pins. The differential voltage that is converted is defined by $V_{IN} = (V_{IN}+ - V_{IN}-)$ where $V_{IN}+$ is the voltage applied at the $V_{IN}+$ pin and $V_{IN}-$ is the voltage applied at the $V_{IN}-$ pin. The input signal level is amplified by the programmable gain amplifier (PGA) before the conversion. The differential input voltage should not exceed an absolute of (V_{REF}/PGA) for accurate measurement, where V_{REF} is the internal reference voltage (2.048V) and PGA is the PGA gain setting. The converter output code will saturate if the input range exceeds (V_{REF}/PGA).

The absolute voltage range on each of the differential input pins is from V_{SS}-0.3V to V_{DD}+0.3V. Any voltage above or below this range will cause leakage currents through the Electrostatic Discharge (ESD) diodes at the input pins. This ESD current can cause unexpected performance of the device. The common mode of the analog inputs should be chosen such that both the differential analog input range and the absolute voltage range on each pin are within the specified operating range defined in **Section 1.0 "Electrical Characteristics"** and **Section 4.0 "Description of Device Operation"**.

3.2 Supply Voltage (V_{DD}, V_{SS})

V_{DD} is the power supply pin for the device. This pin requires an appropriate bypass capacitor of about 0.1 µF (ceramic) to ground. An additional 10 µF capacitor (tantalum) in parallel is also recommended to further attenuate high frequency noise present in some application boards. The supply voltage (V_{DD}) must be maintained in the 2.7V to 5.5V range for specified operation.

V_{SS} is the ground pin and the current return path of the device. The user must connect the V_{SS} pin to a ground plane through a low impedance connection. If an analog ground path is available in the application PCB (printed circuit board), it is highly recommended that the V_{SS} pin be tied to the analog ground path or isolated within an analog ground plane of the circuit board.

3.3 Serial Clock Pin (SCL)

SCL is the serial clock pin of the I^2C interface. The MCP3421 acts only as a slave and the SCL pin accepts only external serial clocks. The input data from the Master device is shifted into the SDA pin on the rising edges of the SCL clock and output from the MCP3421 occurs at the falling edges of the SCL clock. The SCL pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor from the V_{DD} line to the SCL pin. Refer to **Section 5.3 "I^2C Serial Communications"** for more details of I^2C Serial Interface communication.

3.4 Serial Data Pin (SDA)

SDA is the serial data pin of the I^2C interface. The SDA pin is used for input and output data. In read mode, the conversion result is read from the SDA pin (output). In write mode, the device configuration bits are written (input) though the SDA pin. The SDA pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor from the V_{DD} line to the SDA pin. Except for start and stop conditions, the data on the SDA pin must be stable during the high period of the clock. The high or low state of the SDA pin can only change when the clock signal on the SCL pin is low. Refer to **Section 5.3 "I^2C Serial Communications"** for more details of I^2C Serial Interface communication.

4.0 DESCRIPTION OF DEVICE OPERATION

4.1 General Overview

The MCP3421 is a low-power, 18-Bit Delta-Sigma A/D converter with an I^2C serial interface. The device contains an on-board voltage reference (2.048V), programmable gain amplifier (PGA), and internal oscillator. The user can select 12, 14, 16, or 18 bit conversion by setting the configuration register bits. The device can be operated in Continuous Conversion or One-Shot Conversion mode. In the Continuous Conversion mode, the device converts the inputs continuously. While in the One-Shot Conversion mode, the device converts the input one time and stays in the low-power standby mode until it receives another command for a new conversion. During the standby mode, the device consumes less than 0.1 µA typical.

4.2 Power-On-Reset (POR)

The device contains an internal Power-On-Reset (POR) circuit that monitors power supply voltage (V_{DD}) during operation. This circuit ensures correct device start-up at system power-up and power-down events. The POR has built-in hysteresis and a timer to give a high degree of immunity to potential ripples and noises on the power supply. A 0.1 µF decoupling capacitor should be mounted as close as possible to the V_{DD} pin for additional transient immunity.

The threshold voltage is set at 2.2V with a tolerance of approximately ±5%. If the supply voltage falls below this threshold, the device will be held in a reset condition. The typical hysteresis value is approximately 200 mV.

The POR circuit is shut-down during the low-power standby mode. Once a power-up event has occurred, the device requires additional delay time (approximately 300 µs) before a conversion can take place. During this time, all internal analog circuitries are settled before the first conversion occurs. Figure 4-1 illustrates the conditions for power-up and power-down events under typical start-up conditions.

When the device powers up, it automatically resets and sets the configuration bits to default settings. The default configuration bit conditions are a PGA gain of 1 V/V and a conversion speed of 240 SPS in Continuous Conversion mode. When the device receives an I^2C General Call Reset command, it performs an internal reset similar to a Power-On-Reset event.

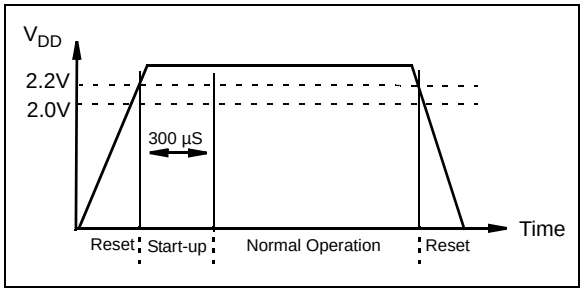


FIGURE 4-1: *POR Operation.*

4.3 Internal Voltage Reference

The device contains an on-board 2.048V voltage reference. This reference voltage is for internal use only and not directly measurable. The specifications of the reference voltage are part of the device's gain and drift specifications. Therefore, there is no separate specification for the on-board reference.

4.4 Analog Input Channel

The differential analog input channel has a switched capacitor structure. The internal sampling capacitor (3.2 pF) is charged and discharged to process a conversion. The charging and discharging of the input sampling capacitor creates dynamic input currents at the V_{IN}+ and V_{IN}- input pins, which is inversely proportional to the internal sampling capacitor and internal frequency. The current is also a function of the differential input voltages. Care must be taken in setting the common-mode voltage and input voltage ranges so that the input limits do not exceed the ranges specified in **Section 1.0 "Electrical Characteristics"**.

4.5 Digital Output Code

The digital output code produced by the MCP3421 is a function of PGA gain, input signal, and internal reference voltage. In a fixed setting, the digital output code is proportional to the voltage difference between the two analog inputs.

The output data format is a binary two's complement. With this code scheme, the MSB can be considered a sign indicator. When the MSB is a logic '0', it indicates a positive value. When the MSB is a logic '1', it indicates a negative value. The following is an example of the output code:

(a) for a negative full-scale input voltage: 100...000

(b) for a zero differential input voltage: 000...000

(c) for a positive full-scale input voltage: 011...111.

The MSB is always transmitted first through the serial port. The number of data bits for each conversion is 18, 16, 14, or 12 bits depending on the conversion mode selection.

The output codes will not roll-over if the input voltage exceeds the maximum input range. In this case, the code will be locked at 0111...11 for all voltages greater than +(V_{REF} - 1 LSB) and 1000...00 for voltages less than -V_{REF}. Table 4-2 shows an example of output codes of various input levels using 18 bit conversion mode. Table 4-3 shows an example of minimum and maximum codes for each data rate option.

The output code is given by:

EQUATION 4-1:

$$Output\ Code = (Max\ Code + 1) \times \frac{(V_{IN}+ - V_{IN}-)}{2.048V}$$

The LSB of the code is given by:

EQUATION 4-2:

$$LSB = \frac{2 \times 2.048V}{2^N}$$

Where:

N = number of bits

TABLE 4-1: LSB SIZE OF VARIOUS BIT CONVERSION MODES

Bit Resolutions	LSB (V)
12 bits	1 mV
14 bits	250 µV
16 bits	62.5 µV
18 bits	15.625 µV

TABLE 4-2: EXAMPLE OF OUTPUT CODE FOR 18 BITS

Input Voltage (V)	Digital Code
≥ V_{REF}	011111111111111111
V_{REF} - 1 LSB	011111111111111111
2 LSB	000000000000000010
1 LSB	000000000000000001
0	000000000000000000
-1 LSB	111111111111111111
-2 LSB	111111111111111110
- V_{REF}	100000000000000000
< -V_{REF}	100000000000000000

TABLE 4-3: MINIMUM AND MAXIMUM CODES

Number of Bits	Data Rate	Minimum Code	Maximum Code
12	240 SPS	-2048	2047
14	60 SPS	-8192	8191
16	15 SPS	-32768	32767
18	3.75 SPS	-131072	131071

Note: Maximum n-bit code = 2^{n-1} - 1
Minimum n-bit code = -1 x 2^{n-1}

4.6 Self-Calibration

The device performs a self-calibration of offset and gain for each conversion. This provides reliable conversion results from conversion-to-conversion over variations in temperature as well as power supply fluctuations.

4.7 Input Impedance

The MCP3421 uses a switched-capacitor input stage using a 3.2 pF sampling capacitor. This capacitor is switched (charged and discharged) at a rate of the sampling frequency that is generated by the on-board clock. The differential mode impedance varies with the PGA settings. The typical differential input impedance during a normal mode operation is given by:

$$Z_{IN}(f) = 2.25\ M\Omega/PGA$$

Since the sampling capacitor is only switching to the input pins during a conversion process, the above input impedance is only valid during conversion periods. In a low power standby mode, the above impedance is not presented at the input pins. Therefore, only a leakage current due to ESD diode is presented at the input pins.

The conversion accuracy can be affected by the input signal source impedance when any external circuit is connected to the input pins. The source impedance adds to the internal impedance and directly affects the time required to charge the internal sampling capacitor. Therefore, a large input source impedance connected to the input pins can increase the system performance errors such as offset, gain, and integral nonlinearity (INL) errors. Ideally, the input source impedance should be zero. This can be achievable by using an operational amplifier with a closed-loop output impedance of tens of ohms.

4.8 Aliasing and Anti-aliasing Filter

Aliasing occurs when the input signal contains time-varying signal components with frequency greater than half the sample rate. In the aliasing conditions, the device can output unexpected output codes. For applications that are operating in electrical noise environments, the time-varying signal noise or high frequency interference components can be easily added to the input signals and cause aliasing. Although the MCP3421 device has an internal first order sinc filter, its' filter response may not give enough attenuation to all aliasing signal components. To avoid the aliasing, an external anti-aliasing filter, which can be accomplished with a simple RC low-pass filter, is typically used at the input pins. The low-pass filter cuts off the high frequency noise components and provides a band-limited input signal to the MCP3421 input pins.

5.0 USING THE MCP3421 DEVICE

5.1 Operating Modes

The user operates the device by setting up the device configuration register and reads the conversion data using serial I^2C interface commands. The MCP3421 operates in two modes: (a) Continuous Conversion Mode or (b) One-Shot Conversion Mode (single conversion). The selection is made by setting the $\overline{O}$/C bit in the Configuration Register. Refer to **Section 5.2 "Configuration Register"** for more information.

5.1.1 CONTINUOUS CONVERSION MODE ($\overline{O}$/C BIT = 1)

The MCP3421 device performs a Continuous Conversion if the $\overline{O}$/C bit is set to logic "high". Once the conversion is completed, the result is placed at the output data register. The device immediately begins another conversion and overwrites the output data register with the most recent data.

The device also clears the data ready flag ($\overline{RDY}$ bit = 0) when the conversion is completed. The device sets the ready flag bit ($\overline{RDY}$ bit = 1), if the latest conversion result has been read by the Master.

5.1.2 ONE-SHOT CONVERSION MODE ($\overline{O}$/C BIT = 0)

Once the One-Shot Conversion (single conversion) Mode is selected, the device performs a conversion, updates the Output Data register, clears the data ready flag ($\overline{RDY}$ = 0), and then enters a low power standby mode. A new One-Shot Conversion is started again when the device receives a new write command with $\overline{RDY}$ = 1.

This One-Shot Conversion Mode is recommended for low power operating applications. During the low current standby mode, the device consumes less than 1 µA typical. For example, if user collects 18 bit conversion data once a second in One-Shot Conversion mode, the device draws only about one fourth of its total operating current. In this example, the device consumes approximately 39 µA (= ~145 µA/3.75 SPS), if the device performs only one conversion per second (1 SPS) in 18-bit conversion mode with 3V power supply.

5.2 Configuration Register

The MCP3421 has an 8-bit wide configuration register to select for: PGA gain, conversion rate, and conversion mode. This register allows the user to change the operating condition of the device and check the status of the device operation. The user can rewrite the configuration byte any time during the device operation. Register 5-1 shows the configuration register bits.

REGISTER 5-1: CONFIGURATION REGISTER

R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
$\overline{RDY}$	C1	C0	$\overline{O}$/C	S1	S0	G1	G0
1 *	0 *	0 *	1 *	0 *	0 *	0 *	0 *
bit 7							bit 0

* Default Configuration after Power-On Reset

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{RDY}$:** Ready Bit

This bit is the data ready flag. In read mode, this bit indicates if the output register has been updated with a new conversion. In One-Shot Conversion mode, writing this bit to "1" initiates a new conversion.

Reading RDY bit with the read command:

1 = Output register has not been updated.
0 = Output register has been updated with the latest conversion data.

Writing $\overline{RDY}$ bit with the write command:

Continuous Conversion mode: No effect

One-Shot Conversion mode:
1 = Initiate a new conversion.
0 = No effect.

bit 6-5 **C1-C0:** Channel Selection Bits

These are the Channel Selection bits, but not used in the MCP3421 device.

bit 4 **$\overline{O}$/C:** Conversion Mode Bit

1 = Continuous Conversion Mode. Once this bit is selected, the device performs data conversions continuously.
0 = One-Shot Conversion Mode. The device performs a single conversion and enters a low power standby mode until it receives another write/read command.

bit 3-2 **S1-S0:** Sample Rate Selection Bit

00 = 240 SPS (12 bits),
01 = 60 SPS (14 bits),
10 = 15 SPS (16 bits),
11 = 3.75 SPS (18 bits)

bit 1-0 **G1-G0:** PGA Gain Selector Bits

00 = 1 V/V,
01 = 2 V/V,
10 = 4 V/V,
11 = 8 V/V

In read mode, the $\overline{RDY}$ bit in the configuration byte indicates the state of the conversion: (a) $\overline{RDY}$ = 1 indicates that the data bytes that have just been read were not updated from the previous conversion. (b) $\overline{RDY}$ = 0 indicates that the data bytes that have just been read were updated.

If the configuration byte is read repeatedly by clocking continuously after the first read (i.e., after the 5th byte in the 18-bit conversion mode), the state of the $\overline{RDY}$ bit indicates whether the device is ready with new conversion data. See Figure 5-2. For example, $\overline{RDY}$ = 0 means new conversion data is ready for reading. In this case, the user can send a stop bit to exit the current read operation and send a new read command to read out updated conversion data. See Figures 5-2 and 5-3 for reading conversion data. The user can rewrite the configuration byte any time for a new setting. Tables 5-1 and 5-2 show the examples of the configuration bit operation.

TABLE 5-1: CONFIGURATION BITS FOR WRITING

R/$\overline{W}$	$\overline{O}$/C	$\overline{RDY}$	Operation
0	0	0	No effect if all other bits remain the same - operation continues with the previous settings
0	0	1	Initiate One-Shot Conversion
0	1	0	Initiate Continuous Conversion
0	1	1	Initiate Continuous Conversion

TABLE 5-2: CONFIGURATION BITS FOR READING

R/$\overline{W}$	$\overline{O}$/C	$\overline{RDY}$	Operation
1	0	0	New conversion data in One-Shot conversion mode has been just read. The $\overline{RDY}$ bit remains low until set by a new write command.
1	0	1	One-Shot Conversion is in progress, The conversion data is not updated yet. The $\overline{RDY}$ bit stays high.
1	1	0	New conversion data in Continuous Conversion mode has been just read. The $\overline{RDY}$ bit changes to high after this read.
1	1	1	The conversion data in Continuous Conversion mode was already read. The latest conversion data is not ready. The $\overline{RDY}$ bit stays high until a new conversion is completed.

5.3 I²C Serial Communications

The MCP3421 device communicates with Master (microcontroller) through a serial I²C (Inter-Integrated Circuit) interface and supports standard (100 kbits/sec), fast (400 kbits/sec) and high-speed (3.4 Mbits/sec) modes. The serial I²C is a bidirectional 2-wire data bus communication protocol using open-drain SCL and SDA lines.

The MCP3421 can only be addressed as a slave. Once addressed, it can receive configuration bits or transmit the latest conversion results. The serial clock pin (SCL) is an input only and the serial data pin (SDA) is bidirectional. An example of a hardware connection diagram is shown in Figure 6-1.

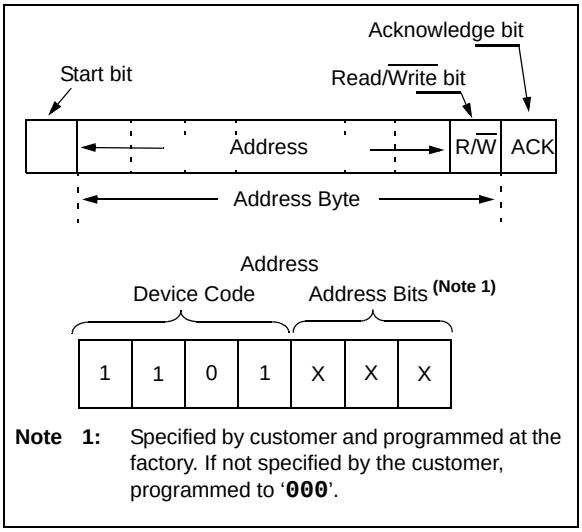
The Master starts communication by sending a START bit and terminates the communication by sending a STOP bit. The first byte after the START bit is always the address byte of the device, which includes the device code, the address bits, and the R/$\overline{W}$ bit. The device code for the MCP3421 device is **1101**. The address bits (A2, A1, A0) are pre-programmed at the factory. In general, the address bits are specified by the customer when they order the device. The three address bits are programmed to "**000**" at the factory, if they are not specified by the customer. Figure 5-1 shows the details of the MCP3421 address byte.

During a low power standby mode, SDA and SCL pins remain at a floating condition.

More details of the I²C bus characteristic is described in **Section 5.6 "I²C Bus Characteristics"**.

5.3.1 DEVICE ADDRESSING

The address byte is the first byte received following the START condition from the Master device. The MCP3421 device code is **1101**. The device code is followed by three address bits (A2, A1, A0) which are programmed at the factory. The three address bits allow up to eight MCP3421 devices on the same data bus line. The (R/$\overline{W}$) bit determines if the Master device wants to read the conversion data or write to the Configuration register. If the (R/$\overline{W}$) bit is set (read mode), the MCP3421 outputs the conversion data in the following clocks. If the (R/$\overline{W}$) bit is cleared (write mode), the MCP3421 expects a configuration byte in the following clocks. When the MCP3421 receives the correct address byte, it outputs an acknowledge bit after the R/$\overline{W}$ bit. Figure 5-1 shows the MCP3421 address byte. See Figures 5-2 and 5-3 for the read and write operations of the device.



Note 1: Specified by customer and programmed at the factory. If not specified by the customer, programmed to '**000**'.

FIGURE 5-1: *MCP3421 Address Byte.*

5.3.2 READING DATA FROM THE DEVICE

When the Master sends a read command (R/$\overline{W}$ = 1), the MCP3421 outputs the conversion data bytes and configuration byte. Each byte consists of 8 bits with one acknowledge (ACK) bit. The ACK bit after the address byte is issued by the MCP3421 and the ACK bits after each conversion data bytes are issued by the Master.

When the device is configured for 18-bit conversion mode, the device outputs three data bytes followed by a configuration byte. The first 7 data bits in the first data byte are the MSB of the conversion data. The user can ignore the first 6 data bits, and take the 7th data bit (D17) as the MSB of the conversion data. The LSB of the 3rd data byte is the LSB of the conversion data (D0).

If the device is configured for 12, 14, or 16 bit-mode, the device outputs two data bytes followed by a configuration byte. In 16 bit-conversion mode, the MSB of the first data byte is the MSB (D15) of the conversion data. In 14-bit conversion mode, the first two bits in the first data byte can be ignored (they are the MSB of the conversion data), and the 3rd bit (D13) is the MSB of the conversion data. In 12-bit conversion mode, the first four bits can be ignored (they are the MSB of the conversion data), and the 5th bit (D11) of the byte represents the MSB of the conversion data. Table 5-3 shows an example of the conversion data output of each conversion mode.

The configuration byte follows the output data byte. The device outputs the configuration byte as long as the SCL pulses are received. The device terminates the current outputs when it receives a Not-Acknowledge (NAK), a repeated start or a stop bit at any time during the output bit stream. It is not required to read the configuration byte. However, the user may read the configuration byte to check the $\overline{RDY}$ bit condition to confirm whether the just received data bytes are updated conversion data. The user may continuously send clock (SCL) to repeatedly read the configuration bytes to check the $\overline{RDY}$ bit status.

Figures 5-2 and 5-3 show the timing diagrams of the reading.

5.3.3 WRITING A CONFIGURATION BYTE TO THE DEVICE

When the Master sends an address byte with the R/$\overline{W}$ bit low (R/$\overline{W}$ = 0), the MCP3421 expects one configuration byte following the address. Any byte sent after this second byte will be ignored. The user can change the operating mode of the device by writing the configuration register bits.

If the device receives a write command with a new configuration setting, the device immediately begins a new conversion and updates the conversion data.

TABLE 5-3: EXAMPLE OF CONVERSION DATA OUTPUT OF EACH CONVERSION MODE

Conversion Mode	Conversion Data Output
18-bits	MMMMMMMD16 (1st data byte) - D15 ~ D8 (2nd data byte) - D7 ~ D0 (3rd data byte) - Configuration byte
16-bits	MD14~D8 (1st data byte) - D7 ~ D0 (2nd data byte) - Configuration byte
14-bits	MMMD12~D8 (1st data byte) - D7 ~ D0 (2nd data byte) - Configuration byte
12-bits	MMMMMD10D9D8 (1st data byte) - D7 ~ D0 (2nd data byte) - Configuration byte
Note:	M is MSB of the data byte.

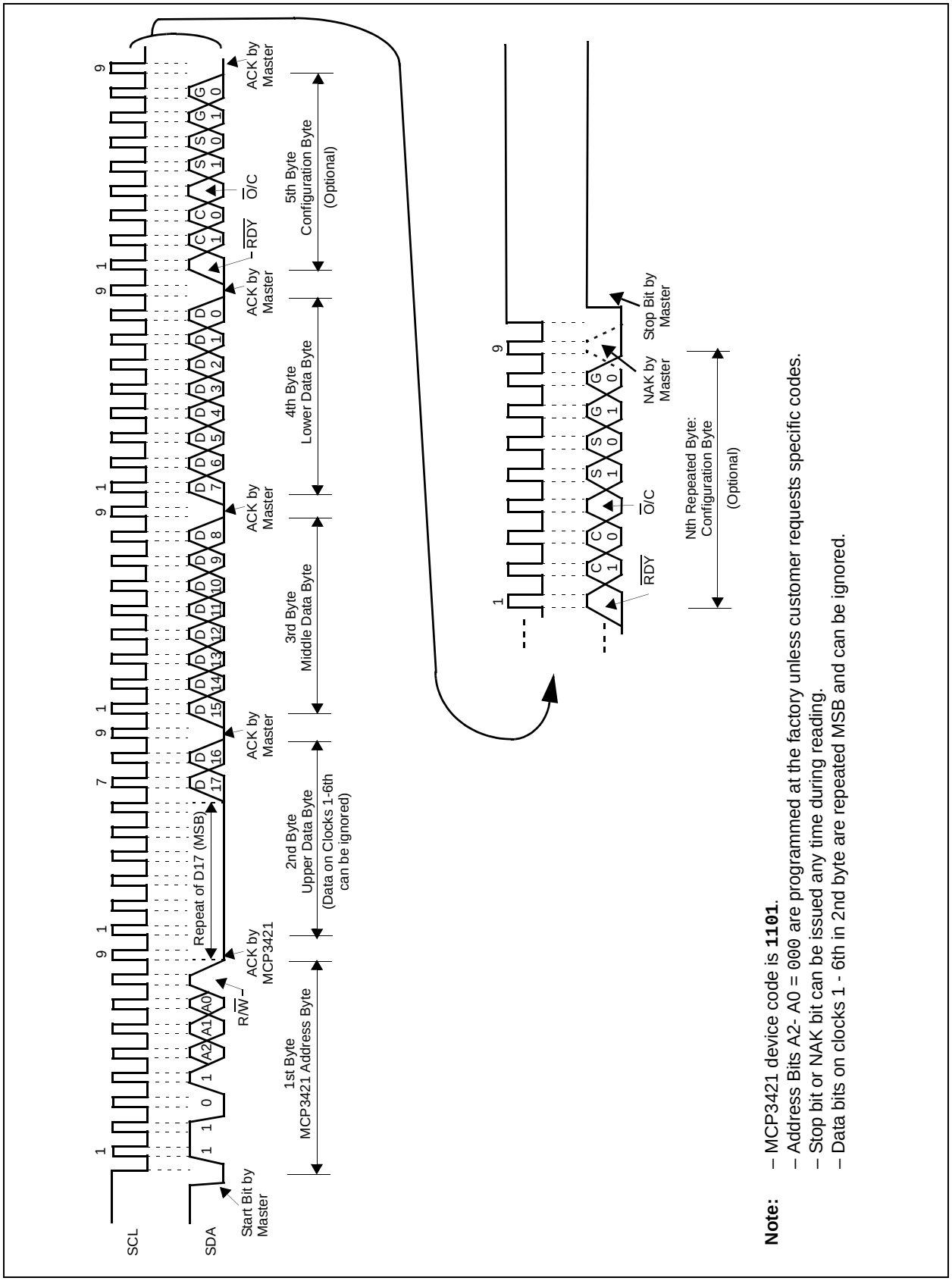


FIGURE 5-2: *Timing Diagram For Reading From The MCP3421 With 18-Bit Mode.*

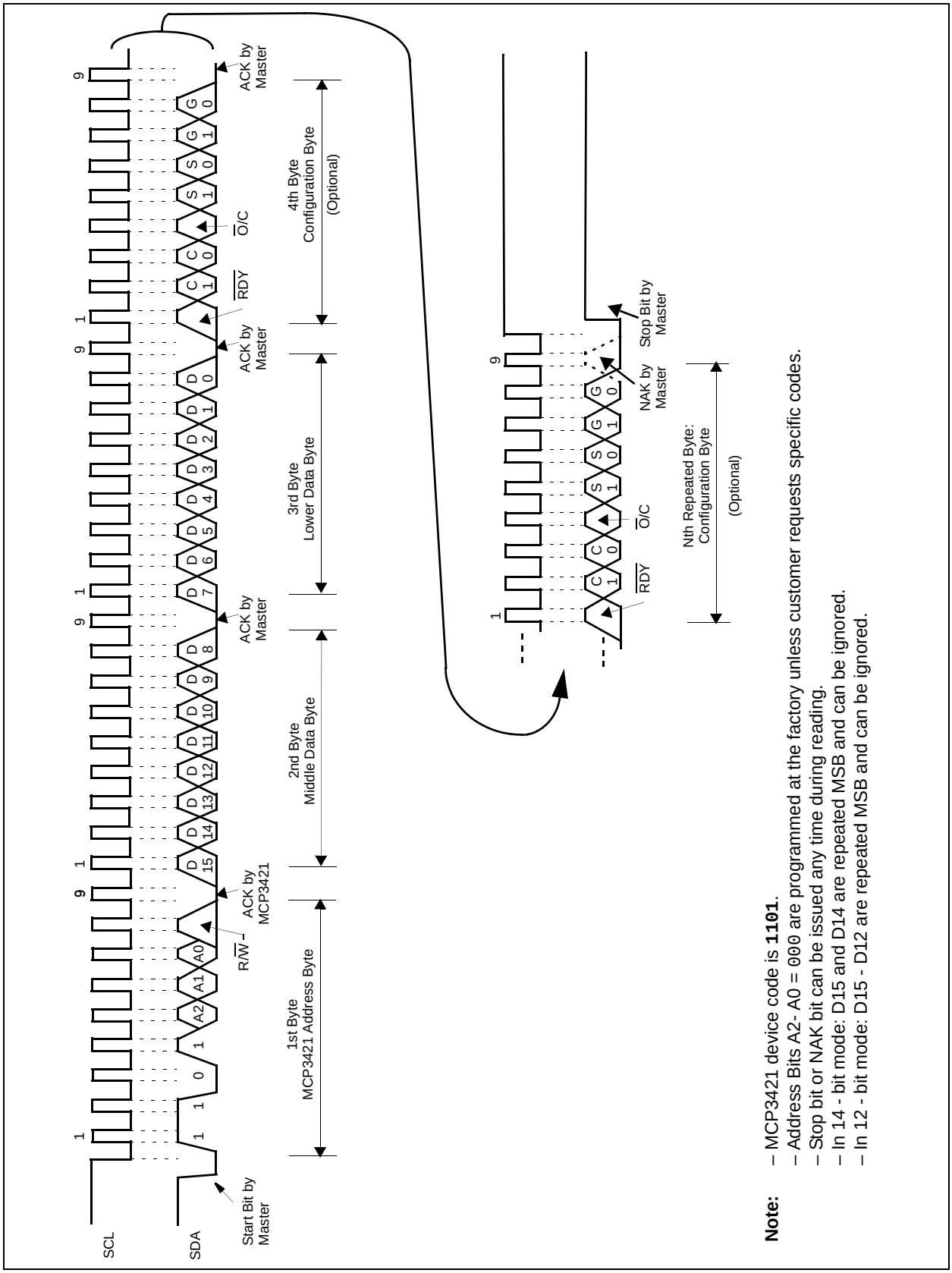
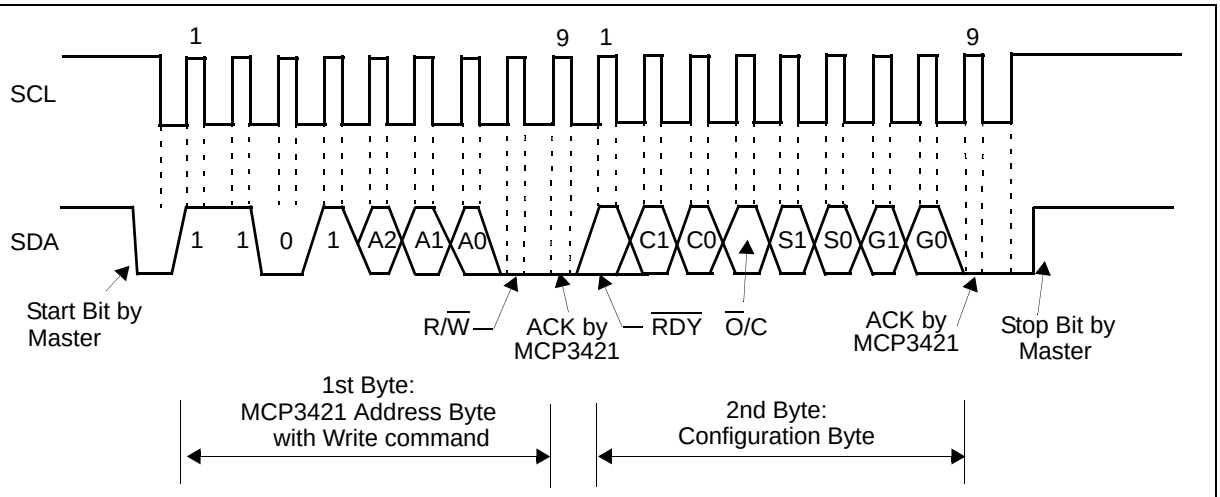


FIGURE 5-3: *Timing Diagram For Reading From The MCP3421 With 12-Bit to 16-Bit Modes.*



Note: – Stop bit can be issued any time during writing.
– **MCP3421** device code is `1101`.
– Address Bits A2- A0 = `000` are programmed at factory unless customer requests different codes.

FIGURE 5-4: *Timing Diigram For Writing To The MCP3421.*

5.4 General Call

The MCP3421 acknowledges the general call address (0x00 in the first byte). The meaning of the general call address is always specified in the second byte. Refer to Figure 5-5. The MCP3421 supports the following general calls:

5.4.1 GENERAL CALL RESET

The general call reset occurs if the second byte is '`00000110`' (06h). At the acknowledgement of this byte, the device will abort current conversion and perform an internal reset similar to a power-on-reset (POR).

5.4.2 GENERAL CALL CONVERSION

The general call conversion occurs if the second byte is '`00001000`' (08h). All devices on the bus initiate a conversion simultaneously. For the MCP3421 device, the configuration will be set to the One-Shot Conversion mode and a single conversion will be performed. The PGA and data rate settings are unchanged with this general call.

Note:	The I^2C specification does not allow to use "`00000000`" (00h) in the second byte.

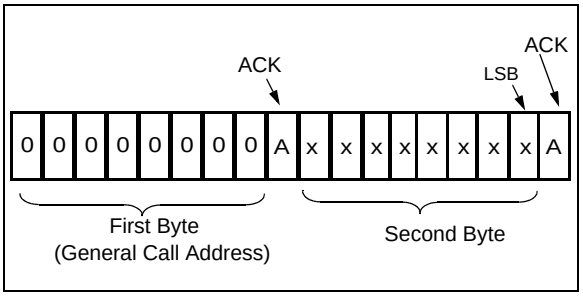


FIGURE 5-5: *General Call Address Format.*

For more information on the general call, or other I^2C modes, please refer to the Phillips I^2C specification.

5.5 High-Speed (HS) Mode

The I^2C specification requires that a high-speed mode device must be 'activated' to operate in high-speed mode. This is done by sending a special address byte of 00001XXX following the START bit. The XXX bits are unique to the High-Speed (HS) mode Master. This byte is referred to as the High-Speed (HS) Master Mode Code (HSMMC). The MCP3421 device does not acknowledge this byte. However, upon receiving this code, the MCP3421 switches on its HS mode filters and communicates up to 3.4 MHz on SDA and SCL. The device will switch out of the HS mode on the next STOP condition.

For more information on the HS mode, or other I^2C modes, please refer to the Phillips I^2C specification.

5.6 I^2C Bus Characteristics

The I^2C specification defines the following bus protocol:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined using Figure 5-6.

5.6.1 BUS NOT BUSY (A)

Both data and clock lines remain HIGH.

5.6.2 START DATA TRANSFER (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

5.6.3 STOP DATA TRANSFER (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations can be ended with a STOP condition.

5.6.4 DATA VALID (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition.

5.6.5 ACKNOWLEDGE

The Master (microcontroller) and the slave (MCP3421) use an acknowledge pulse as a hand shake of communication for each byte. The ninth clock pulse of each byte is used for the acknowledgement. The acknowledgement is achieved by pulling-down the SDA line "LOW" during the 9th clock pulse. The clock pulse is always provided by the Master (microcontroller) and the acknowledgement is issued by the receiving device of the byte (Note: The transmitting device must release the SDA line ("HIGH") during the acknowledge pulse.). For example, the slave (MCP3421) issues the acknowledgement (bring down the SDA line "LOW") after the end of each receiving byte, and the master (microcontroller) issues the acknowledgement when it reads data from the Slave (MCP3421).

When the MCP3421 is addressed, it generates an acknowledge after receiving each byte successfully. The Master device (microcontroller) must provide an extra clock pulse (9th pulse of each byte) for the acknowledgement from the MCP3421 (slave).

The MCP3421 (slave) pulls-down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge clock pulse.

During reads, the Master (microcontroller) can terminate the current read operation by not providing an acknowledge bit on the last byte that has been clocked out from the MCP3421. In this case, the MCP3421 releases the SDA line to allow the master (microcontroller) to generate a STOP or repeated START condition.

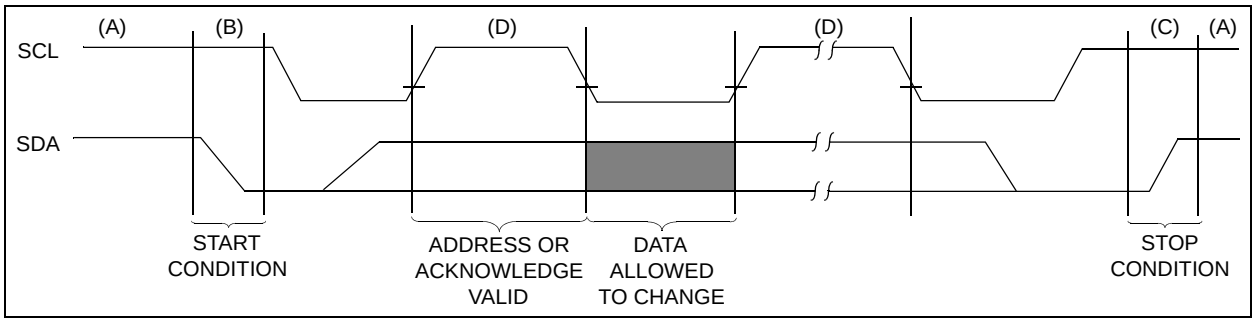


FIGURE 5-6: *Data Transfer Sequence on the Serial Bus.*

TABLE 5-4: I²C SERIAL TIMING SPECIFICATIONS

Electrical Specifications: Unless otherwise specified, all limits are specified for T_A = -40 to +85°C, V_{DD} = +2.7V, +3.3V or +5.0V, V_{SS} = 0V, $V_{IN}+ = V_{IN}- = V_{REF}/2$.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Standard Mode						
Clock frequency	f_{SCL}	0	—	100	kHz	
Clock high time	T_{HIGH}	4000	—	—	ns	
Clock low time	T_{LOW}	4700	—	—	ns	
SDA and SCL rise time **(Note 1)**	T_R	—	—	1000	ns	From V_{IL} to V_{IH}
SDA and SCL fall time **(Note 1)**	T_F	—	—	300	ns	From V_{IH} to V_{IL}
START condition hold time	$T_{HD:STA}$	4000	—	—	ns	After this period, the first clock pulse is generated.
Repeated START condition setup time	$T_{SU:STA}$	4700	—	—	ns	Only relevant for repeated Start condition
Data hold time **(Note 3)**	$T_{HD:DAT}$	0	—	3450	ns	
Data input setup time	$T_{SU:DAT}$	250	—	—	ns	
STOP condition setup time	$T_{SU:STO}$	4000	—	—	ns	
STOP condition hold time	$T_{HD:STD}$	4000	—	—	ns	
Output valid from clock **(Notes 2 and 3)**	T_{AA}	0	—	3750	ns	
Bus free time	T_{BUF}	4700	—	—	ns	Time between START and STOP conditions.
Fast Mode						
Clock frequency	T_{SCL}	0	—	400	kHz	
Clock high time	T_{HIGH}	600	—	—	ns	
Clock low time	T_{LOW}	1300	—	—	ns	
SDA and SCL rise time **(Note 1)**	T_R	20 + 0.1Cb	—	300	ns	From V_{IL} to V_{IH}
SDA and SCL fall time **(Note 1)**	T_F	20 + 0.1Cb	—	300	ns	From V_{IH} to V_{IL}
START condition hold time	$T_{HD:STA}$	600	—	—	ns	After this period, the first clock pulse is generated
Repeated START condition setup time	$T_{SU:STA}$	600	—	—	ns	Only relevant for repeated Start condition
Data hold time **(Note 4)**	$T_{HD:DAT}$	0	—	900	ns	
Data input setup time	$T_{SU:DAT}$	100	—	—	ns	
STOP condition setup time	$T_{SU:STO}$	600	—	—	ns	
STOP condition hold time	$T_{HD:STD}$	600	—	—	ns	
Output valid from clock **(Notes 2 and 3)**	T_{AA}	0	—	1200	ns	
Bus free time	T_{BUF}	1300	—	—	ns	Time between START and STOP conditions.
Input filter spike suppression **(Note 5)**	T_{SP}	0	—	50	ns	SDA and SCL pins

Note 1: This parameter is ensured by characterization and not 100% tested.

2: This specification is not a part of the I²C specification. This specification is equivalent to the Data Hold Time ($T_{HD:DAT}$) plus SDA Fall (or rise) time: $T_{AA} = T_{HD:DAT} + T_F$ (OR T_R).

3: If this parameter is too short, it can create an unintended Start or Stop condition to other devices on the bus line. If this parameter is too long, Clock Low time (T_{LOW}) can be affected.

4: For Data Input: This parameter must be longer than t_{SP}. If this parameter is too long, the Data Input Setup ($T_{SU:DAT}$) or Clock Low time (T_{LOW}) can be affected.
For Data Output: This parameter is characterized, and tested indirectly by testing T_{AA} parameter.

5: This parameter is ensured by characterization and not 100% tested. This parameter is not available for Standard Mode.

TABLE 5-4: I²C SERIAL TIMING SPECIFICATIONS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all limits are specified for T_A = -40 to +85°C, V_{DD} = +2.7V, +3.3V or +5.0V, V_{SS} = 0V, $V_{IN}+ = V_{IN}- = V_{REF}/2$.

Parameters	Sym	Min	Typ	Max	Units	Conditions
High Speed Mode						
Clock frequency	f_{SCL}	0	—	3.4 1.7	MHz MHz	C_b = 100 pF C_b = 400 pF
Clock high time	T_{HIGH}	60 120	—	—	ns ns	C_b = 100 pF C_b = 400 pF
Clock low time	T_{LOW}	160 320	—	—	ns	C_b = 100 pF C_b = 400 pF
SCL rise time **(Note 1)**	T_R	—	—	40 80	ns	From V_{IL} to V_{IH},C_b = 100 pF C_b = 400 pF
SCL fall time **(Note 1)**	T_F	—	—	40 80	ns	From V_{IH} to V_{IL},C_b = 100 pF C_b = 400 pF
SDA rise time **(Note 1)**	$T_{R: DAT}$	—	—	80 160	ns	From V_{IL} to V_{IH},C_b = 100 pF C_b = 400 pF
SDA fall time **(Note 1)**	$T_{F: DATA}$	—	—	80 160	ns	From V_{IH} to V_{IL},C_b = 100 pF C_b = 400 pF
START condition hold time	$T_{HD:STA}$	160	—	—	ns	After this period, the first clock pulse is generated
Repeated START condition setup time	$T_{SU:STA}$	160	—	—	ns	Only relevant for repeated Start condition
Data hold time **(Note 4)**	$T_{HD:DAT}$	0 0	—	70 150	ns	C_b = 100 pF C_b = 400 pF
Data input setup time	$T_{SU:DAT}$	10	—	—	ns	
STOP condition setup time	$T_{SU:STO}$	160	—	—	ns	
STOP condition hold time	$T_{HD:STD}$	160	—	—	ns	
Output valid from clock **(Notes 2 and 3)**	T_{AA}	—	—	150 310	ns	C_b = 100 pF C_b = 400 pF
Bus free time	T_{BUF}	160	—	—	ns	Time between START and STOP conditions.
Input filter spike suppression **(Note 5)**	T_{SP}	0	—	10	ns	SDA and SCL pins

Note 1: This parameter is ensured by characterization and not 100% tested.

2: This specification is not a part of the I²C specification. This specification is equivalent to the Data Hold Time ($T_{HD:DAT}$) plus SDA Fall (or rise) time: $T_{AA} = T_{HD:DAT} + T_F$ (OR T_R).

3: If this parameter is too short, it can create an unintended Start or Stop condition to other devices on the bus line. If this parameter is too long, Clock Low time (T_{LOW}) can be affected.

4: For Data Input: This parameter must be longer than t_{SP}. If this parameter is too long, the Data Input Setup ($T_{SU:DAT}$) or Clock Low time (T_{LOW}) can be affected.
For Data Output: This parameter is characterized, and tested indirectly by testing T_{AA} parameter.

5: This parameter is ensured by characterization and not 100% tested. This parameter is not available for Standard Mode.

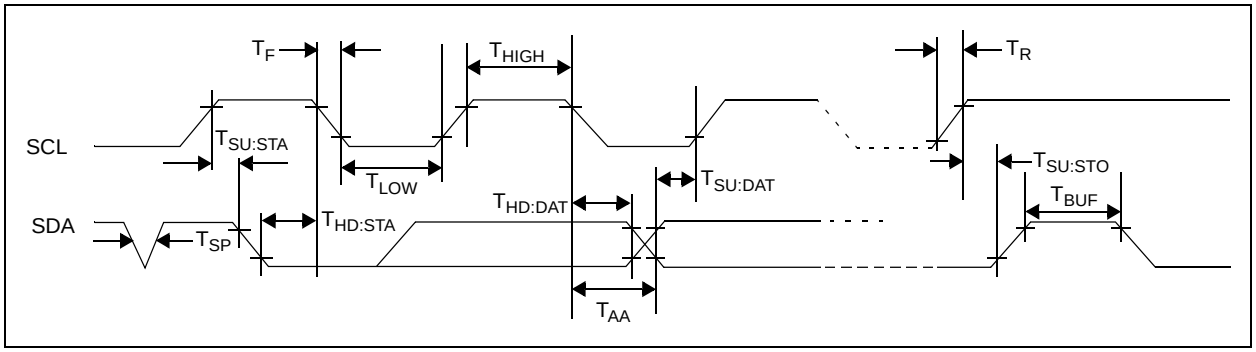


FIGURE 5-7: *I^2C Bus Timing Data.*

6.0 BASIC APPLICATION CONFIGURATION

The MCP3421 device can be used for various precision analog-to-digital converter applications. The device operates with very simple connections to the application circuit. The following sections discuss the examples of the device connections and applications.

6.1 Connecting to the Application Circuits

6.1.1 INPUT VOLTAGE RANGE

The fully differential input signals can be connected to the V_{IN}+ and V_{IN}- input pins. The input range should be within absolute common mode input voltage range: V_{SS} - 0.3V to V_{DD} + 0.3V. Outside this limit, the ESD protection diode at the input pin begins to conduct and the error due to input leakage current increases rapidly. Within this limit, the differential input V_{IN} (= V_{IN}+ - V_{IN}-) is boosted by the PGA before a conversion takes place. The MCP3421 can not accept negative input voltages on the input pins. Figure 6-1 and Figure 6-2 show typical connection examples for differential inputs and a single-ended input, respectively. For the single-ended input, the input signal is applied to one of the input pins (typically connected to the V_{IN}+ pin) while the other input pin (typically V_{IN}- pin) is grounded. The input signal range of the single-ended configuration is from 0V to 2.048V. All device characteristics hold for the single-ended configuration, but this configuration loses one bit resolution because the input can only stand in positive half scale. Refer to **Section 1.0 "Electrical Characteristics"**.

6.1.2 BYPASS CAPACITORS ON V_{DD} PIN

For accurate measurement, the application circuit needs a clean supply voltage and must block any noise signal to the MCP3421 device. Figure 6-1 shows an example of using two bypass capacitors (a 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor) in parallel on the V_{DD} line. These capacitors are helpful to filter out any high frequency noises on the V_{DD} line and also provide the momentary bursts of extra currents when the device needs from the supply. These capacitors should be placed as close to the V_{DD} pin as possible (within one inch). If the application circuit has separate digital and analog power supplies, the V_{DD} and V_{SS} of the MCP3421 should reside on the analog plane.

6.1.3 CONNECTING TO I²C BUS USING PULL-UP RESISTORS

The SCL and SDA pins of the MCP3421 are open-drain configurations. These pins require a pull-up resistor as shown in Figure 6-1. The value of these pull-up resistors depends on the operating speed (standard, fast, and high speed) and loading capacitance of the I²C bus line. Higher value of pull-up resistor consumes less power, but increases the signal transition time (higher RC time constant) on the bus. Therefore, it can limit the bus operating speed. The lower value of resistor, on the other hand, consumes higher power, but allows higher operating speed. If the bus line has higher capacitance due to long bus line or high number of devices connected to the bus, a smaller pull-up resistor is needed to compensate the long RC time constant. The pull-up resistor is typically chosen between 1 kΩ and 10 kΩ ranges for standard and fast modes, and less than 1 kΩ for high speed mode in high loading capacitance environments.

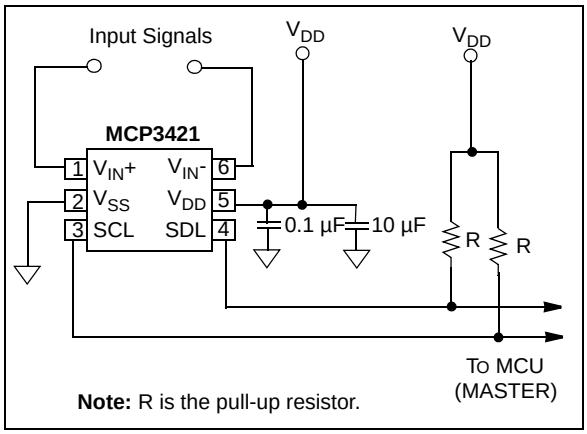


FIGURE 6-1: *Typical Connection Example for Differential Inputs.*

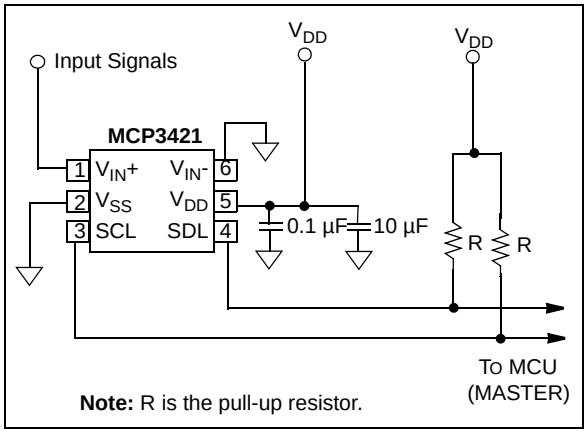


FIGURE 6-2: *Typical Connection Example for Single-Ended Input.*

The number of devices connected to the bus is limited only by the maximum bus capacitance of 400 pF. The bus loading capacitance affects on the bus operating speed. For example, the highest bus operating speed for the 400 pF bus capacitance is 1.7 MHz, and 3.4 MHz for 100 pF. Figure 6-3 shows an example of multiple device connections.

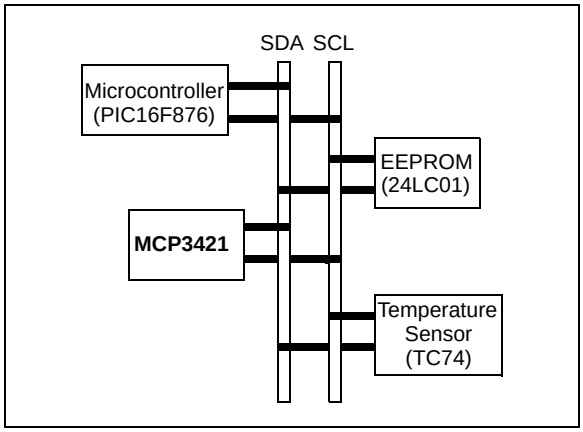


FIGURE 6-3: *Example of Multiple Device Connection on I²C Bus.*

6.2 Device Connection Test

The user can test the presence of the MCP3421 on the I²C bus line without performing an input data conversion. This test can be achieved by checking an acknowledge response from the MCP3421 after sending a read or write command. Here is an example using Figure 6-4:

(a) Set the R/$\overline{W}$ bit "HIGH" in the address byte.

(b) The MCP3421 will then acknowledge by pulling SDA bus LOW during the ACK clock and then release the bus back to the I²C Master.

(c) A STOP or repeated START bit can then be issued from the Master and I²C communication can continue.

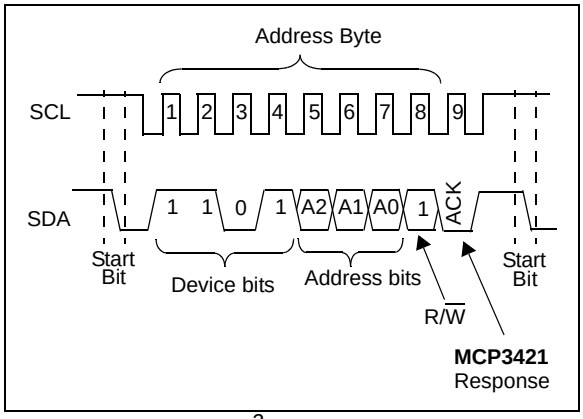


FIGURE 6-4: *I²C Bus Connection Test.*

6.3 Application Examples

The MCP3421 device can be used in a broad range of sensor and data acquisition applications. Figure 6-5, shows an example of interfacing with a bridge sensor for pressure measurement.

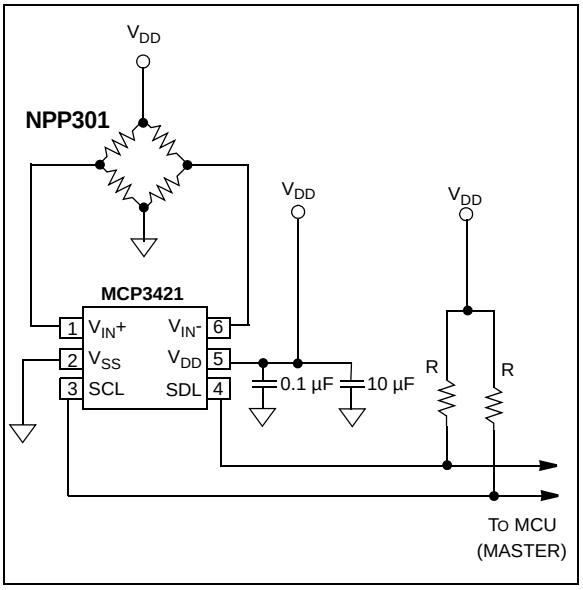


FIGURE 6-5: *Example of Pressure Measurement.*

In this circuit example, the sensor full scale range is ±7.5 mV with a common mode input voltage of V_{DD} / 2. This configuration will provide a full 14-bit resolution across the sensor output range. The alternative circuit for this amount of accuracy would involve an analog gain stage prior to a 16-bit ADC.

Figure 6-6 shows an example of temperature measurement using a thermistor. This example can achieve a linear response over a 50°C temperature range. This can be implemented using a standard resistor with 1% tolerance in series with the thermistor. The value of the resistor is selected to be equal to the thermistor value at the mid-point of the desired temperature range.

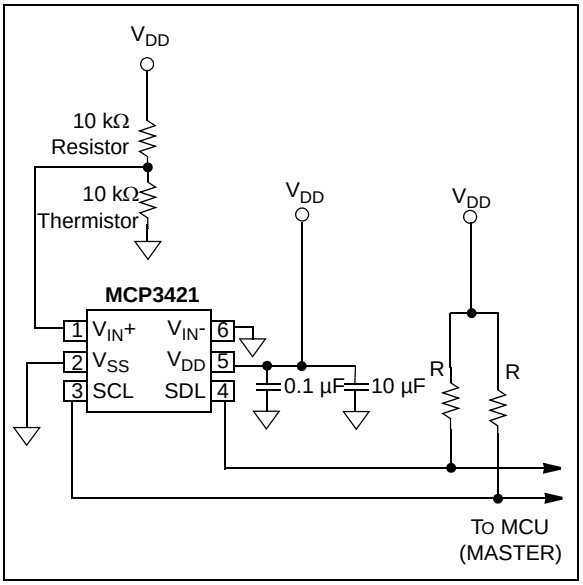
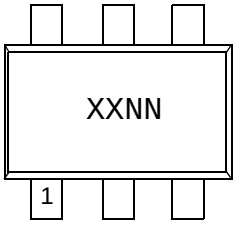


FIGURE 6-6: *Example of Temperature Measurement.*

7.0 PACKAGING INFORMATION

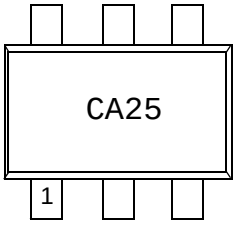
7.1 Package Marking Information

6-Lead SOT-23



Part Number	Address Option	Code
MCP3421A0T-E/CH	A0 (000)	CANN
MCP3421A1T-E/CH	A1 (001)	CBNN
MCP3421A2T-E/CH	A2 (010)	CCNN
MCP3421A3T-E/CH	A3 (011)	CDNN
MCP3421A4T-E/CH	A4 (100)	CENN
MCP3421A5T-E/CH	A5 (101)	CFNN
MCP3421A6T-E/CH	A6 (110)	CGNN
MCP3421A7T-E/CH	A7 (111)	CHNN

Example

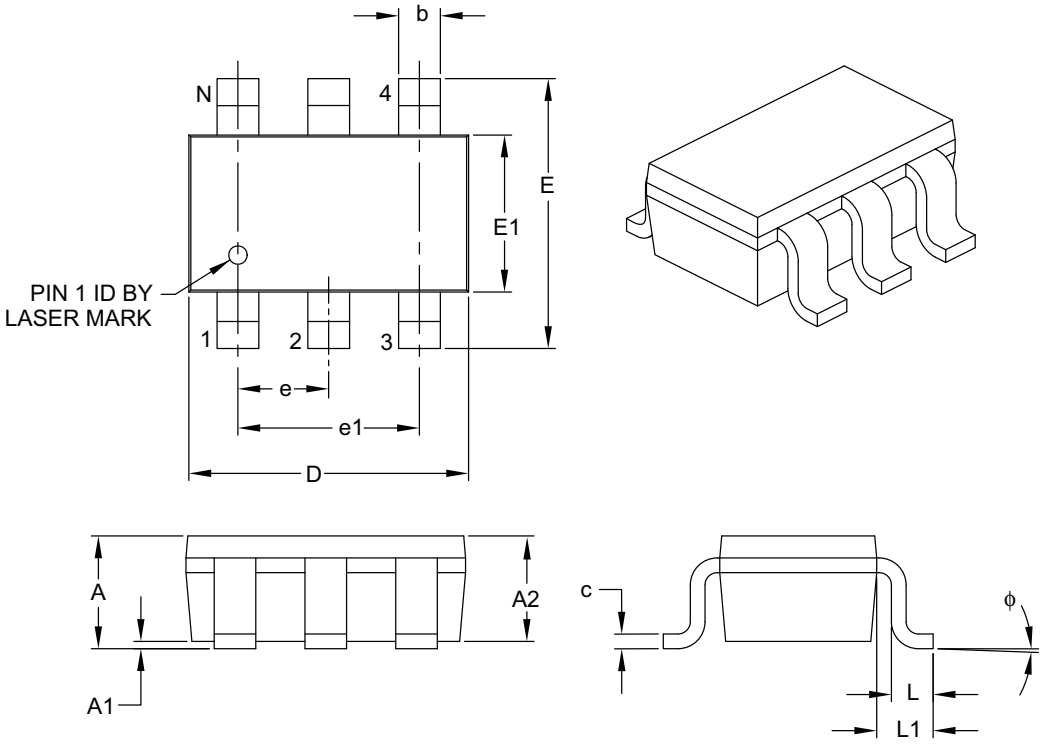


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

6-Lead Plastic Small Outline Transistor (CH) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

APPENDIX A: REVISION HISTORY

Revision D (November 2007)

The following is the list of modifications:

1. Section 1.0 Electrical Characteristics: Changed Gain Error Drift typical from 5 to 15, and Maximum from 40 to —.

Revision C (October 2007)

The following is the list of modifications:

1. Figure 5-4: Changed O/$\overline{C}$ designation to $\overline{O}$/C.
2. Updated package outline drawing.
3. Updated revision history.

Revision B (December 2006)

The following is the list of modifications:

1. Changes to Electrical Characteristics tables
2. Added characterization data
3. Changes to I^2C Serial Timing Specification table
4. Change to Figure 5-7.
5. Updated package outline drawings

Revision A (August 2006)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	X	X	/XX
Device	Address Options	Tape and Reel	Temperature Range	Package

Device: MCP3421: Single Channel ΔΣ A/D Converter

Address Options:

XX		A2	A1	A0
A0 *	=	0	0	0
A1	=	0	0	1
A2	=	0	1	0
A3	=	0	1	1
A4	=	1	0	0
A5	=	1	0	1
A6	=	1	1	0
A7	=	1	1	1

* Default option. Contact Microchip factory for other address options

Tape and Reel: T = Tape and Reel

Temperature Range: E = -40°C to +125°C

Package: CH = Plastic Small Outline Transistor (SOT-23-6), 6-lead

Examples:

a) MCP3421A0T-E/CH: Tape and Reel, Single Channel ΔΣ A/D Converter, SOT-23-6 package, Address Option = A0.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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