

MOSFETs Silicon N-Channel MOS (DTMOSIV)

TK12V60W

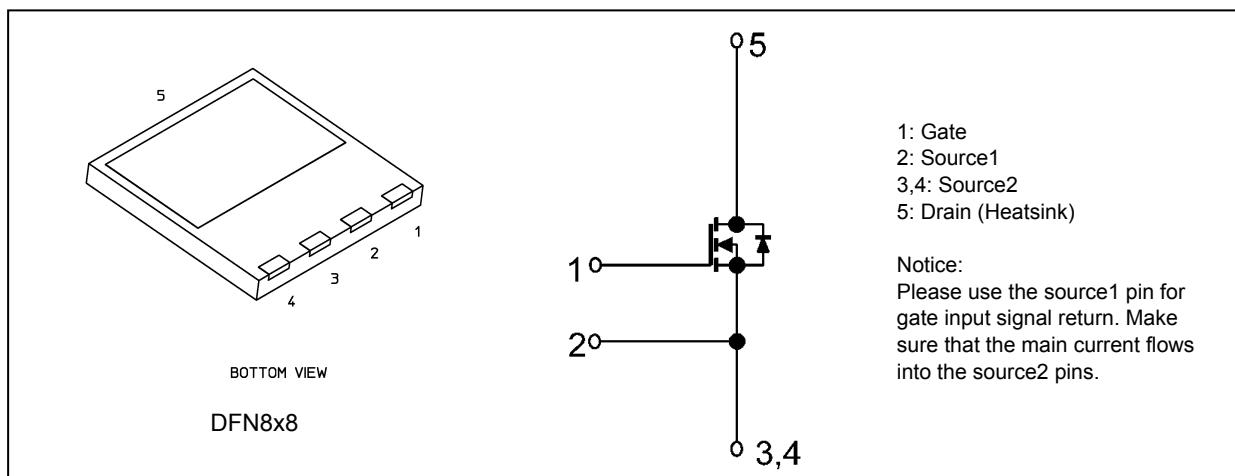
1. Applications

- Switching Voltage Regulators

2. Features

- (1) Low drain-source on-resistance: $R_{DS(ON)} = 0.265 \Omega$ (typ.)
by used to Super Junction Structure : DTMOS
- (2) Easy to control Gate switching
- (3) Enhancement mode: $V_{th} = 2.7$ to 3.7 V ($V_{DS} = 10$ V, $I_D = 0.6$ mA)

3. Packaging and Internal Circuit



4. Absolute Maximum Ratings (Note) ($T_a = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	600	V
Gate-source voltage	V_{GSS}	± 30	
Drain current (DC)	I_D	11.5	A
Drain current (pulsed)	I_{DP}	46	
Power dissipation ($T_c = 25^\circ\text{C}$)	P_D	104	W
Single-pulse avalanche energy	E_{AS}	93	mJ
Avalanche current	I_{AR}	3	A
Reverse drain current (DC)	I_{DR}	11.5	
Reverse drain current (pulsed)	I_{DRP}	46	
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Start of commercial production

2013-05

5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	$R_{th(ch-c)}$	1.2	°C/W

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: $V_{DD} = 90$ V, $T_{ch} = 25$ °C (initial), $L = 18.2$ mH, $R_G = 25$ Ω, $I_{AR} = 3$ A

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

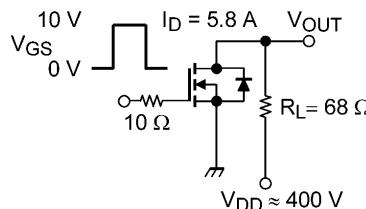
6. Electrical Characteristics

6.1. Static Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	± 1	μA
Drain cut-off current	I_{DSS}	$V_{DS} = 600 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$	600	—	—	
Gate threshold voltage	V_{th}	$V_{DS} = 10 \text{ V}, I_D = 0.6 \text{ mA}$	2.7	—	3.7	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = 10 \text{ V}, I_D = 5.8 \text{ A}$	—	0.265	0.3	Ω

6.2. Dynamic Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	$V_{DS} = 300 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	890	—	pF
Reverse transfer capacitance	C_{rss}		—	2.8	—	
Output capacitance	C_{oss}		—	23	—	
Effective output capacitance	$C_{o(er)}$	$V_{DS} = 0 \text{ to } 400 \text{ V}, V_{GS} = 0 \text{ V}$	—	41	—	
Gate resistance	r_g	$V_{DS} = \text{OPEN}, f = 1 \text{ MHz}$	—	6.5	—	Ω
Switching time (rise time)	t_r	See Figure 6.2.1	—	23	—	ns
Switching time (turn-on time)	t_{on}		—	45	—	
Switching time (fall time)	t_f		—	5.5	—	
Switching time (turn-off time)	t_{off}		—	85	—	
MOSFET dv/dt ruggedness	dv/dt	$V_{DD} = 0 \text{ to } 400 \text{ V}, I_D = 5.8 \text{ A}$	50	—	—	V/ns



Duty $\leq 1\%$, $t_w = 10 \mu\text{s}$

Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	$V_{DD} \approx 400 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 11.5 \text{ A}$	—	25	—	nC
Gate-source charge 1	Q_{gs1}		—	5.5	—	
Gate-drain charge	Q_{gd}		—	11	—	

6.4. Source-Drain Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage	V_{DSF}	$I_{DR} = 11.5 \text{ A}, V_{GS} = 0 \text{ V}$	—	—	-1.7	V
Reverse recovery time	t_{rr}	$I_{DR} = 5.8 \text{ A}, V_{GS} = 0 \text{ V}$ $-dI_{DR}/dt = 100 \text{ A}/\mu\text{s}$	—	250	—	ns
Reverse recovery charge	Q_{rr}		—	2.3	—	
Peak reverse recovery current	I_{rr}		—	20	—	
Diode dv/dt ruggedness	dv/dt	$I_{DR} = 5.8 \text{ A}, V_{GS} = 0 \text{ V}, V_{DD} = 400 \text{ V}$	15	—	—	V/ns

7. Marking



Fig. 7.1 Marking

8. Characteristics Curves (Note)

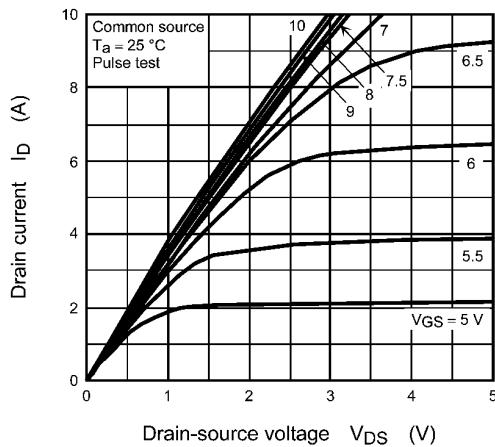


Fig. 8.1 I_D - V_{DS}

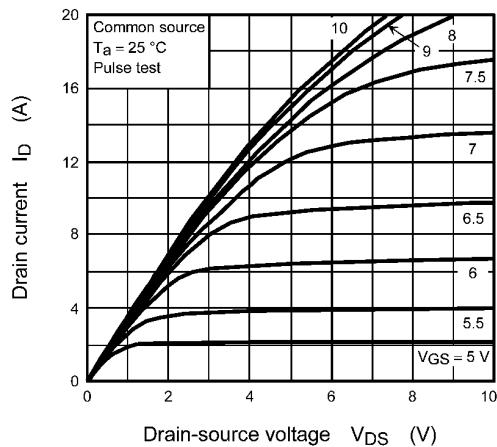


Fig. 8.2 I_D - V_{DS}

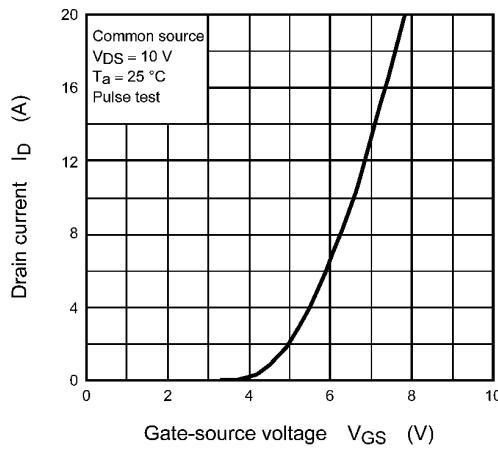


Fig. 8.3 I_D - V_{GS}

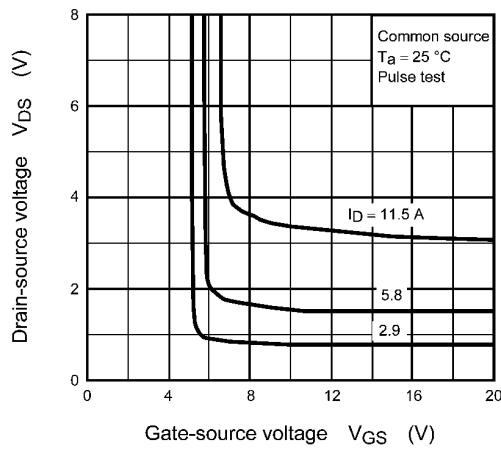


Fig. 8.4 V_{DS} - V_{GS}

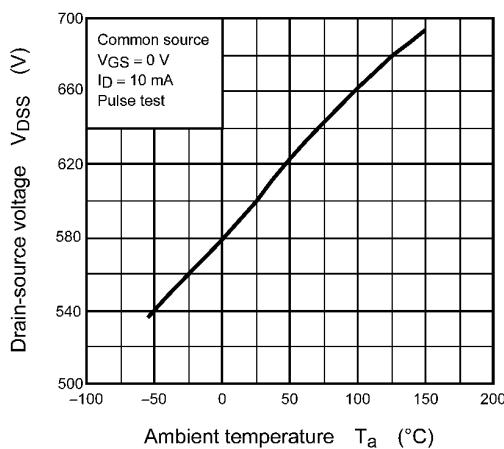


Fig. 8.5 V_{DS} - T_a

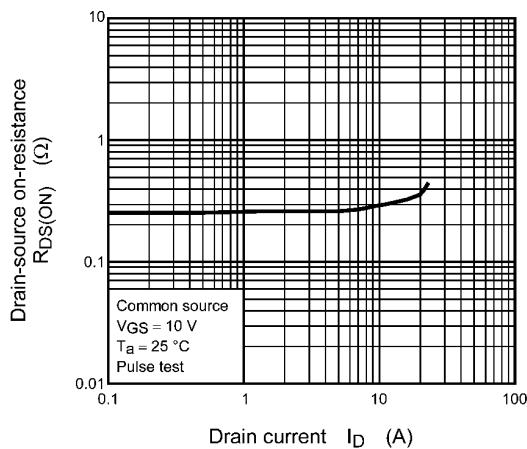


Fig. 8.6 $R_{DS(on)}$ - I_D

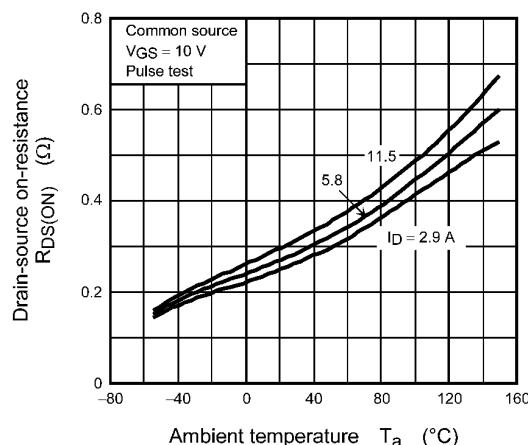
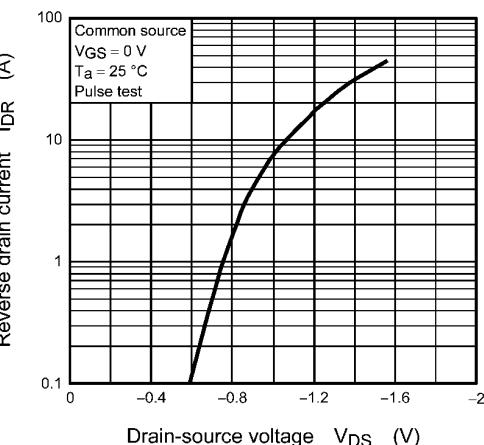
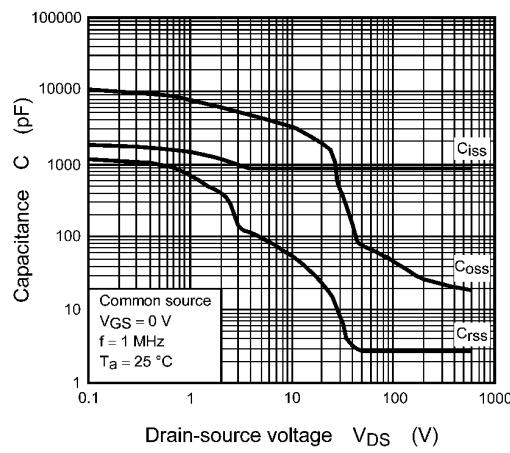
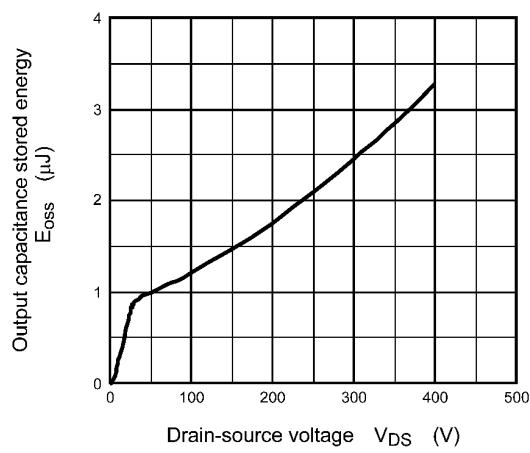
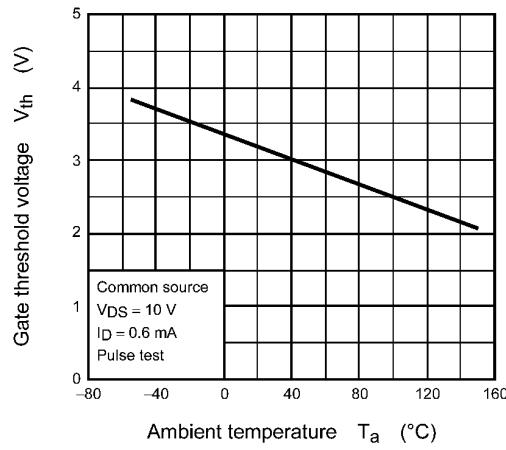
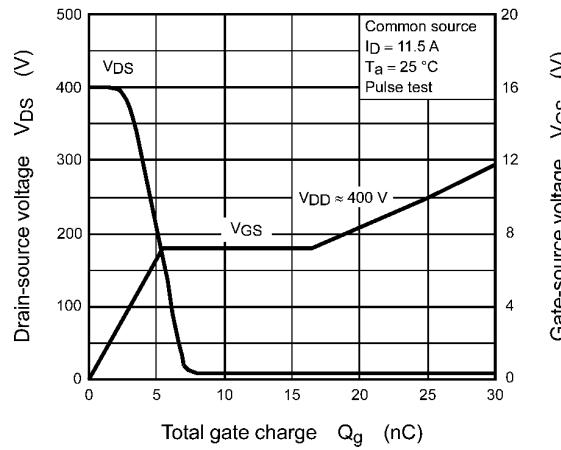
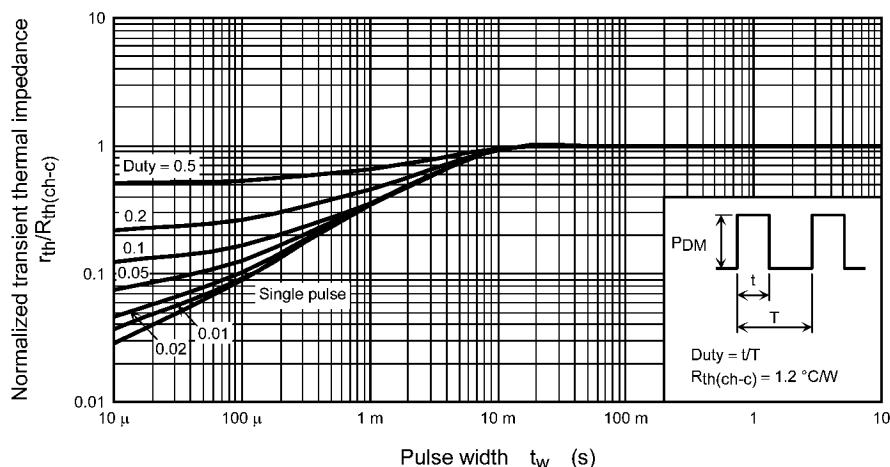
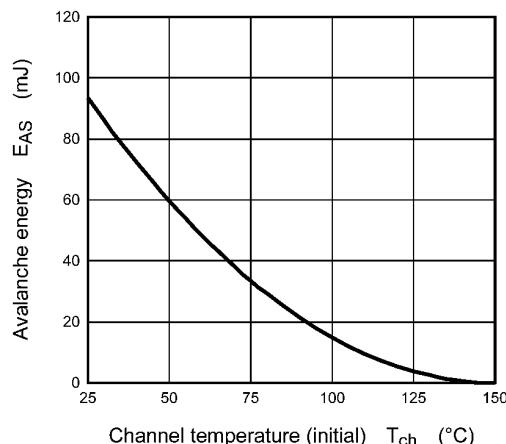
Fig. 8.7 $R_{DS(ON)} - T_a$ Fig. 8.8 $I_{DR} - V_{DS}$ Fig. 8.9 $C - V_{DS}$ Fig. 8.10 $E_{oss} - V_{DS}$ Fig. 8.11 $V_{th} - T_a$ 

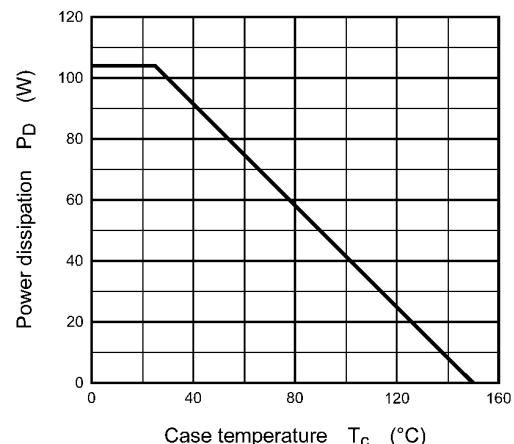
Fig. 8.12 Dynamic Input/Output Characteristics



**Fig. 8.13 $R_{th} - t_w$
(Guaranteed Maximum)**



**Fig. 8.14 $E_{AS} - T_{ch}$
(Guaranteed Maximum)**



**Fig. 8.15 $P_D - T_c$
(Guaranteed Maximum)**

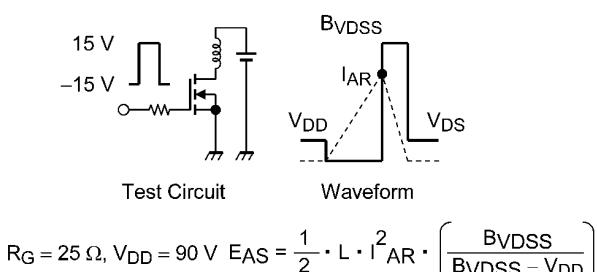


Fig. 8.16 Test Circuit/Waveform

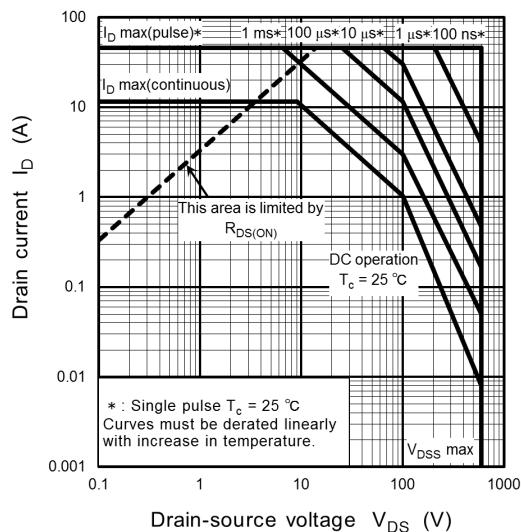
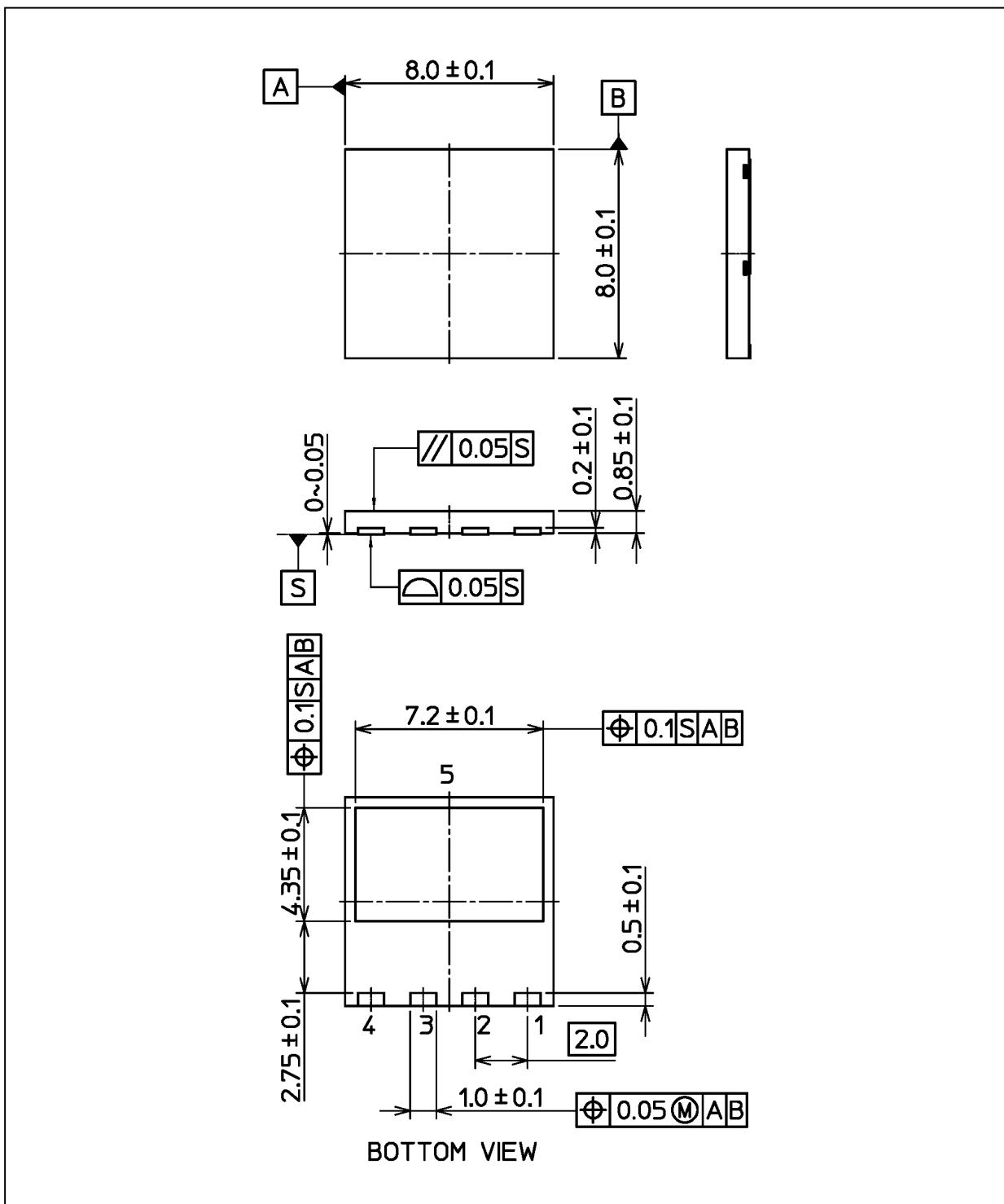


Fig. 8.17 Safe Operating Area (Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 0.175 g (typ.)

Package Name(s)
TOSHIBA: 2-8T1A
Nickname: DFN8x8

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