

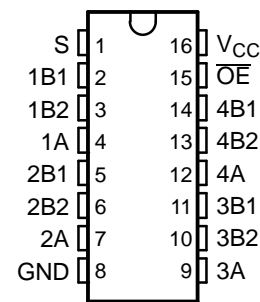
## FEATURES

- **Low and Flat ON-State Resistance ( $r_{on}$ ) Characteristics Over Operating Range ( $r_{on} = 3 \Omega$  Typ)**
- **0- to 10-V Switching on Data I/O Ports**
- **Bidirectional Data Flow With Near-Zero Propagation Delay**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ( $C_{io(OFF)} = 20$  pF Max, B Port)**
- **$V_{CC}$  Operating Range From 4.75 V to 5.25 V**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- **Supports Both Digital and Analog Applications**

## APPLICATIONS

- **PCI Interface**
- **Differential Signal Interface**
- **Memory Interleaving**
- **Bus Isolation**
- **Low-Distortion Signal Gating**

DBQ OR PW PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

The TS5N412 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance ( $r_{on}$ ). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the TS5N412 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The TS5N412 is a 4-bit 1-of-2 multiplexer/demultiplexer with a single output-enable ( $\overline{OE}$ ) input. The select (S) inputs control the data path of the multiplexer/demultiplexer. When  $\overline{OE}$  is low, the multiplexer/demultiplexer is enabled and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the multiplexer/demultiplexer is disabled and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP (QSOP) – DBQ	Tape and reel	TS5N412DBQR	YB412
	TSSOP – PW	Tape and reel	TS5N412PWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

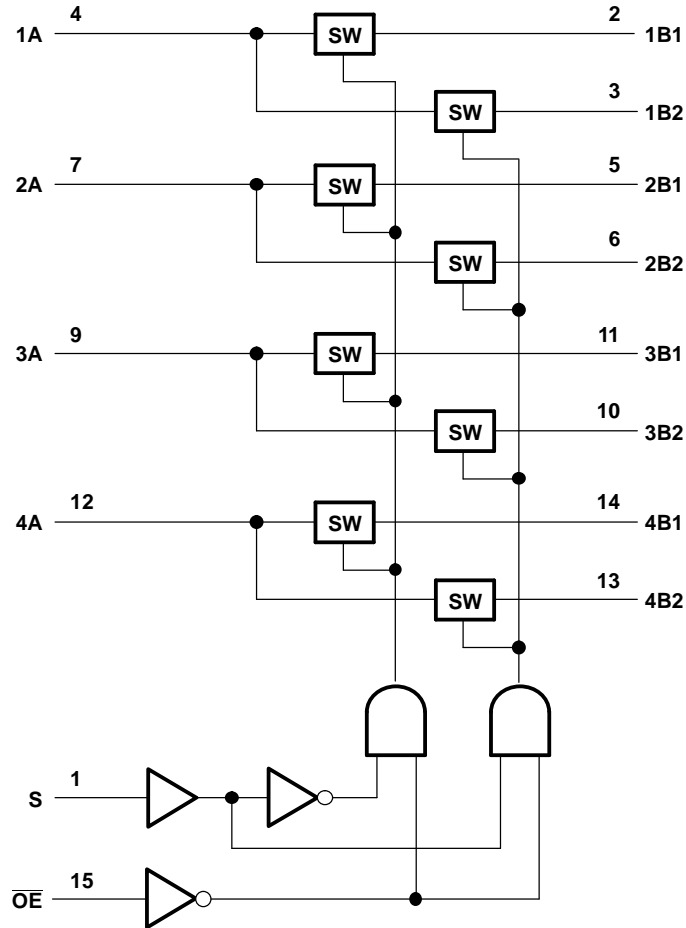
**TS5N412**  
**4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER**  
**HIGH-BANDWIDTH BUS SWITCH**

SCDS207–AUGUST 2005

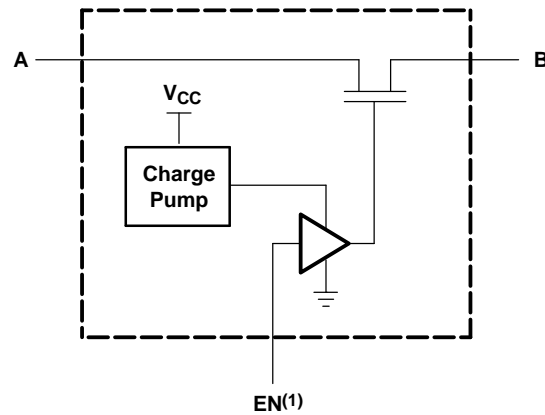
**FUNCTION TABLE**

INPUTS		INPUT/OUTPUT A	FUNCTION
$\overline{OE}$	S		
L	L	B1	A port = B1 port
L	H	B2	A port = B2 port
H	X	Z	Disconnect

**LOGIC DIAGRAM (POSITIVE LOGIC)**



SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



(1) EN is the internal enable signal applied to the switch.

**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	7	V
$V_{IN}$	Control input voltage range <sup>(2)(3)</sup>	-0.5	7	V
$V_{I/O}$	Switch I/O voltage range <sup>(2)(3)(4)</sup>	-0.5	11	V
$I_{I/O}$	ON-state switch current <sup>(5)</sup>		±100	mA
	Continuous current through $V_{CC}$ or GND		±100	mA
$\theta_{JA}$	Package thermal impedance <sup>(6)</sup>		90	°C/W
			108	
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4)  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .
- (5)  $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

**Recommended Operating Conditions<sup>(1)</sup>**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.75	5.25	V
$V_{IH}$	High-level control input voltage	2	5.25	V
$V_{IL}$	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	10	V
$T_A$	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# TS5N412

## 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

### HIGH-BANDWIDTH BUS SWITCH

SCDS207–AUGUST 2005

### Electrical Characteristics<sup>(1)</sup>

over recommended operating free-air temperature range, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(2)</sup>	MAX	UNIT	
$I_{IN}$	Control inputs	$V_{CC} = 5.25\text{ V}$ ,	$V_{IN} = 0\text{ to }V_{CC}$			10	$\mu\text{A}$	
$I_{OZ}$ <sup>(3)</sup>		$V_{CC} = 5.25\text{ V}$ ,	$V_O = 0\text{ to }10\text{ V}$ , $V_I = 0$ ,	Switch OFF, $V_{IN} = V_{CC}\text{ or GND}$		10	$\mu\text{A}$	
		$V_{CC} = 0\text{ V}$ ,	$V_O = \text{Open}$ ,	$V_I = 0\text{ to }10\text{ V}$		10		
$I_{CC}$		$V_{CC} = 5.25\text{ V}$ ,	$I_{I/O} = 0$ , Switch ON or OFF,	$V_{IN} = V_{CC}\text{ or GND}$		10	mA	
$C_{in}$	Control inputs	$V_{CC} = 5\text{ V}$ ,	$V_{IN} = 10\text{ V or }0$			10	pF	
$C_{io(OFF)}$	A port	$V_{CC} = 5\text{ V}$ ,	Switch OFF, $V_{IN} = V_{CC}\text{ or GND}$ ,	$V_{I/O} = 10\text{ V or }0$		35	pF	
	B port	$V_{CC} = 5\text{ V}$ ,	Switch OFF, $V_{IN} = V_{CC}\text{ or GND}$ ,	$V_{I/O} = 10\text{ V or }0$		20		
$C_{io(ON)}$		$V_{CC} = 5\text{ V}$ ,	Switch ON, $V_{IN} = V_{CC}\text{ or GND}$ ,	$V_{I/O} = 10\text{ V or }0$		80	pF	
$r_{on}$ <sup>(4)</sup>		$V_{CC} = 4.75\text{ V}$ , TYP at $V_{CC} = 5\text{ V}$	$V_I = 0$ ,	$I_O = 50\text{ mA}$		3	7.5	$\Omega$
			$V_I = 8\text{ V}$ ,	$I_O = -50\text{ mA}$			7.5	
			$V_I = 10\text{ V}$ ,	$I_O = -50\text{ mA}$			12.5	

- (1)  $V_{IN}$  and  $I_{IN}$  refer to control inputs.  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to data pins  
(2) All typical values are at  $V_{CC} = 5\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .  
(3) For I/O ports, the parameter  $I_{OZ}$  includes the I/O leakage current.  
(4) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

### Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V} \pm 0.25\text{ V}$		UNIT
			MIN	MAX	
$t_{pd}^{(1)}$	A or B	B or A		3	ns
$t_{pd(s)}$	S	A		200	ns
$t_{en}$	S	B		200	ns
	$\overline{OE}$	A or B		200	
$t_{dis}$	S	B		200	ns
	OE	A or B		200	

- (1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

### Dynamic Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 5\%$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
Bandwidth (BW) <sup>(2)</sup>	$R_L = 50\ \Omega$ , $V_I = 0.632\text{ V (P-P)}$ , See <a href="#">Figure 4</a>		25		MHz
OFF isolation ( $O_{ISO}$ )	$R_L = 50\ \Omega$ , $V_I = 0.632\text{ V (P-P)}$ , $f = 25\text{ MHz}$ , See <a href="#">Figure 5</a>		-50		dB
Crosstalk ( $X_{TALK}$ )	$R_L = 50\ \Omega$ , $V_I = 0.632\text{ V (P-P)}$ , $f = 25\text{ MHz}$ , See <a href="#">Figure 6</a> and <a href="#">Figure 7</a>		-50		dB

- (1) All typical values are at  $V_{CC} = 5\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .  
(2) Bandwidth is the frequency at which the gain is -3 dB below the DC gain.

**TYPICAL PERFORMANCE**

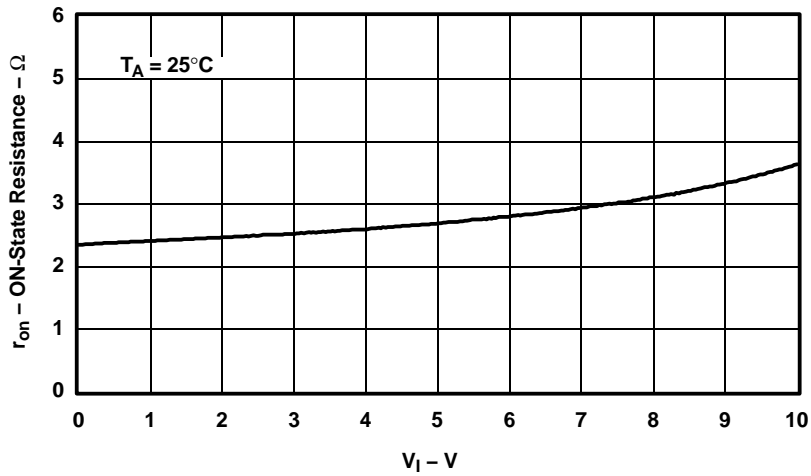


Figure 1. Typical  $r_{on}$  vs  $V_I$ ,  $V_{CC} = 5\text{ V}$  and  $I_O = -50\text{ mA}$

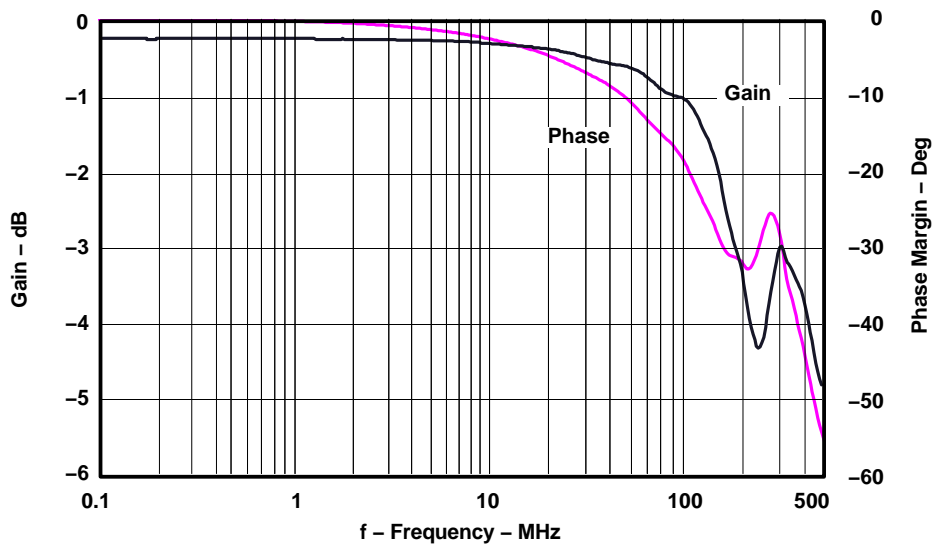


Figure 2. Frequency Response vs Bandwidth

TYPICAL PERFORMANCE

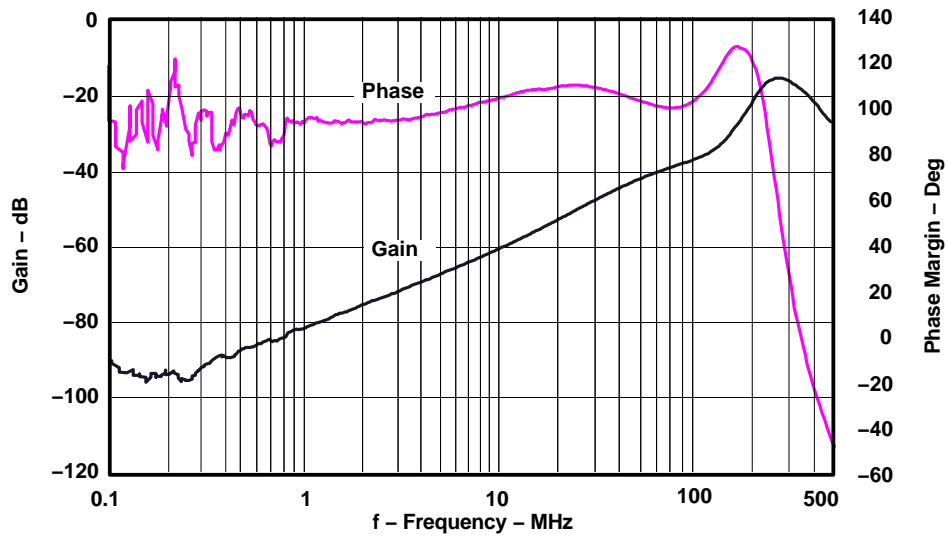


Figure 3. Frequency Response vs OFF Isolation

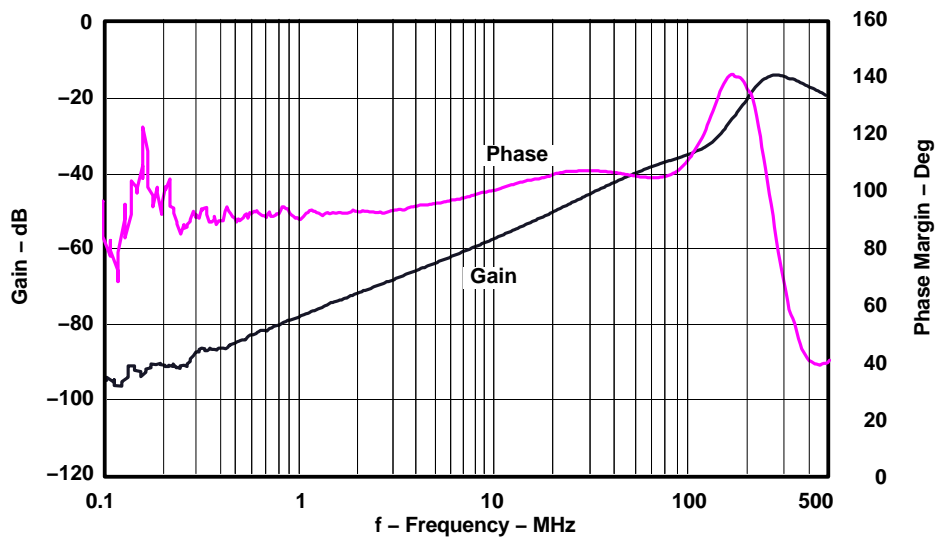
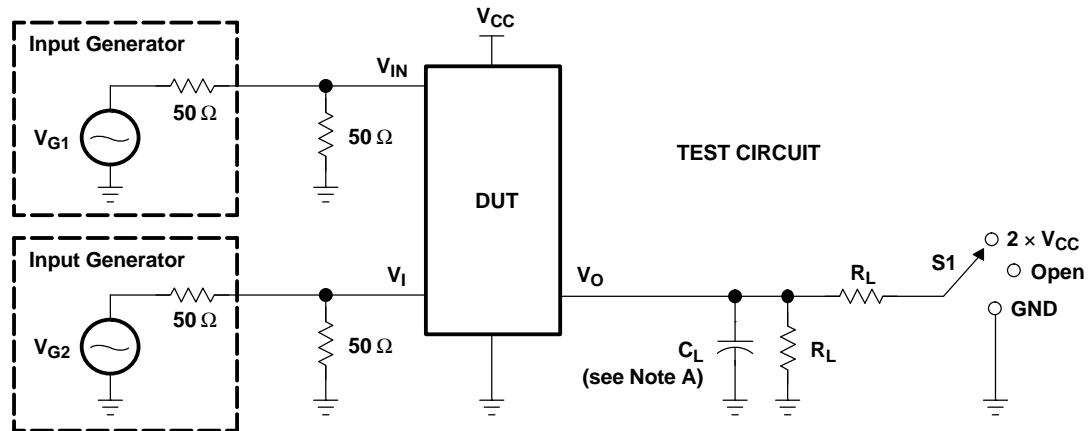


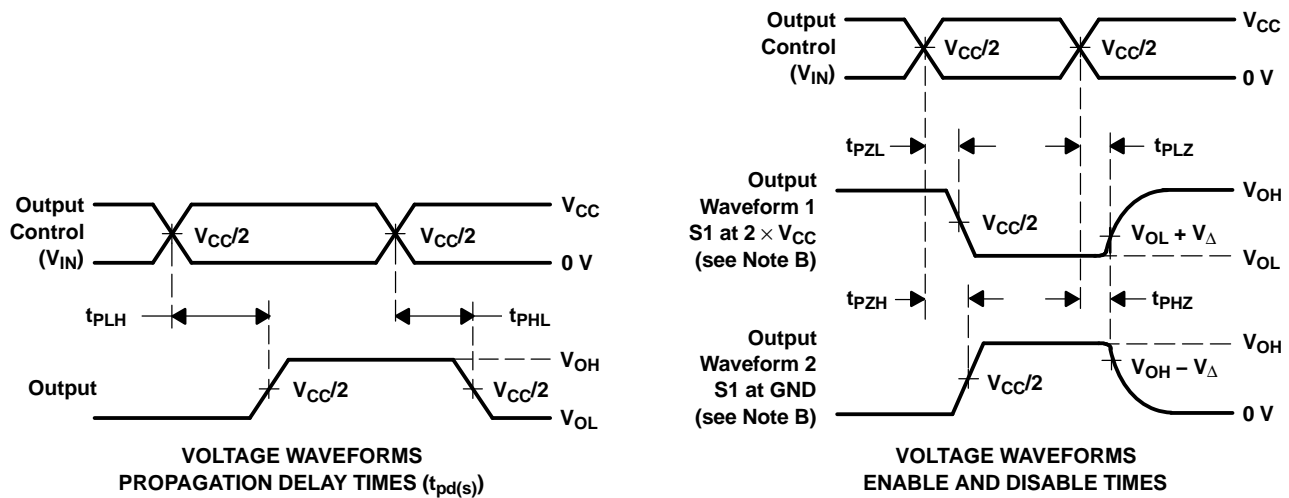
Figure 4. Frequency Response vs Crosstalk

PARAMETER MEASUREMENT INFORMATION



TEST	V <sub>CC</sub>	S1	R <sub>L</sub>	V <sub>I</sub>	C <sub>L</sub>	V <sub>Δ</sub>
t <sub>pd(s)</sub> <sup>†</sup>	5 V ± 0.25 V	Open	100 Ω	V <sub>CC</sub>	35 pF	
t <sub>PLZ</sub> /t <sub>PZL</sub>	5 V ± 0.25 V	2 × V <sub>CC</sub>	100 Ω	GND	35 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	5 V ± 0.25 V	GND	100 Ω	V <sub>CC</sub>	35 pF	0.3 V

<sup>†</sup> t<sub>pd(s)</sub> is measured with Demux inputs at opposite voltage levels, i.e. V<sub>B1</sub> = 5 V, V<sub>B2</sub> = GND.



- NOTES:
- A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> < 25 ns, t<sub>f</sub> < 25 ns.
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd(s)</sub>. The t<sub>pd</sub> propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
  - H. All parameters and waveforms are not applicable to all devices.

Figure 5. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

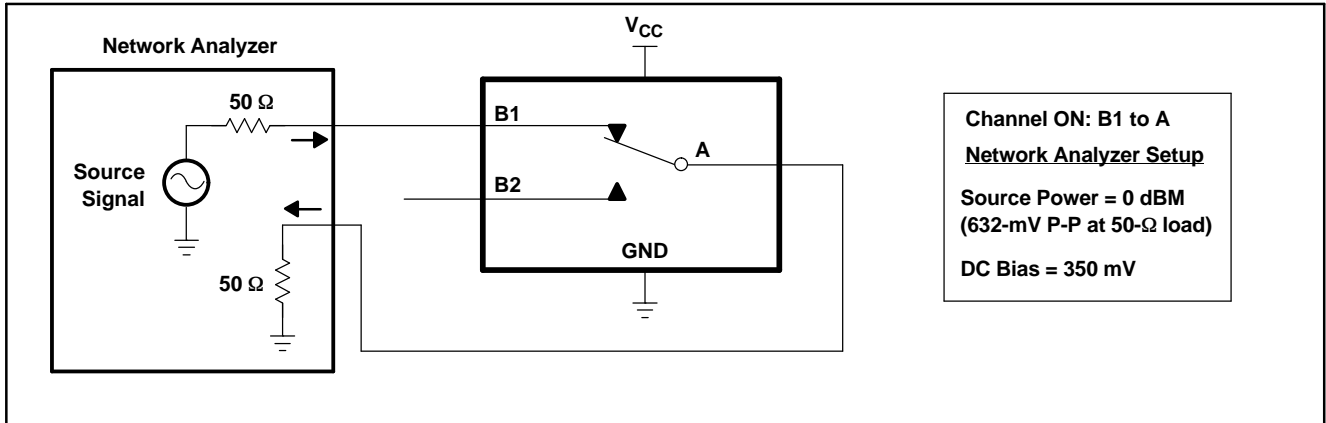


Figure 6. Bandwidth (BW)

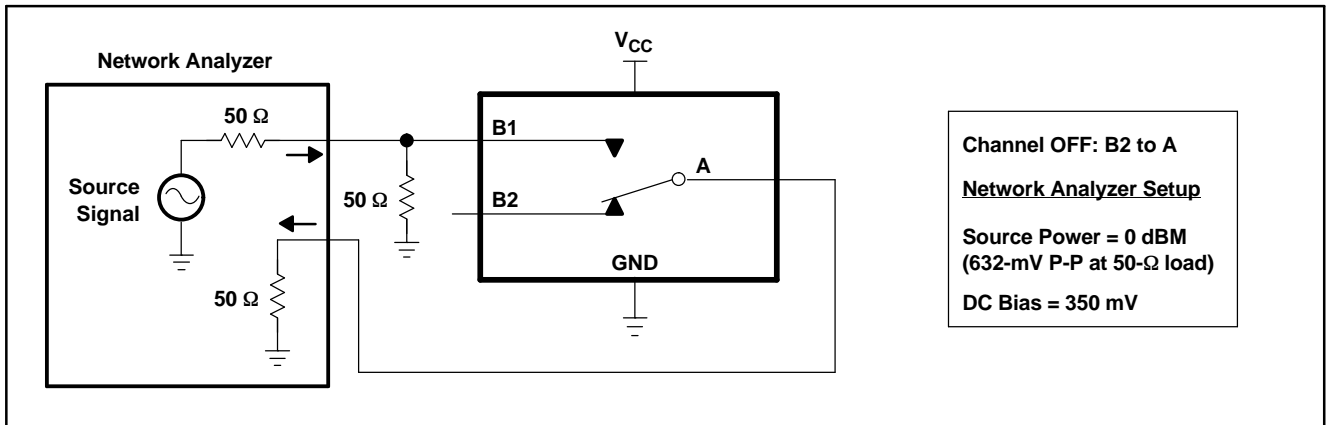


Figure 7. OFF Isolation ( $O_{ISO}$ )

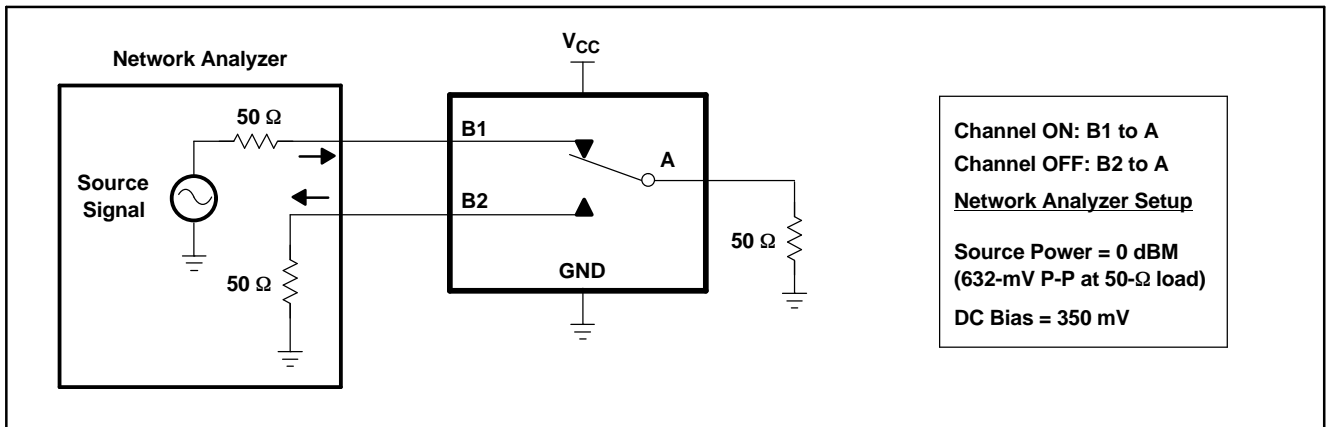
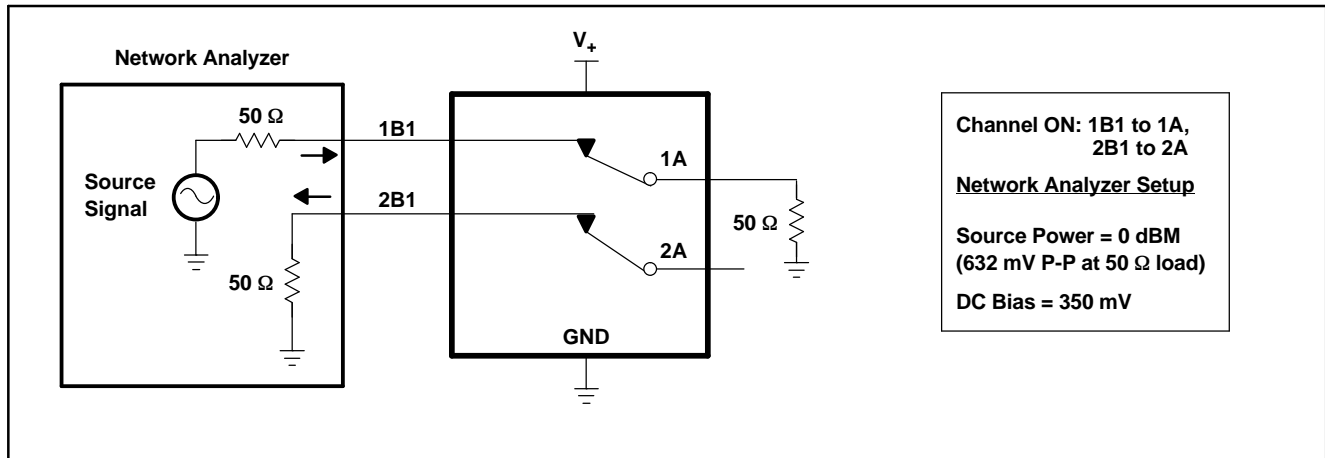


Figure 8. Crosstalk ( $X_{TALK}$ )



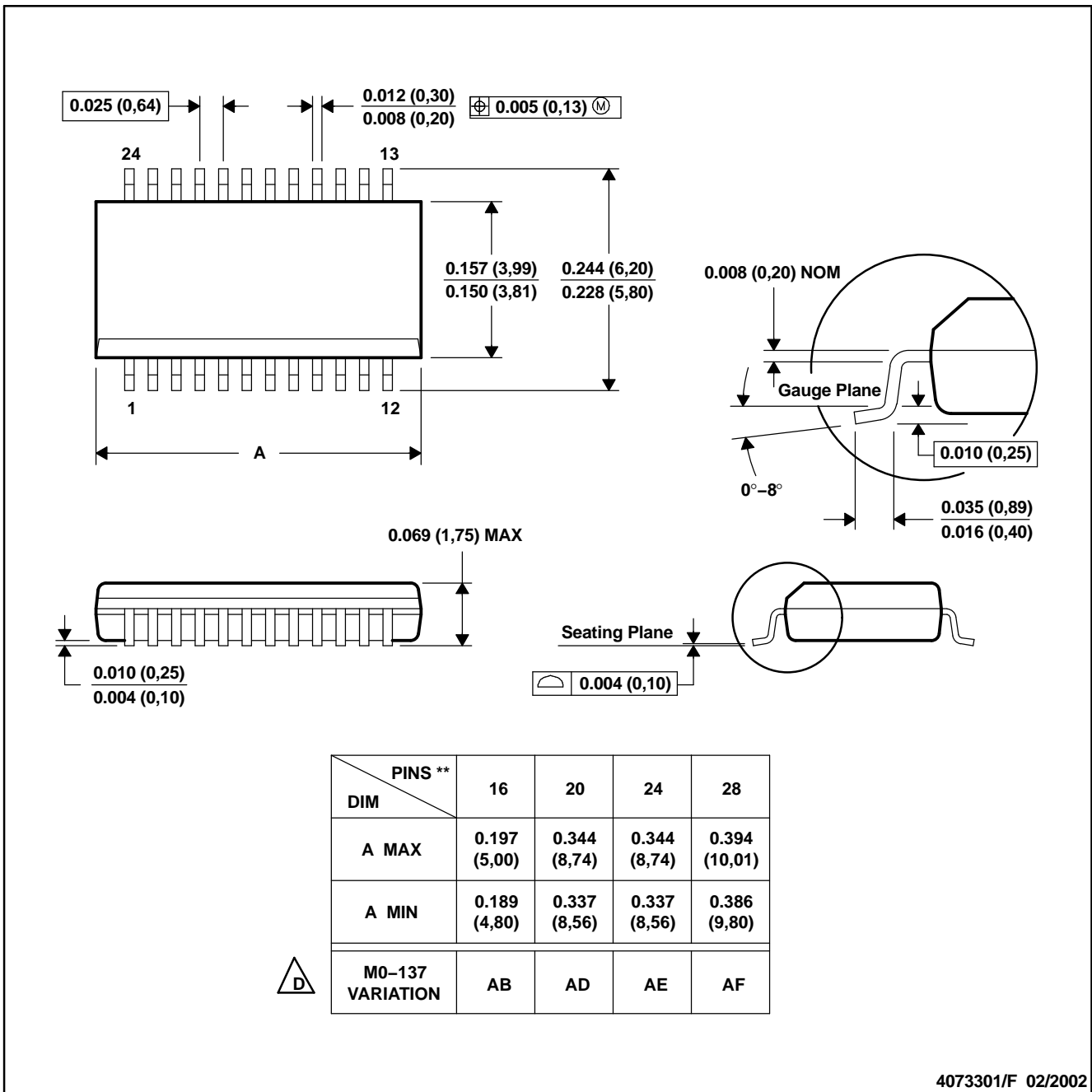
**PARAMETER MEASUREMENT INFORMATION (continued)**



**Figure 9. Adjacent Channel Crosstalk ( $X_{TALK}$ )**

MECHANICAL DATA

DBQ (R-PDSO-G\*\*)

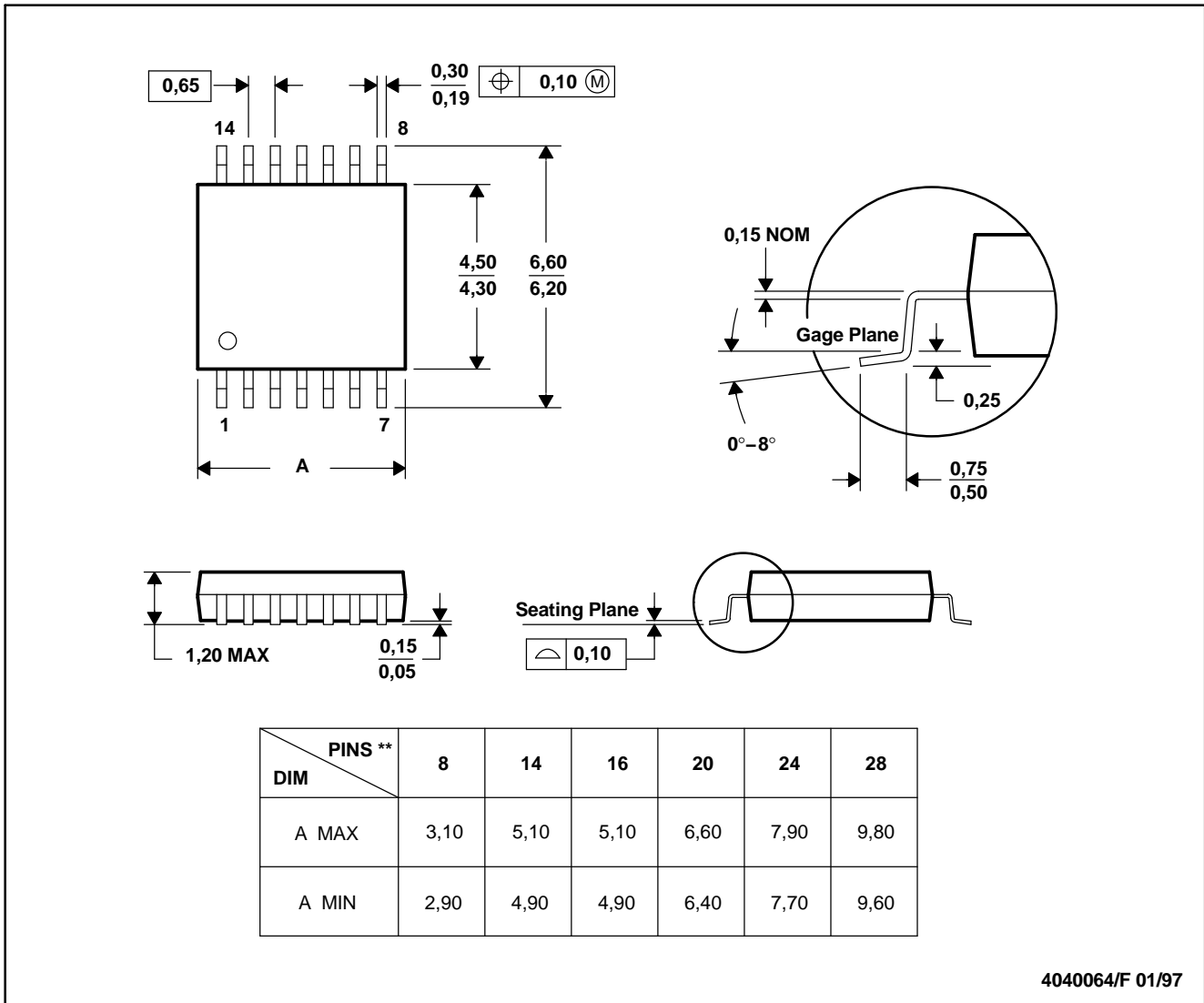


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-137.

### MECHANICAL DATA

#### PW (R-PDSO-G\*\*)

14 PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - D. Falls within JEDEC MO-153

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5N412DBQR	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YB412	<a href="#">Samples</a>
TS5N412PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YB412	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5N412DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

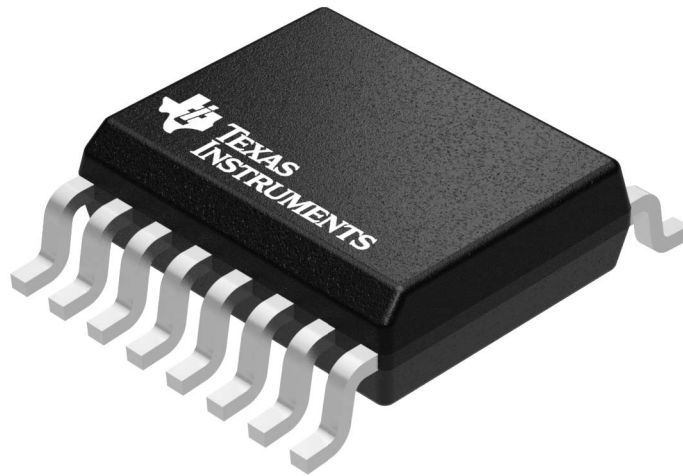
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5N412DBQR	SSOP	DBQ	16	2500	340.5	338.1	20.6

**GENERIC PACKAGE VIEW**

**DBQ 16**

**SSOP - 1.75 mm max height**

SHRINK SMALL-OUTLINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4073301-2/1





# DBQ0016A

# PACKAGE OUTLINE

## SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



4214846/A 03/2014

### NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

# EXAMPLE BOARD LAYOUT

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.127 MM] THICK STENCIL  
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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