QUARTZ CRYSTAL OSCILLATOR

■ GENERAL DESCRIPTION

The NJU6373 series is a C-MOS quartz crystal oscillator which consists of an oscillation amplifier, 3-stage divider and 3-state output buffer.

This series are classed into three groups A to D, H to L and Q to T according to their oscillation frequency range mentioned in the line-up table.

The oscillation amplifier incorporates feed-back resistance and oscillation capacitors(Cg, Cd), therefore, it requires no external component except quartz crystal.

The 3-stage divider generates f_O, $f_O/2$, $f_O/4$ and $f_O/8$ and only one frequency selected by internal circuits is output.

The 3-state output buffer is TTL compatible and capable of 10 TTL driving.

The NJU6373 series is suitable for the 3rd Over Tone and its pad location is the same as NJU6322 series.

■ FEATURES

- Operating Voltage. -- 4.0~6.0V
- Maximum Oscillation Frequency (See Line-Up Table)
- Low Operating Current
- High Fan-out -- TTL 10
- 3-state Output Buffer
- Selected Frequency Output (mask option)
  Only one frequency out of f_O, $f_O/2$, $f_O/4$ and $f_O/8$ output
- Oscillation Capacitors Cg and Cd on-chip
- Oscillation and/or Output Stand-by Function
- Package Outline -- CHIP/EMP 8
- C-MOS Technology

■ LINE-UP TABLE

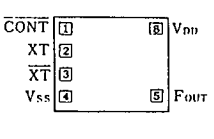
Type No.	Recommended Osc. Freq.	Output Freq.	Cg,Cd
NJU6373A 6373B 6373C 6373D	From 20 to 35MHz	f_O $f_O/2$ $f_O/4$ $f_O/8$	28pF
NJU6373H 6373J 6373K 6373L	From 30 to 50MHz	f_O $f_O/2$ $f_O/4$ $f_O/8$	20pF
NJU6373Q 6373R 6373S 6373T	From 45 to 75MHz	f_O $f_O/2$ $f_O/4$ $f_O/8$	17pF

■ PACKAGE OUTLINE

NJU6373XC

NJU6373XE

■ PIN CONFIGURATION/PAD LOCATION



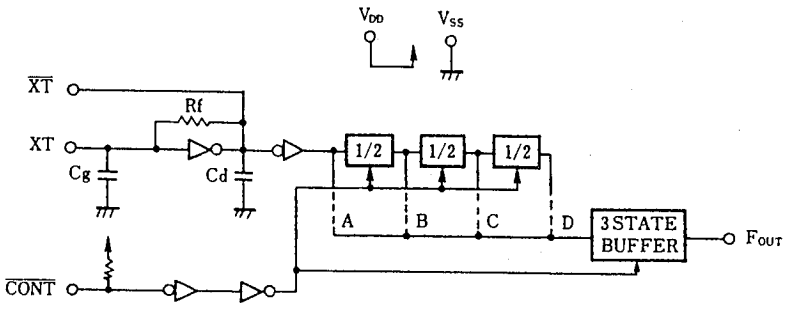
■ COORDINATES

Unit: μm

No.	PAD	X	Y
1	$\overline{CONT}$	-408	248
2	XT	-408	81
3	$\overline{XT}$	-408	-86
4	V_{SS}	-408	-248
5	F_{OUT}	464	-248
6	NC	-	-
7	NC	-	-
8	V_{DD}	464	248

Chip Size : 1.29 X 0.8mm
Chip Center : X=0μm,Y=0μm
Chip Thickness : 400μm±30μm
(Note) No. 6 and 7 terminals are only for package type information. There are no PAD on the chip.

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

NO.	SYMBOL	FUNCTION
1	$\overline{CONT}$	3-State Output Control and Divider Reset

$\overline{CONT}$	F_{OUT}
H	Output either one frequency from f_0, $f_0/2$, $f_0/4$ and $f_0/8$
L	Output High Impedance and Divider Reset

2 3	XT $\overline{XT}$	Quartz Crystal Connecting Terminals
5	F_{OUT}	Output either one frequency from f_0, $f_0/2$, $f_0/4$ and $f_0/8$
8	V_{DD}	+ 5V
4	V_{SS}	GND

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.5 ~ +7.0	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_O	-0.5 ~ V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Output Current	I_O	±25	mA
Power Dissipation (EMP)	P_D	200	mW
Operating Temperature Range	Topr	-40 ~ + 85	℃
Storage Temperature Range	Tstg	-55 ~ +125	℃

Note) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the circuit.

■ ELECTRICAL CHARACTERISTICS

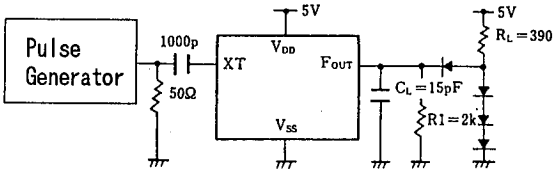
(Ta=25℃, V_{DD}=5V)

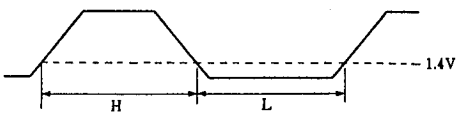
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V_{DD}		4		6	V
Operating Current	I_{DD1}	A,B,C,D f_{OSC}=24MHz, No Load			15	mA
	I_{DD2}	H,J,K,L f_{OSC}=48MHz, No Load			25	
	I_{DD3}	Q,R,S,T f_{OSC}=48MHz, No Load			28	
Stand-by Current	Ist	$\overline{CONT}$,XT=V_{SS}, No Load (Note)			1	μA
Input Voltage	V_{IH}		3.5		5.0	V
	V_{IL}		0		1.5	
Output Current	I_{OH}	V_{OH}=4.5V	4			mA
	I_{OL}	V_{OL}=0.5V	16			
Input Current	I_{IN}	$\overline{CONT}$ Terminal, $\overline{CONT}$=V_{SS}	125	250	500	μA
3-St Off-leakage Current	I_{OZ}	$\overline{CONT}$=V_{SS}, F_{OUT}=V_{SS} or V_{DD}			±0.1	μA
Internal Capacitor	Cg,Cd	A,B,C,D Version, f_{OSC}=24MHz		28		pF
		H,J,K,L Version, f_{OSC}=48MHz		20		
		Q,R,S,T Version, f_{OSC}=48MHz		17		
Max. Oscillation Freq.	f_{MAX}	A,B,C,D Version	35			MHz
		H,J,K,L Version	50			
		Q,R,S,T Version	75			
Output Signal Symmetry	SYM	C_L=15pF, RL=390Ω at 1.4V	45	50	55	%
Output Signal Rise Time	t_r	C_L=15pF, R_L=390Ω, 2.4V-0.4V			6	ns
Output Signal Fall Time	t_f	C_L=15pF, R_L=390Ω, 2.4V-0.4V			4	ns

Note) Excluding input current on $\overline{CONT}$ terminal.

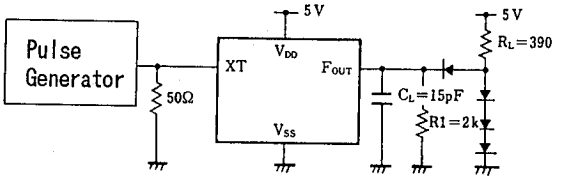
■ MEASUREMENT CIRCUITS

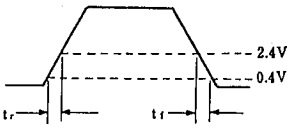
(1) Output Signal Symmetry (C_L=15pF, R_L=390Ω)





(2) Output Signal Rise/Fall Time (C_L=15pF, R_L=390Ω)





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