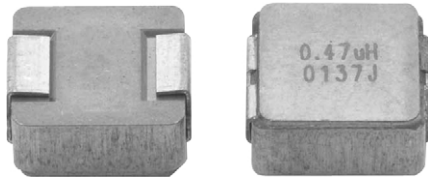


# IHLP<sup>®</sup> Commercial Inductors, Low DCR Series



**DESIGN SUPPORT TOOLS** click logo to get started



STANDARD ELECTRICAL SPECIFICATIONS				
L <sub>0</sub> INDUCTANCE ± 20 % AT 100 kHz, 0.25 V, 0 A (µH)	DCR TYP. 25 °C (mΩ)	DCR MAX. 25 °C (mΩ)	HEAT RATING CURRENT DC TYP. (A) (1)	SATURATION CURRENT DC TYP. (A) (2)
1.0	7.6	8.0	12.5	9.5
2.2	15.7	16.5	9.0	7.0
3.3	24.8	26.0	7.0	6.5
4.7	31.8	33.4	6.0	4.0
6.8	44.6	46.8	5.5	4.0
8.2	52.3	54.9	5.0	4.0
10	67.8	71.2	4.0	3.5
22	128.9	135.0	2.9	2.5

**Notes**

- All test data is referenced to 25 °C ambient
- Operating temperature range -55 °C to +125 °C
- The part temperature (ambient + temp. rise) should not exceed 125 °C under worst case operating conditions. Circuit design, component placement, PWB trace size and thickness, airflow and other cooling provisions all affect the part temperature. Part temperature should be verified in the end application.
- Rated operating voltage (across inductor) = 50 V
- (1) DC current (A) that will cause an approximate ΔT of 40 °C
- (2) DC current (A) that will cause L<sub>0</sub> to drop approximately 20 %

**FEATURES**

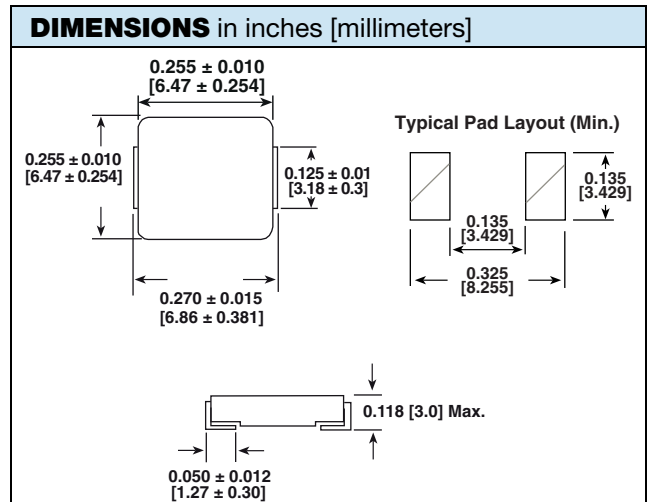
- Shielded construction
- Frequency range up to 1.0 MHz
- Lowest DCR/µH, in this package size
- Powered iron composition provides soft saturation
- Handles high transient current spikes without hard saturation
- Ultra low buzz noise, due to composite construction
- IHLP design. PATENT(S): [www.vishay.com/patents](http://www.vishay.com/patents)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

**APPLICATIONS**

- PDA / notebook / desktop / server applications
- High current POL converters
- Low profile, high current power supplies
- Battery powered devices
- DC/DC converters in distributed power systems
- DC/DC converter for Field Programmable Gate Array (FPGA)



DESCRIPTION				
IHLP-2525CZ-11	1.0 µH	± 20 %	ER	e3
MODEL	INDUCTANCE VALUE	INDUCTANCE TOLERANCE	PACKAGE CODE	JEDEC <sup>®</sup> LEAD (Pb)-FREE STANDARD

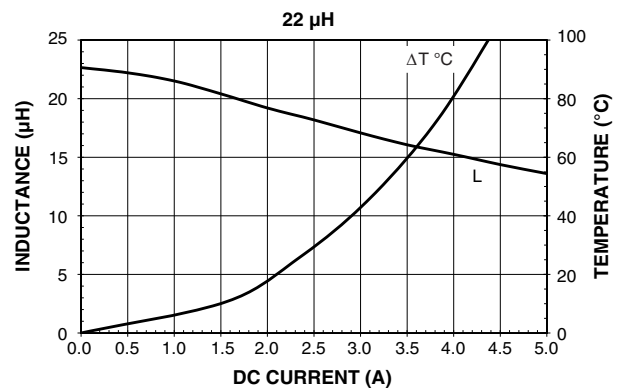
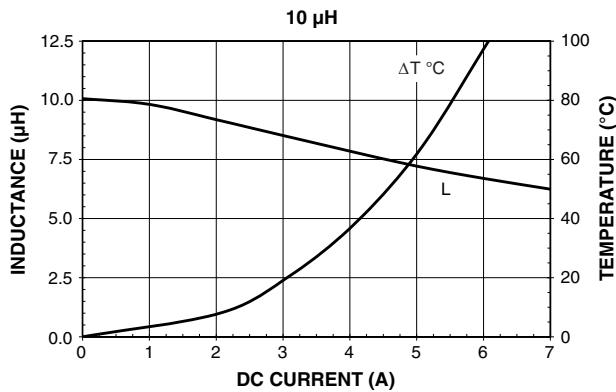
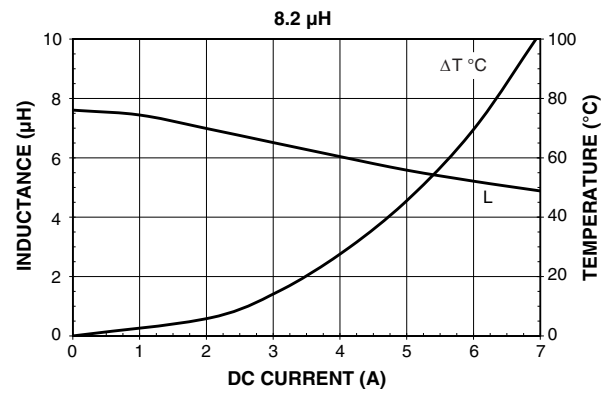
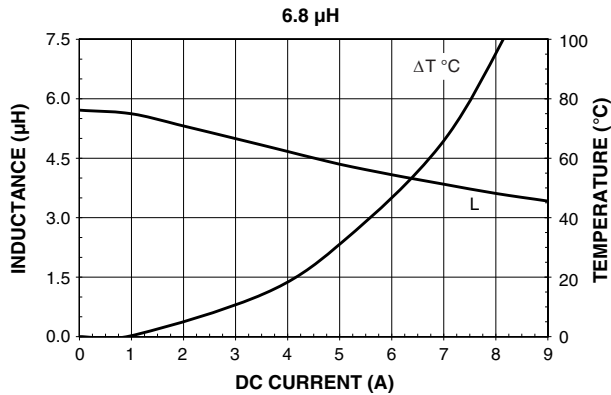
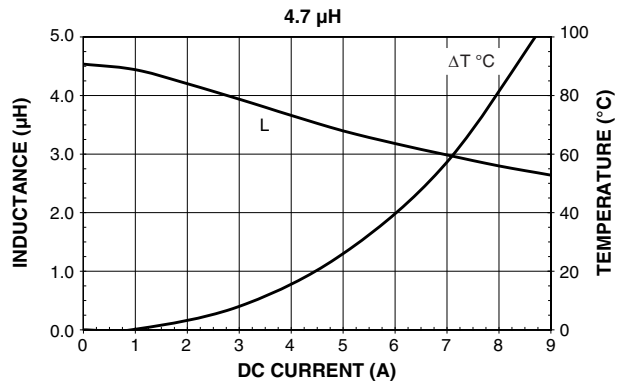
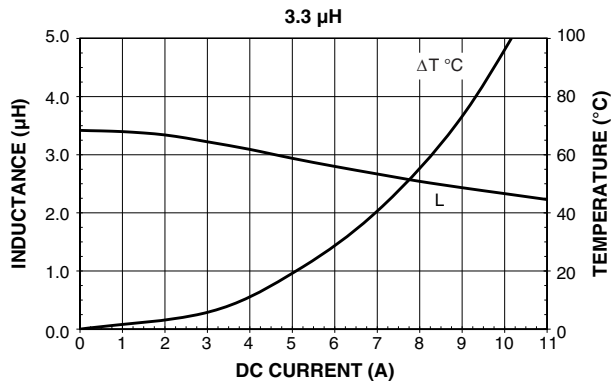
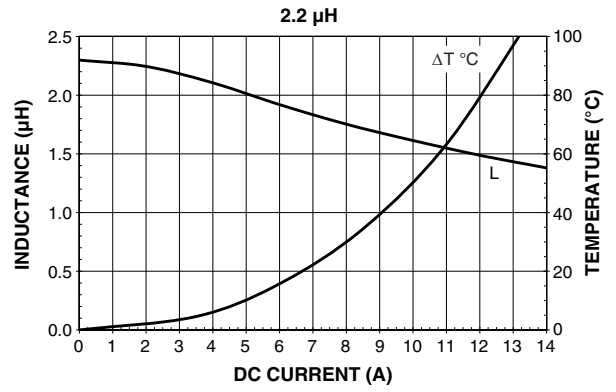
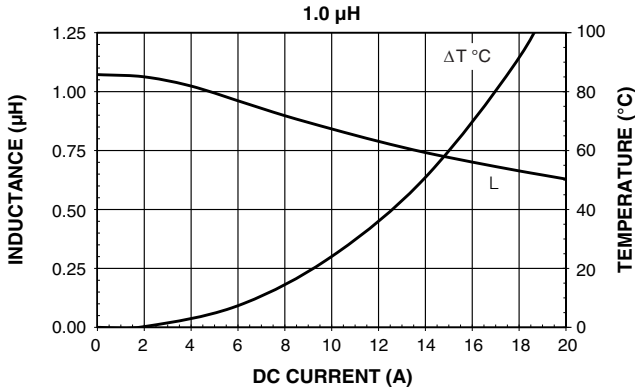
GLOBAL PART NUMBER																	
I	H	L	P	2	5	2	5	C	Z	E	R	1	R	0	M	1	1
PRODUCT FAMILY				SIZE				PACKAGE CODE		INDUCTANCE VALUE		TOL.	SERIES				

**PATENT(S):** [www.vishay.com/patents](http://www.vishay.com/patents)

This Vishay product is protected by one or more United States and international patents.



PERFORMANCE GRAPHS





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