4-TO-2 DVI/HDMI SWITCH

FEATURES

- **A 4-to-2 Single-Link or 2-to-1 Dual-Link DVI/HDMI Physical Layer Switch**
- **Compatible with HDMI 1.3a**
- **Supports 2.25 Gbps Signaling Rate for 480i/p, 720i/p, and 1080i/p Resolutions up to 12-Bit Color Depth**
- **Integrated Receiver Terminations**
- **8-dB Receiver Equalizer Compensates for Losses From Standard HDMI Cables**
- **Selectable Output De-Emphasis Compensates for Losses From Flat Cables**
- **High-Impedance Outputs When Disabled**
- **I^2C Repeater Isolates Bus Capacitance at Both Ends**
- **TMDS Inputs HBM ESD Protection Exceeds 6 kV**
- **3.3-V Supply Operation**
- **128-Pin TQFP Package**
- **ROHS Compatible and 260°C Reflow Rated**

APPLICATIONS

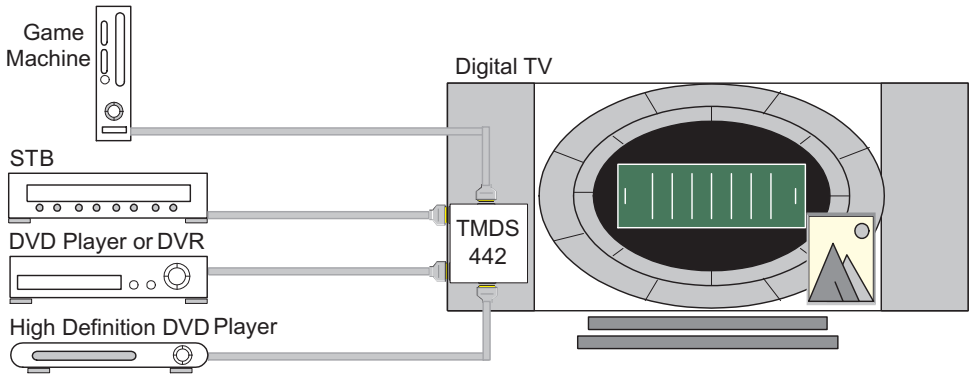
- **Digital TV**
- **Digital Projector**
- **Audio Video Receiver**
- **DVI or HDMI Switch**

DESCRIPTION

The TMDS442, 4-to-2 port DVI/HDMI switch, allows up to 4 digital video interface (DVI) or high-definition multimedia interface (HDMI) ports to be switched to two independent display blocks. The essential requirement of picture-in-picture display from two digital audiovisual sources is having two individual DVI or HDMI receivers in a digital display system. TMDS442 supports two DVI or HDMI receivers to enable multiple-source selection (picture-in-picture), as well as supports acting as a 4-input 1-output video switch.

Each input or output port contains one 5-V power indicator (5V_PWR), one hot plug detector (HPD), a pair of I^2C interface signals (SCL/SDA), and four TMDS channels supporting data rates up to 2.25 Gbps. The 5-V power indicator and the hot plug detector are pulled down with internal resistors, forcing a low state on these pins until receiving a valid high signal. The I^2C interface is constructed by an I^2C repeater circuit to isolate the capacitance form both ends of the buses. TMDS receivers integrate 50-Ω termination resistors pulled up to V_{CC}, which eliminates the need for external terminations. An 8-dB input equalization cooperates to each TMDS receiver inputs to optimize system performance through 5-meter or longer DVI or HDMI compliant cables.

TYPICAL APPLICATION



A precision resistor is connected externally from the VSADJ pin to ground, for setting the differential output voltage to be compliant with the TMDS standard for all TMDS driver outputs. The PRE pin controls the TMDS output to be operated under either a standard TMDS mode or an AC de-emphasis mode. When PRE = high, a 3-dB AC de-emphasis TMDS output swing is selected to pre-condition the output signals to overcome signal impairments that may exist between the output of the TMDS442 and the HDMI receiver placed at a remote location.

Each sink output port can be configured with the SA, SB, $\overline{OE}$, I2CEN, and PRE pins. SA1, SB1, $\overline{OE1}$, I2CEN1, and PRE1 regulate the behaviour of sink port 1; SA2, SB2, $\overline{OE2}$, I2CEN2, and PRE2 regulate the behaviour of sink port 2. These control signals are hard-wire controlled by GPIO interface, or through a local I^2C interface. When GE = low, the configurations are done through a local I^2C interface, LC_SCL, LC_SDA, LC_A0, and LC_A1 pins, and the 5V_EN can be programmed through the local I^2C interface. It is default high after device powered on. When GE = high, the configurations are done through GPIO pins regardless the value of the 5V_EN in the internal I^2C registers.

The two bit source selector pins, SA and SB, determine the source transferred to the sink port. The internal multiplexer interconnects the TMDS channels and I^2C interface from the selected source port to the sink port. The HPD output of the selected source port follows the status of the HPD_SINK. Since two of the source ports will always be unconnected to any output, the I^2C interfaces of unselected ports are isolated and the HPD outputs of an unselected port are pulled low.

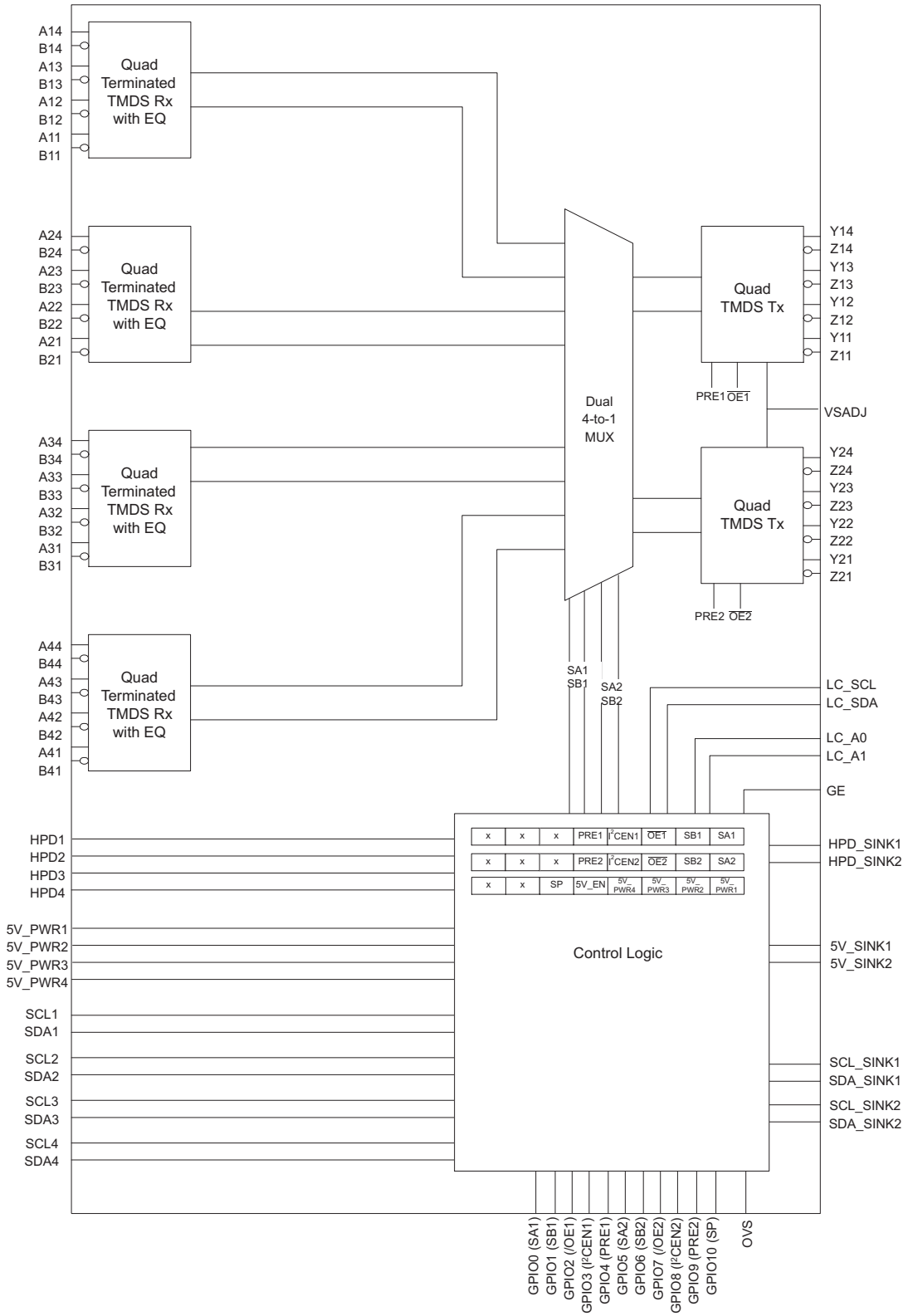
The TMDS outputs of each of the sink ports are enabled based on the $\overline{OE}$ signal and 5V_PWR signal (from the selected source port). When $\overline{OE}$ is low, for an output port, and the 5V_PWR signal from the selected source port is high, the TMDS output signals are enabled; otherwise they are disabled, and high impedance.

The I^2C driver at sink side, SCL_SINK and SDA_SINK, are enabled by setting I2CEN high. When I2CEN is low, the I^2C driver can not forward a low state to the I^2C bus connected at the sink port. A hard wire output voltage select pin, OVS, allows adjustable output voltage level to SCL_SINK and SDA_SINK to optimise noise margins while interfacing to different HDMI receivers. The I^2C driver of each source port, SCL and SDA, is controlled by its 5V_PWR signal. A valid 5-V signal appearing at the input of 5V_PWR enables the I^2C driver of the source port.

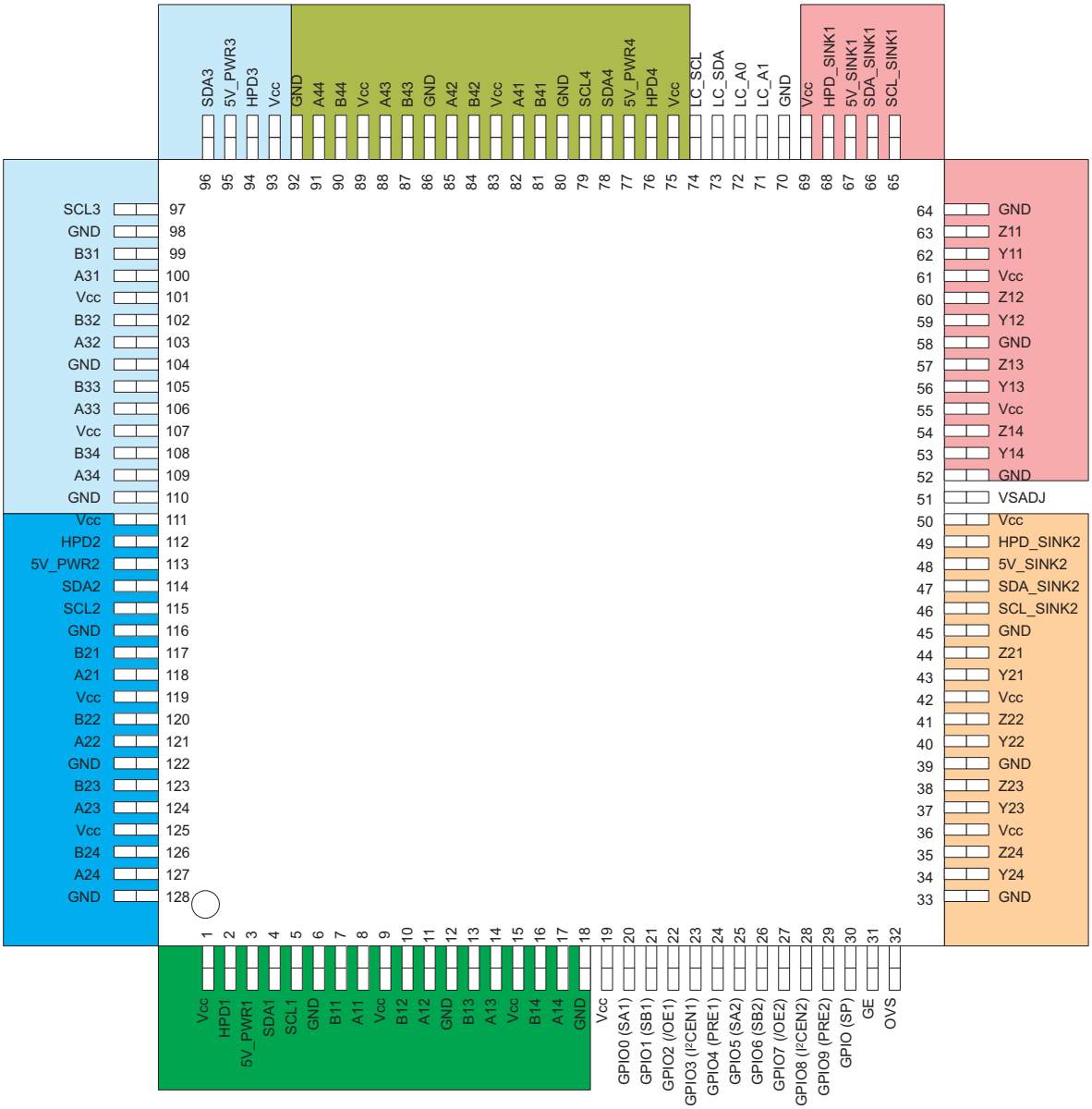
The device is packaged in a 128-pin PowerPAD TQFP package and characterized for operation from 0°C to 70°C.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



PNP PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

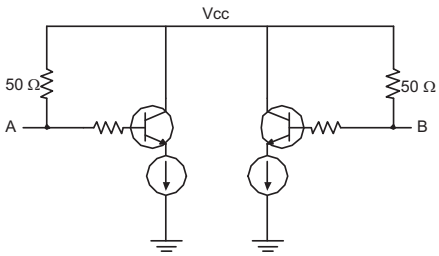
TERMINAL		I/O	DESCRIPTION
NAME	NO.		
A11, A12, A13, A14 A21, A22, A23, A24 A31, A32, A33, A34 A41, A42, A43, A44	8, 11, 14, 17 118, 121, 124, 127 100, 103, 106, 109 82, 85, 88, 91	I	Source port 1 TMDS positive inputs Source port 2 TMDS positive inputs Source port 3 TMDS positive inputs Source port 4 TMDS positive inputs
B11, B12, B13, B14 B21, B22, B23, B24 B31, B32, B33, B34 B41, B42, B43, B44	7, 10, 13, 16 117, 120, 123, 126 99, 102, 105, 108 81, 84, 87, 90	I	Source port 1 TMDS negative inputs Source port 2 TMDS negative inputs Source port 3 TMDS negative inputs Source port 4 TMDS negative inputs

TERMINAL FUNCTIONS (continued)

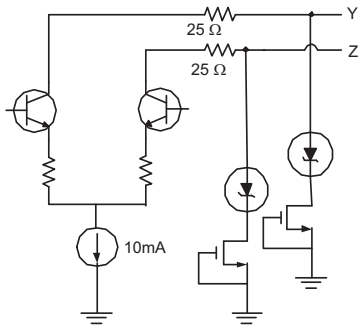
TERMINAL		I/O	DESCRIPTION
NAME	NO.		
Y11, Y12, Y13, Y14 Y21, Y22, Y23, Y24	62, 59, 56, 53 43, 40, 37, 34	O	Sink port 1 TMDS positive outputs Sink port 2 TMDS positive outputs
Z11, Z12, Z13, Z14 Z21, Z22, Z23, Z24	63, 60, 57, 54 44, 41, 38, 35	O	Sink port 1 TMDS negative outputs Sink port 2 TMDS negative outputs
SCL1 SDA1	54	IO	Source Port 1 DDC I^2C clock line Source Port 1 DDC I^2C data line
SCL2 SDA2	115 114	IO	Source Port 2 DDC I^2C clock line Source Port 2 DDC I^2C data line
SCL3 SDA3	97 96	IO	Source Port 3 DDC I^2C clock line Source Port 3 DDC I^2C data line
SCL4 SDA4	79 78	IO	Source Port 4 DDC I^2C clock line Source Port 4 DDC I^2C data line
SCL_SINK1 SDA_SINK1	65 66	IO	Sink port 1 DDC I^2C clock line Sink port 1 DDC I^2C data line
SCL_SINK2 SDA_SINK2	46 47	IO	Sink port 2 DDC I^2C clock line Sink port 2 DDC I^2C data line
HPD1 HPD2 HPD3 HPD4	2 112 94 76	O	Source Port 1 hot plug detector output Source Port 2 hot plug detector output Source Port 3 hot plug detector output Source Port 4 hot plug detector output
HPD_SINK1 HPD_SINK2	68 49	I	Sink port 1 hot plug detector input Sink port 2 hot plug detector input
5V_PWR1 5V_PWR 2 5V_PWR 3 5V_PWR 4	3 113 95 77	I	Source Port 1 5-V power signal input Source Port 2 5-V power signal input Source Port 3 5-V power signal input Source Port 4 5-V power signal input
5V_SINK1 5V_SINK 2	67 48	O	Sink Port 1 5-V power indicator output Sink Port 2 5-V power indicator output
LC_SCL LC_SDA	74 73	IO	Local I^2C clock line Local I^2C data line
LC_A0 LC_A1	72 71	I	Local I^2C address bit 0 Local I^2C address bit 1
GE	31	I	GPIO Enable L: Local I^2C pins are active, GPIO pins are high impedance H: GPIO pins are active, local I^2C pins are high impedance
GPIO0 GPIO1 GPIO2 GPIO3 GPIO4	20 21 22 23 24	I	SA1 – Sink port 1 source selector $\overline{SB1}$ – Sink port 1 source selector $\overline{OE1}$ – Sink port 1 TMDS output enable I2CEN1 – Sink port 1 DDC I^2C output enable PRE1 – Sink port 1 TMDS AC de-emphasis mode selector
GPIO5 GPIO6 GPIO7 GPIO8 GPIO9 GPIO10 GPIO11	25 26 27 28 29 30 32	I	SA2 – Sink port 2 source selector $\overline{SB2}$ – Sink port 2 source selector $\overline{OE2}$ – Sink port 2 TMDS output enable I2CEN2 – Sink port 2 DDC I^2C output enable PRE2 – Sink port 2 TMDS AC de-emphasis mode selector SP – Sink priority selector OVS – SCL_SINK/SDA_SINK output voltage select
VSADJ	51	I	TMDS compliant voltage swing control
Vcc	1, 9, 15, 19 36, 42, 50, 55, 61 69, 75, 83, 89, 93 101, 107, 111, 119, 125		Power supply
GND	6, 12, 18, 33, 39, 45, 52, 58, 64 70, 80, 86, 92 98, 104, 110, 116, 122, 128		Ground

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

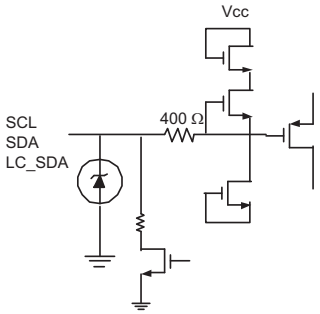
TMDS Input Stage



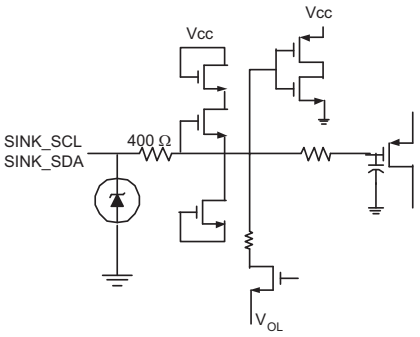
TMDS Output Stage



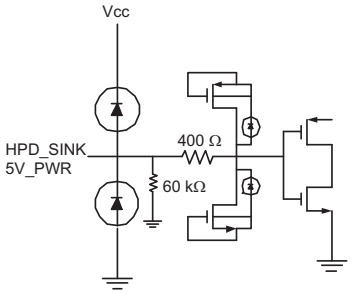
Source-Side I2C Input/Output Stage



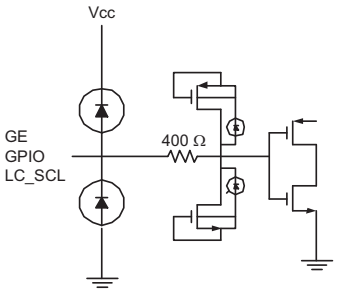
Sink-Side I2C Input/Output Stage



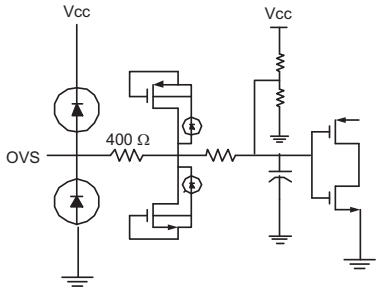
Status Input Stage



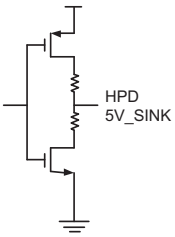
Control Input Stage



Control Input Stage



Status Output Stage



ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE
TMDS442PNP	TMDS442	128-PIN TQPF
TMDS442PNPR	TMDS442	128-PIN TQPF Tape/Reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
V_{CC} Supply voltage range (2)			–0.5 V to 4 V
Voltage range	Aim*, Bim		2.5 V to 4 V
	Yjm, Zjm, , Vsadjj, HPDi, 5V_SINKj, LC_SCL, LC_SDA, LC_A0, LC_A1, GE, GPIO		–0.5V to 4 V
	SCLi, SCL_SINKj, SDAi, SDA_SINKj, HPD_SINKj, 5V_PWRi		–0.5 V to 6 V
Electrostatic discharge	Human body model(3)	Aim, Bim	±6 kV
		All pins	±5 kV
	Charged-device model(4) (all pins)		±1500 V
	Machine model (5) (all pins)		±200 V
Continuous power dissipation			See Dissipation Rating Table

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A

DISSIPATION RATINGS

PACKAGE	PCB JEDEC STANDARD	$T_A \le 25°C$	DERATING FACTOR (1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
128-TQFP PNP	Low-K(2)	2129.47 mW	21.2947 mW/°C	1171.20 mW
128-TQFP PNP	High-K(3)	4308.48 mW	43.0848 mW/°C	2369.66 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3
(3) In accordance with the High-K thermal metric definitions of EIA/JESD51-7

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance			7.86		°C/W
$R_{\theta JC}$	Junction- to-case thermal resistance			19.5		°C/W
P_D	Device power dissipation	$V_{IH} = V_{CC}$, $V_{IL} = V_{CC}$ - 0.6 V, R_T = 50 Ω, AV_{CC} = 3.3 V, V_{CC} = 3.6 V, R_{VSADJ} = 4.6 kΩ, PRE = Low or high Ai/Bi(2:4)= 1.65 Gbps HDMI data pattern, Ai/Bi(1) = 165 MHz clock			1431	mW

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
T_A	Operating free-air temperature	0		70	°C
TMDS DIFFERENTIAL PINS (A/B)					
V_{IC}	Input common mode voltage	V_{CC}–400		V_{CC}+10	mV
V_{ID}	Receiver peak-to-peak differential input voltage	150		1560	mVp-p
R_{VSADJ}	Resistor for TMDS compliant voltage swing range	4.6	4.64	4.68	kΩ
AV_{CC}	TMDS Output termination voltage, see Figure 3	3	3.3	3.6	V
R_T	Termination resistance, see Figure 3	45	50	55	Ω
	Signaling rate	0		2.25	Gbps
CONTROL PINS (LC_A0, LC_A1, GE, GPIO)					
V_{IH}	LVTTL High-level input voltage	2		V_{CC}	V

RECOMMENDED OPERATING CONDITIONS (continued)

		MIN	NOM	MAX	UNIT
V_{IL}	LVTTL Low-level input voltage	GND		0.8	V
CONTROL PINS (OVS)					
V_{IH}	LVTTL High-level input voltage	3		3.6	V
V_{IL}	LVTTL Low-level input voltage	-0.5		0.5	V
STATUS PINS (HPD_SINK, 5V_PWR)					
V_{IH}	High-level input voltage	2		5.3	V
V_{IL}	Low-level input voltage	GND		0.8	V
DDC I/O PINS (SCL_SINK, SDA_SINK)					
V_{IH}	High-level input voltage	$0.7V_{CC}$		5.5	V
V_{IL}	Low-level input voltage	-0.5		$0.3V_{CC}$	V
V_{ILC}	Low-level input voltage contention (1)	-0.5		0.4	V
DDC I/O PINS (SCL, SDA)					
V_{IH}	High-level input voltage	2.1		5.5	V
V_{IL}	Low-level input voltage	-0.5		1.5	V
LOCAL I^2C PINS (LC_SCL, LC_SDA)					
V_{IH}	High-level input voltage	$0.7V_{CC}$		V_{CC}	V
V_{IL}	Low-level input voltage	-0.5		$0.3V_{CC}$	V

(1) V_{IL} specification is for the first low level seen by the SCL_SINK/SDA_SINK lines. V_{ILC} is for the second and subsequent low levels seen by the SCL_SINK/SDA_SINK lines.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
I_{CC}	Supply current	$V_{IH} = V_{CC}$, $V_{IL} = V_{CC} - 0.4$ V, $R_T = 50\ \Omega$, $AV_{CC} = 3.3$ V, Ai/Bi(2:4) = 1.65-Gbps HDMI data pattern, Ai/Bi(1) = 165-MHz Pixel clock			250	412 (2)	mA
P_D	Power dissipation	$V_{IH} = V_{CC}$, $V_{IL} = V_{CC} - 0.4$ V, $R_T = 50\ \Omega$, $AV_{CC} = 3.3$ V, Ai/Bi(2:4) = 1.65-Gbps HDMI data pattern, Ai/Bi(1) = 165-MHz Pixel clock			640	1344 (2)	mW
TMDS DIFFERENTIAL PINS (A/B, Y/Z)							
V_{OH}	Single-ended high-level output voltage	See Figure 4, $AV_{CC} = 3.3$ V, $R_T = 50\ \Omega$		AV_{CC}–10		AV_{CC}+10	mV
V_{OL}	Single-ended low-level output voltage			AV_{CC}–600		AV_{CC}–400	mV
V_{swing}	Single-ended output swing voltage			400		600	mV
$V_{OD(O)}$	Overshoot of output differential voltage					15%	$2\times V_{swing}$
$V_{OD(U)}$	Undershoot of output differential voltage					25%	$2\times V_{swing}$
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states					5	mV
$I_{(O)OFF}$	Single-ended standby output current	$0\ V \le V_{CC} \le 1.5$ V, $AV_{CC} = 3.3$ V, $R_T = 50\ \Omega$		–10		10	µA
$V_{OD(pp)}$	Peak-to-peak output differential voltage	See Figure 5, PRE = High, $AV_{CC} = 3.3$ V, $R_T = 50\ \Omega$		800		1200	mVp-p
$V_{ODE(SS)}$	Steady state output differential voltage with de-emphasis			560		840	
$I_{(OS)}$	Short circuit output current	See Figure 6	PRE = Low	-12		12	mA
			PRE = High	-15		15	
$V_{I(open)}$	Single-ended input voltage under high impedance input or open input	$I_I = 10$ µA		V_{CC}–10		V_{CC}+10	mV
R_{INT}	Input termination resistance	$V_{IN} = 2.9$ V		45	50	55	Ω
STATUS PINS (HPD_SINK, 5V_PWR)							

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) The maximum rating is characterized under 3.6 V V_{CC}.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{IH}	High-level digital input current	V_{IH} = 5.3 V		-150		150	µA
		V_{IH} = 2 V or V_{CC}		-85		85	
I_{IL}	Low-level digital input current	V_{IL} = GND or 0.8 V		-20		20	µA
STATUS PINS (HPD, 5V_SINK)							
V_{OH}	High-level output voltage	I_{OH} = -4 mA		2.4		V_{CC}	V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA		GND		0.4	V
CONTROL PINS (LC_A0, LC_A1, GE, GPIO)							
I_{IH}	High-level digital input current	V_{IH} = 2 V or V_{CC}		-10		10	µA
I_{IL}	Low-level digital input current	V_{IL} = GND or 0.8 V		-10		10	µA
C_I	Input capacitance	V_I = GND or V_{CC}				10	pF
DDC I/O PINS (SCL_SINK, SDA_SINK)							
I_{lkg}	Input leakage current	V_I = 5.5 V		-50		50	µA
		V_I = V_{CC}		-10		10	
I_{OH}	High-level output current	V_O = 3.6 V		-10		10	µA
I_{IL}	Low-level input current	V_{IL} = GND		-40		40	µA
V_{OL}	Low-level output voltage	I_{OL} = 400 µA or 4 mA	OVS = NC	470		620	V
			OVS = GND	620		775	
			OVS = V_{CC}	775		950	
V_{OL}-V_{ILC}	Low-level input voltage below output low-level voltage level	Ensured by design	OVS = NC		70		mV
			OVS = GND		240		
			OVS = V_{CC}		420		
C_{IO}	Input/output capacitance	V_I = 5.0 V or 0 V, Freq = 100 kHz				25	pF
		V_I = 3.0 V or 0 V, Freq = 100 kHz				10	
DDC I/O PINS (SCL, SDA) AND LOCAL I^2C PINS (LC_SCL, LC_SDA)							
I_{lkg}	Input leakage current	V_I = 5.5 V		-50		50	µA
		V_I = V_{CC}		-10		10	
I_{OH}	High-level output current	V_O = 3.6 V		-10		10	µA
I_{IL}	Low-level input current	V_{IL} = GND		-10		10	µA
V_{OL}	Low-level output voltage	I_{OL} = 4 mA				0.2	V
C_I	Input capacitance	V_I = 5.0 V or 0 V, Freq = 100 kHz				25	pF
		V_I = 3.0 V or 0 V, Freq = 100 kHz				10	

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
TMDS DIFFERENTIAL PINS (Y/Z)						
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 4, AV_{CC} = 3.3 V, R_T = 50 Ω	250		800	ps
t_{PHL}	Propagation delay time, high-to-low-level output		250		800	ps
t_r	Differential output signal rise time (20% - 80%)		80		240	ps
t_f	Differential output signal fall time (20% - 80%)		80		240	ps
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)(2)				50	ps
$t_{sk(D)}$	Intra-pair differential skew, see Figure 7				75	ps
$t_{sk(o)}$	Inter-pair channel-to-channel output skew(3)				150	ps
$t_{sk(bb)}$	Bank-to-bank skew				300	ps
$t_{sk(pp)}$	Part-to-part skew (4)				1	ns
t_{en}	Enable time	See Figure 8			20	ns
t_{dis}	Disable time				20	ns
t_{sx}	TMDS Switch time				20	ns
$t_{jit(pp)}$	Peak-to-peak output jitter from Y/Z(1), residual jitter	See Figure 9, Ai/Bi(1) = 165-MHz clock, Ai/Bi(2:4) = 1.65-Gbps HDMI pattern, PRE = low Input: 5m 28AWG HDMI cable, Output: 3-Inch 8-mil trace width		10	30	ps
$t_{jit(pp)}$	Peak-to-peak output jitter from Y/Z(2:4), residual jitter			48	74	ps
$t_{jit(pp)}$	Peak-to-peak output jitter from Y/Z(1), residual jitter	See Figure 9, Ai/Bi(1) = 225-MHz clock, Ai/Bi(2:4) = 2.25-Gbps HDMI pattern, PRE = low Input: 5m 28AWG HDMI cable, Output: 3-Inch 8-mil trace width		18	33	ps
$t_{jit(pp)}$	Peak-to-peak output jitter from Y/Z(2:4), residual jitter			56	71	ps
CONTROL AND STATUS PINS (HPD_SINK, HPD, 5V_PWR, 5V_SINK)						
$t_{pd(HPD)}$	Propagation delay time	See Figure 8 C_L= 10 pF, $C_{L(DDC)}$ = 100 pF			15	ns
$t_{pd(5V)}$	Propagation delay time				15	ns
$t_{sx(HPD)}$	HPD Switch time				15	ns
$t_{sx(5V)}$	5-V Power switch time				15	ns
t_{sx}	DDC Switch time				1	µs
DDC I/O PINS (SCL, SCL_SINK, SDA, SDA_SINK)						
t_{PLH}	Propagation delay time, low-to-high-level output SCL_SINK/SDA_SINK to SCL/SDA	See Figure 11, OVS = NC	204		459	ns
t_{PHL}	Propagation delay time, high-to-low-level outputSCL_SINK/SDA_SINK to SCL/SDA		35		140	ns
t_{PLH}	Propagation delay time, low-to-high-level output SCL/SDA to SCL_SINK/SDA_SINK		194		351	ns
t_{PHL}	Propagation delay time, high-to-low-level output SCL/SDA to SCL_SINK/SDA_SINK		35		140	ns
t_r	Output signal rise time, SCL_SINK/SDA_SINK		500		800	ns
t_f	Output signal fall time, SCL_SINK/SDA_SINK		20		72	ns
t_r	Output signal rise time, SCL/SDA		796		999	ns
t_f	Output signal fall time, SCL/SDA		20		72	ns
t_{set}	Enable to start condition	See Figure 12	100			ns
t_{hold}	Enable after stop condition		100			ns

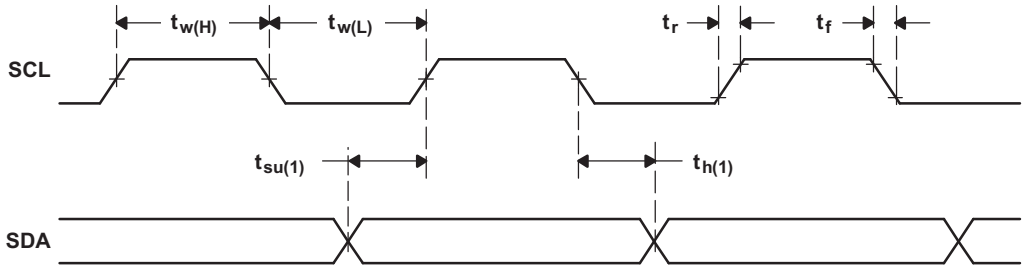
(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(p)}$ is the magnitude of the time difference between t_{PLH} and t_{PHL} of a specified terminal.
(3) $t_{sk(o)}$ is the magnitude of the difference in propagation delay times between any specified terminals of channel 2 to 4 of a device when inputs are tied together.
(4) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of channel 2 to 4 of two devices, or between channel 1 of two devices, when both devices operate with the same source, the same supply voltages, at the same temperature, and have identical packages and test circuits.

TIMING CHARACTERISTICS FOR LOCAL I²C INTERFACE (LC_SCL, LC_SDA, LC_AO, LC_A1)

PARAMETER		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	Clock frequency, SCL		100		400	kHz
$t_{w(L)}$	Clock low period, SCL low	4.7		1.3		μs
$t_{w(H)}$	Clock high period, SCL high	4		0.6		μs
t_r	Rise time, SCL and SDA		1000		300	μs
t_f	Fall time, SCL and SDA		300		300	μs
$t_{su(1)}$	Setup time, SDA to SCL	250		100		μs
$t_{h(1)}$	Hold time, SCL to SDA	0		0		μs
$t_{(buf)}$	BUS Free time between a STOP and START condition	4.7		1.3		μs
$t_{su(2)}$	Setup time, SCL to start condition	4.7		0.6		μs
$t_{h(2)}$	Hold time, start condition to SCL	4		0.6		μs
$t_{su(3)}$	Setup time, SCL to stop condition	4		0.6		μs
C_b (1)	Capacitive load for each bus line		400		400	pF

(1) C_b is the total capacitance of one bus line in pF.

PARAMETER MEASUREMENT INFORMATION



A. t_r and t_f are measured at 20% - 80% refered to V_{IHmin} and V_{ILmax} levels.

Figure 1. SCL and SDA Timing

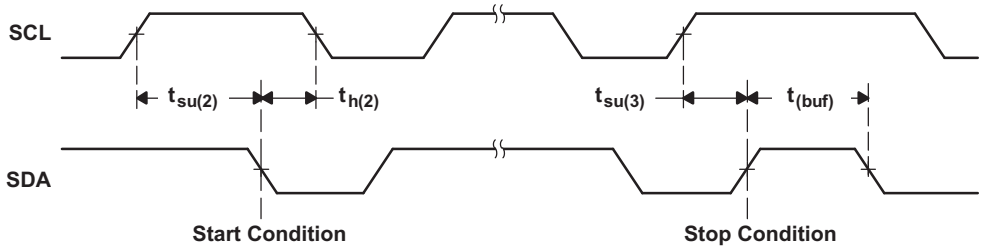


Figure 2. Start and Stop Conditions

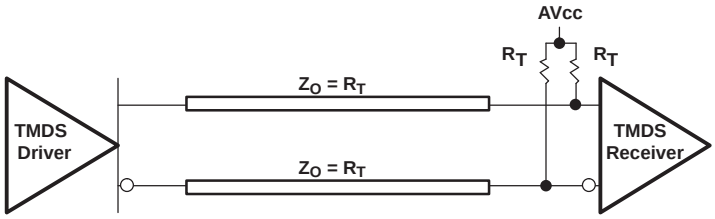
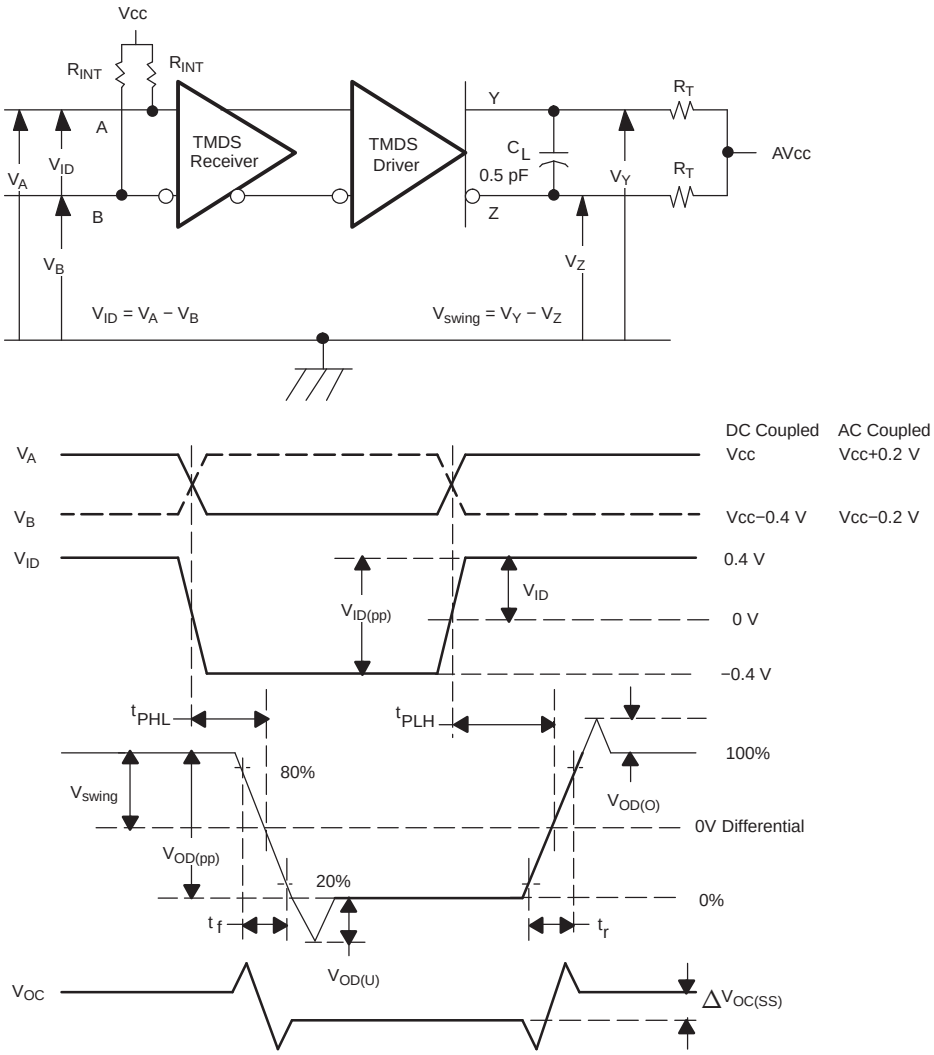


Figure 3. Typical Termination for TMDS Output Driver

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: PRE = low. All input pulses are supplied by a generator having the following characteristics: t_r or t_f < 100 ps, 100 MHz from Agilent 81250. C_L includes instrumentation and fixture capacitance within 0.06 m of the D.U.T. Measurement equipment provides a bandwidth of 20 GHz minimum.

Figure 4. TMDS Timing Test Circuit and Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

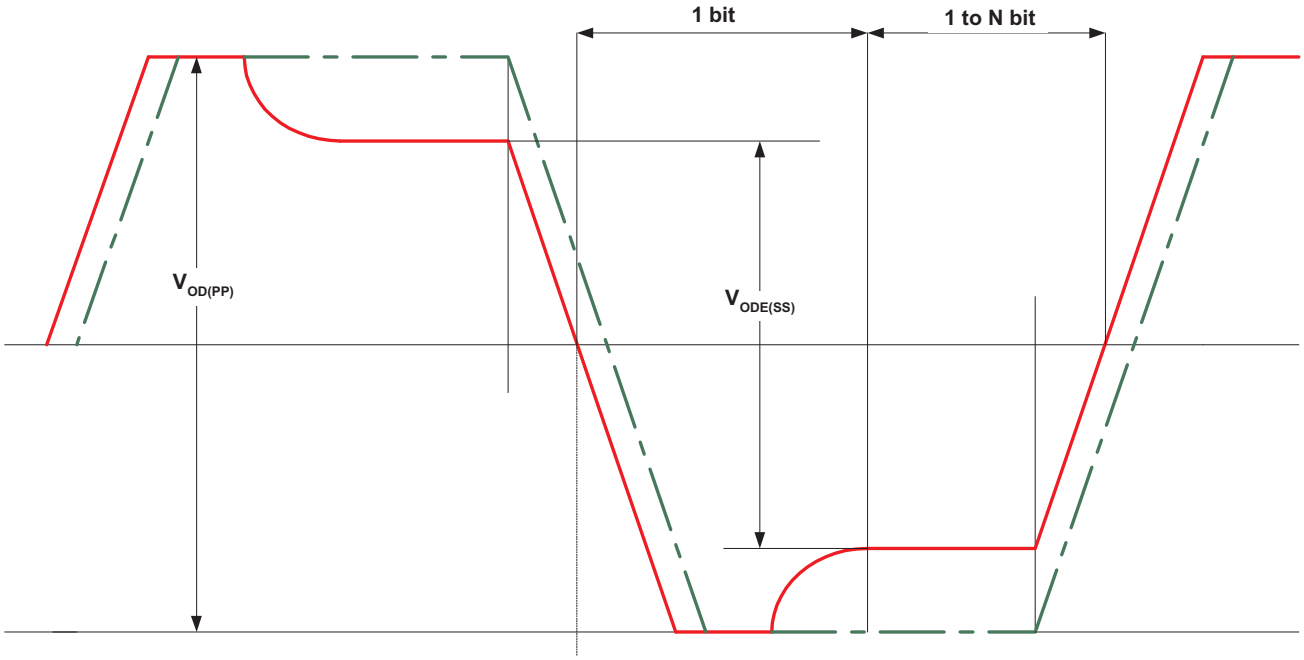


Figure 5. De-Emphasis Output Voltage Waveforms and Duration Measurement Definitions

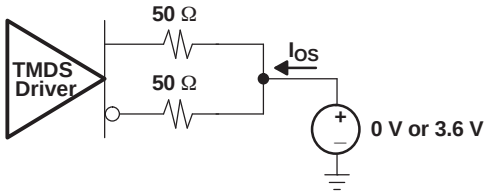


Figure 6. Short Circuit Output Current Test Circuit

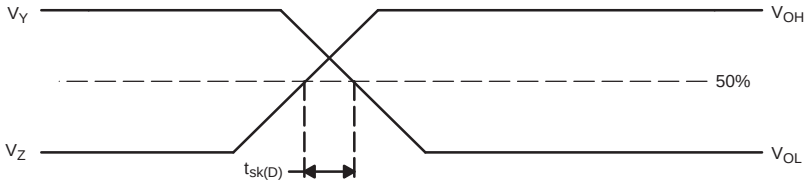


Figure 7. Definition of Intra-Pair Differential Skew

PARAMETER MEASUREMENT INFORMATION (continued)

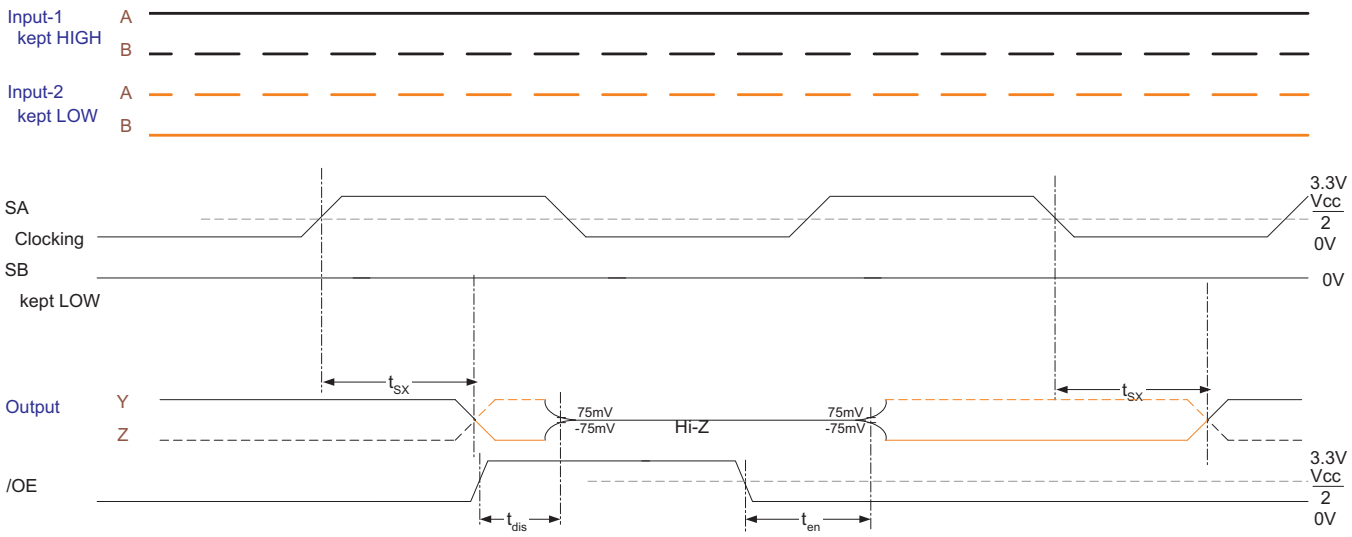
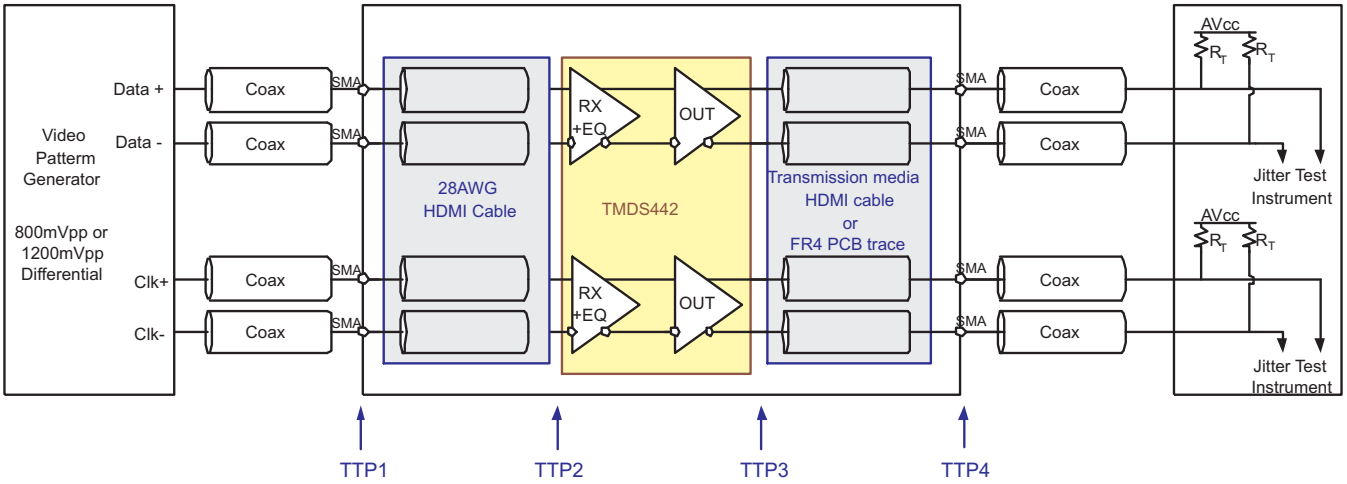


Figure 8. TMDS Outputs Control Timing Definitions



A. All jitters are measured in BER of 10^{-12}

B. The residual jitter reflects the total jitter measured at the TMDS442 output, TP3, subtract the total jitter from the signal generator, TP1

C. The input cable length and the output transmission media are specified in the test conditions.

Figure 9. Jitter Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

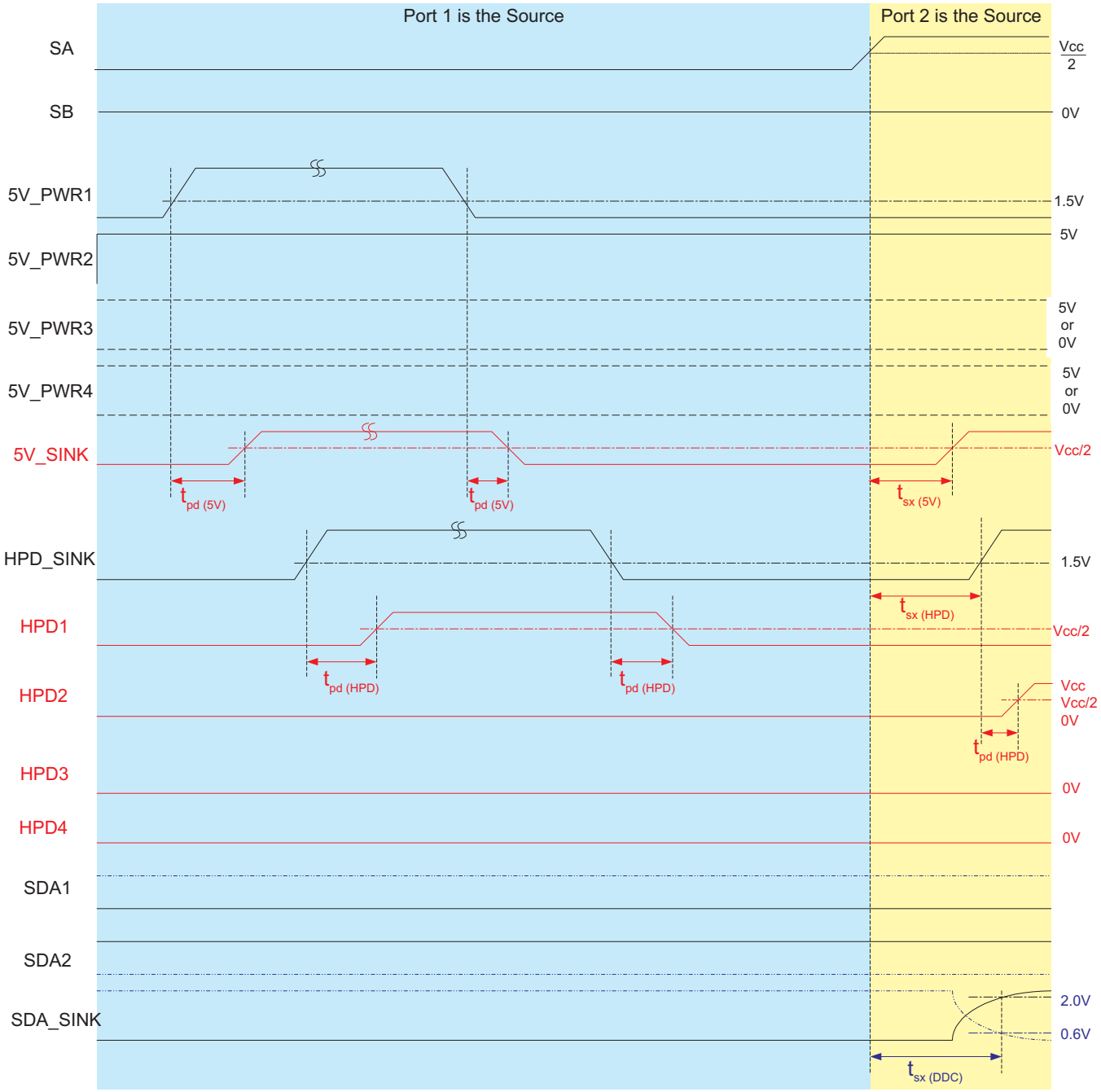


Figure 10. Post Switch Timing Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

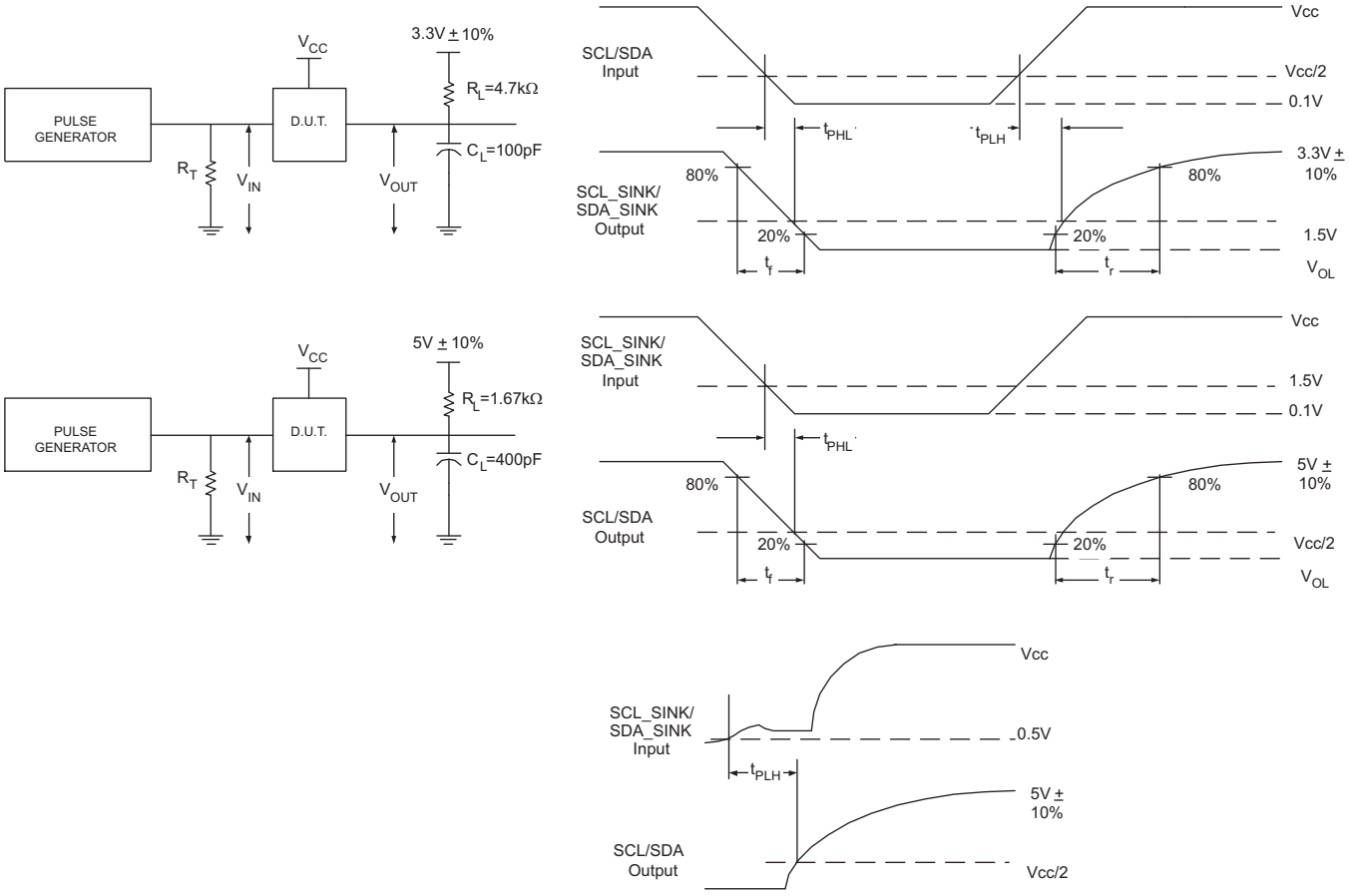


Figure 11. I²C Timing Test Circuit and Definition

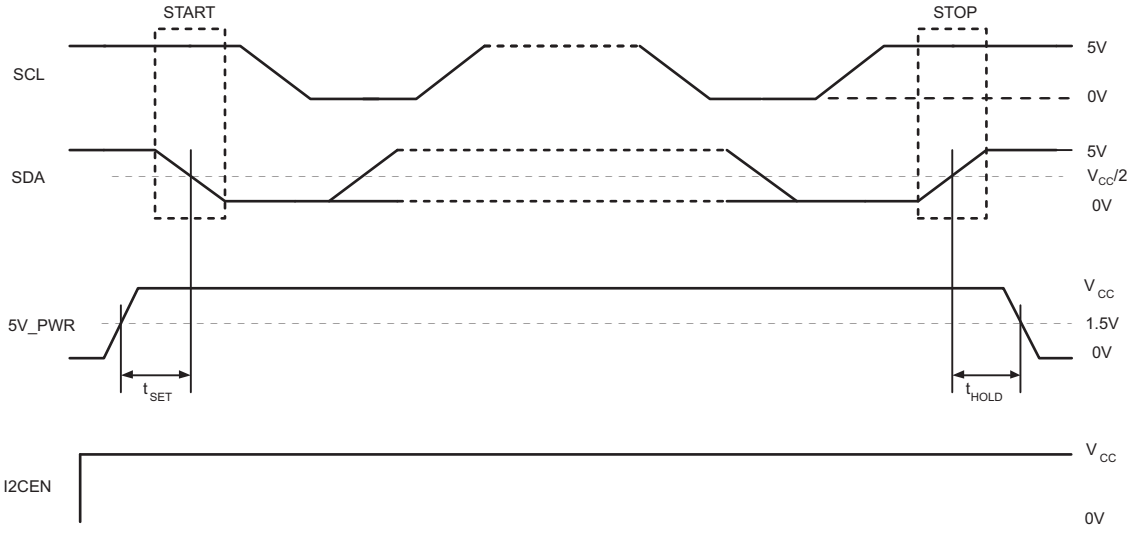


Figure 12. I²C Setup and Hold Definition

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREQUENCY

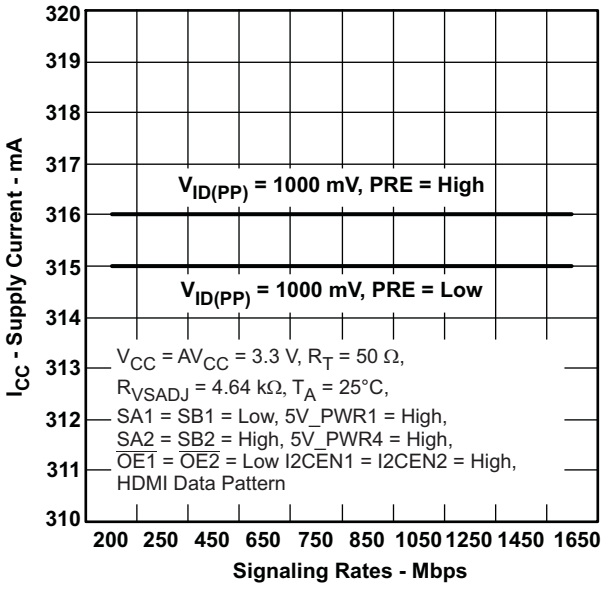


Figure 13.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

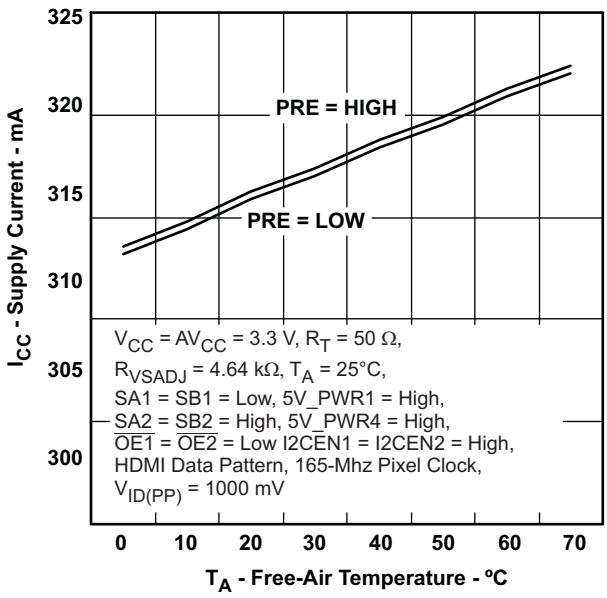


Figure 14.

RESIDUAL PEAK-TO-PEAK JITTER vs DATA RATE (DC Coupled Input: 5m Cable, Output: 1m Cable)

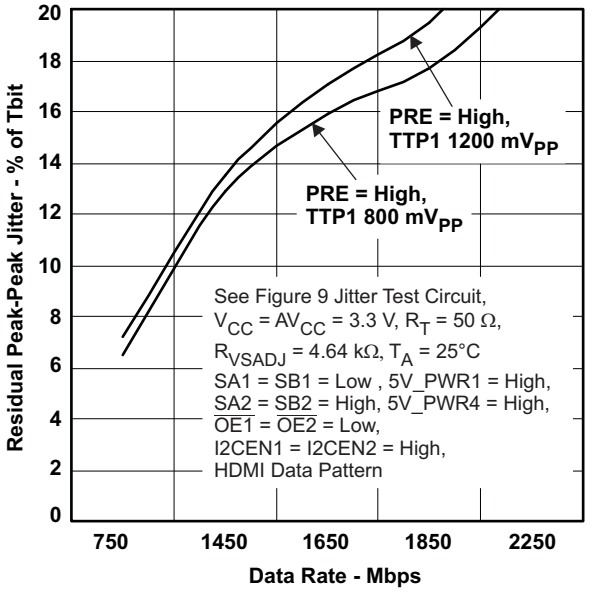


Figure 15.

RESIDUAL PEAK-TO-PEAK JITTER vs DATA RATE (DC Coupled Input: 5m Cable, Output: 0m Cable)

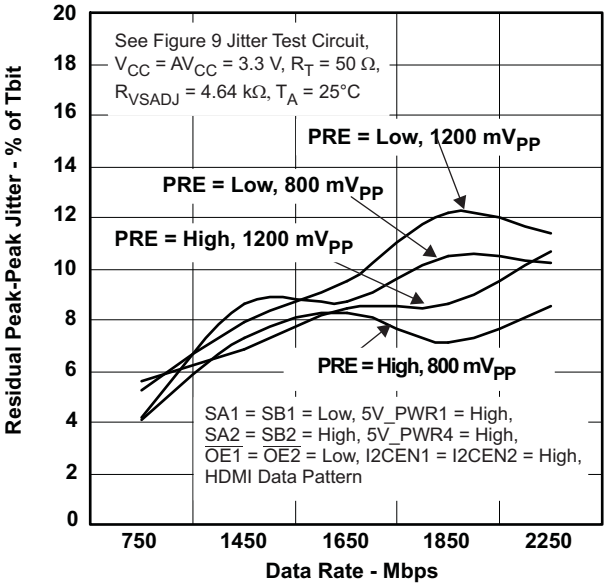


Figure 16.

TYPICAL CHARACTERISTICS (continued)

RESIDUAL PEAK-TO-PEAK JITTER vs DATA RATE (AC Coupled Input: 3m Cable, Output: 1m Cable)

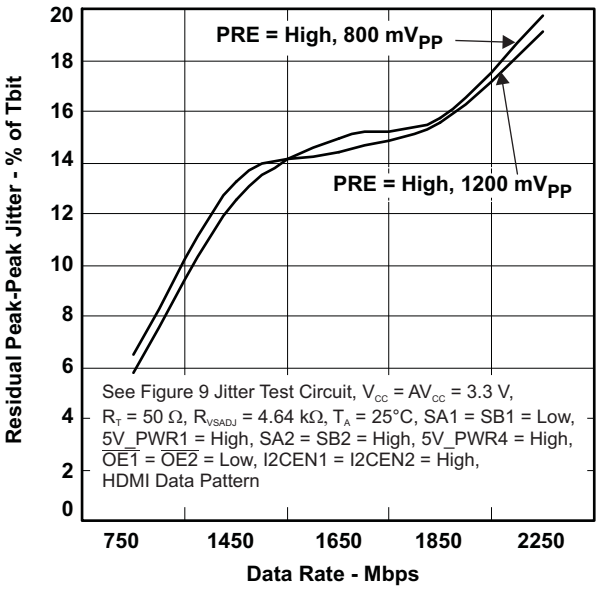


Figure 17.

RESIDUAL PEAK-TO-PEAK JITTER vs DATA RATE (AC Coupled Input: 3m Cable, Output: 0m Cable)

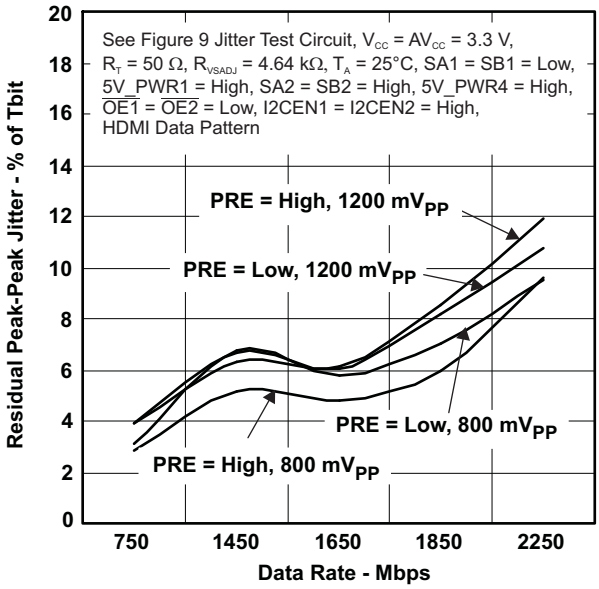


Figure 18.

RESIDUAL PEAK-TO-PEAK JITTER vs 8-MIL FR4 TRACE OUTPUT (DC Coupled Input: 5m Cable)

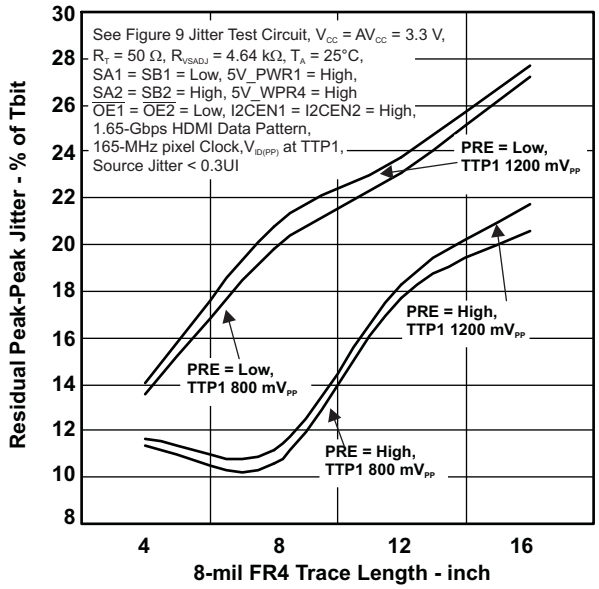


Figure 19.

RESIDUAL PEAK-TO-PEAK JITTER vs PEAK-TO-PEAK DIFFERENTIAL INPUT VOLTAGE (at TTP1, DC Coupled: 5m Cable)

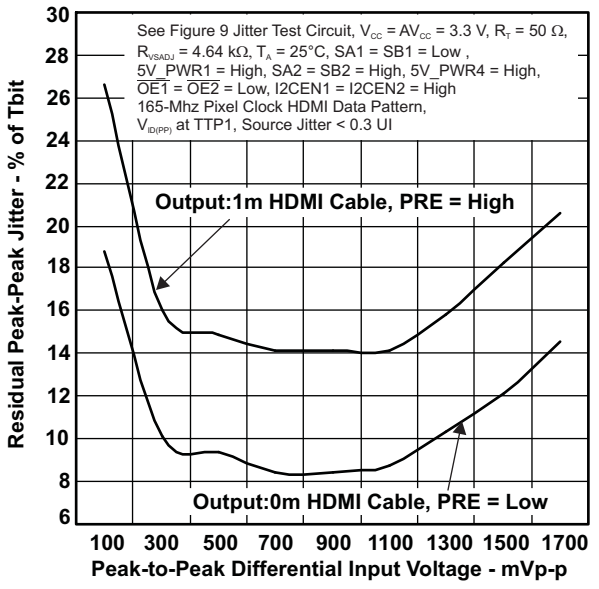


Figure 20.

TYPICAL CHARACTERISTICS (continued)

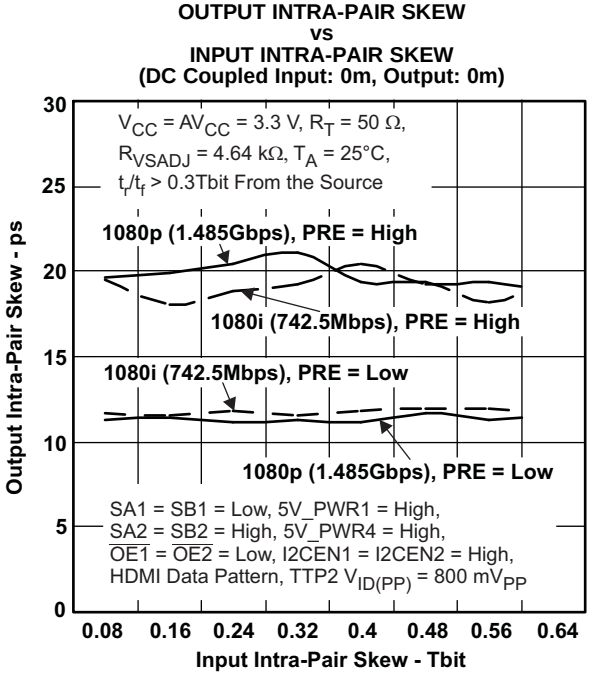


Figure 21.

TYPICAL CHARACTERISTICS (continued)

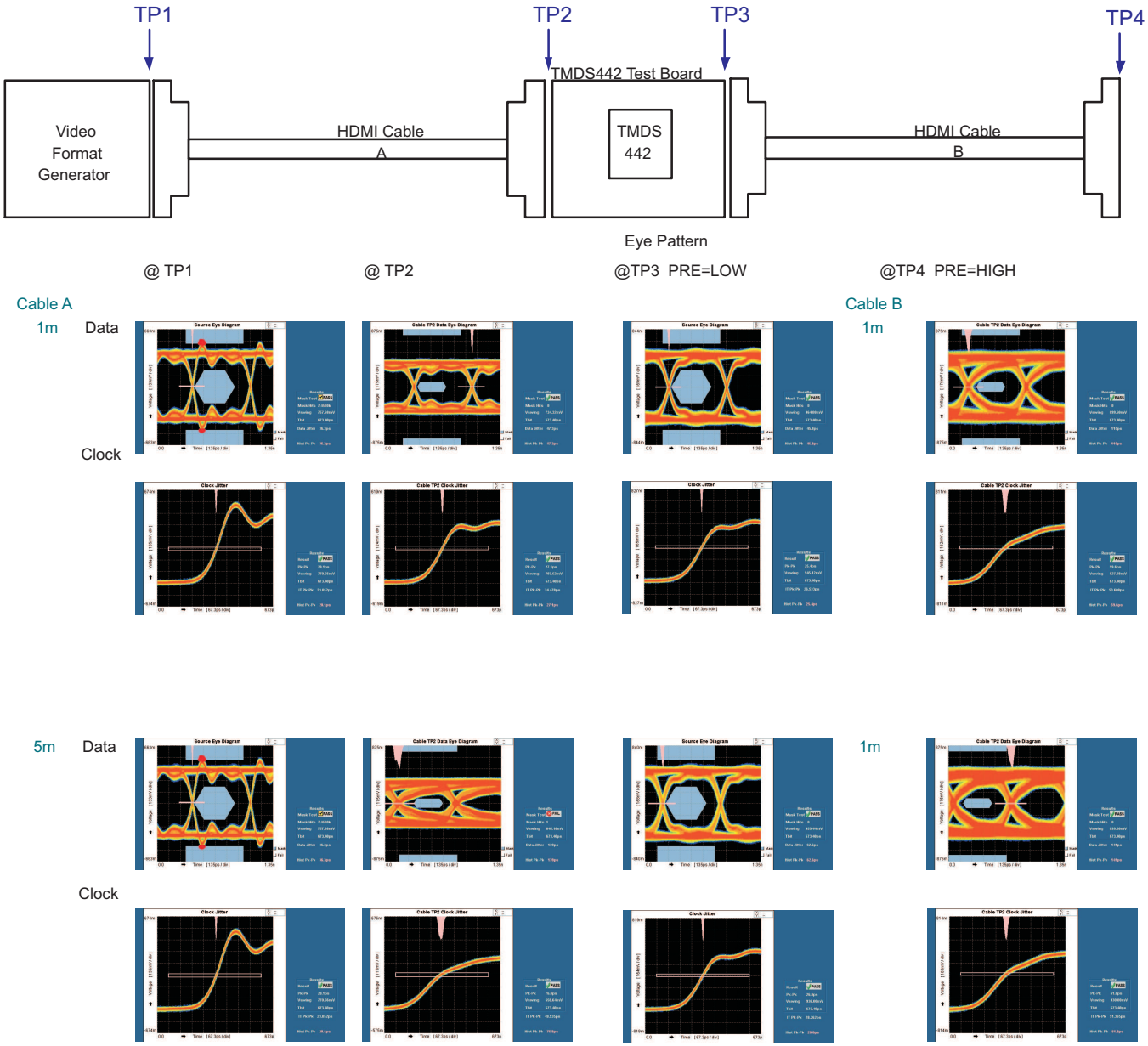


Figure 22. Eye Patterns at 148.5-MHz Pixel Clock

DESCRIPTION

SOURCE SELECTION LOOKUP

CONTROL REGISTER BITS				I/O SELECTED		HOT PLUG DETECT STATUS			
SB	SA	$\overline{OE}$	I2CEN	Y/Z	SCL_SINK SDA_SINK	HPD1	HPD2	HPD3	HPD4
L	L	L	H	A1/B1	SCL1 SDA1	HPD_SINK	L	L	L
L	H	L	H	A2/B2	SCL2 SDA2	L	HPD_SINK	L	L
H	L	L	H	A3/B3	SCL3 SDA3	L	L	HPD_SINK	L
H	H	L	H	A4/B4	SCL4 SDA4	L	L	L	HPD_SINK
X	X	L	L	A/B	Z	HPD_SINK is transmitted to corresponding source port			
X	X	H	H	Z	SCL SDA	HPD_SINK is transmitted to corresponding source port			
X	X	H	L	Z	Z	HPD_SINK is transmitted to corresponding source port			

SINK PRIORITY CONTROL
(SA1 = SA2 = Low, SB1 = SB2 = Low, $\overline{OE1}$ = $\overline{OE2}$ = Low, I2CEN1 = I2CEN2 = High)

SINK PRIORITY	SINK PORT 1		SINK PORT 2		
SP	Y1/Z1	SCL_SINK1/SDA_SINK1	Y2/Z2	SCL_SINK2/SDA_SINK2	HPD1
L	A1/B1	SCL1/SDA1	A1/B1	Z	HPD_SINK1
H	A1/B1	Z	A1/B1	SCL1/SDA1	HPD_SINK2

5V_PWR STATUS
(SA = Low, SB = Low, $\overline{OE}$ = Low, I2CEN = High)

CONTROL STATUS SOURCE PLUG IN STATUS			I/O SELECTED		HOT PLUG DETECT STATUS			
GE	5V_EN	5V_PWR1	Y/Z	SCL_SINK/SDA_SINK	HPD1	HPD2	HPD3	HPD4
L	H	H	A1/B1	SCL1/SDA1	HPD_SINK	L	L	L
L	H	L	Z	Z	L	L	L	L
L	L	X	A1/B1	SCL1/SDA1	HPD_SINK	L	L	L
H	X	H	A1/B1	SCL1/SDA1	HPD_SINK	L	L	L
H	X	L	Z	Z	L	L	L	L

I^2C POINTER REGISTER

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	X	X

01, Sink port 1 configuration register

10, Sink port 2 configuration register

11, Source plug-in status register

Power up default is 0000 0011

SINK PORT 1 CONFIGURATION REGISTER

C7	C6	C5	C4	C3	C2	C1	C0
0	0	0	PRE1	I2CEN1	$\overline{OE1}$	SB1	SA1

Power up default is 0000 1000

SINK PORT 2 CONFIGURATION REGISTER

C7	C6	C5	C4	C3	C2	C1	C0
0	0	0	PRE2	I2CEN2	$\overline{OE2}$	SB2	SA2

Power up default is 0000 1001

SOURCE PLUG-IN STATUS REGISTER

S7	S6	S5	S4	S3	S2	S1	S0
0	0	SP	5V_EN	5V_PWR4	5V_PWR3	5V_PWR2	5V_PWR1

Power up default is 0001 0000

APPLICATION INFORMATION

I²C Interface Notes

The I²C interface is used to access the internal registers of the TMDS442. I²C is a two-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device. The TMDS442 works as a slave and supports the standard mode transfer (100 kbps) and fast mode transfer (400 kbps) as defined in the I²C-Bus Specification. The TMDS442 has been tested to be fully functional with the high-speed mode (3.4 Mbps) but is not ensured at this time.

The basic I²C start and stop access cycles are shown in Figure 23. The basic access cycle consists of the following:

- A start condition
- A slave address cycle
- Any number of data cycles
- A stop condition

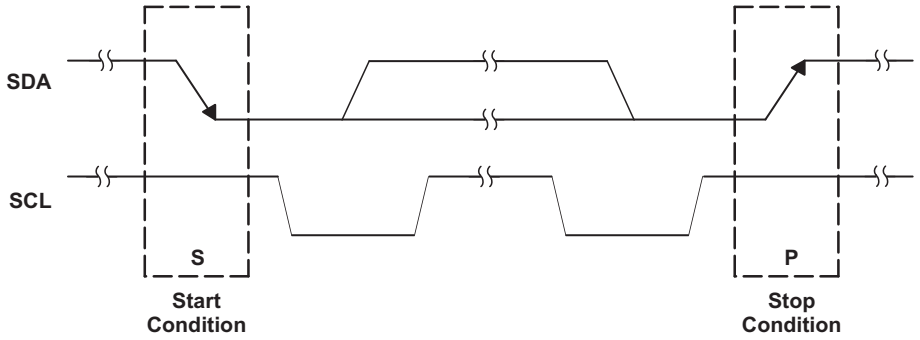


Figure 23. I²C Start and Stop Conditions

General I²C Protocol

- The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 23. All I²C-compatible devices should recognize a start condition.
- The master then generates the SCL pulses and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 23). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 25) by pulling the SDA line low during the entire high period of the ninth SCL cycle. On detecting this acknowledge, the master knows that a communication link with a slave has been established.
- The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary (see Figure 26).
- To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 23). This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

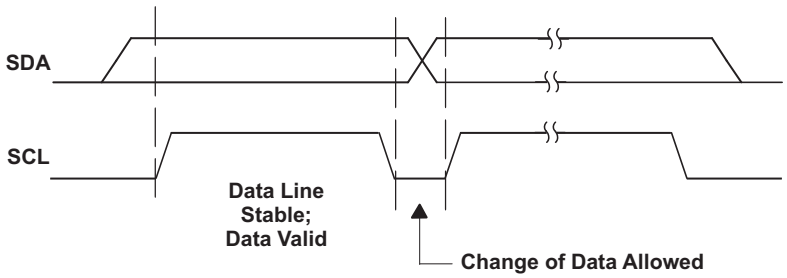


Figure 24. I²C Bit Transfer

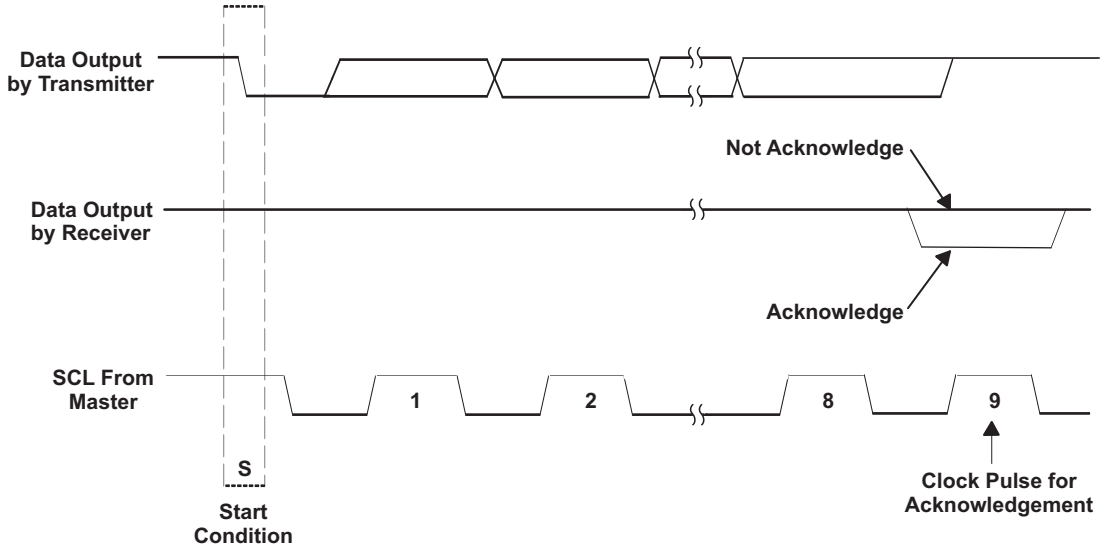


Figure 25. I²C Acknowledge

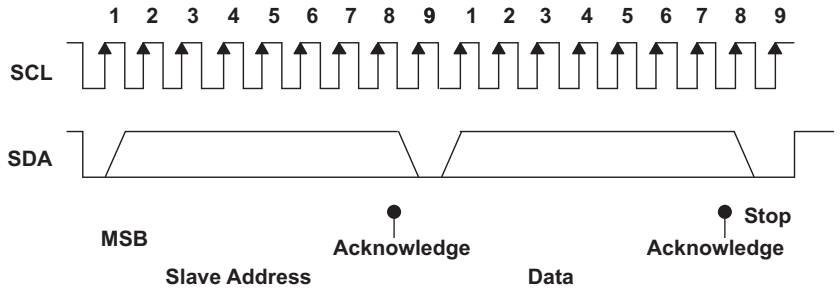


Figure 26. I²C Address and Data Cycles

During a write cycle, the transmitting device must not drive the SDA signal line during the acknowledge cycle so that the receiving device may drive the SDA signal low. After each byte transfer following the address byte, the receiving device will pull the SDA line low for one SCL clock cycle. A stop condition will be initiated by the transmitting device after the last byte is transferred. An example of a write cycle can be found in Figure 27 and Figure 28. Note that the TMDS442 does not allow multiple write transfers to occur. See Example – Writing to the TMDS442 section for more information.

During a read cycle, the slave receiver will acknowledge the initial address byte if it decodes the address as its address. Following this initial acknowledge by the slave, the master device becomes a receiver and

acknowledges data bytes sent by the slave. When the master has received all of the requested data bytes from the slave, the not acknowledge (A) condition is initiated by the master by keeping the SDA signal high just before it asserts the stop (P) condition. This sequence terminates a read cycle as shown in Figure 29 and Figure 30. Note that the TMDS442 does not allow multiple read transfers to occur. See Example – Reading from the TMDS442 section for more information.

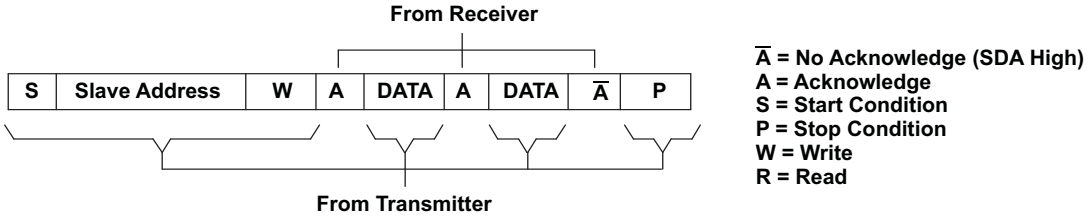


Figure 27. I²C Write Cycle

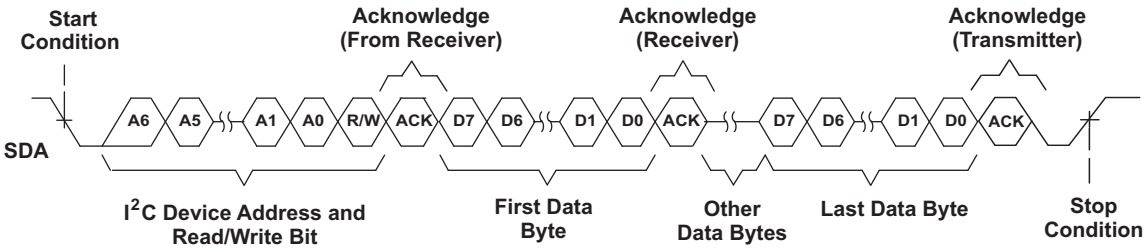


Figure 28. Multiple Byte Write Transfer

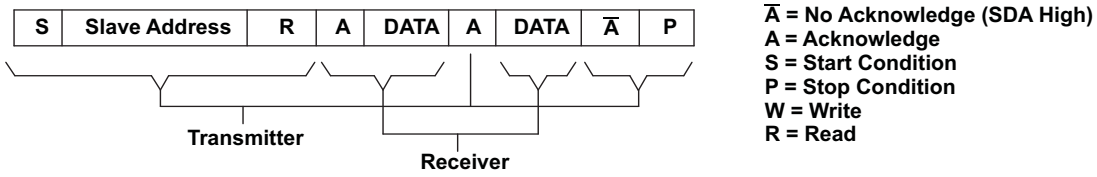


Figure 29. I²C Read Cycle

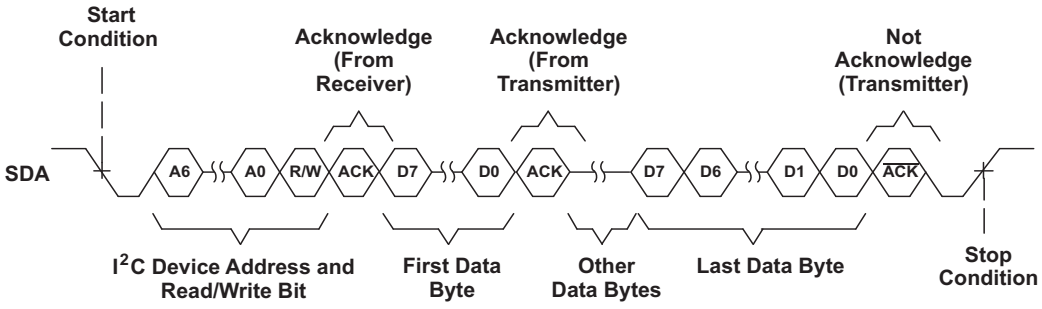


Figure 30. Multiple Byte Read Transfer

Slave Address

Both SDA and SCL must be connected to a positive supply voltage via a pull-up resistor. These resistors should comply with the I²C specification that ranges from 2 kΩ to 19 kΩ. When the bus is free, both lines are high. The address byte is the first byte received following the START condition from the master device. The first 5 Bits (MSBs) of the address are factory preset to 01011. The next two bits of the TMDS442 address are controlled by

the logic levels appearing on the I2C-A1 and I2C-A0 pins. The I2C-A1 and I2C-A0 address inputs can be connected to V_{CC} for logic 1, GND for logic 0, or can be actively driven by TTL/CMOS logic levels. The device addresses are set by the state of these pins and are not latched. Thus a dynamic address control system could be utilized to incorporate several devices on the same system. Up to four TMDS442 devices can be connected to the same I^2C-Bus without requiring additional glue logic. Table 1 lists the possible addresses for the TMDS442.

Table 1. TMDS442 Slave Addresses

FIXED ADDRESSES					SELECTABLE WITH ADDRESS PINS		READ/WRITE BIT
BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2 (A1)	BIT 1 (A0)	BIT 0 (R/W)
0	1	0	1	1	0	0	0
0	1	0	1	1	0	0	1
0	1	0	1	1	0	1	0
0	1	0	1	1	0	1	1
0	1	0	1	1	1	0	0
0	1	0	1	1	1	0	1
0	1	0	1	1	1	1	0
0	1	0	1	1	1	1	1

Sink Port Selection Register and Source Plug-In Status Register Description (Sub-Address)

The TMDS442 operates using only a single byte transfer protocol similar to Figure 27 and Figure 29. The internal sub-address registers and the functionality of each can be found in Table 2. When writing to the device, it is required to send one byte of data to the corresponding internal sub-address. If control of two sink ports and source plug-in status is desired, then the master will have to cycle through the sub-addresses (sink ports) one at a time as illustrated in the Example – Writing to the TMDS442 section for the proper procedure of writing to the TMDS442.

During a read cycle, the TMDS442 sends the data in its selected sub-address in a single transfer to the master device requesting the information. See the Example – Reading from the TMDS442 section of this document for the proper procedure on reading from the TMDS442. Upon power up, the TMDS442 registers are in a default value, 0000 0011.

Table 2. TMDS442 Sink Port and Source Plug-In Status Registers Selection

REGISTER NAME	BIT ADDRESS ($b_7b_6b_5...b_0$)
Sink port 1	0000 0001
Sink port 2	0000 0010
Source plug-in status	0000 0011

Sink Port Register Bit Descriptions

Each bit of the first two sub-addresses, sink port 1 and port 2 control registers, allows the user to individually control the functionality of the TMDS442. The benefit of this process allows the user to control the functionality of each sink port independent of the other sink port. The bit description is decoded in Table 3.

Table 3. TMDS442 Sink Port Register Bit Decoder

BIT	FUNCTION	BIT VALUES	RESULT
7, 6, 5	Reserved	000	Default value
4	PRE	0	3dB De-emphasis off
		1	3dB De-emphasis on
3	I2CEN	0	Sink side I^2C buffer is disabled (Hi-Z)
		1	Sink side I^2C buffer is enabled
2	OE	0	Sink side TMDS on
		1	Sink side TMDS off (Hi-Z)

Table 3. TMDS442 Sink Port Register Bit Decoder (continued)

BIT	FUNCTION	BIT VALUES	RESULT
1, 0	SB SA	00	Source port 1 select
		01	Source port 2 select
		10	Source port 3 select
		11	Source port 4 select

Bits 7 (MSB), 6 and 5 – Reserved bits without function.

Bit 4 – Controls the TMDS output differential voltage.

Bit 3 – Controls the status of DDC interface, SCL_SINK and SDA_SINK.

Bit 2 – Controls the status of TMDS interface, Y/Z.

Bits 1, and 0 (LSB) – Selects the source input of the TMDS442.

The 5-V plug in status can be read through each bit of the sub-address (source plug-in status) status register. Each bit of the third sub-address, source plug-in status registers, allows the user to read the cable plug-in status based on the appearance of a valid +5-V power signal from each source input port. The bit description is decoded in Table 4.

Table 4. TMDS442 Source Plug-In Status Register Bit Decoder

BIT	FUNCTION	BIT VALUES	RESULT
7, 6	Reserved	0 0	Default value
5	SP	0	Sink port1 is the main display when the same source is selected by both sinks
		1	Sink port2 is the main display when the same source is selected by both sinks
4	5V_EN	0	TMDS output status is not controlled by the corresponding +5-V power signal
		1	TMDS output status is controlled by the corresponding +5-V power signal
3	5V_PWR4	0	Source side I^2C buffer is disabled (Hi-Z) When source port 4 is selected by sink, TMDS is Hi-Z
		1	Source side I^2C buffer is enabled When source port 4 is selected by sink, TMDS is under the control of $\overline{OE}$
2	5V_PWR3	0	Source side I^2C buffer is disabled (Hi-Z)
		1	When source port 3 is selected by sink, TMDS is Hi-Z
1	5V_PWR2	0	Source side I^2C buffer is disabled (Hi-Z) When source port 2 is selected by sink, TMDS is Hi-Z
		1	Source side I^2C buffer is enabled When source port 2 is selected by sink, TMDS is under the control of $\overline{OE}$
0	5V_PWR1	0	Source side I^2C buffer is disabled (Hi-Z) When source port 1 is selected by sink, TMDS is Hi-Z
		1	Source side I^2C buffer is enabled When source port 1 is selected by sink, TMDS is under the control of $\overline{OE}$

Example - Writing to the TMDS442

The proper way to write to the TMDS442 is illustrated as follows:

An I^2C master initiates a write operation to the TMDS442 by generating a start condition (S) followed by the TMDS442 I^2C address (as shown below), in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving an acknowledge from the TMDS442, the master presents the sub-address (sink port) it wants to write consisting of one byte of data, MSB first. The TMDS442 acknowledges the byte after completion of the transfer. Finally the master presents the data it wants to write to the register (sink port) and the TMDS442 acknowledges the byte. The I^2C master then terminates the write operation by generating a stop condition (P). Note that the TMDS442 does not support multi-byte transfers. To write to both sink ports – or registers - this procedure must be repeated for each register one series at a time (i.e. repeat steps 1 through 8 for each sink port).

STEP 1	0
I^2C Start (Master)	S

STEP 2	7	6	5	4	3	2	1	0
I^2C General Address (Master)	0	1	0	1	1	X	X	0

Where each X logic state is defined by I2C-A1 and I2C-A0 pins being tied to either Vs+ or GND.

STEP 3	9
I^2C Acknowledge (Slave)	A

STEP 4	7	6	5	4	3	2	1	0
I^2C Write Sink Port Address (Master)	0	0	0	0	0	0	Addr	Addr

Where Addr is determined by the values shown in Table 2.

STEP 5	9
I^2C Acknowledge (Slave)	A

STEP 6	7	6	5	4	3	2	1	0
I^2C Write Data (Master)	Data	Data	Data	Data	Data	Data	Data	Data

Where Data is determined by the values shown in Table 3.

STEP 7	9
I^2C Acknowledge (Slave)	A

STEP 8	0
I^2C Stop (Master)	P

For step 4, an example of the proper bit control for selecting sink port 2 is 0000 0010.
For step 6, an example of the proper bit control for selecting source port B, enabling TMDS outputs and DDC link of the sink port 2 without 3.5dB de-emphasis is 0000 1001.

Example - Reading From the TMDS442

The read operation consists of two phases. The first phase is the address phase. In this phase, an I^2C master initiates a write operation to the TMDS442 by generating a start condition (S) followed by the TMDS442 I^2C address, in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving acknowledges from the TMDS442, the master presents the sub-address (sink port) of the register it wants to read. After the cycle is acknowledged (A), the master terminates the cycle immediately by generating a stop condition (P).

The second phase is the data phase. In this phase, an I^2C master initiates a read operation to the TMDS442 by generating a start condition followed by the TMDS442 I^2C address (as shown below for a read operation), in MSB first bit order, followed by a 1 to indicate a read cycle. After an acknowledge from the TMDS442, the I^2C master receives one byte of data from the TMDS442. After the data byte has been transferred from the TMDS442 to the master, the master generates a NOT-acknowledge followed by a stop. Similar to the write function, to read both sink ports steps 1 through 11 must be repeated for each and every sink port desired.

TMDS Read Phase 1:

STEP 1	0
I^2C Start (Master)	S

STEP 2	7	6	5	4	3	2	1	0
I^2C General Address (Master)	0	1	0	1	1	X	X	0

Where each X logic state is defined by I2C-A1 and I2C-A0 pins being tied to either Vs+ or GND.

STEP 3	**9**
I^2C Acknowledge (Slave)	A

STEP 4	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I^2C Read Sink Port Address (Master)	0	0	0	0	0	0	Addr	Addr

Where Addr is determined by the values shown in Table 2.

STEP 5	**9**
I^2C Acknowledge (Slave)	A

STEP 6	**0**
I^2C Stop (Master)	P

TMDS442 Read Phase 2:

STEP 7	**0**
I^2C Start (Master)	S

STEP 8	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I^2C General Address (Master)	0	1	0	1	1	X	X	1

Where X logic state is defined by I2C-A1 and I2C-A0 pins being tied to either Vs+ or GND.

STEP 9	**9**
I^2C Acknowledge (Slave)	A

STEP 10	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I^2C Read Data (Slave)	Data	Data	Data	Data	Data	Data	Data	Data

Where Data is determined by the logic values contained in the Sink Port Register.

STEP 11	**9**
I^2C Not-Acknowledge (Master)	A

STEP 12	**0**
I^2C Stop (Master)	P

Supply Voltage

All V_{CC} pins can be tied to a single 3.3-V power source. A 0.01-µF capacitor is connected from each V_{CC} pin directly to ground to filter supply noise.

TMDS Inputs

Standard TMDS terminations are integrated on all TMDS inputs. External terminations are not required. Each input channel contains an 8-dB equalization circuit to compensate for cable losses. The voltage at the TMDS input pins must be limited per the absolute maximum ratings. An unused input should not be connected to ground as this would result in excessive current flow damaging the device. TMDS input pins do not incorporate failsafe circuits. An unused input channel can be externally biased to prevent output oscillation. The complementary input pin is recommended to be grounded through a 1-kΩ resistor and the other pin left open.

TMDS Outputs

A 1% precision resister, 4.64-kΩ, connected from VSADJ to ground is recommended to allow the differential output swing to provide TMDS signal levels. The differential output driver provides a typical 10-mA current sink capability, which provides a typical 500-mV voltage drop across a 50-Ω termination resistor. A 10% accuracy resistor is allowed to be connected when the output swing is not strictly required to meet the TMDS signal levels. A 10% resistor provides differential output voltages in the range of 438 mV and 532 mV.

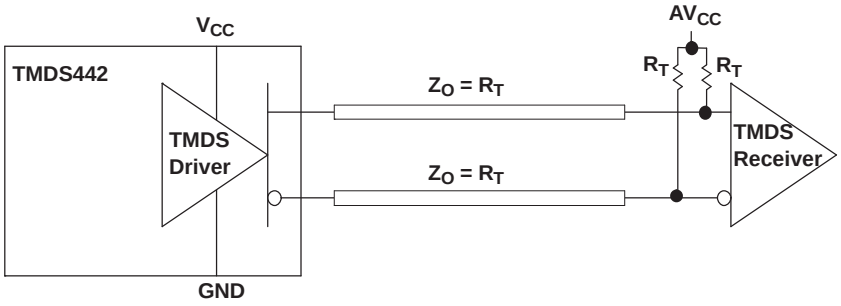


Figure 31. TMDS Driver and Termination Circuit

Referring to Figure 31, if both V_{CC} (TMDS442 supply) and AV_{CC} (sink termination supply) are both powered, the TMDS output signals are high impedance when $\overline{OE}$ = high. Both supplies being active is the normal operating condition.

Again refer to Figure 31, if V_{CC} is on and AV_{CC} is off, the TMDS outputs source a typical 5-mA current through each termination resistor to ground. A total of 10-mW of power is consumed by the terminations independent of the $\overline{OE}$ logical selection. When AV_{CC} is powered on, normal operation ($\overline{OE}$ controls output impedance) is resumed.

When the power source of the device is off and the power source to termination is on, the $I_{O(off)}$, output leakage current, specification ensures the leakage current is limited 10-µA or less.

The PRE pin provides 3dB de-emphasis, allowing output signal pre-conditioning to offset interconnect losses from the TMDS442 outputs to a TMDS receiver. PRE is recommended to be set low while connecting to a receiver throw short PCB route.

HPD Pins

The HPD signals (HPD1, HPD2, HPD3) have an output impedance of 47-Ω typically. In certain applications, a 931-Ω resistor from the HPD output to the connector pin is recommended, to increase the output resistance to 1-KΩ +/- 20%.

DDC Channels

The DDC channels are designed using I^2C drivers with 5-V signal tolerance, allowing direct connection to standard I^2C buses.

Dual-Link 2-to-1 Switch Configurations

TMDS442 can be simply configured to operate as a dual-link DVI/HDMI, 2-to-1 switch, by configuring the device as follows, see Figure 32:

1. Set SA1 = low and SA2 = high
2. Set SB1 = SB2
3. When the 5V_SINK1, HPD_SINK1, SCL_SINK1, and SDA_SINK1 are selected as the control channels from/to the SINK, connect the 5V_PWR1, HPD1, SCL1, and SDA1 to the dual-link source 1, and connect the 5V_PWR3, HPD3, SCL3, and SDA3 to the dual-link source 2.
4. When the 5V_SINK2, HPD_SINK2, SCL_SINK2, and SDA_SINK2 are selected as the control channels from/to the SINK, connect the 5V_PWR2, HPD2, SCL2, and SDA2 to the dual-link source 1, and connect the 5V_PWR4, HPD4, SCL4, and SDA4 to the dual-link source 2.

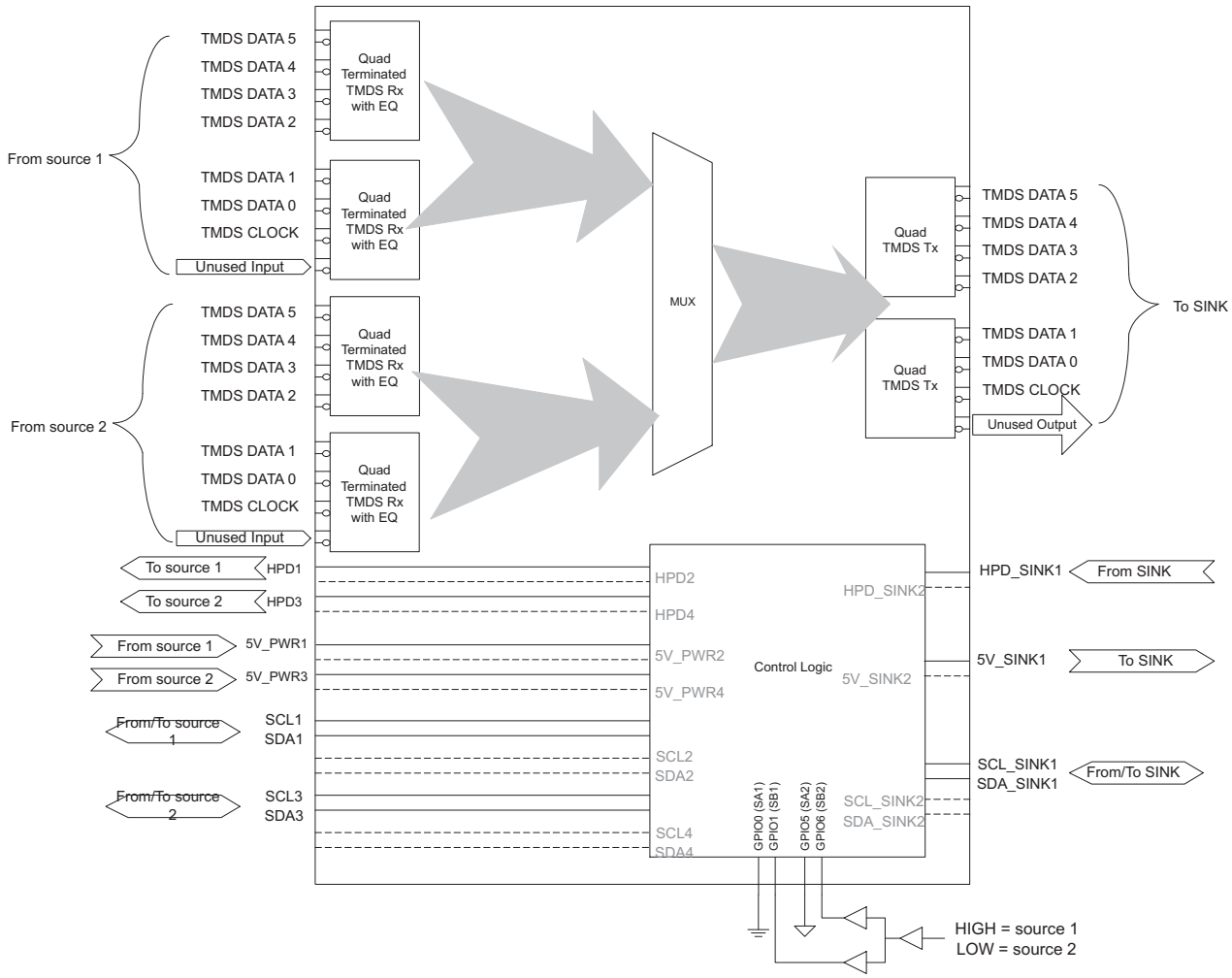


Figure 32. Dual-Link 2-to-1 DVI/HDMI Switch Configuration

In a dual link application, the unused TMDS input should be configured as follows: the complementary input pin is grounded through a 1-kΩ resistor, and the other pin left open.

Layout Considerations

The high-speed TMDS inputs are the most critical paths for the TMDS442. There are several considerations to minimize discontinuities on these transmission lines between the connectors and the device:

- The TMDS differential inputs should be layout in the shortest stubs from connectors directly
- Maintain 100-Ω differential impedance into and out of the TMDS442
- Keep an uninterrupted ground plane beneath the high-speed I/Os
- Keep the ground-path vias to the device as close as possible to allow the shortest return current path

I²C Function Description

The SCL/SDA and SCL_SINK/SDA_SINK pins are 5-V tolerant when the device is powered off and high impedance under low supply voltage, 1.5 V or below. If the device is powered up and the I²C circuits are enabled, and EN = high, the driver T (see Figure 33) is turned on or off depending up on the corresponding R side voltage level.

When the R side is pulled low below 1.5 V, the corresponding T side driver turns on and pulls the T side down to a low level output voltage, V_{OL}. The value of V_{OL} depends on the input to the OVS pin. When OVS is left floating

or not connected, V_{OL} is typically 0.5 V. When OVS is connected to GND, V_{OL} is typically 0.65 V. When OVS is connected to V_{CC}, V_{OL} is typically 0.8 V. V_{OL} is always higher than the driver R input threshold, V_{IL}, which is typically 0.4 V, preventing lockup of the repeater loop. The V_{OL} value can be selected to improve or optimize noise margins between V_{OL} and the V_{IL} of the repeater itself or the V_{IL} of some external device connected on the T side.

When the R side is pulled up, above 1.5 V, the T side driver turns off and the T side pin is high impedance.

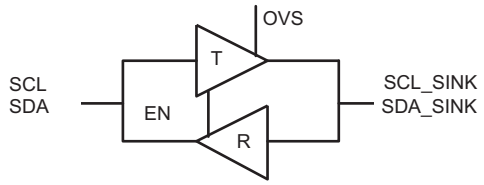


Figure 33. I²C Drivers in TMDS442

When the T side is pulled below 0.4 V by an external I²C driver, both drivers R and T are turned on. Driver R pulls the R side to near 0 V, and driver T is on, but is overridden by the external I²C driver. If driver T is already on, due to a low on the R side, driver R just turns on.

When the T side is released by the external I²C driver, driver T is still on, so the T side is only able to rise to the V_{OL} of driver T. Driver R turns off, since V_{OL} is above its 0.4-V V_{IL} threshold, releasing the R side. If no external I²C driver is keeping the R side low, the R side rises, and driver T turns off once the R side rises above 1.5 V, see Figure 34.

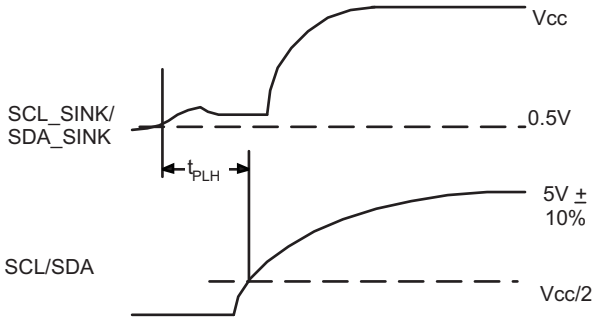


Figure 34. Waveform of Turning Driver T Off

It is important that any external I²C driver on the T side is able to pull the bus below 0.4 V to ensure full operation. If the T side cannot be pulled below 0.4 V, driver R may not recognize and transmit the low value to the R side.

I²C Enable

The I2C drivers are enabled with an internal EN signal. This EN signal is the AND gate result of the 5V_PWR signal from the selected input port and the I2CEN signal for the output. This AND gate is turned on based on an OR gate result of the GE and the 5V_EN settings.

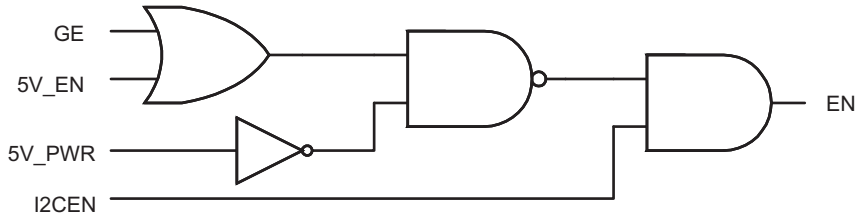


Figure 35. I²C Enable Equivalent Logic

When GE sets high, or GE sets low and 5V_EN sets high, the EN signal is the AND result of the 5V_PWR and the I2CEN. When GE sets low and 5V_EN sets low, the EN signals follows the status of I2CEN. See Table 5.

Table 5. Truth Table for the EN Signal of the I^2C Driver

GE	5V_EN(1)	5V_PWR	I2CEN	EN
1	X	1	1	1
1	X	1	0	0
1	X	0	1	0
1	X	0	0	0
0	1	1	1	1
0	1	1	0	0
0	1	0	1	0
0	1	0	0	0
0	0	1	1	1
0	0	1	0	0
0	0	0	1	1
0	0	0	0	0

(1) X is 1 or 0

The I2CEN pin is active-high with an internal pull-up to V_{CC}. It can be used to isolate a badly behaved slave during powering up. It should never change state during an I^2C operation because disabling during a bus operation may hang the bus and enabling part way through a bus cycle could confuse the I^2C parts being enabled.

I^2C Behavior

The typical application of the TMDS442 is as a repeater in a TV connecting the HDMI input connector and an internal HDMI Rx through flat cables. The I^2C repeater is 5-V tolerant, and no additional circuitry is required to translate between 3.3-V to 5-V bus voltages. In the following example, the system master is running on an R-side I^2C-bus while the slave is connected to a T-side bus. Both buses run at 100 kHz supporting standard-mode I^2C operation. Master devices can be placed on either bus.

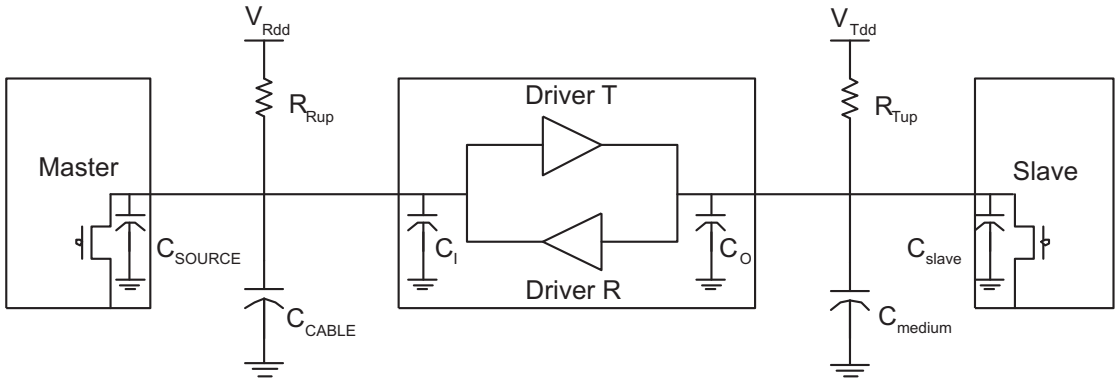


Figure 36. Typical Application

Figure 37 illustrates the waveforms seen on the R-side I^2C-bus when the master writes to the slave through the I^2C repeater circuit of the TMDS442. This looks like a normal I^2C transmission, and the turn on and turn off of the acknowledge signals are slightly delayed.

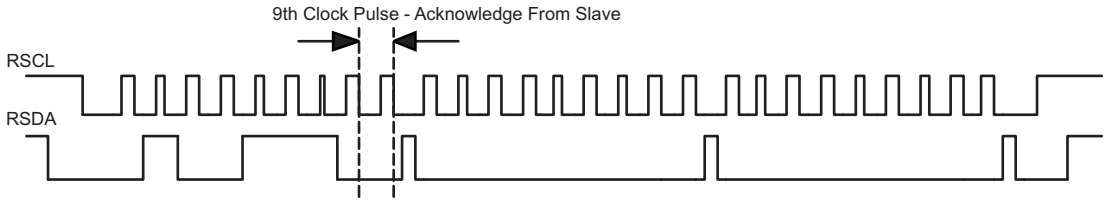


Figure 37. Bus R Waveform

Figure 38 illustrates the waveforms seen on the T-side I²C-bus under the same operation in Figure 37. On the T-side of the I²C repeater, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the driver T. After the 8th clock pulse, the data line is pulled to the V_{OL} of the slave device which is very close to ground in this example. At the end of the acknowledge, the slave device releases and the bus level rises back to the V_{OL} set by the driver until the R-side rises above $V_{CC}/2$, after which it continues to high. It is important to note that any arbitration or clock stretching events require that the low level on the T-side bus at the input of the TMDS442 I²C repeater is below 0.4 V to be recognized by the device and then transmitted to the R-side I²C bus.

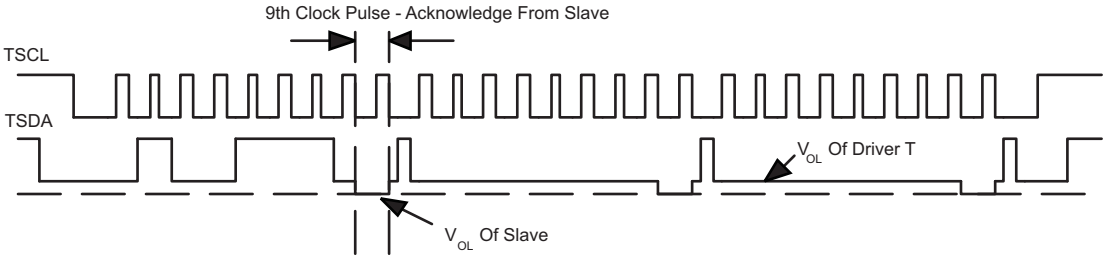


Figure 38. Bus T Waveform

The I²C circuitry inside the TMDS442 allows multiple stage operation as shown in Figure 39. I²C-Bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time of flight considerations for the maximum bus speed requirements.

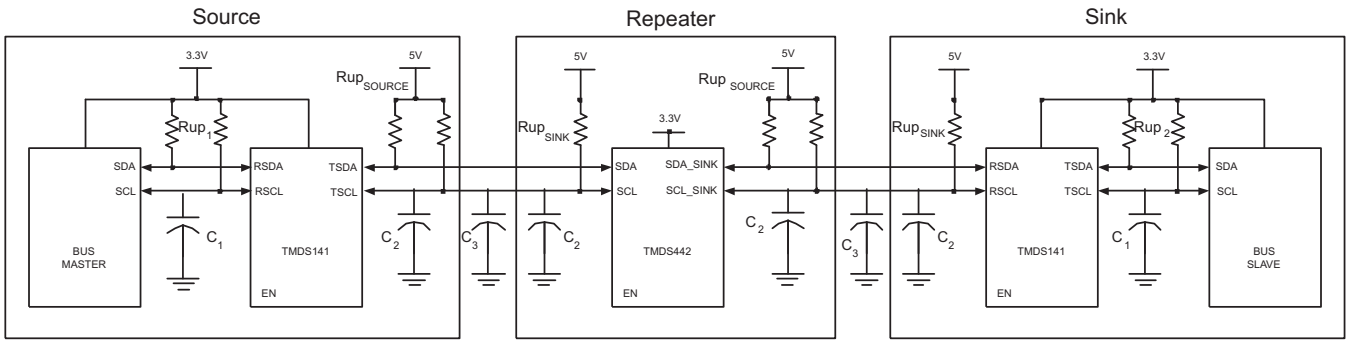


Figure 39. Typical Series Application

I²C Pull-up Resistors

The pull-up resistor value is determined by two requirements:

1. The maximum sink current of the I²C buffer:

   The maximum sink current is 3 mA or slightly higher for an I²C driver supporting standard-mode I²C operation,.

   $$R_{up(min)} = V_{DD}/Isink \quad (1)$$

2. The maximum transition time on the bus:

   The maximum transition time, T, of an I²C bus is set by an RC time constant, where R is the pull-up resistor

value, and C is the total load capacitance. The parameter, k, can be calculated from equation 3 by solving for t, the times at which certain voltage thresholds are reached. Different input threshold combinations introduce different values of t. Table 6 summarizes the possible values of k under different threshold combinations.

$$T = k \times RC \quad (2)$$

$$V(t) = V_{DD}(1 - e^{-t/RC}) \quad (3)$$

Table 6. Value K Upon Different Input Threshold Voltages

V_{th-}\V_{th+}	$0.7V_{DD}$	$0.65V_{DD}$	$0.6V_{DD}$	$0.55V_{DD}$	$0.5V_{DD}$	$0.45V_{DD}$	$0.4V_{DD}$	$0.35V_{DD}$	$0.3V_{DD}$
$0.1V_{DD}$	1.0986	0.9445	0.8109	0.6931	0.5878	0.4925	0.4055	0.3254	0.2513
$0.15V_{DD}$	1.0415	0.8873	0.7538	0.6360	0.5306	0.4353	0.3483	0.2683	0.1942
$0.2V_{DD}$	0.9808	0.8267	0.6931	0.5754	0.4700	0.3747	0.2877	0.2076	0.1335
$0.25V_{DD}$	0.9163	0.7621	0.6286	0.5108	0.4055	0.3102	0.2231	0.1431	0.0690
$0.3V_{DD}$	0.8473	0.6931	0.5596	0.4418	0.3365	0.2412	0.1542	0.0741	-

From equation 1, $R_{up(min)}$ = 5.5V/3mA = 1.83 kΩ to operate the bus under a 5-V pull-up voltage and provide less than 3 mA when the I^2C device is driving the bus to a low state. If a higher sink current, for example 4 mA, is allowed, $R_{up(min)}$ can be as low as 1.375 kΩ.

Given a 5-V I^2C device with input low and high threshold voltages at 0.3 V_{dd} and 0.7 V_{dd}, the valued of k is 0.8473 from Table 6. Taking into account the 1.83-kΩ pull-up resistor, the maximum total load capacitance is $C_{(total-5V)}$ = 645 pF. $C_{cable(max)}$ should be restricted to be less than 545 pF if C_{source} and C_i can be as heavy as 50 pF. Here the C_i is treated as C_{sink}, the load capacitance of a sink device.

Fixing the maximum transition time from Table 6, T = 1 µs, and using the k values from Table 6, the recommended maximum total resistance of the pull-up resistors on an I^2C bus can be calculated for different system setups.

To support the maximum load capacitance specified in the HDMI spec, $C_{cable(max)}$ = 700pF/C_{source} = 50pF/C_i = 50pF, $R_{(max)}$ can be calculated as shown in Table 7.

Table 7. Pull-Up Resistor Upon Different Threshold Voltages and 800-pF Loads

V_{th-}\V_{th+}	$0.7V_{DD}$	$0.65V_{DD}$	$0.6V_{DD}$	$0.55V_{DD}$	$0.5V_{DD}$	$0.45V_{DD}$	$0.4V_{DD}$	$0.35V_{DD}$	$0.3V_{DD}$	UNIT
$0.1V_{DD}$	1.14	1.32	1.54	1.80	2.13	2.54	3.08	3.84	4.97	kΩ
$0.15V_{DD}$	1.20	1.41	1.66	1.97	2.36	2.87	3.59	4.66	6.44	kΩ
$0.2V_{DD}$	1.27	1.51	1.80	2.17	2.66	3.34	4.35	6.02	9.36	kΩ
$0.25V_{DD}$	1.36	1.64	1.99	2.45	3.08	4.03	5.60	8.74	18.12	kΩ
$0.3V_{DD}$	1.48	1.80	2.23	2.83	3.72	5.18	8.11	16.87	-	kΩ

Or, limiting the maximum load capacitance of each cable to be 400 pF to accommodate with I^2C spec version 2.1. $C_{cable(max)}$ = 400pF/C_{source}=50pF/C_i = 50pF, the maximum values of R are calculated as shown in Table 8.

Table 8. Pull-Up Resistor Upon Different Threshold Voltages and 500-pF Loads

V_{th-}\V_{th+}	$0.7V_{DD}$	$0.65V_{DD}$	$0.6V_{DD}$	$0.55V_{DD}$	$0.5V_{DD}$	$0.45V_{DD}$	$0.4V_{DD}$	$0.35V_{DD}$	$0.3V_{DD}$	UNIT
$0.1V_{DD}$	1.82	2.12	2.47	2.89	3.40	4.06	4.93	6.15	7.96	kΩ
$0.15V_{DD}$	1.92	2.25	2.65	3.14	3.77	4.59	5.74	7.46	10.30	kΩ
$0.2V_{DD}$	2.04	2.42	2.89	3.48	4.26	5.34	6.95	9.63	14.98	kΩ
$0.25V_{DD}$	2.18	2.62	3.18	3.92	4.93	6.45	8.96	13.98	28.99	kΩ
$0.3V_{DD}$	2.36	2.89	3.57	4.53	5.94	8.29	12.97	26.99	-	kΩ

Obviously, to accommodate the 3-mA drive current specification, a narrower threshold voltage range is required to support a maximum 800-pF load capacitance for a standard-mode I^2C bus.

When the input low and high level threshold voltages, V_{th-} and V_{th+}, are 0.7 V and 1.9 V, which is 0.15 V_{DD} and 0.4 V_{DD} approximately with V_{DD} = 5 V, from Table 7, the maximum pull-up resistor is 3.59 kΩ. The allowable pull-up resistor is in the range of 1.83 kΩ and 3.59 kΩ.

Thermal Dissipation

High-K board – It is always recommended to solder the PowerPAD™ onto the thermal land. A thermal land is the area of solder-tinned-copper underneath the PowerPAD package. Thermal simulation shows the θJA of the TMDS442 is 23.2°C/W on a high-K board with a 4 x 4 thermal via array, or is 29.4°C/W under the same condition without a via array. The maximum junction temperature is 103°C with via arrays and 112°C without via arrays when the maximum power dissipation from the device is 1.43W. The maximum recommended junction temperature is 125°C, allowing the TMDS442 to operate over the full temperature range (0°C - 70°C) when the PowerPAD is soldered onto the thermal land.

Low-K board – Simulation also shows the θJA of the TMDS442 is 46.9°C/W on a low-K board with the PowerPAD soldered and no thermal vias. To ensure the maximum junction temperature does not exceed 125°C with a worst case power dissipation from the device of 1.43W, the ambient temperature needs to be lower than 58°C, when the device is placed on a low-K board.

A general PCB design guide to PowerPAD package is provided in slma002 - PowerPAD Thermally Enhanced Package.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION 30-August-2006

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TMDS442PNP	ACTIVE	HTQFP	PNP	128	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TMDS442PNPG4	ACTIVE	HTQFP	PNP	128	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

1. The marketing status values are defined as follows:

   ACTIVE: Product device recommended for new designs.

   LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

   NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

   PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

   OBSOLETE: TI has discontinued the production of the device.

2. Eco Plan -The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) -please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

   TBD: The Pb-Free/Green conversion plan has not been defined.

   Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

   Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

   Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

3. MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Revision History

Changes from Original (August 2006) to Revision A **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMDS442PNP	ACTIVE	HTQFP	PNP	128	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	0 to 70	TMDS442	Samples
TMDS442PNPR	ACTIVE	HTQFP	PNP	128	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	0 to 70	TMDS442	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

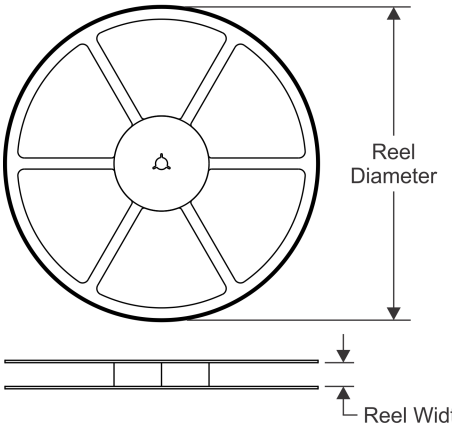
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

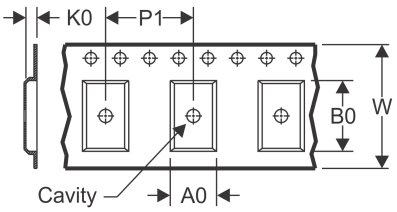
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

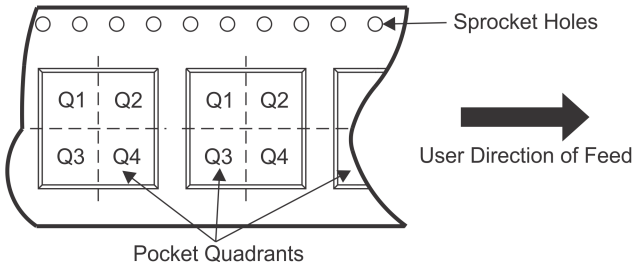


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

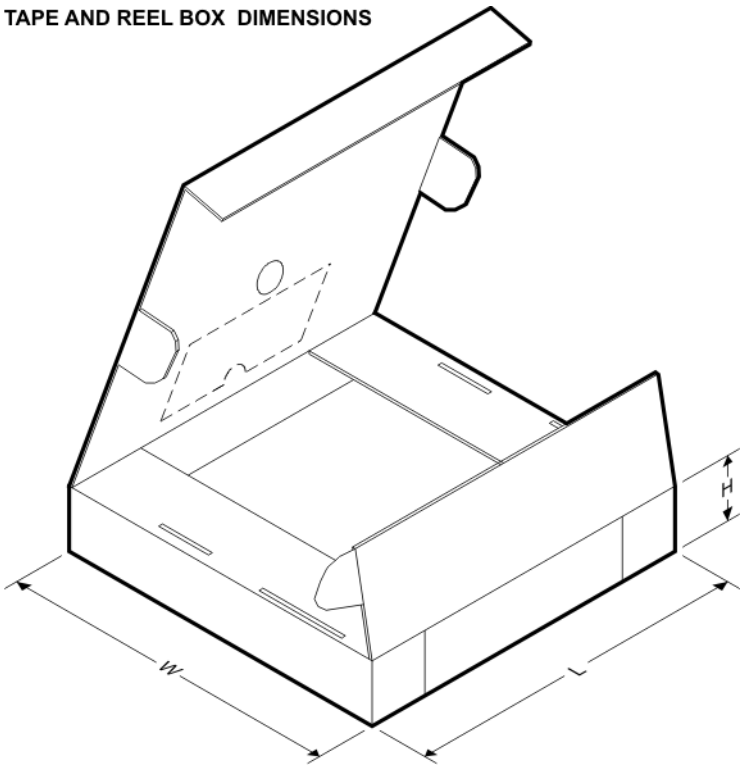
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMDS442PNPR	HTQFP	PNP	128	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

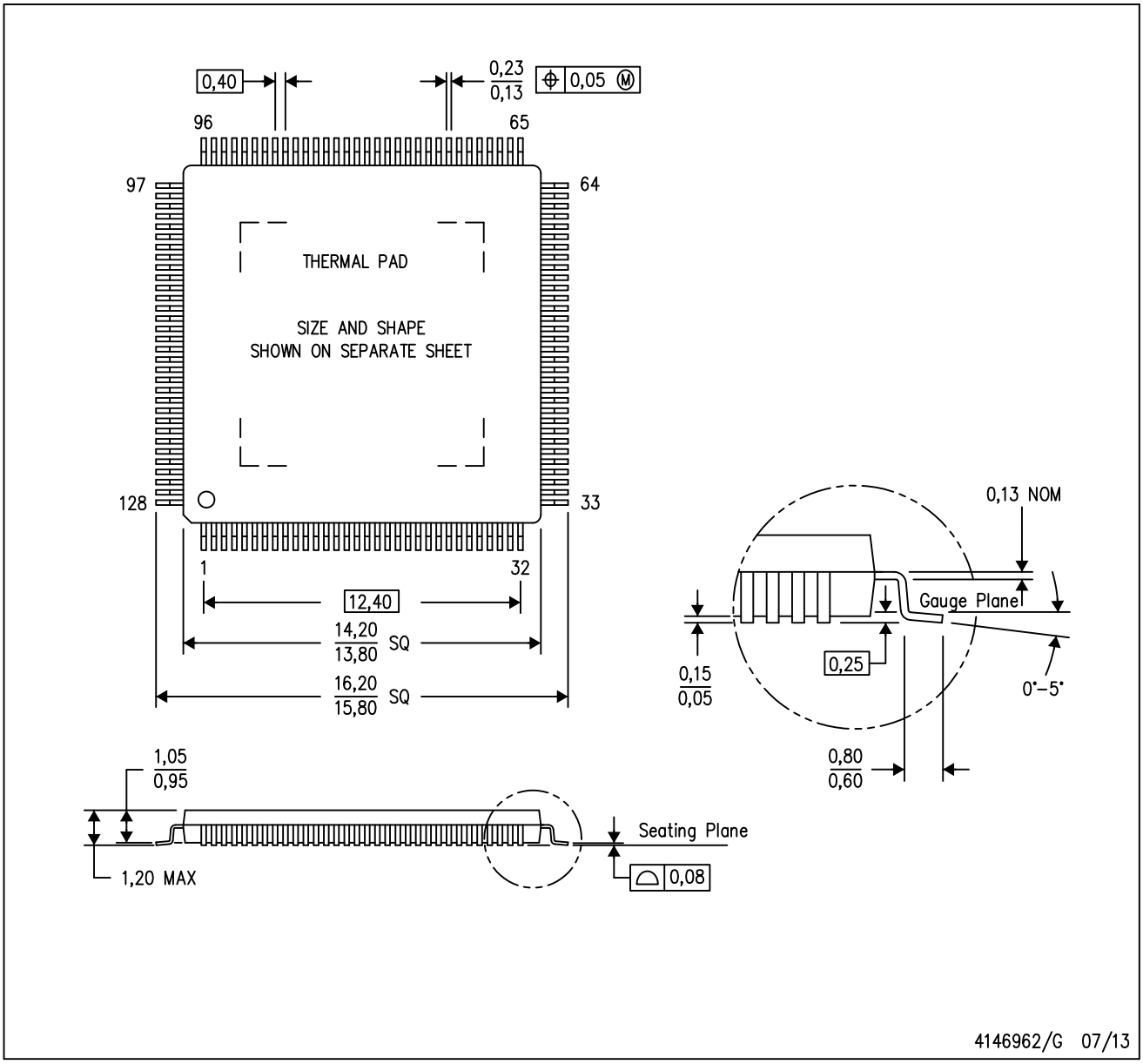
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMDS442PNPR	HTQFP	PNP	128	1000	350.0	350.0	43.0

PNP (S–PQFP–G128) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

PowerPAD is a trademark of Texas Instruments.

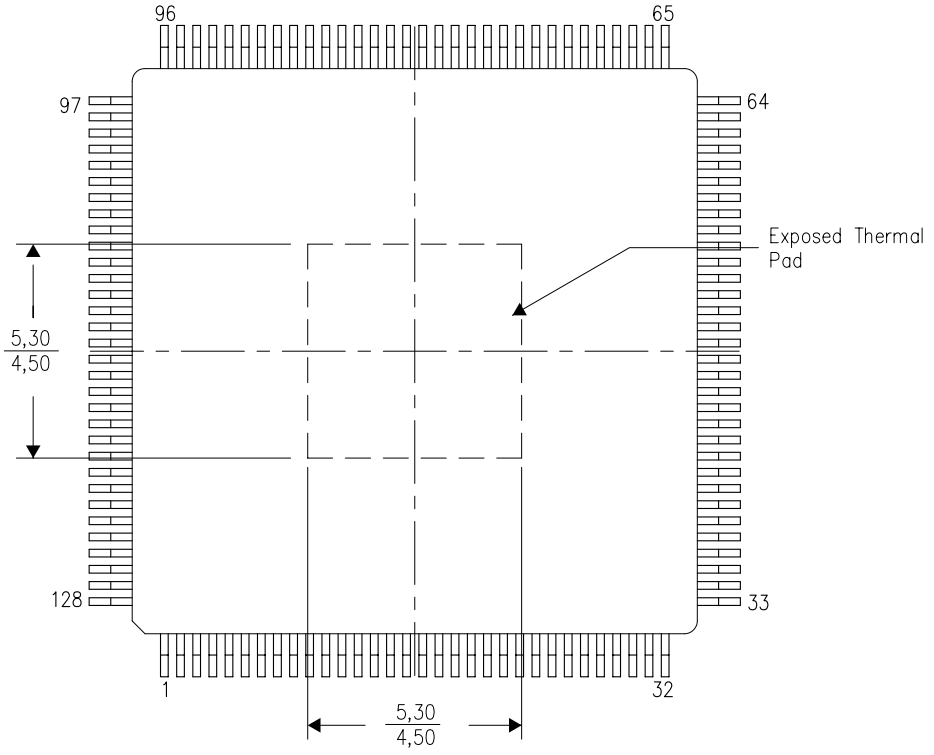
PNP (S–PQFP–G128) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206232–5/L 10/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

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