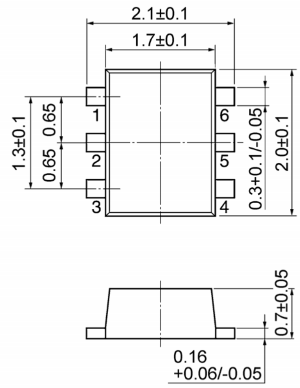
TOSHIBA Field Effect Transistor Silicon P Channel MOS Type (U-MOSⅢ)

SSM6J50TU

○ High Current Switching Applications

Unit: mm



1,2,5,6 : Drain
3 : Gate
4 : Source

UF6

JEDEC	-
JEITA	-
TOSHIBA	2-2T1D

Weight: 7 mg (typ.)

- Compact package suitable for high-density mounting
- Low on-resistance: R_{on} = 205mΩ (max) (@V_{GS} = -2.0 V)
  R_{on} = 100mΩ (max) (@V_{GS} = -2.5 V)
  R_{on} = 64mΩ (max) (@V_{GS} = -4.5 V)

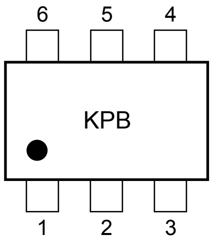
Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DS}	-20	V
Gate-Source voltage		V_{GSS}	±10	V
Drain current	DC	I_D	-2.5	A
	Pulse	I_{DP}	-5	
Drain power dissipation		P_D (Note 1)	500	mW
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

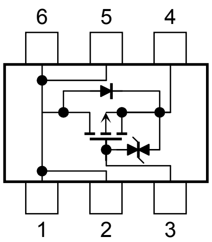
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board.
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 645 mm^2)

Marking



Equivalent Circuit



Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, be sure that the environment is protected against electrostatic discharge. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Start of commercial production
2003-11

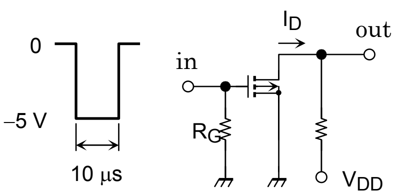
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±8 V, V_{DS} = 0	—	—	±10	μA
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = –10 mA, V_{GS} = 0	-20	—	—	V
		$V_{(BR)\ DSX}$	I_D = –10 mA, V_{GS} = +10 V	-10	—	—	
Drain cut-off current		I_{DSS}	V_{DS} = –20 V, V_{GS} = 0	—	—	–10	μA
Gate threshold voltage		V_{th}	V_{DS} = –10 V, I_D = –0.2 mA	–0.5	—	–1.2	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = –10 V, I_D = –1.5 A (Note2)	3.1	6.2	—	S
Drain-Source on-resistance		$R_{DS\ (ON)}$	I_D = –1.5 A, V_{GS} = –4.5 V (Note2)	—	49	64	mΩ
			I_D = –1.5 A, V_{GS} = –2.5 V (Note2)	—	73	100	
			I_D = –1.5 A, V_{GS} = –2.0 V (Note2)	—	105	205	
Input capacitance		C_{iss}	V_{DS} = –10 V, V_{GS} = 0, f = 1 MHz	—	800	—	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = –10 V, V_{GS} = 0, f = 1 MHz	—	120	—	pF
Output capacitance		C_{oss}	V_{DS} = –10 V, V_{GS} = 0, f = 1 MHz	—	160	—	pF
Switching time	Turn-on time	t_{on}	V_{DD} = –10 V, I_D = –1.5 A,	—	15	—	ns
	Turn-off time	t_{off}	V_{GS} = 0 to –5 V, R_G = 4.7 Ω	—	51	—	

Note2: Pulse test

Switching Time Test Circuit

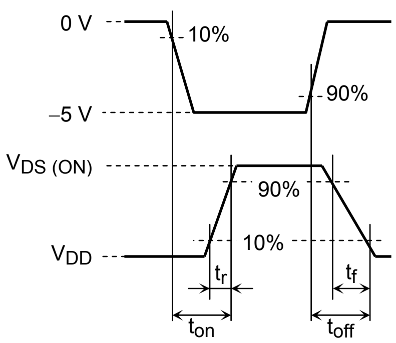
(a) Test Circuit



V_{DD} = -10 V
R_G = 4.7 Ω
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

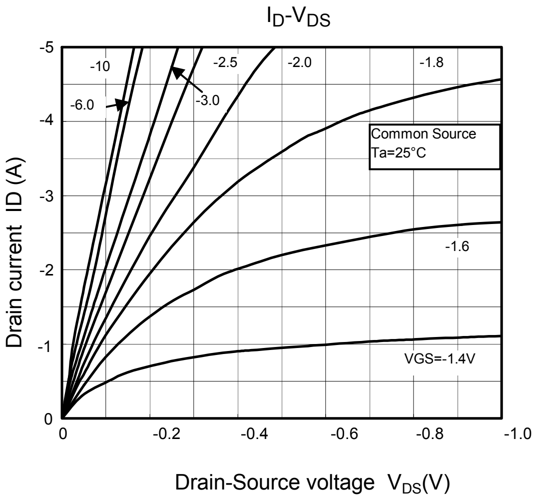
(b) V_{IN}

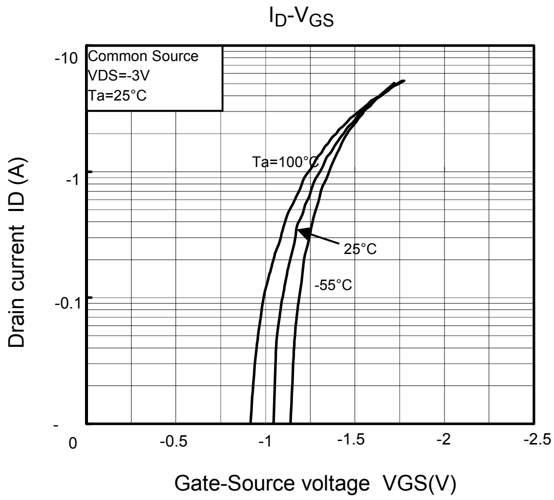
(c) V_{OUT}

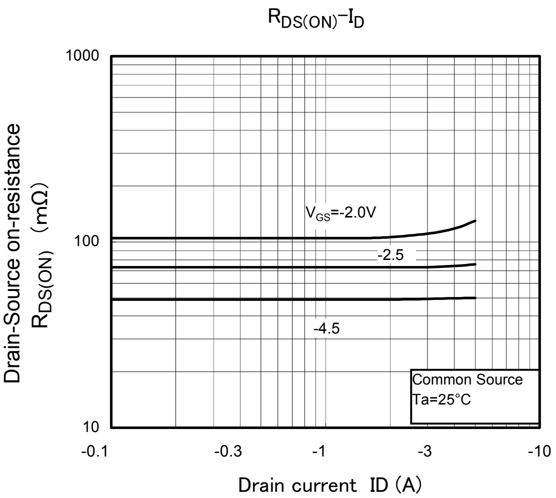


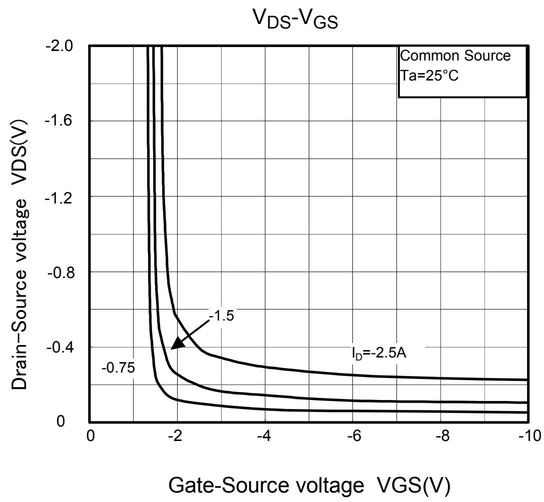
Precaution

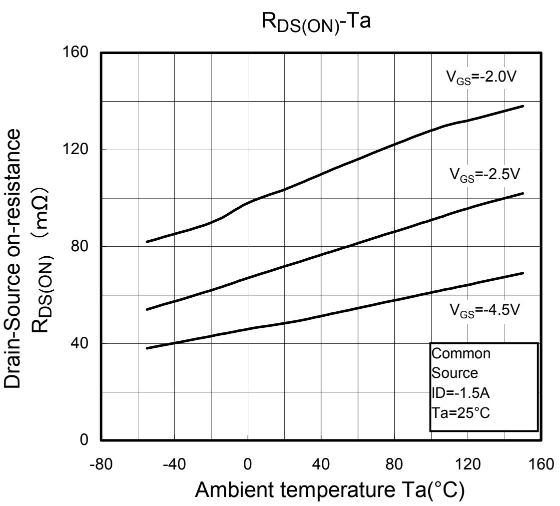
V_{th} can be expressed as the voltage between gate and source when the low operating current value is I_D=-200 μA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than V_{th} and $V_{GS\ (off)}$ requires a lower voltage than V_{th}.
(The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$)
Be sure to take this into consideration when using the device.

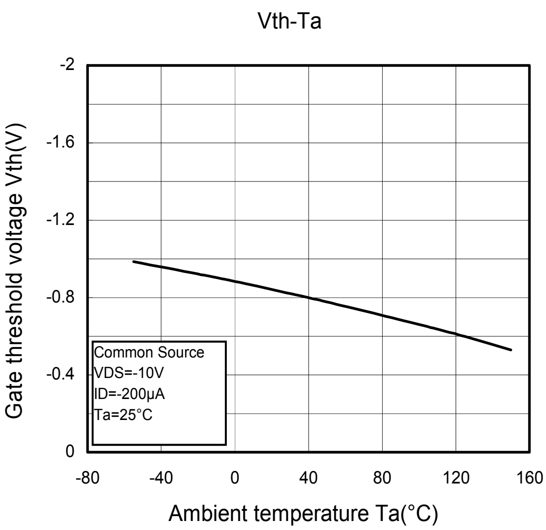

ID-VDS
-10
-6.0
-2.5
-3.0
-2.0
-1.8
Common Source
Ta=25°C
-1.6
VGS=-1.4V
-5
-4
-3
-2
-1
0
0
-0.2
-0.4
-0.6
-0.8
-1.0
Drain current ID (A)
Drain-Source voltage VDS(V)


ID-VGS
Common Source
VDS=-3V
Ta=25°C
Ta=100°C
25°C
-55°C
-10
-1
-0.1
0
-0.5
-1
-1.5
-2
-2.5
Drain current ID (A)
Gate-Source voltage VGS(V)

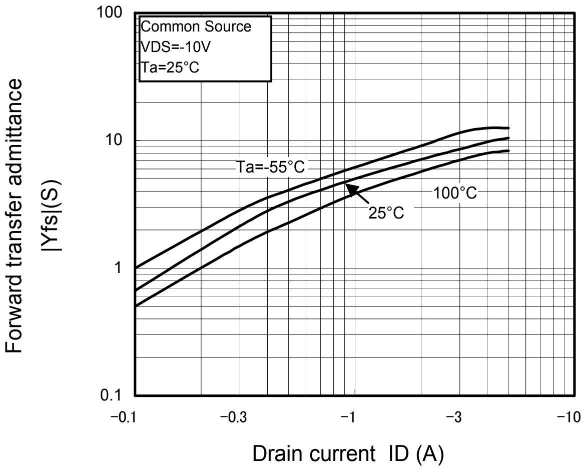

RDS(ON)−ID
VGS=-2.0V
-2.5
-4.5
Common Source
Ta=25°C
1000
100
10
-0.1
-0.3
-1
-3
-10
Drain-Source on-resistance RDS(ON) (mΩ)
Drain current ID (A)


VDS-VGS
Common Source
Ta=25°C
-1.5
ID=-2.5A
-0.75
-2.0
-1.6
-1.2
-0.8
-0.4
0
0
-2
-4
-6
-8
-10
Drain−Source voltage VDS(V)
Gate-Source voltage VGS(V)

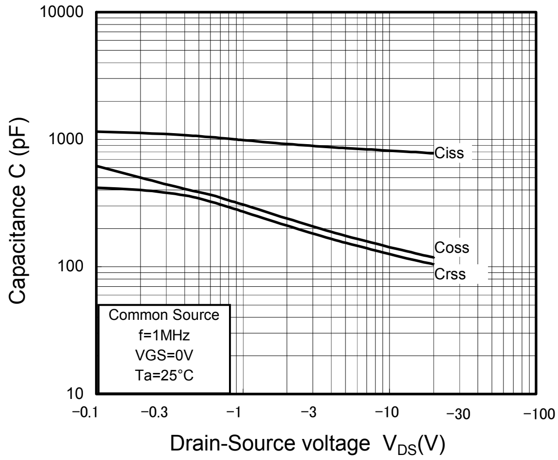

RDS(ON)-Ta
VGS=-2.0V
VGS=-2.5V
VGS=-4.5V
Common Source
ID=-1.5A
Ta=25°C
160
120
80
40
0
-80
-40
0
40
80
120
160
Drain-Source on-resistance RDS(ON) (mΩ)
Ambient temperature Ta(°C)


Vth-Ta
Common Source
VDS=-10V
ID=-200μA
Ta=25°C
-2
-1.6
-1.2
-0.8
-0.4
0
-80
-40
0
40
80
120
160
Gate threshold voltage Vth(V)
Ambient temperature Ta(°C)

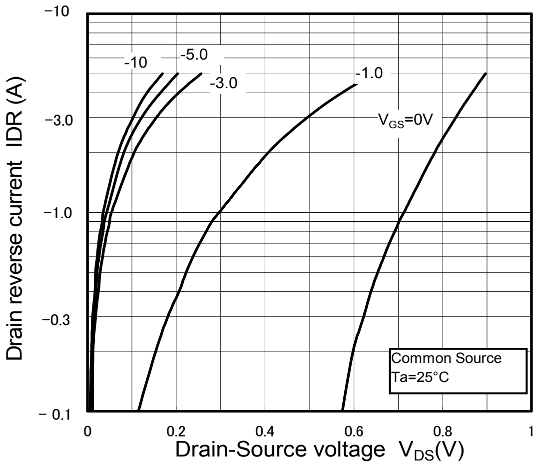
$|Y_{fs}|-I_D$

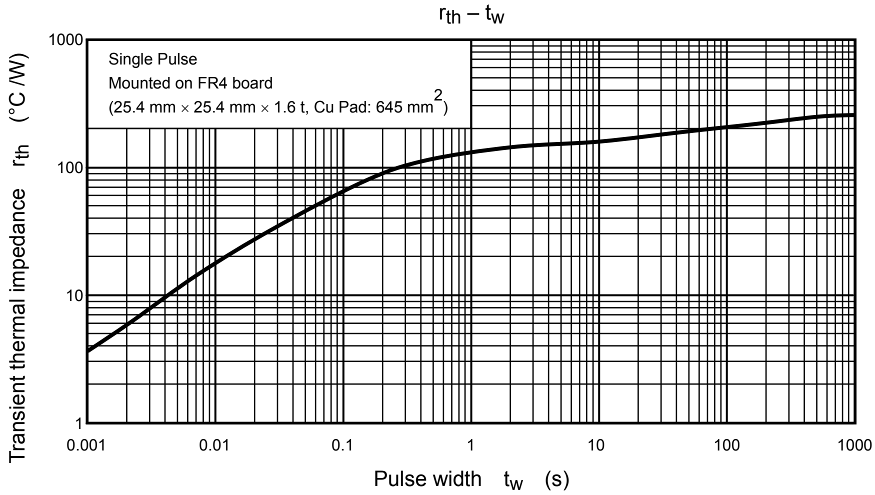


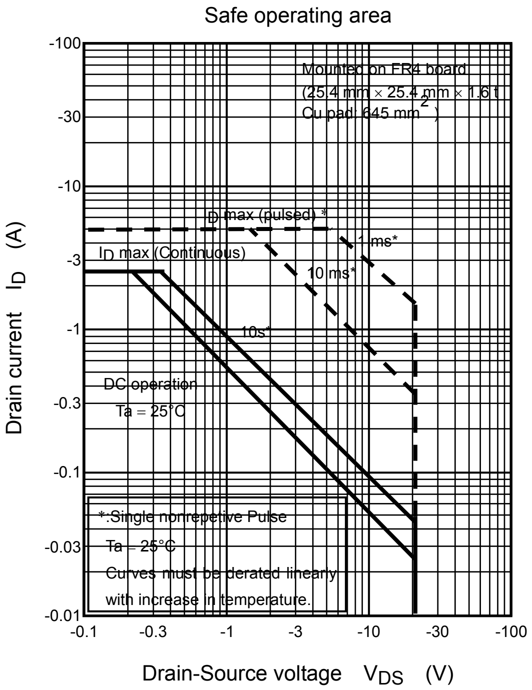
$C-V_{DS}$

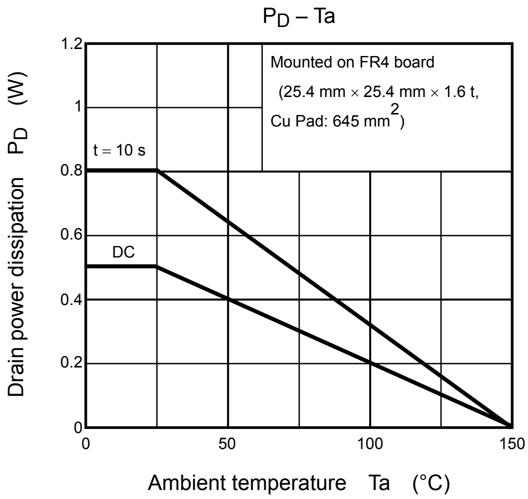


$I_{DR}-V_{DS}$




rth – tw
Single Pulse
Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 645 mm2)
Transient thermal impedance rth (°C /W)
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000
Pulse width tw (s)


Safe operating area
Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 t
Cu pad: 645 mm2)
ID max (pulsed) *
1 ms*
ID max (Continuous)
10 ms*
10s*
DC operation
Ta = 25°C
*:Single nonrepetive Pulse
Ta = 25°C
Curves must be derated linearly
with increase in temperature.
Drain current ID (A)
-100
-30
-10
-3
-1
-0.3
-0.1
-0.03
-0.01
-0.1
-0.3
-1
-3
-10
-30
-100
Drain-Source voltage VDS (V)


PD – Ta
Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 t,
Cu Pad: 645 mm2)
t = 10 s
DC
Drain power dissipation PD (W)
1.2
1
0.8
0.6
0.4
0.2
0
0
50
100
150
Ambient temperature Ta (°C)

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