9-Output 1.5V PCIe Gen1-2-3 Fanout Buffer with Zo=100ohms

9DBU0941

DATASHEET

Description

The 9DBU0941 is a member of IDT's 1.5V Ultra-Low-Power (ULP) PCIe family. It has integrated terminations for direct connection to 100Ω transmission lines. The device has 9 output enables for clock management, and 3 selectable SMBus addresses.

Recommended Application

1.5V PCIe Gen1-2-3 Fanout Buffer (FOB)

Output Features

• 9 1–167MHz Low-Power (LP) HCSL DIF pairs with Zo=100 $\!\Omega$

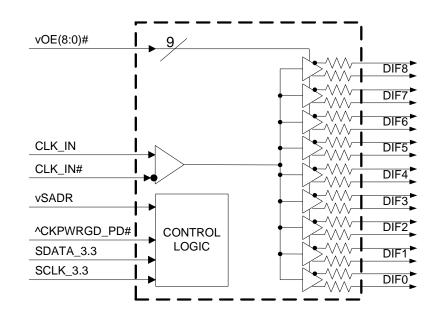
Key Specifications

- DIF additive cycle-to-cycle jitter < 5ps
- DIF output-to-output skew < 60ps
- DIF additive phase jitter is < 300fs rms for PCIe Gen3
- DIF additive phase jitter < 350s rms for SGMII

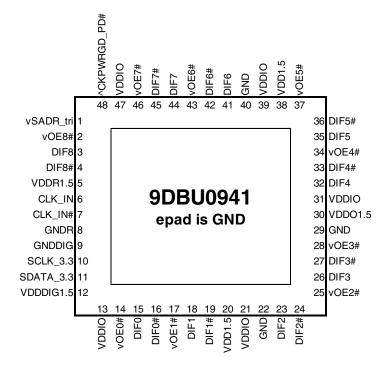
Features/Benefits

- Direct connection to 100Ω transmission lines; save 36 resistors compared to standard HCSL outputs
- 47mW typical power consumption; eliminates thermal concerns
- Outputs can optionally be supplied from any voltage between 1.05 and 1.5V; maximum power savings
- Spread Spectrum (SS) compatible; allows SS for EMI reduction
- OE# pins for each output; support DIF power management
- HCSL-compatible differential input; can be driven by common clock sources
- SMBus-selectable features; optimize signal integrity to application
 - slew rate for each output
 - differential output amplitude
- Device contains default configuration; SMBus interface not required for device operation
- Selectable SMBus addresses; multiple devices can easily share an SMBus segment
- 3.3V tolerant SMBus interface works with legacy controllers
- 6 × 6 mm 48-VFQFPN; minimal board space





Pin Configuration



48-pin VFQFPN, 6x6 mm, 0.4mm pitch

- ^v prefix indicates internal 120KOhm pull up AND pull down resistor (biased to VDD/2)
- v prefix indicates internal 120KOhm pull down resistor
- ^ prefix indicates internal 120KOhm pull up resistor

SMBus Address Selection Table

	SADR	Address	+ Read/Write bit
State of SADR on first application of CKPWRGD_PD#	0	1101011	x
	М	1101100	x
	1	1101101	x

Power Management Table

CKPWRGD PD#	CLK IN	SMBus	OEx# Pin DIFx		x
		OEx bit		True O/P	Comp. O/P
0	Х	Х	Х	Low	Low
1	Running	0	Х	Low	Low
1	Running	1	0	Running	Running
1	Running	1	1	Low	Low

Power Connections

Pin Number			Description
VDD	VDDIO	GND	Description
5		8	Input receiver analog
12		9	Digital power
20,30,31,38	13,21,31,39,47	22,29,40	DIF outputs

Note: EPAD on this device is not electrically connected to the die. It should be connected to ground for best thermal performance.

Pin Descriptions

VSADP_In LATCHED Tri-level latch to select SMBus Address. It has an internal 120kohm pull down resistor. See SMBus Address Selection Table. 2 VOE8# IN Active Iow input for enabling output 8. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs. 3 DIF8 OUT Differential inco clock output. 4 DIF8# OUT Differential inco clock (receiver). This VDD should be treated as an Analog power rail and filterential inco clock (receiver). This VDD should be treated as an Analog power rail and filterential incortock (receiver). 6 CLK, IN IN Complementary input for differential incortock (receiver). 9 GNDDIG GND GND Gound pin for digital circuitry, 3.3V tolerant. 11 SDATA_3.3 IN Clock pin of SMBus circuitry, 3.3V tolerant. 12 VDDDI01.5 PWR N.SV digital power (diffy power) 13 VDDI0 PWR Power supply for differential outputs. 14 vOE0# IN Active low input for differential outputs. 15 DIF0 OUT Differential complementary clock output. 14 vOE0# IN Active low input for orabiling output 1. This p	PIN #	PIN NAME	TYPE	DESCRIPTION
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2 VOE0# IN 1 = disable outputs, 0 = enable outputs. 3 DIF8 OUT Differential ucclock output. 4 DIF8# OUT Differential complementary clock output. 5 VDDR1.5 PVM Nalog power rail and filtered appropriately. 6 CLK_IN IN True input for differential represence clock. 7 CLK IN# IN True input for differential represence clock. 8 GNDR GND Analog ground pin for the differential input (seciever) 9 GNDDG GND Ground pin for digital circuitry. 10 SCLK.3.3 IN Clock pin of SMBus circuitry. 3.3V tolerant. 11 SDDATA.3.3 I/O Data pin for SMBus circuitry. 3.3V tolerant. 12 VDDDIG1.5 PVM Power supply for differential output 0. This pin has an internal 120kohm pull-down. 14 vOE0# IN Active low input for enabling output 0. This pin has an internal 120kohm pull-down. 15 DIF0 OUT Differential complementary clock output. 16 DIF0# OUT Differential true clock output. 17 vOE1# IN Active low input for enabling output 3. 18 DIF1# OUT Differential complementary clock output. <td< td=""><td>I</td><td>VSADR_tri</td><td>IN</td><td>resistor. See SMBus Address Selection Table.</td></td<>	I	VSADR_tri	IN	resistor. See SMBus Address Selection Table.
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28VOE3#IN1 = disable outputs, 0 = enable outputs.29GNDGNDGround pin.30VDD01.5PWRPower supply for outputs, nominally 1.5V.31VDDOPWRPower supply for differential outputs32DIF4OUTDifferential true clock output.33DIF4#OUTDifferential complementary clock output.34vOE4#INActive low input for enabling output 4. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs.35DIF5OUTDifferential true clock output.36DIF5#OUTDifferential complementary clock output.37vOE5#INActive low input for enabling output 5. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs.38VDD1.5PWRPower supply, nominally 1.5V39VDDIOPWRPower supply for differential outputs	27	DIF3#	OUT	Differential complementary clock output.
1 = disable outputs, 0 = enable outputs.29GNDGNDGround pin.30VDD01.5PWRPower supply for outputs, nominally 1.5V.31VDDIOPWRPower supply for differential outputs32DIF4OUTDifferential true clock output.33DIF4#OUTDifferential complementary clock output.34vOE4#INActive low input for enabling output 4. This pin has an internal 120kohm pull-down. 1 = disable outputs.35DIF5OUTDifferential true clock output.36DIF5#OUTDifferential complementary clock output.37vOE5#INActive low input for enabling output 5. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs.38VDD1.5PWRPower supply, nominally 1.5V39VDDIOPWRPower supply for differential outputs	20	VOE2#	INI	Active low input for enabling output 3. This pin has an internal 120kohm pull-down.
30VDDO1.5PWRPower supply for outputs, nominally 1.5V.31VDDIOPWRPower supply for differential outputs32DIF4OUTDifferential true clock output.33DIF4#OUTDifferential complementary clock output.34vOE4#INActive low input for enabling output 4. This pin has an internal 120kohm pull-down.35DIF5OUTDifferential true clock output.36DIF5#OUTDifferential complementary clock output.37vOE5#INActive low input for enabling output 5. This pin has an internal 120kohm pull-down.38VDD1.5PWRPower supply, nominally 1.5V39VDDIOPWRPower supply for differential outputs			IIN	
31VDDIOPWRPower supply for differential outputs32DIF4OUTDifferential true clock output.33DIF4#OUTDifferential complementary clock output.34vOE4#INActive low input for enabling output 4. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs.35DIF5OUTDifferential true clock output.36DIF5#OUTDifferential complementary clock output.37vOE5#INActive low input for enabling output 5. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs.38VDD1.5PWRPower supply, nominally 1.5V39VDDIOPWRPower supply for differential outputs	29	GND	GND	Ground pin.
32DIF4OUTDifferential true clock output.33DIF4#OUTDifferential complementary clock output.34vOE4#INActive low input for enabling output 4. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs.35DIF5OUTDifferential true clock output.36DIF5#OUTDifferential complementary clock output.37vOE5#INActive low input for enabling output 5. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs.38VDD1.5PWRPower supply, nominally 1.5V39VDDIOPWRPower supply for differential outputs	30	VDDO1.5	PWR	Power supply for outputs, nominally 1.5V.
33DIF4#OUTDifferential complementary clock output.34vOE4#INActive low input for enabling output 4. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs.35DIF5OUTDifferential true clock output.36DIF5#OUTDifferential complementary clock output.37vOE5#INActive low input for enabling output 5. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs.38VDD1.5PWRPower supply, nominally 1.5V39VDDIOPWRPower supply for differential outputs	31	VDDIO	PWR	Power supply for differential outputs
34vOE4#INActive low input for enabling output 4. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs.35DIF5OUTDifferential true clock output.36DIF5#OUTDifferential complementary clock output.37vOE5#INActive low input for enabling output 5. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs.38VDD1.5PWRPower supply, nominally 1.5V39VDDIOPWRPower supply for differential outputs	32	DIF4	OUT	Differential true clock output.
34VOE4#IN1 = disable outputs, 0 = enable outputs.35DIF5OUTDifferential true clock output.36DIF5#OUTDifferential complementary clock output.37vOE5#INActive low input for enabling output 5. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs.38VDD1.5PWRPower supply, nominally 1.5V39VDDIOPWRPower supply for differential outputs	33	DIF4#	OUT	Differential complementary clock output.
35 DIF5 OUT Differential true clock outputs. 36 DIF5# OUT Differential complementary clock output. 37 vOE5# IN Active low input for enabling output 5. This pin has an internal 120kohm pull-down. 38 VDD1.5 PWR Power supply, nominally 1.5V 39 VDDIO PWR Power supply for differential outputs	34	vOE4#	IN	
36DIF5#OUTDifferential complementary clock output.37vOE5#INActive low input for enabling output 5. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs.38VDD1.5PWRPower supply, nominally 1.5V39VDDIOPWRPower supply for differential outputs				
37vOE5#INActive low input for enabling output 5. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs.38VDD1.5PWRPower supply, nominally 1.5V39VDDIOPWRPower supply for differential outputs	-			
37 VOES# IN 1 = disable outputs, 0 = enable outputs. 38 VDD1.5 PWR Power supply, nominally 1.5V 39 VDDIO PWR Power supply for differential outputs	36	DIF5#	OUT	
38 VDD1.5 PWR Power supply, nominally 1.5V 39 VDDIO PWR Power supply for differential outputs	37	vOE5#	IN	
39 VDDIO PWR Power supply for differential outputs	38	VDD1.5	PWR	

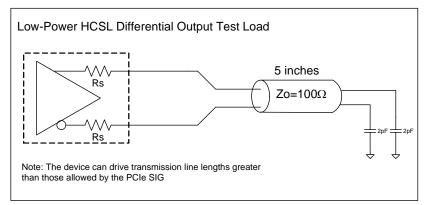
3



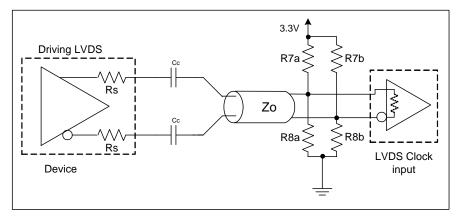
Pin Descriptions (cont.)

PIN #	PIN NAME	TYPE	DESCRIPTION			
41	DIF6	OUT	Differential true clock output.			
42	DIF6# OUT Differential complementary clock output.					
43	vOE6#	IN	Active low input for enabling output 6. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs.			
44	14 DIF7 OUT Differential true clock output.					
45	15 DIF7# OUT Differential complementary clock output.					
46	vOE7#	IN	Active low input for enabling output 7. This pin has an internal 120kohm pull-down. 1 = disable outputs, 0 = enable outputs.			
47	VDDIO	PWR	Power supply for differential outputs			
48	^CKPWRGD_PD#	IN	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal 120kohm pull-up resistor.			
49	EPAD	GND	Connect EPAD to ground.			

Test Loads



Driving LVDS



Driving LVDS inputs

	\ \		
Component	Receiver has	Receiver does not	Note
	termination	have termination	
R7a, R7b	10K ohm	140 ohm	
R8a, R8b	5.6K ohm	75 ohm	
Cc	0.1µF	0.1µF	
Vcm	1.2 volts	1.2 volts	

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9DBU0941. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDx	Applies to VDD, VDDA and VDDIO	-0.5		2	V	1,2
Input Voltage	V _{IN}		-0.5		V _{DD} +0.5	V	1,
Input High Voltage, SMBus	VIHSMB	SMBus clock and data pins			3.3	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

¹ Guaranteed by design and characterization, not 100% tested in production.

² Operation under these conditions is neither implied nor guaranteed.

³ Not to exceed 2.0V.

Electrical Characteristics–Clock Input Parameters

TA = TAMB, Supply voltages per normal operation conditions; see Test Loads for loading conditions

SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
V _{COM}	Common Mode Input Voltage	200		725	mV	1
V _{SWING}	Differential value	300		1450	mV	1
dv/dt	Measured differentially	0.4		8	V/ns	1,2
I _{IN}	$V_{IN} = V_{DD}, V_{IN} = GND$	-5		5	μA	
d _{tin}	Measurement from differential waveform	45	50	55	%	1
J_{DIFIn}	Differential Measurement	0		150	ps	1
	V _{COM} V _{SWING} dv/dt I _{IN} d _{tin}	$\begin{tabular}{ c c c c c } \hline V_{COM} & Common Mode Input Voltage \\ \hline V_{SWING} & Differential value \\ \hline dv/dt & Measured differentially \\ \hline I_{IN} & V_{IN} = V_{DD}, V_{IN} = GND \\ \hline d_{tin} & Measurement from differential waveform \\ \hline \end{tabular}$	$\begin{tabular}{ c c c c c c } \hline V_{COM} & Common Mode Input Voltage & 200 \\ \hline V_{SWING} & Differential value & 300 \\ \hline dv/dt & Measured differentially & 0.4 \\ \hline I_{IN} & V_{IN} = V_{DD}, V_{IN} = GND & -5 \\ \hline d_{tin} & Measurement from differential waveform & 45 \\ \hline \end{tabular}$	$\begin{tabular}{ c c c c c c } \hline V_{COM} & Common Mode Input Voltage & 200 \\ \hline V_{SWING} & Differential value & 300 \\ \hline dv/dt & Measured differentially & 0.4 \\ \hline I_{IN} & V_{IN} = V_{DD}, V_{IN} = GND & -5 \\ \hline d_{tin} & Measurement from differential waveform & 45 & 50 \\ \hline \end{array}$	V_{COM} Common Mode Input Voltage200725 V_{SWING} Differential value3001450 dv/dt Measured differentially0.48 I_{IN} $V_{IN} = V_{DD}$, $V_{IN} = GND$ -55 d_{tin} Measurement from differential waveform455055	$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$

¹ Guaranteed by design and characterization, not 100% tested in production.

² Slew rate measured through +/-75mV window centered around differential zero.

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

TA = TAMB, Supply voltages per normal operation conditions; see Test Loads for loading conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDx	Supply voltage for core and analog	1.425	1.5	1.575	V	
Output Supply Voltage	VDDIO	Low voltage supply LP-HCSL outputs	0.95	1.05-1.5	1.575	V	
Ambient Operating	T _{AMB}	Commercial range	0	25	70	°C	1
Temperature	' AMB	Industrial range	-40	25	85	°C	1
Input High Voltage	VIH	Single-ended inputs, except SMBus	$0.75 V_{DD}$		$V_{DD} + 0.3$	V	
Input Mid Voltage	V _{IM}	Single-ended tri-level inputs ('_tri' suffix)	$0.4 V_{DD}$		$0.6 V_{DD}$	V	
Input Low Voltage	V _{IL}	Single-ended inputs, except SMBus	-0.3		$0.25 V_{DD}$	V	
	I _{IN}	Single-ended inputs, $V_{IN} = GND$, $V_{IN} = VDD$	-5		5	μA	
Input Current	I _{INP}	Single-ended inputs $V_{IN} = 0 \text{ V}$; Inputs with internal pull-up resistors $V_{IN} = \text{VDD}$; Inputs with internal pull-down resistors	-200		200	μA	
Input Frequency	F _{in}		1		167	MHz	2
Pin Inductance	L _{pin}				7	nH	1
	C _{IN}	Logic inputs, except DIF_IN	1.5		5	pF	1
Capacitance	CINDIF_IN	DIF_IN differential clock inputs	1.5		2.7	pF	1,5
	C _{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T _{STAB}	From V _{DD} power-up and after input clock stabilization or de-assertion of PD# to 1st clock			1	ms	1,2
Input SS Modulation Frequency PCIe	f _{MODINPCIe}	Allowable Frequency for PCIe Applications (Triangular modulation)	30		33	kHz	
Input SS Modulation Frequency non-PCIe	f _{MODIN}	Allowable Frequency for non-PCIe Applications (Triangular Modulation)	0		66	kHz	
OE# Latency	t _{LATOE#}	DIF start after OE# assertion DIF stop after OE# deassertion	1		3	clocks	1,3
Tdrive_PD#	t _{DRVPD}	DIF output enable after PD# de-assertion			300	μs	1,3
Tfall	t _F	Fall time of single-ended control inputs			5	ns	2
Trise	t _R	Rise time of single-ended control inputs			5	ns	2
SMBus Input Low Voltage	VILSMB				0.6	V	
SMBus Input High Voltage	VIHSMB	$V_{DDSMB} = 3.3V$, see note 4 for $V_{DDSMB} < 3.3V$	2.1		3.3	V	4
SMBus Output Low Voltage	V _{OLSMB}	at I _{PULLUP}			0.4	V	
SMBus Sink Current	I _{PULLUP}	at V _{OL}	4			mA	
Nominal Bus Voltage	V _{DDSMB}	Bus Voltage	1.425		3.3	V	
SCLK/SDATA Rise Time	t _{RSMB}	(Max VIL - 0.15V) to (Min VIH + 0.15V)			1000	ns	1
SCLK/SDATA Fall Time	t _{FSMB}	(Min VIH + 0.15V) to (Max VIL - 0.15V)			300	ns	1
SMBus Operating Frequency	f _{MAXSMB}	Maximum SMBus operating frequency			400	kHz	6

¹ Guaranteed by design and characterization, not 100% tested in production.

 $^{\rm 2}$ Control input must be monotonic from 20% to 80% of input swing.

³ Time from deassertion until outputs are > 200 mV.

 4 For V_{DDSMB} < 3.3V, V_{IHSMB} > = $~0.8 x V_{DDSMB.}$

⁵ DIF_IN input.

⁶ The differential input clock must be running for the SMBus to be active.

Electrical Characteristics–DIF Low-Power HCSL Outputs

$TA = T_{AMB}$	Supply volta	ages per norma	l operation	conditions; see	Test Loads	for loading conditions
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AND, CAPPER STORAGE							
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew Rate	dV/dt	Scope averaging on, fast setting	1	2.4	3.5	V/ns	1,2,3
Siew Hale	dV/dt	Scope averaging on, slow setting	0.7	1.7	2.5	V/ns	1,2,3
Slew Rate Matching	∆dV/dt	Slew rate matching, scope averaging on		9	20	%	1,2,4
Voltage High	V _{HIGH}	Statistical measurement on single-ended signal using oscilloscope math function. (Scope	630	750	850	mV	7
Voltage Low	V _{LOW}	averaging on)		26	150		7
Max Voltage	Vmax	Measurement on single ended signal using		763	1150	mV	7
Min Voltage	Vmin	absolute value. (Scope averaging off)	-300	22			7
Vswing	Vswing	Scope averaging off	300	1448		mV	1,2
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250	390	550	mV	1,5
Crossing Voltage (var)	∆-Vcross	Scope averaging off		11	140	mV	1,6

¹Guaranteed by design and characterization, not 100% tested in production.

² Measured from differential waveform

³ Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ -Vcross to be smaller than Vcross absolute.

⁷ At default SMBus settings.

Electrical Characteristics–Current Consumption

 $TA = T_{AMB}$; Supply voltages per normal operation conditions; see Test Loads for loading conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	I _{DDA}	VDDO1.5+VDDR, at 100MHz		2.3	3	mA	
	I _{DDx}	VDDx, All outputs active at 100MHz		4.5	6	mA	
	I _{DDIO}	VDDIO, All outputs active at 100MHz		33	40	mA	
Powerdown Current	I _{DDAPD}	VDDO1.5+VDDR, CKPWRGD_PD# = 0		0.4	1	mA	2
	I _{DDxPD}	VDDx, CKPWRGD_PD $\#$ = 0		0.2	0.6	mA	2
	IDDIOPD	VDDIO, CKPWRGD_PD# = 0		0.001	0.1	mA	2

¹ Guaranteed by design and characterization, not 100% tested in production.

² Input clock stopped.

Electrical Characteristics–Output Duty Cycle, Jitter, Skew and PLL Characteristics

TA = T_{AMB}, Supply voltages per normal operation conditions; see Test Loads for loading conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Duty Cycle Distortion	t _{DCD}	Measured differentially, at 100MHz	-1	-0.2	0.5	%	1,3
Skew, Input to Output	t _{pdBYP}	V _T = 50%	2400	2862	3700	ps	1
Skew, Output to Output	t _{sk3}	V _T = 50%		30	60	ps	1,4
Jitter, Cycle to Cycle	t _{jcyc-cyc}	Additive Jitter		0.1	5	ps	1,2

¹ Guaranteed by design and characterization, not 100% tested in production.

² Measured from differential waveform.

³ Duty cycle distortion is the difference in duty cycle between the output and the input clock.

⁴ All outputs at default slew rate.

Electrical Characteristics–Phase Jitter Parameters

 $TA = T_{AMB}$, Supply voltages per normal operation conditions; see Test Loads for loading conditions

						INDUSTRY		
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	LIMIT	UNITS	Notes
	t _{jphPCleG1}	PCIe Gen 1		0.1	5	N/A	ps (p-p)	1,2,3,5
		PCIe Gen 2 Lo Band		0.1	0.4	N/A	ps (rma)	1,2,3,4,
	t _{jphPCleG2}	10kHz < f < 1.5MHz PCIe Gen 2 High Band					(rms)	5
		1.5MHz < f < Nyquist (50MHz)		0.1	0.7	N/A	ps (rms)	1,2,3,4
Additive Phase Jitter	t _{jphPCleG3}	PCIe Gen 3 (2-4MHz or 2-5MHz, CDR = 10MHz)		0.1	0.3	N/A	ps (rms)	1,2,3,4
	t _{jphSGMIIM0}	125MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz		200	250	N/A	fs (rms)	1,6
	t _{jphSGMIIM1}	125MHz, 12kHz to 20MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz		313	350	N/A	fs (rms)	1,6

¹Guaranteed by design and characterization, not 100% tested in production.

² See http://www.pcisig.com for complete specs.

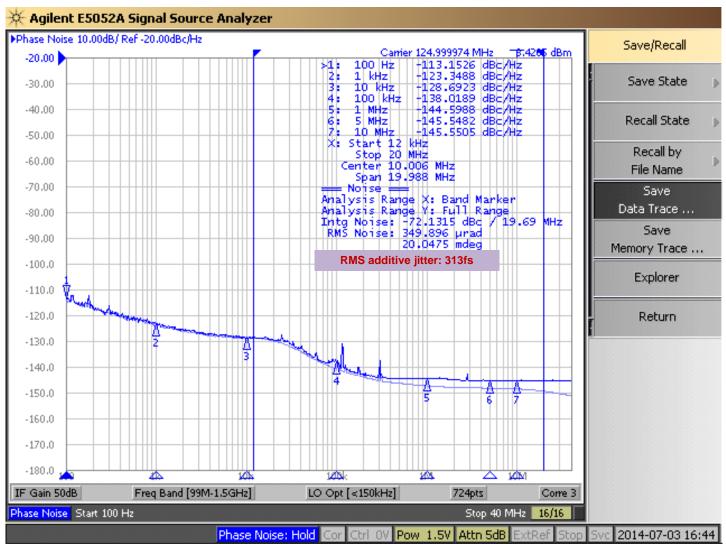
³ Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

⁴ For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = SQRT[(total jitter)² - (input jitter)²].

⁵ Driven by 9FGV0831 or equivalent.

⁶ Rohde & Schwarz SMA100.

Additive Phase Jitter Plot: 125M (12kHz to 20MHz)



General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will acknowledge
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will acknowledge each byte one at a time
- Controller (host) sends a stop bit

	Index Bl	ock \	Write Operation
Controll	er (Host)		IDT (Slave/Receiver)
Т	starT bit		
Slave A	Address		
WR	WRite		
			ACK
Beginning	g Byte = N		
			ACK
Data Byte	Count = X		
			ACK
Beginnin	g Byte N		
			ACK
0		\times	
0		X Byte	0
0		Ö	0
			0
Byte N	+ X - 1		
			ACK
Р	stoP bit		

Note: SMBus Address is Latched on SADR pin.

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will acknowledge
- Controller (host) sends the beginning byte location = N
- IDT clock will acknowledge
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will acknowledge
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends Byte 0 through Byte X (if X_(H) was written to Byte 8)
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

	Index Block F	lead O	peration
Cor	ntroller (Host)		IDT (Slave/Receiver)
Т	starT bit		
SI	ave Address	-	
WR	WRite	-	
		-	ACK
Begi	nning Byte = N	-	
			ACK
RT	Repeat starT	-	
SI	ave Address		
RD	ReaD		
			ACK
			Data Byte Count=X
	ACK		
			Beginning Byte N
	ACK		
		e	0
	0	X Byte	0
	0	×	0
	0		
			Byte N + X - 1
N	Not acknowledge		
Р	stoP bit		

SMBus Table: Output Enable Register¹

Byte 0	Name	Control Function	Туре	0	1	Default
Bit 7	DIF OE7	Output Enable	RW	Low/Low	Enabled	1
Bit 6	DIF OE6	Output Enable	RW	Low/Low	Enabled	1
Bit 5	DIF OE5	Output Enable	RW	Low/Low	Enabled	1
Bit 4	DIF OE4	Output Enable	RW	Low/Low	Enabled	1
Bit 3	DIF OE3	Output Enable	RW	Low/Low	Enabled	1
Bit 2	DIF OE2	Output Enable	RW	Low/Low	Enabled	1
Bit 1	DIF OE1	Output Enable	RW	Low/Low	Enabled	1
Bit 0	DIF OE0	Output Enable	RW	Low/Low	Enabled	1

1. A low on these bits will override the OE# pin and force the differential output Low/Low

SMBus Table: Output Enable and Output Amplitude Control Register

Byte 1	Name	Control Function	Туре	0	1	Default
Bit 7	Reserved					
Bit 6	Reserved					1
Bit 5	DIF OE8	Output Enable	Output Enable RW Low/Lo		Enabled	1
Bit 4	Reserved					0
Bit 3		Reserved				1
Bit 2		Reserved				1
Bit 1	AMPLITUDE 1	Controls Output Amplitude	RW	00 = 0.55V	01= 0.65V	1
Bit 0	AMPLITUDE 0		RW	10 = 0.7V	11 = 0.8V	0

1. A low on the DIF OE bit will override the OE# pin and force the differential output Low/Low

SMBus Table: DIF Slew Rate Control Register

Byte 2	Name	Control Function	Туре	0	1	Default
Bit 7	SLEWRATESEL DIF7	Adjust Slew Rate of DIF7	RW	Slow Setting	Fast Setting	1
Bit 6	SLEWRATESEL DIF6	Adjust Slew Rate of DIF6	RW	Slow Setting	Fast Setting	1
Bit 5	SLEWRATESEL DIF5	Adjust Slew Rate of DIF5	RW	Slow Setting	Fast Setting	1
Bit 4	SLEWRATESEL DIF4	Adjust Slew Rate of DIF4	RW	Slow Setting	Fast Setting	1
Bit 3	SLEWRATESEL DIF3	Adjust Slew Rate of DIF3	RW	Slow Setting	Fast Setting	1
Bit 2	SLEWRATESEL DIF2	Adjust Slew Rate of DIF2	RW	Slow Setting	Fast Setting	1
Bit 1	SLEWRATESEL DIF1	Adjust Slew Rate of DIF1	RW	Slow Setting	Fast Setting	1
Bit 0	SLEWRATESEL DIF0	Adjust Slew Rate of DIF0	RW	Slow Setting	Fast Setting	1

SMBus Table: DIF Slew Rate Control Register

Byte 3	Name	Control Function	Туре	0	1	Default
Bit 7		Reserved				1
Bit 6	Reserved					
Bit 5		Reserved				0
Bit 4	Reserved					
Bit 3		Reserved				0
Bit 2		Reserved				1
Bit 1	Reserved					1
Bit 0	SLEWRATESEL DIF8	Adjust Slew Rate of DIF8	RW	Slow Setting	Fast Setting	1

Byte 4 is Reserved and reads back 'hFF

SMBus Table: Revision and Vendor ID Register

Byte 5	Name	Control Function	Туре	0	1	Default
Bit 7	RID3		R		0	
Bit 6	RID2	Revision ID	R	A rev = 0000		0
Bit 5	RID1		R	A lev	0	
Bit 4	RID0		R		0	
Bit 3	VID3		R			0
Bit 2	VID2	VENDOR ID	R	0001		0
Bit 1	VID1		R	0001 = IDT		0
Bit 0	VID0		R		1	

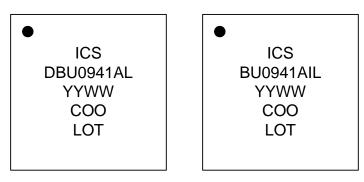
SMBus Table: Device Type/Device ID

Byte 6	Name	Control Function	Туре	0	1	Default
Bit 7	Device Type1	Device Type	R	00 = FGx,	01 = DBx,	1
Bit 6	Device Type0	Device Type	R	10 = DMx, 11=	1	
Bit 5	Device ID5		R			0
Bit 4	Device ID4		R			0
Bit 3	Device ID3	Device ID	R	001001binar	v or 09 bev	1
Bit 2	Device ID2		R	00100101101	y of 09 fiex	0
Bit 1	Device ID1		R			0
Bit 0	Device ID0		R			1

SMBus Table: Byte Count Register

Byte 7	Name	Control Function	Туре	0	1	Default
Bit 7	Reserved					
Bit 6	Reserved					
Bit 5	Reserved					
Bit 4	BC4		RW			0
Bit 3	BC3		RW	Writing to this regist	er will configure how	1
Bit 2	BC2	Byte Count Programming	RW	many bytes will be r	ead back, default is	0
Bit 1	BC1		RW	= 8 b	ytes.	0
Bit 0	BC0		RW			0

Marking Diagrams



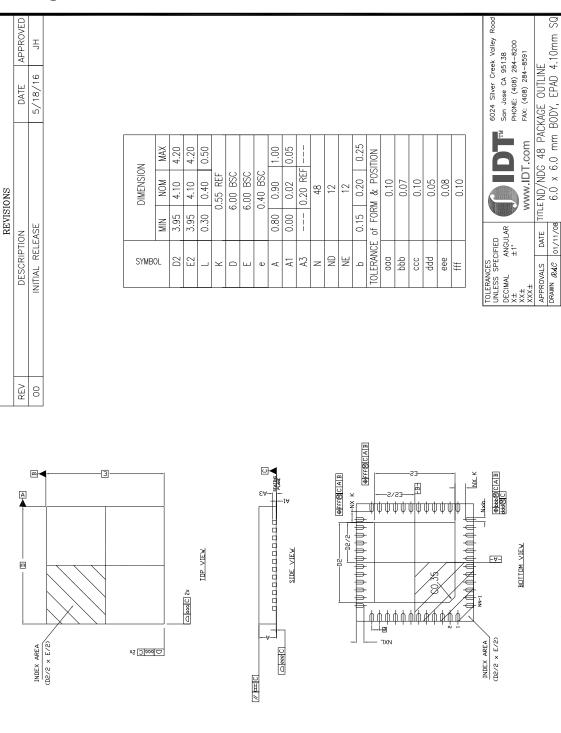
Notes:

- 1. "LOT" is the lot sequence number.
- 2. "COO" denotes country of origin.
- 3. YYWW is the last two digits of the year and week that the part was assembled.
- 4. Line 2: truncated part number
- 5. "L" denotes RoHS compliant package.
- 6. "I" denotes industrial temperature range device.

Thermal Characteristics

PARAMETER	SYMBOL	CONDITIONS	PKG	TYP VALUE	UNITS	NOTES
	θ _{JC}	Junction to Case		33	°C/W	1
	θ_{Jb}	Junction to Base		2.1	°C/W	1
Thermal Resistance	θ _{JΑ0θ}	Junction to Air, still air	NDG48	37	°C/W	1
mermai nesistance	θ_{JA1}	Junction to Air, 1 m/s air flow	NDG40	30	°C/W	1
	θ_{JA3}	Junction to Air, 3 m/s air flow	27		°C/W	1
	θ_{JA5}	Junction to Air, 5 m/s air flow		26	°C/W	1

¹ePad soldered to board



14

Package Outline and Dimensions (NDG48)

9DBU0941 DATASHEET

0F 2

-

SHEET -01

DO NOT SCALE DRAWING drawing no. PSC-

REV 00

-4212-

SIZE

0.40 mm PITCH VFQFN

CHECKED

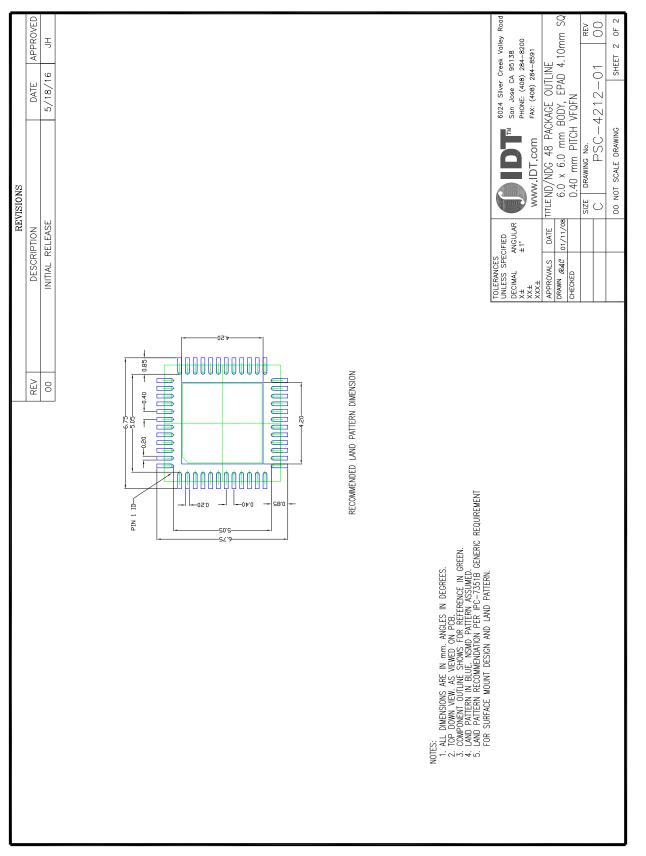
ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982 ALL DIMENSIONS ARE IN MILLINGERS. IN REFERS TO THE UNMER OF LEADS. IN AND NE REFER TO THE NUMBER OF LEADS PER SIDE.

- ~ ~ ~ ,

NOTES:

() IDT

Package Outline and Dimensions (NDG48), cont.



Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature	
9DBU0941AKLF	Trays	48-pin VFQFPN	0 to +70° C	
9DBU0941AKLFT	Tape and Reel	48-pin VFQFPN	0 to +70° C	
9DBU0941AKILF	Trays	48-pin VFQFPN	-40 to +85° C	
9DBU0941AKILFT	Tape and Reel	48-pin VFQFPN	-40 to +85° C	

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant. "A" is the device revision designator (will not correlate with the datasheet revision).

Revision History

Rev.	Initiator	Issue Date	Description	Page #
А	RDW	7/15/2014	Final update and release - front page and electrical tables.	
В	RDW	9/19/2014	Updated SMBus Input High/Low parameters conditions, MAX values, and footnotes.	
с	RDW	4/17/2015	 Minor updates to front page text for family consistency. Updated Clock Input Parameters table to be consistent with PCIe Vswing parameter. 	1,5
D	RDW	2/16/2017	1. Updated pins 30 and 29 from VDDA1.5 and GNDA to VDDO1.5 and GND to clearly indicate that this part has no PLL.	2, 3
E	RDW	3/9/2017	 Removed "Bypass Mode" reference in "Output Duty Cycle" and "Phase Jitter Parameters" tables; update note 3 under Output Duty Cycle table. Corrected spelling errors/typos. Change VDDA to VDDO1.5 in Current Consumption table. Update Additive Phase Jitter conditions for PCIe Gen3. 	



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