SN74LV244A Octal Buffers and Drivers With 3-State Outputs

1 Features

- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 6.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250-mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Servers and Network Switches
- LED Displays
- Telecom Infrastructure
- Motor-Drive Control Boards

3 Description

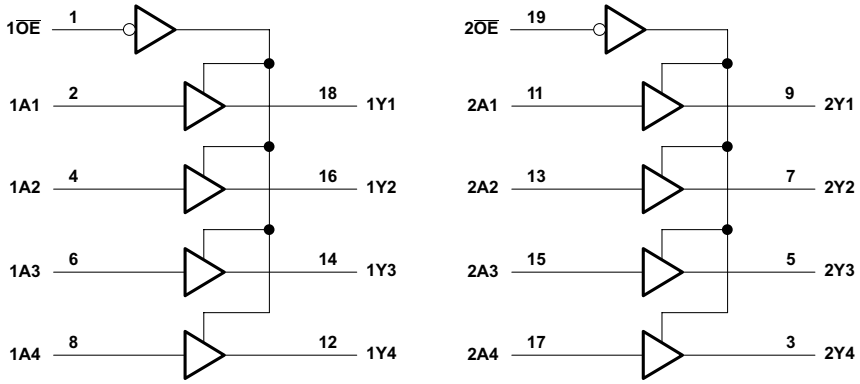
The SN74LV244A octal buffers and line drivers are designed for 2-V to 5.5-V V_{CC} operation.

The SN74LV244A devices are designed specifically to improve both performance and density of the 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices are organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs.

Device Information

PART NUMBER	PACKAGE (PIN)	BODY SIZE
SN74LV244ADGV	TVSOP (20)	5.00 mm × 4.40 mm
SN74LV244ADW	SOIC (20)	12.80 mm × 7.50 mm
SN74LV244ANS	SOP (20)	12.60 mm × 5.30 mm
SN74LV244APW	TSSOP (20)	6.50 mm × 4.40 mm
SN74LV244ARGY	VQFN (20)	4.50 mm × 3.50 mm

Logic Diagram (Positive Logic)



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (June 2013) to Revision N **Page**

- Added *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Detailed Description* section, *Applications and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted SN54LV244A part number from the data sheet ... 1
- Removed the T_A = –40°C to 85°C test conditions with the same values as the T_A = –40°C to 125°C Recommended test conditions in the *Electrical Characteristics* and *Switching Characteristics* tables ... 6
- Removed the word 'Recommended' in the T_A = –40°C to 125°C Recommended test conditions in the *Electrical Characteristics* and *Switching Characteristics* tables ... 6

Changes from Revision L (August 2010) to Revision M **Page**

- Changed document format from Quicksilver to DocZone ... 1
- Changed Extended operating temperature range to 125°C ... 1

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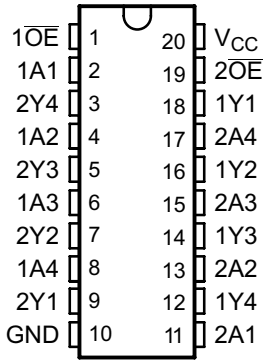
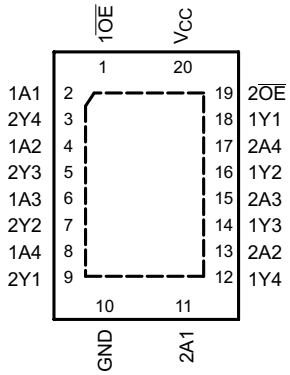
5 Pin Configuration and Functions

DB, DGV, DW, NS, PW Package
20-Pin SSOP, TVSOP, SOIC, SO, TSSOP
Top View



RGY Package
20-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A1	2	I	Input
1A2	4	I	Input
1A3	6	I	Input
1A4	8	I	Input
$1\overline{OE}$	1	I	Output enable
1Y1	18	O	Output
1Y2	16	O	Output
1Y3	14	O	Output
1Y4	12	O	Output
2A1	11	I	Input
2A2	13	I	Input
2A3	15	I	Input
2A4	17	I	Input
$2\overline{OE}$	19	I	Output enable
2Y1	9	O	Output
2Y2	7	O	Output
2Y3	5	O	Output
2Y4	3	O	Output
GND	10	—	Ground
V_{CC}	20	—	Power pin

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I	Input voltage(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
V_O	Output voltage(2)(3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_j	Junction temperature		–65	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5-V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2 V		–50	µA
		V_{CC} = 2.3 V to 2.7 V		–2	mA
		V_{CC} = 3 V to 3.6 V		–8	
		V_{CC} = 4.5 V to 5.5 V		–16	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 2.3 V to 2.7 V		2	mA
		V_{CC} = 3 V to 3.6 V		8	
		V_{CC} = 4.5 V to 5.5 V		16	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200	ns/V
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		SN74LV244A						UNIT
		DB (SSOP)	DGV (TVSOP)	DW (SOIC)	NS (SO)	PW (TSSOP)	RGY (VQFN)	
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.7	115.9	79.4	76.9	102.6	34.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.7	31.1	43.8	43.4	36.7	43.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.9	57.4	47.2	44.5	53.6	12.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.7	1.0	18.8	17.0	2.4	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.5	56.7	46.7	44.1	53.1	12.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	7.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –50 µA	T_A = –40°C to 125°C	2 V to 5.5 V	V_{CC} – 0.1			V
	I_{OH} = –2 mA	T_A = –40°C to 125°C	2.3 V	2			
	I_{OH} = –8 mA	T_A = –40°C to 125°C	3 V	2.48			
	I_{OH} = 16 mA	T_A = –40°C to 125°C	4.5 V	3.8			
V_{OL}	I_{OL} = 50 µA	T_A = –40°C to 125°C	2 V to 5.5 V			0.1	V
	I_{OL} = 2 mA	T_A = –40°C to 125°C	2.3 V			0.4	
	I_{OL} = 8 mA	T_A = –40°C to 125°C	3 V			0.44	
	I_{OL} = 16 mA	T_A = –40°C to 125°C	4.5 V			0.55	
I_I	V_I = 5.5 V or GND	T_A = –40°C to 125°C	0 to 5.5 V			±1	µA
I_{OZ}	V_O = V_{CC} or GND	T_A = –40°C to 125°C	5.5 V			±5	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	T_A = –40°C to 125°C	5.5 V			20	µA
I_{off}	V_I or V_O = 0 to 5.5 V	T_A = –40°C to 125°C	0			5	µA
C_i	V_I = V_{CC} or GND	T_A = –40°C to 125°C	3.3 V		2.3		pF

6.6 Noise Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C(1)

		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic		0.55		V
$V_{OL(V)}$	Quiet output, minimum dynamic		–0.5		V
$V_{OH(V)}$	Quiet output, minimum dynamic		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

6.7 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	3.3 V	14	pF
			5 V	16	

6.8 Switching Characteristics: V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	A	Y	C_L = 15 pF	T_A = 25°C		7.5(1)	12.5(1)	ns
				T_A = –40°C to 125°C	1		15	
t_{en}	$\overline{OE}$	Y	C_L = 15 pF	T_A = 25°C		8.9(1)	14.6(1)	ns
				T_A = –40°C to 125°C	1		17	
t_{dis}	$\overline{OE}$	Y	C_L = 15 pF	T_A = 25°C		9.1(1)	14.1(1)	ns
				T_A = –40°C to 125°C	1		16	
t_{pd}	A	Y	C_L = 50 pF	T_A = 25°C		9.5(1)	15.3	ns
				T_A = –40°C to 125°C	1		18	
t_{en}	$\overline{OE}$	Y	C_L = 50 pF	T_A = 25°C		10.8	17.8	ns
				T_A = –40°C to 125°C	1		21	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

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Switching Characteristics: V_{CC} = 2.5 V ± 0.2 V (continued)

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{dis}	$\overline{OE}$	Y	C_L = 50 pF	T_A = 25°C		13.4	19.2	ns
				T_A = –40°C to 125°C	1		21	
$t_{sk(o)}$			C_L = 50 pF	T_A = 25°C			2	ns
				T_A = –40°C to 125°C			2	

6.9 Switching Characteristics: V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	A	Y	C_L = 15 pF	T_A = 25°C		5.4(1)	8.4(1)	ns
				T_A = –40°C to 125°C	1		10	
t_{en}	$\overline{OE}$	Y	C_L = 15 pF	T_A = 25°C		6.3(1)	10.6(1)	ns
				T_A = –40°C to 125°C	1		12.5	
t_{dis}	$\overline{OE}$	Y	C_L = 15 pF	T_A = 25°C		7.6(1)	11.7(1)	ns
				T_A = –40°C to 125°C	1		13	
t_{pd}	A	Y	C_L = 50 pF	T_A = 25°C		6.8	11.9	ns
				T_A = –40°C to 125°C	1		13.5	
t_{en}	$\overline{OE}$	Y	C_L = 50 pF	T_A = 25°C		7.8	14.1	ns
				T_A = –40°C to 125°C	1		16	
t_{dis}	$\overline{OE}$	Y	C_L = 50 pF	T_A = 25°C		11	16	ns
				T_A = –40°C to 125°C	1		18	
$t_{sk(o)}$			C_L = 50 pF	T_A = 25°C			1.5	ns
				T_A = –40°C to 125°C			1.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.10 Switching Characteristics: V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	A	Y	C_L = 15 pF	T_A = 25°C		3.9(1)	5.5(1)	ns
				T_A = –40°C to 125°C	1		6.5	
t_{en}	$\overline{OE}$	Y	C_L = 15 pF	T_A = 25°C		4.5(1)	7.3(1)	ns
				T_A = –40°C to 125°C	1		8.5	
t_{dis}	$\overline{OE}$	Y	C_L = 15 pF	T_A = 25°C		6.5(1)	12.2(1)	ns
				T_A = –40°C to 125°C	1		13.5	
t_{pd}	A	Y	C_L = 50 pF	T_A = 25°C		4.9	7.5	ns
				T_A = –40°C to 125°C	1		8.5	
t_{en}	$\overline{OE}$	Y	C_L = 50 pF	T_A = 25°C		5.6	9.3	ns
				T_A = –40°C to 125°C	1		10.5	
t_{dis}	$\overline{OE}$	Y	C_L = 50 pF	T_A = 25°C		8.8	14.2	ns
				T_A = –40°C to 125°C	1		15.5	
$t_{sk(o)}$				T_A = 25°C			1	ns
				T_A = –40°C to 85°C			1	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

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6.11 Typical Characteristics

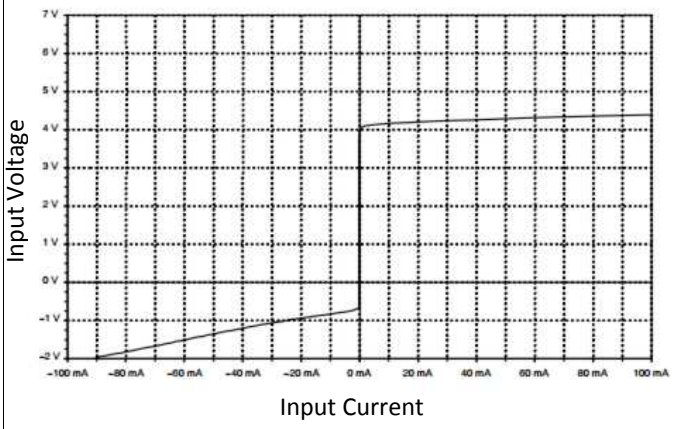

Figure 1. Input Voltage vs Input Current

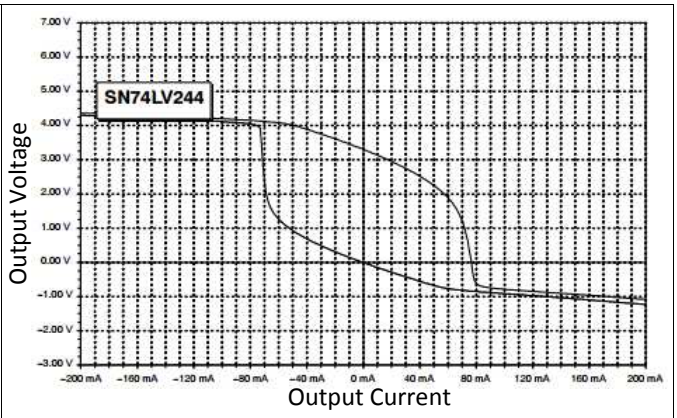

Figure 2. Output Voltage vs Output Current

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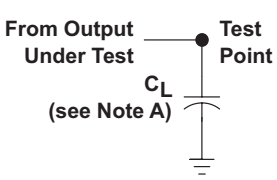
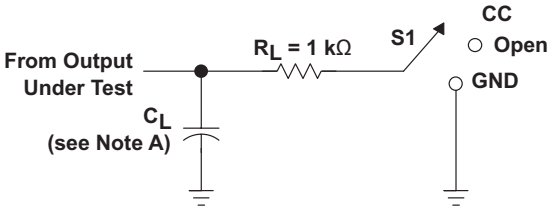
7 Parameter Measurement Information

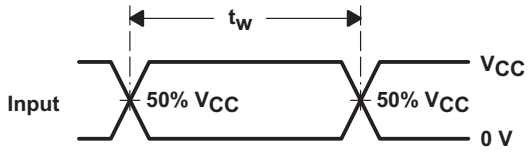


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

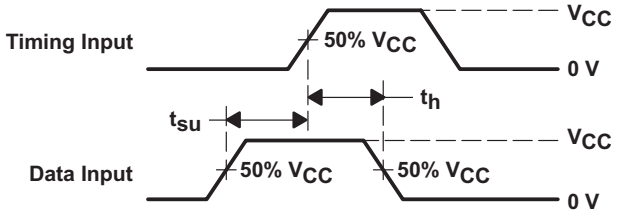


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

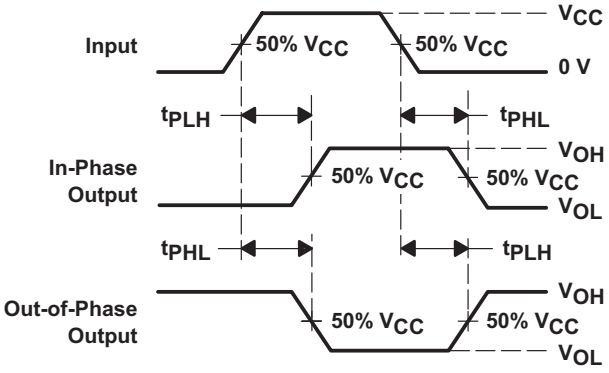
LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS



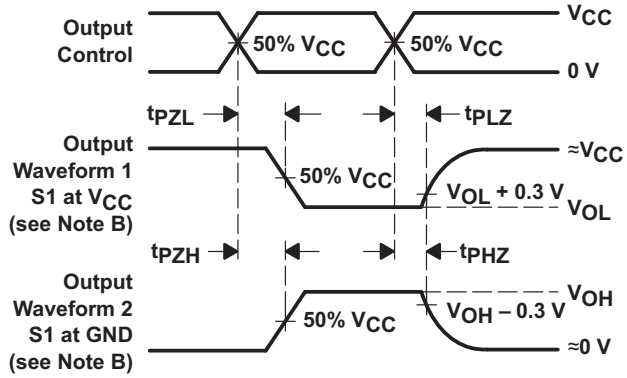
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.

D. The outputs are measured one at a time, with one input transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PHL} and t_{PLH} are the same as t_{pd}.

H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

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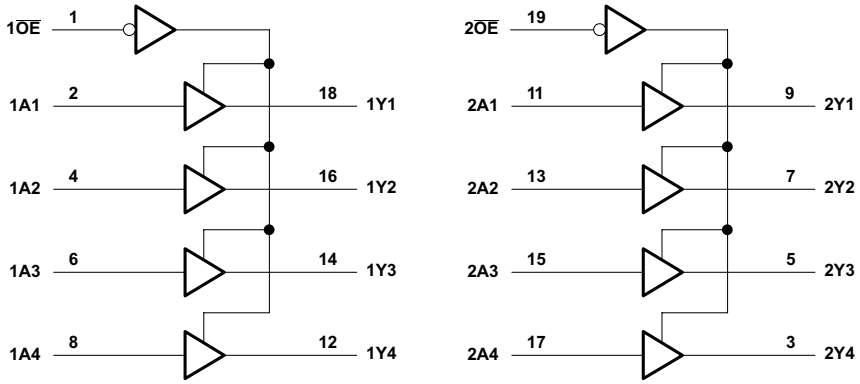
8 Detailed Description

8.1 Overview

The SN74LV244 devices are octal buffers grouped in fours, with each group having its own enable pin. The LV family supports high current drive of about 16 mA, thus making it suitable for driving digital signals over longer board lengths. This device is generally used to buffer or incorporate delays between the signals between two microcontroller or peripheral devices.

8.2 Functional Block Diagram



8.3 Feature Description

The SN74LV244A, a part of LV family, can work over a wide voltage range from 2 V to 5.5 V. The device features a very low propagation delay of about 6.5 ns when enabled for 5-V V_{CC}, which allows the device to be used for high-speed applications. The device supports a partial-power-down mode for low quiescent current application, thus making it the buffer of choice in power-efficient circuits. The I_{off} circuitry also disables the outputs, preventing damaging current backflow through the devices when they are powered down.

8.4 Device Functional Modes

The SN74LV244A devices are organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state. To ensure the high-impedance state during power up or power down, $\overline{OE}$ must be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Table 1. Function Table

INPUTS		OUTPUTS
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	Z

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LV244A device can be used as an 8-channel buffer to drive signals from one controller to another device. Buffers are typically used for signals running on long traces on printed circuit boards or going through connectors linking two printed circuit boards together. Buffers are also used to create delay between the lines to match the edges of two clock or data signals. The high-current capability of the SN74LV244A device also allows a controller to drive LEDs up to 16 mA.

9.2 Typical Application

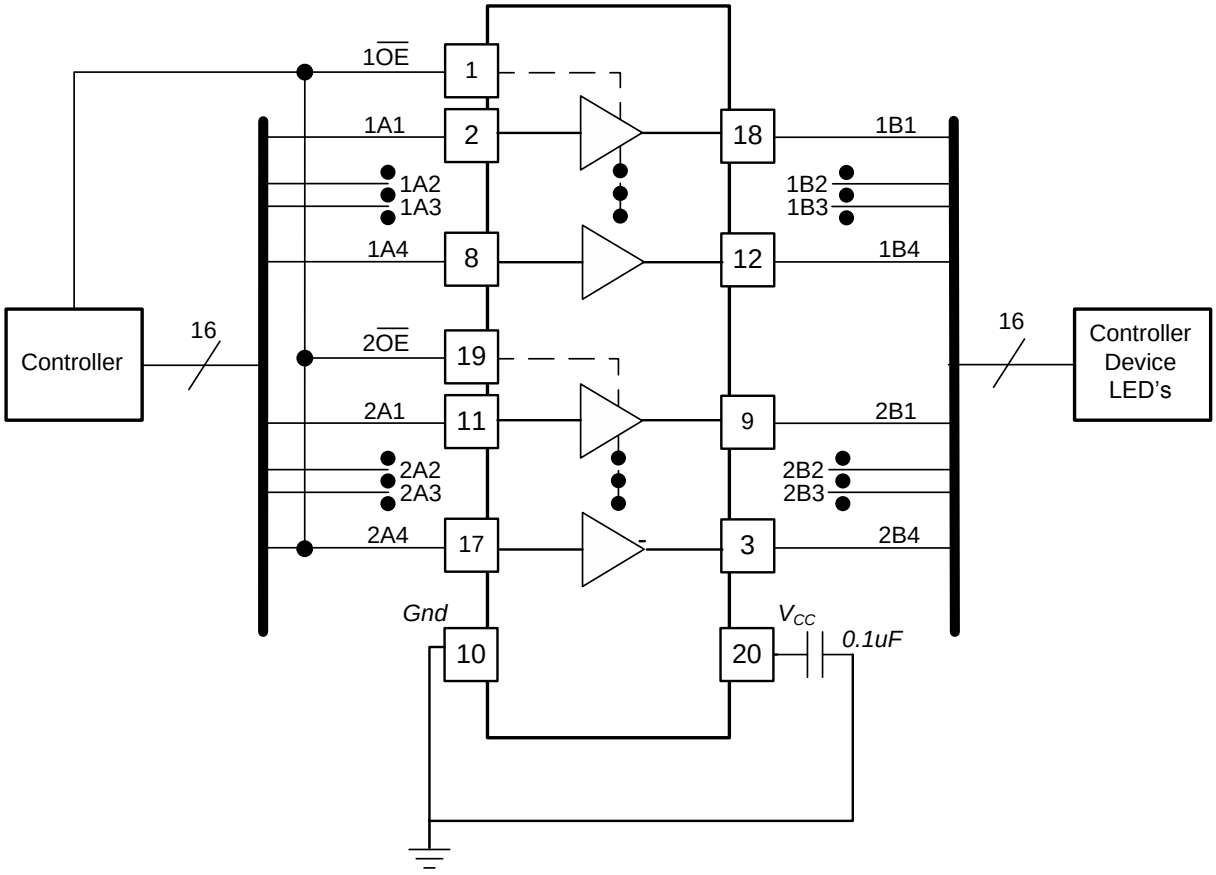

Figure 4. Typical Application Diagram

Typical Application (continued)

9.2.1 Design Requirements

A 0.1-µF bypass capacitor must be placed between each V_{CC} pin and GND. For best results, each capacitor must be placed as close as possible to the SN74LV244A device.

9.2.2 Detailed Design Procedure

1. Recommended input conditions:
   - For specified high and low levels, see V_{IH} and V_{IL} in *Recommended Operating Conditions*
   - Inputs and outputs are overvoltage tolerant, which allows them to go as high as 5.5 V at any valid V_{CC}
2. Recommended output conditions:
   - Load currents must not exceed limits as mentioned in Recommended Operating Conditions
3. Frequency selection criterion:
   - Added trace resistance or capacitance can reduce maximum frequency capability; use layout practices as directed in *Layout Guidelines*

9.2.3 Application Curve

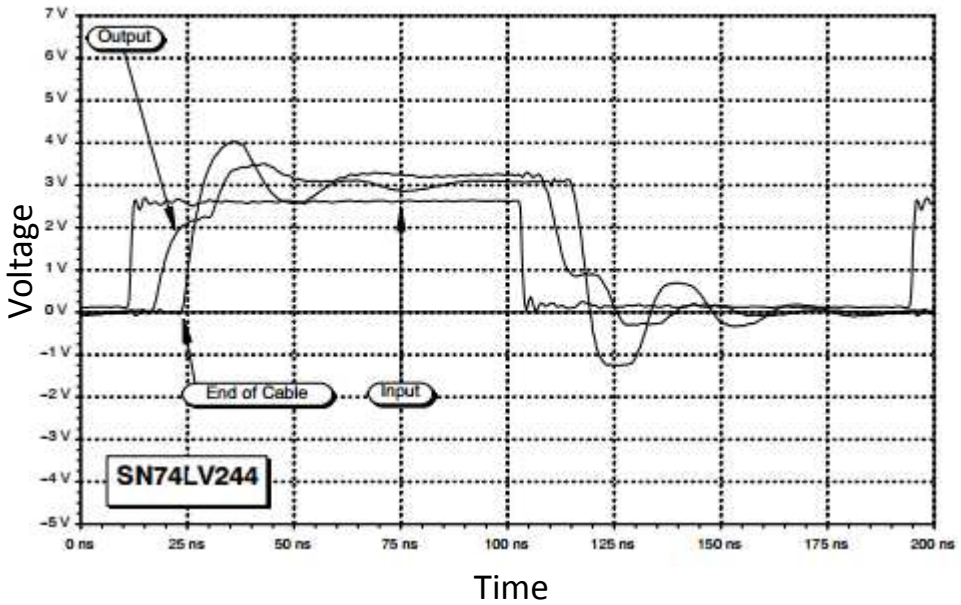

Figure 5. SN74LV244A Transient response

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10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply-voltage rating listed in the *Absolute Maximum Ratings* table.

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF bypass capacitor is recommended. If multiple pins are labeled V_{CC}, then a 0.01-µF or 0.022-µF capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-µF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 µF and 1 µF are commonly used in parallel. For best results, the bypass capacitor must be installed as close as possible to the power terminal.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace, which results in the reflection. Not all PCB traces can be straight; therefore, some traces must turn corners. Figure 6 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

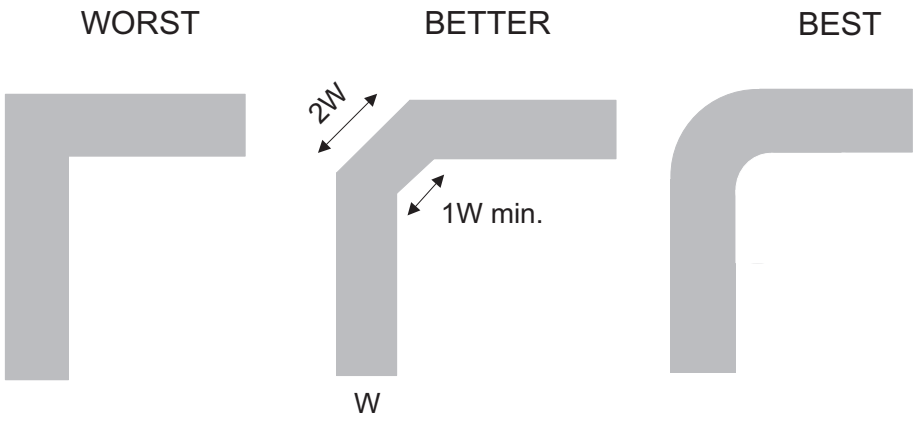

Figure 6. Trace Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV244ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV244A	Samples
SN74LV244ADBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV244A	Samples
SN74LV244ADBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV244A	Samples
SN74LV244ADGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV244A	Samples
SN74LV244ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV244A	Samples
SN74LV244ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV244A	Samples
SN74LV244ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV244A	Samples
SN74LV244ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV244A	Samples
SN74LV244ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV244A	Samples
SN74LV244ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV244A	Samples
SN74LV244APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV244A	Samples
SN74LV244APWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV244A	Samples
SN74LV244APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LV244A	Samples
SN74LV244APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV244A	Samples
SN74LV244APWRG3	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LV244A	Samples
SN74LV244APWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV244A	Samples
SN74LV244APWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV244A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV244ARGYR	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV244A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV244A :

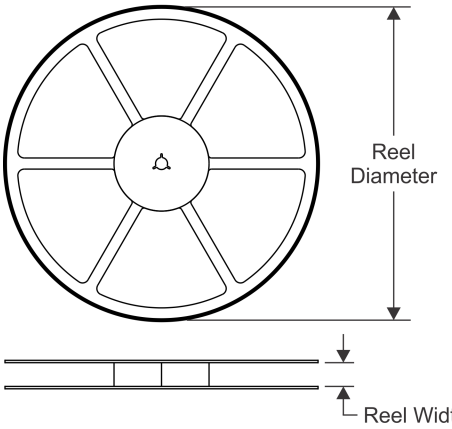
- Enhanced Product: SN74LV244A-EP

NOTE: Qualified Version Definitions:

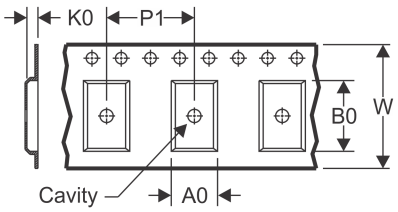
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

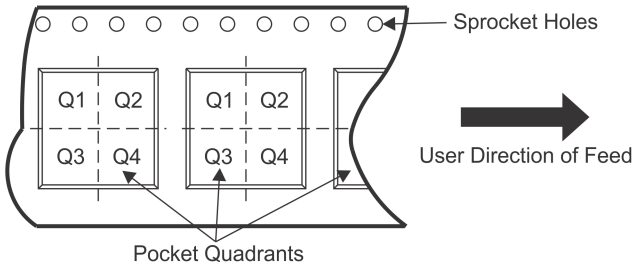


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

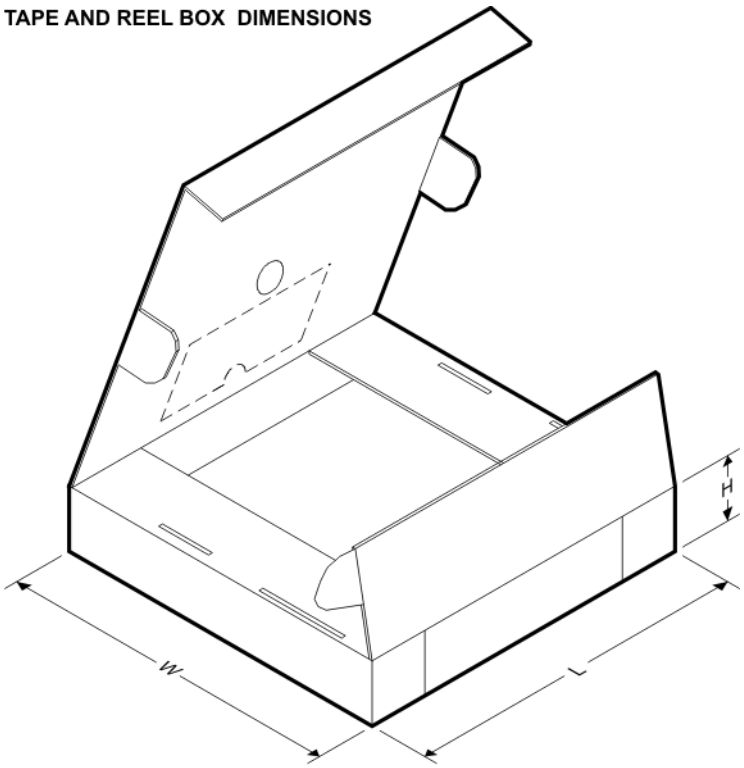
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV244ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LV244ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV244ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LV244ANSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LV244APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LV244APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV244APWRG3	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LV244APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LV244ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

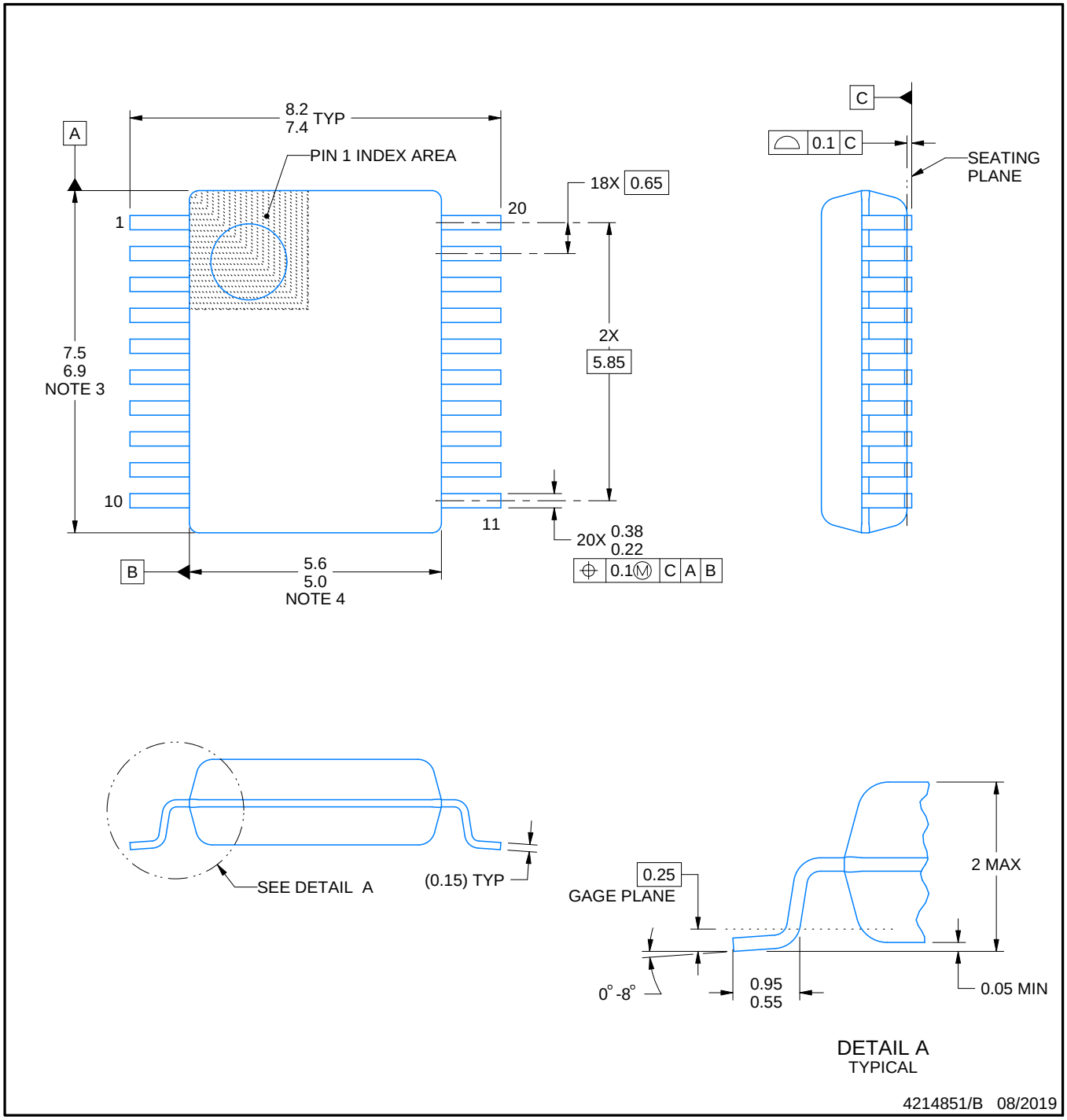
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV244ADBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74LV244ADGVR	TVSOP	DGV	20	2000	367.0	367.0	35.0
SN74LV244ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LV244ANSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LV244APWR	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74LV244APWR	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74LV244APWRG3	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74LV244APWT	TSSOP	PW	20	250	367.0	367.0	38.0
SN74LV244ARGYR	VQFN	RGY	20	3000	367.0	367.0	35.0

PACKAGE OUTLINE

DB0020A

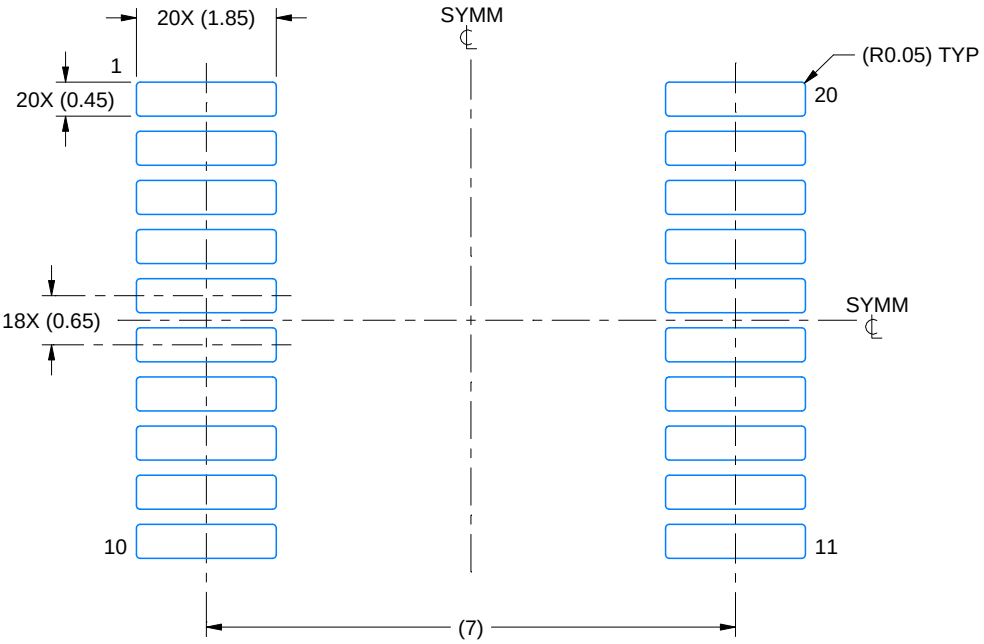
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

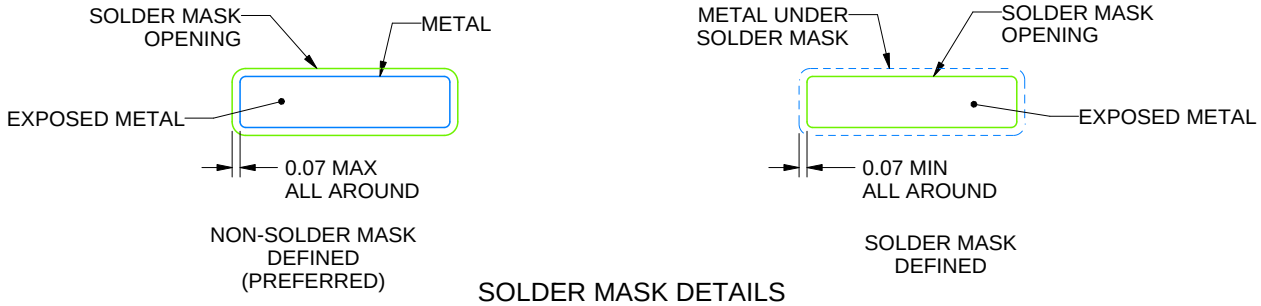


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

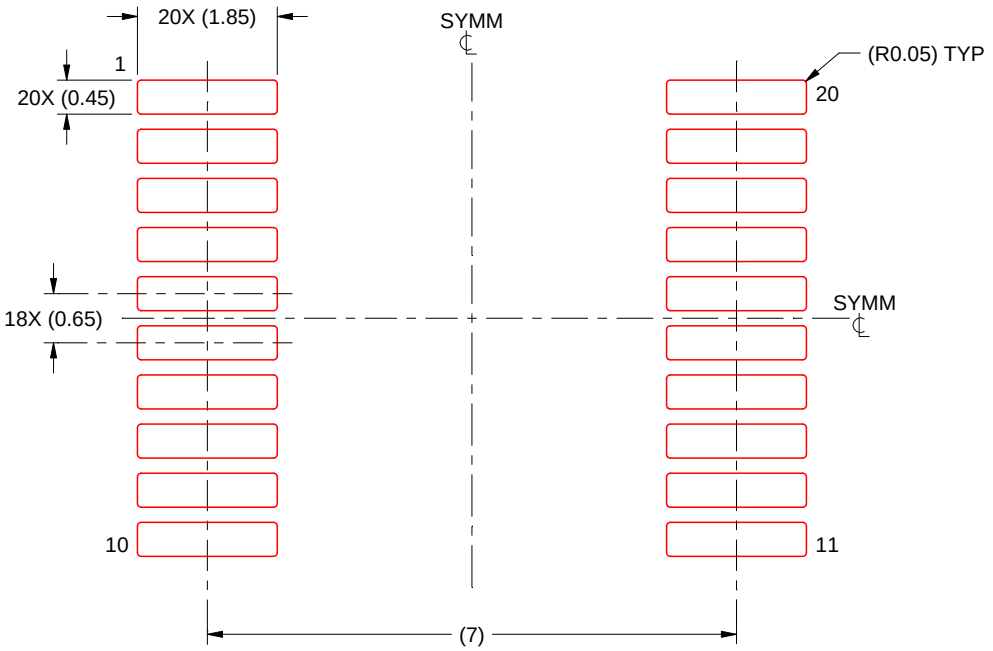
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

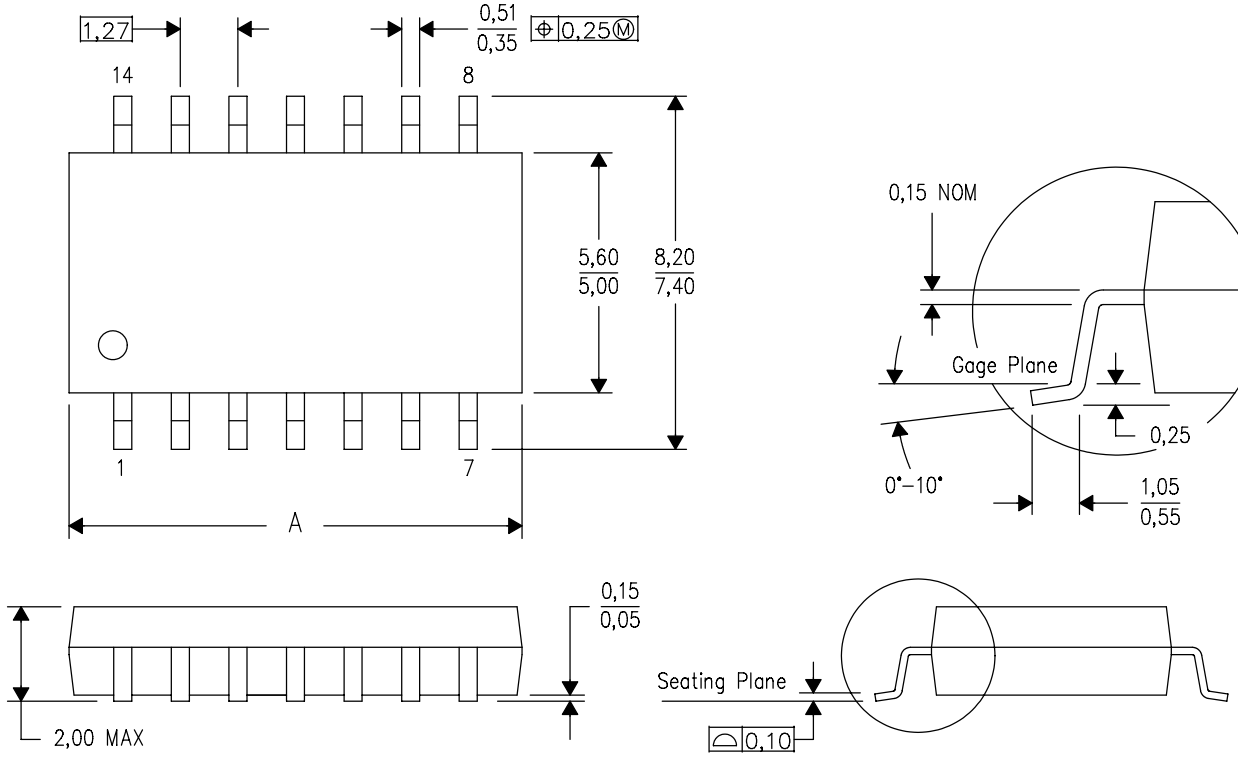
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



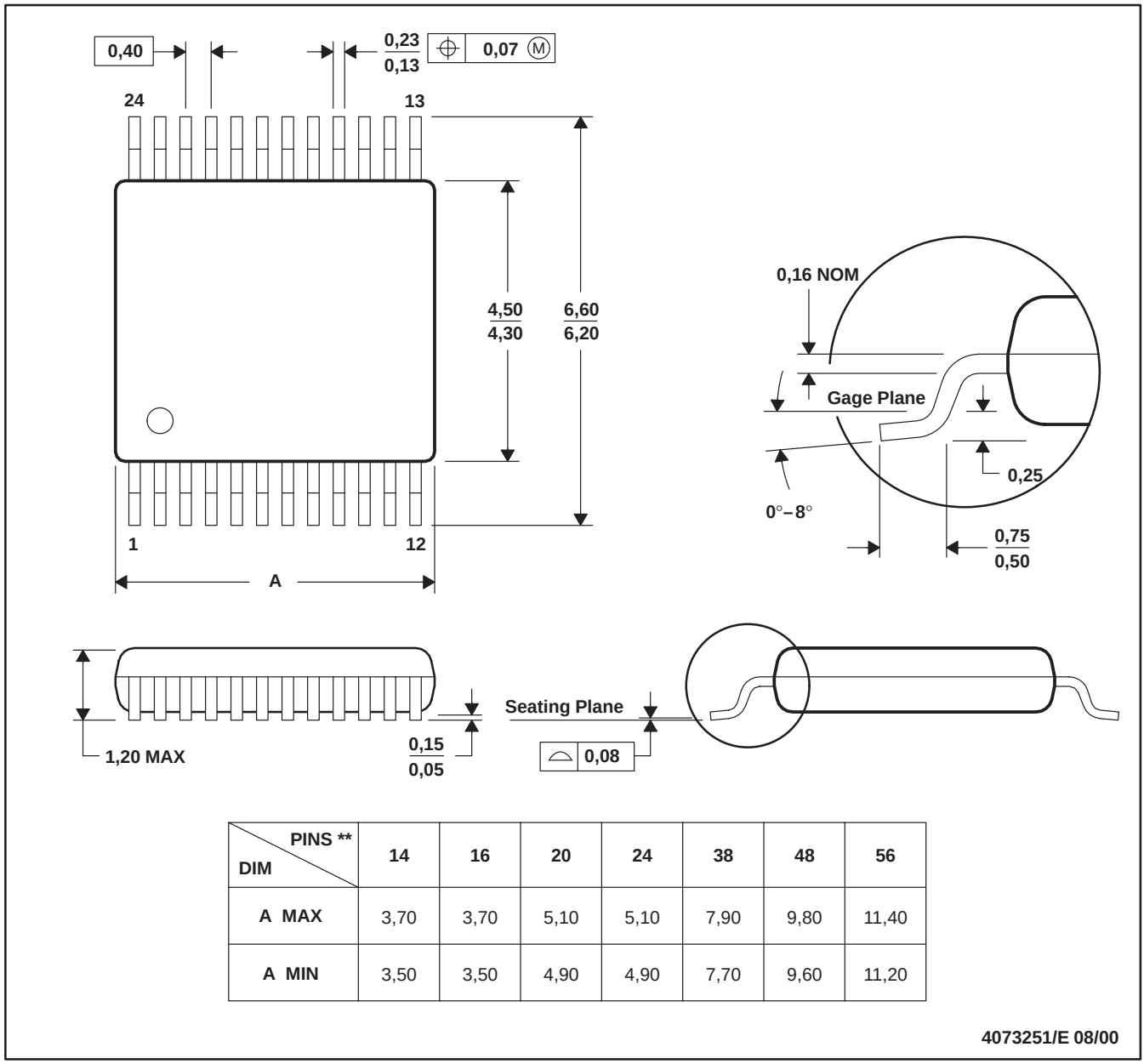
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

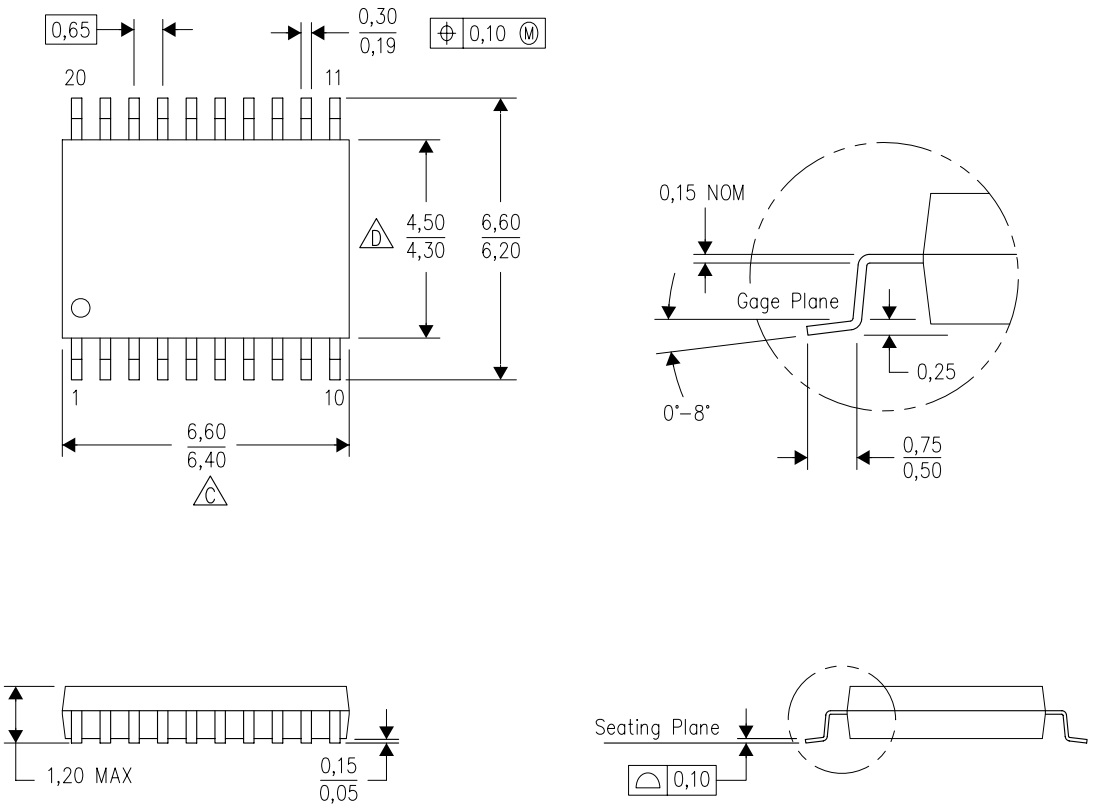


DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

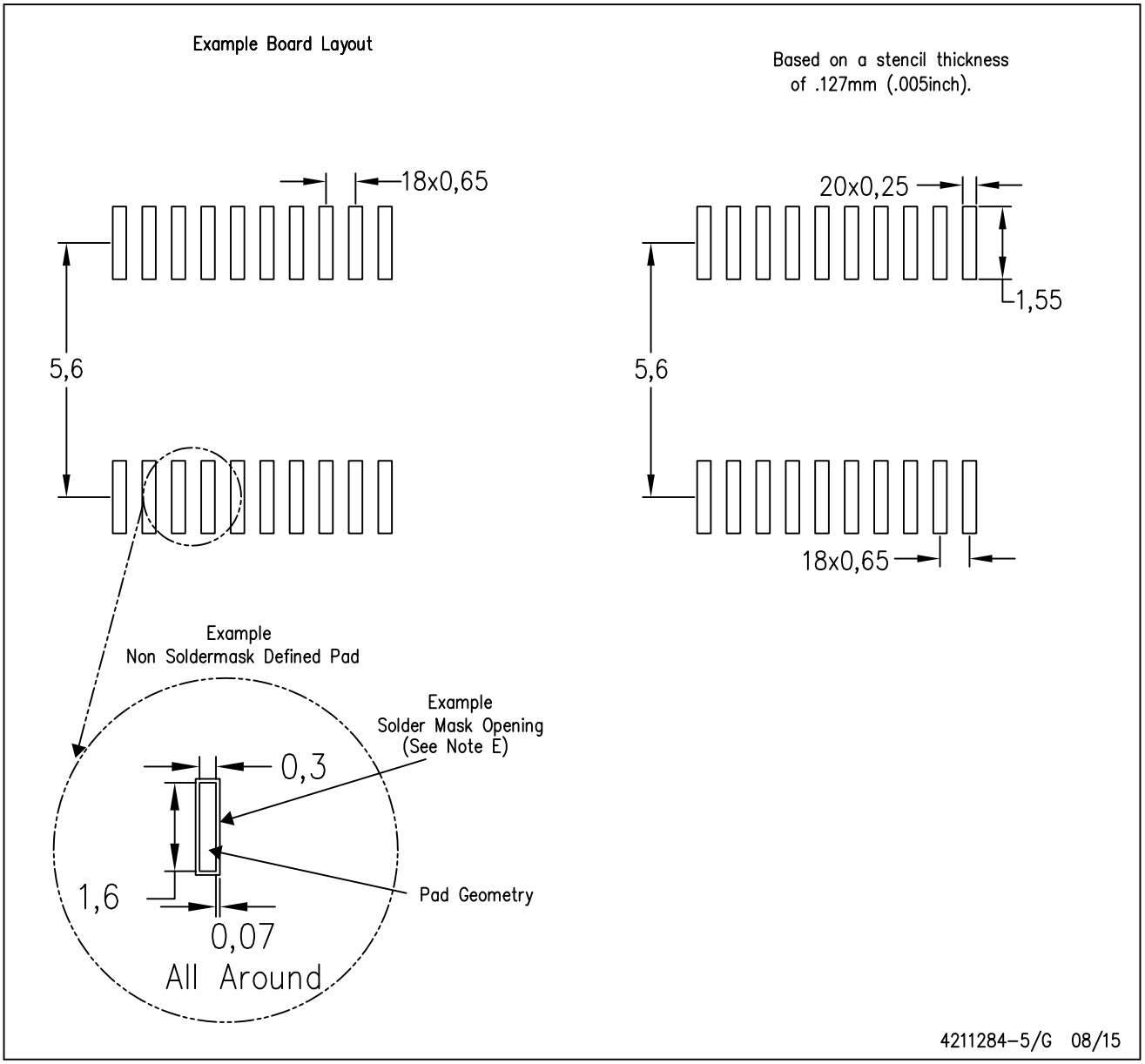
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

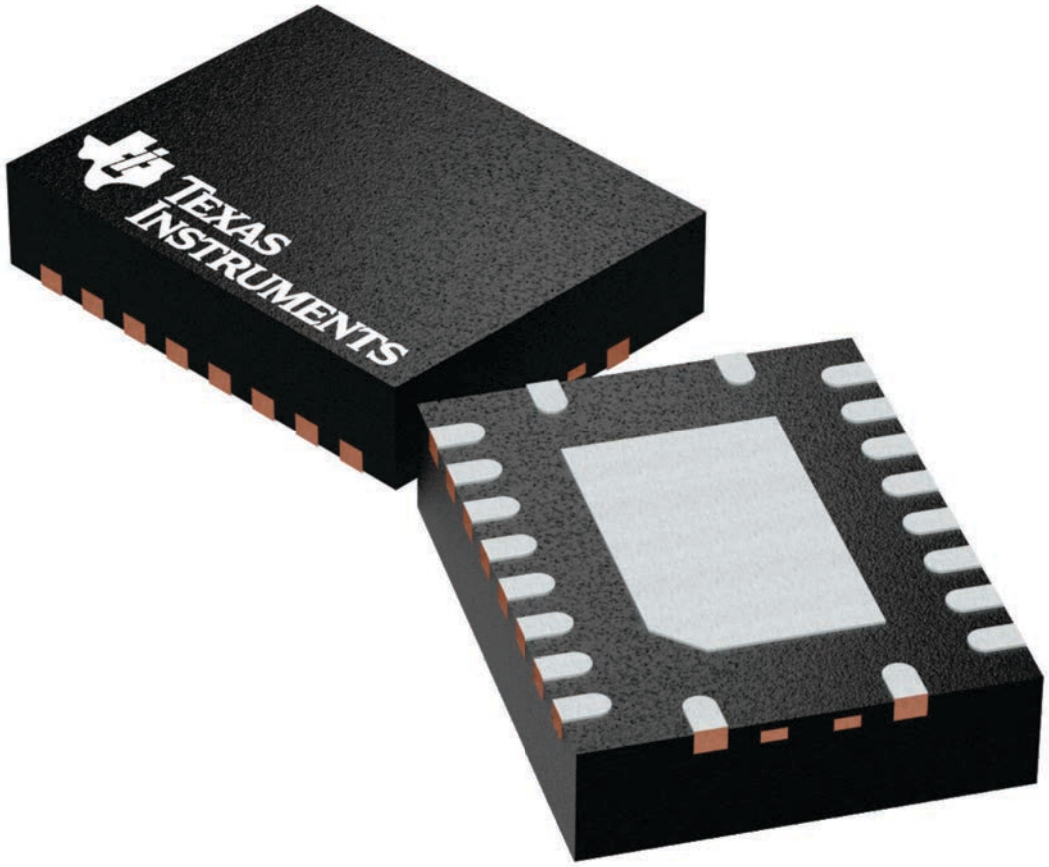
RGY 20

VQFN - 1 mm max height

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



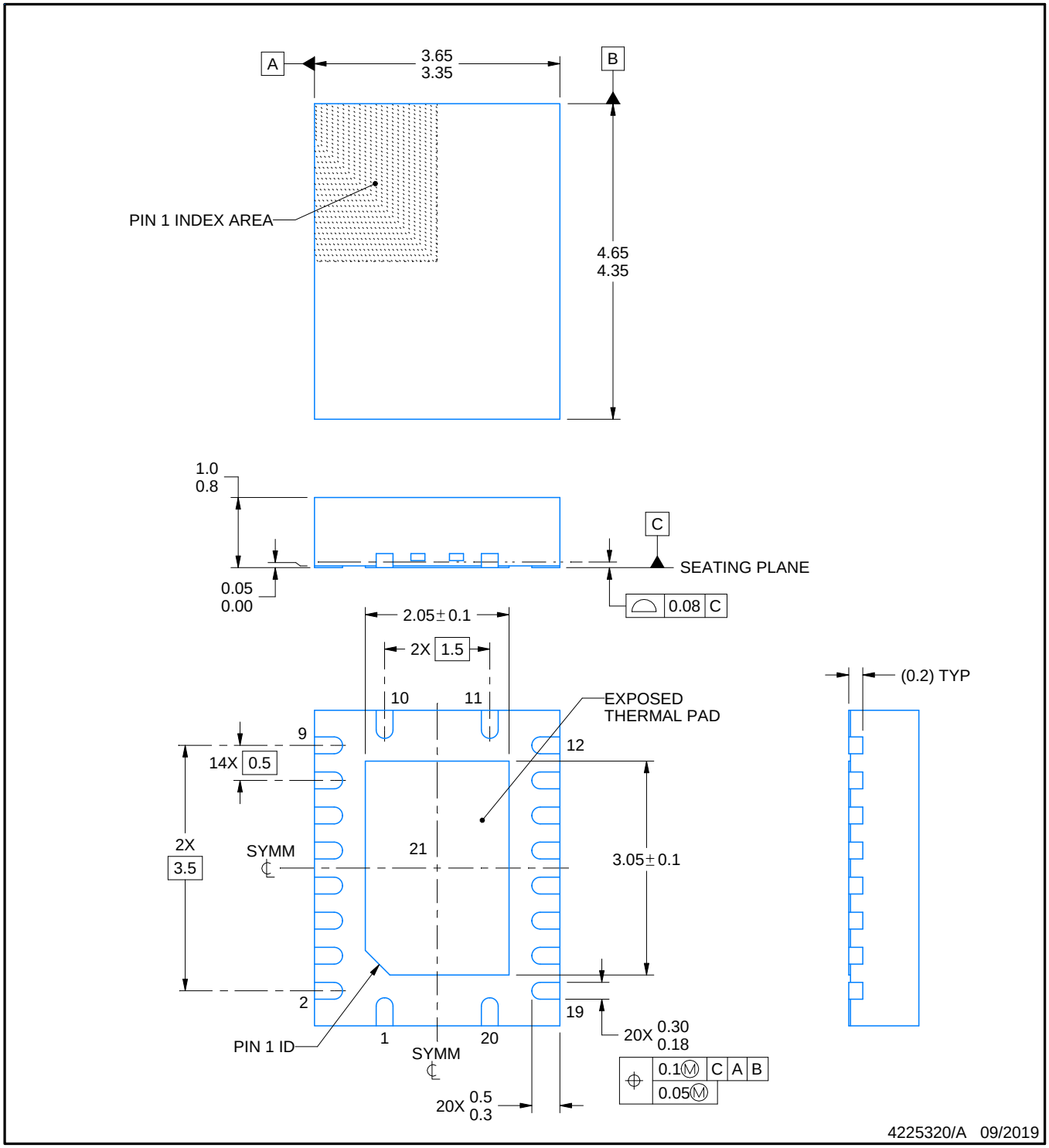
4225264/A

PACKAGE OUTLINE

RGY0020A

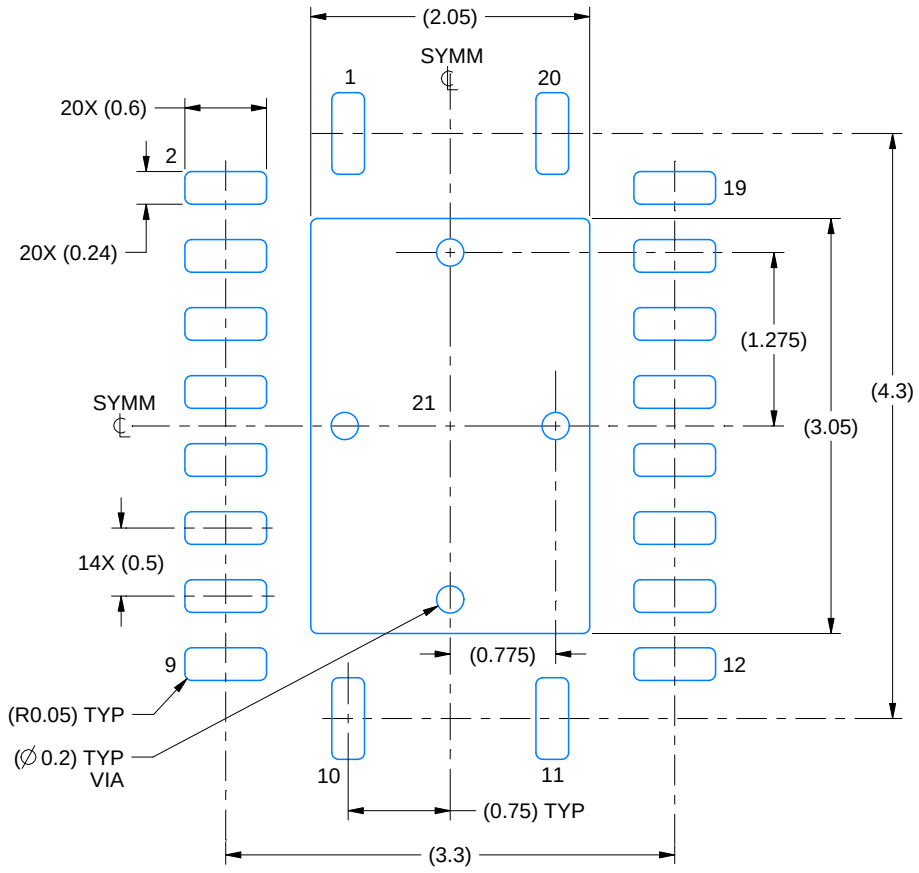
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

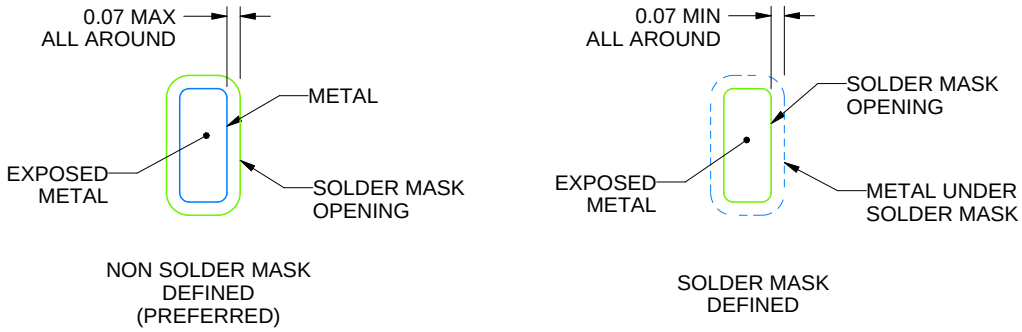


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

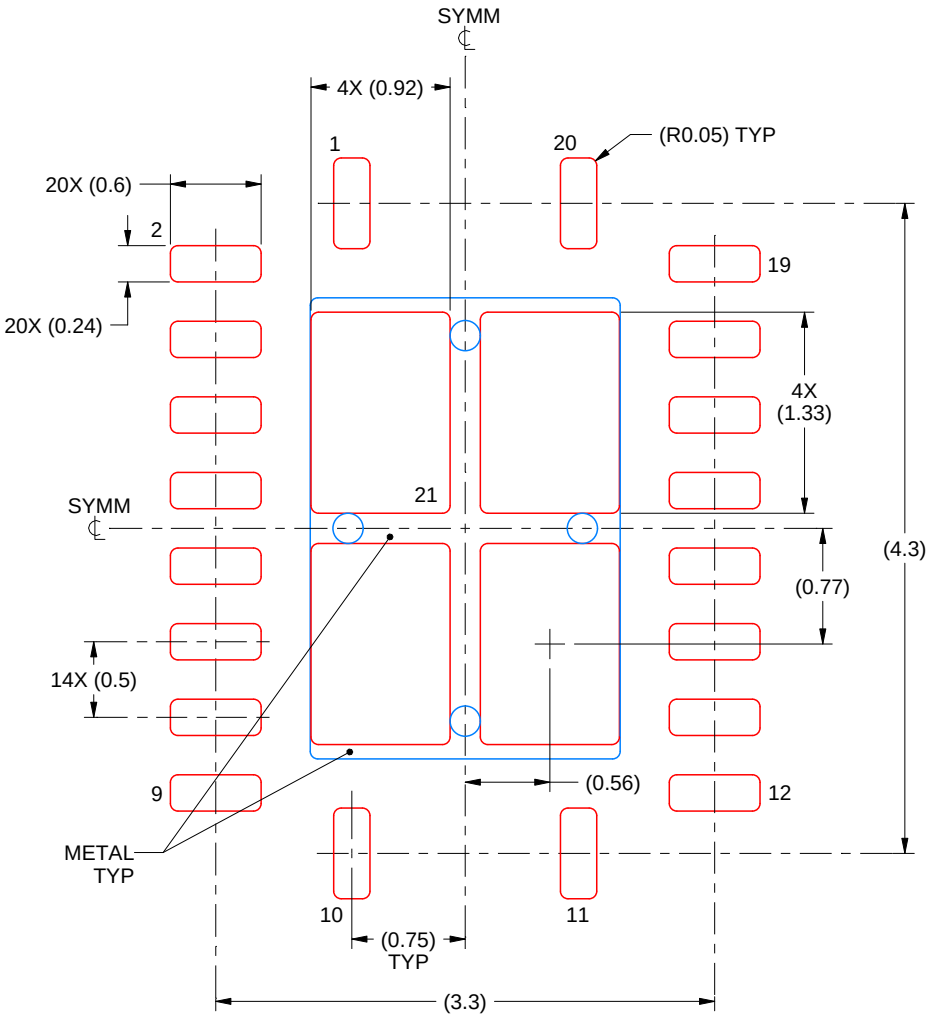


SOLDER MASK DETAILS

4225320/A 09/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



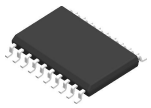
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

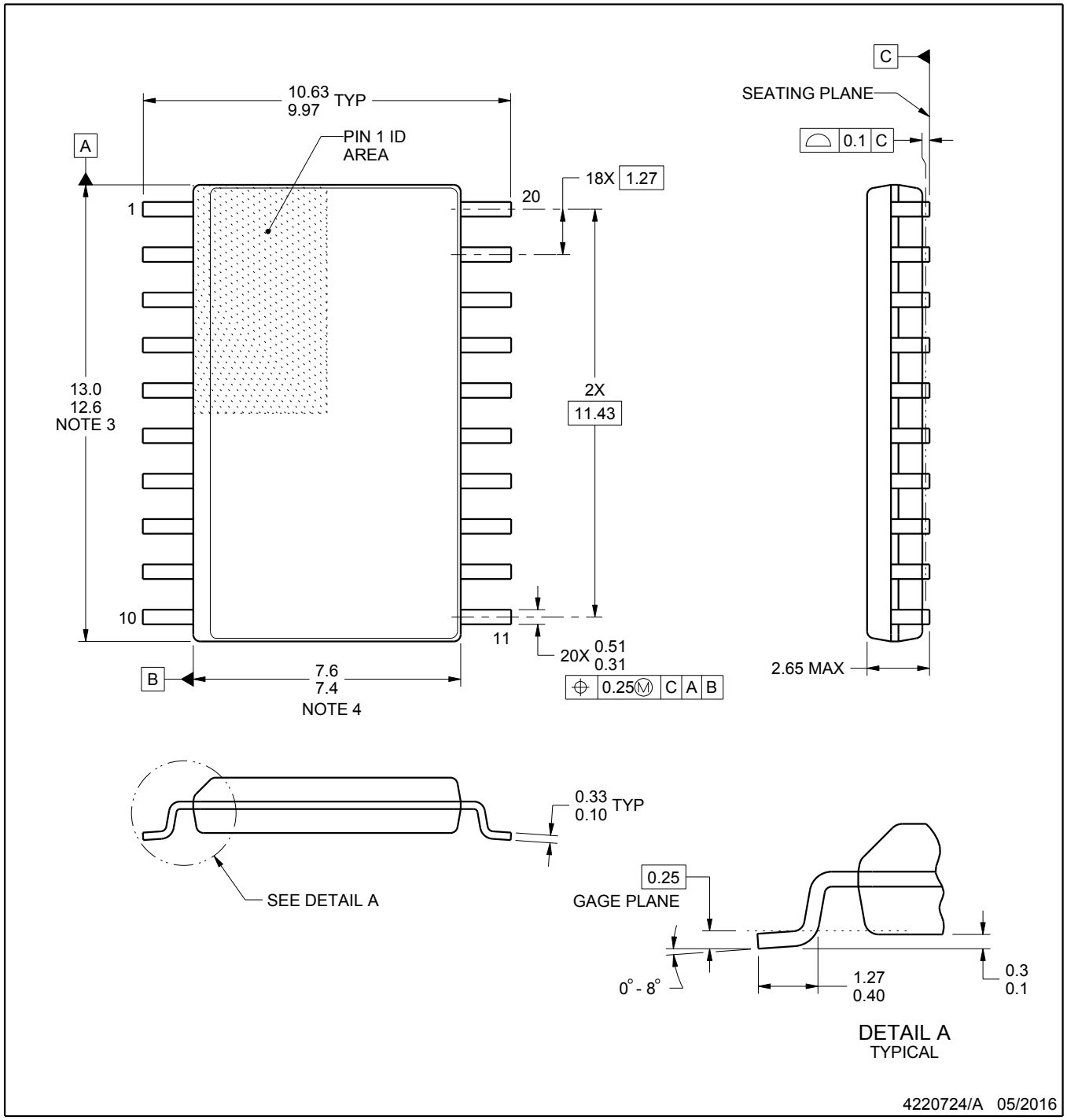


PACKAGE OUTLINE

DW0020A

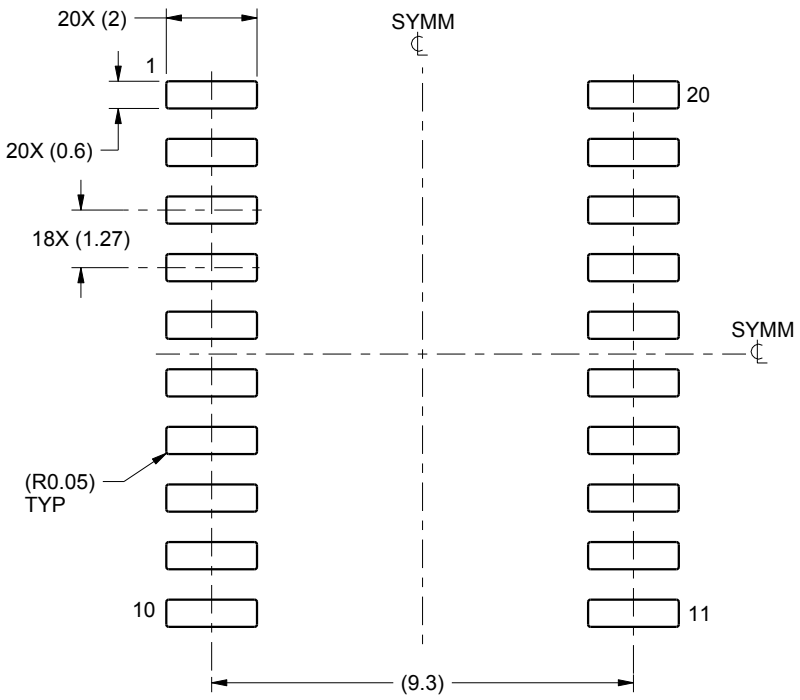
SOIC - 2.65 mm max height

SOIC

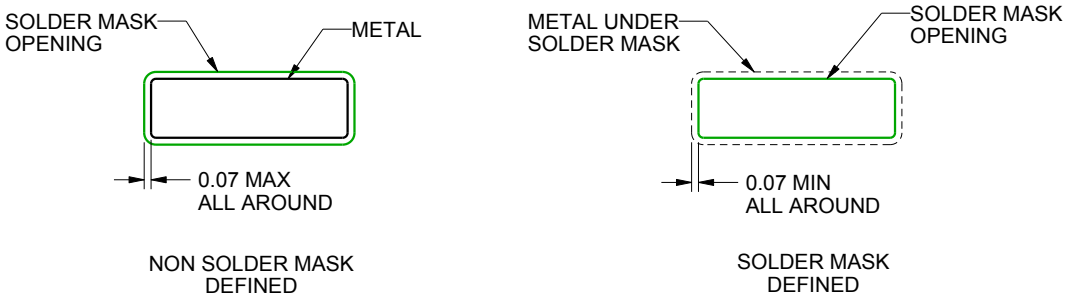


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

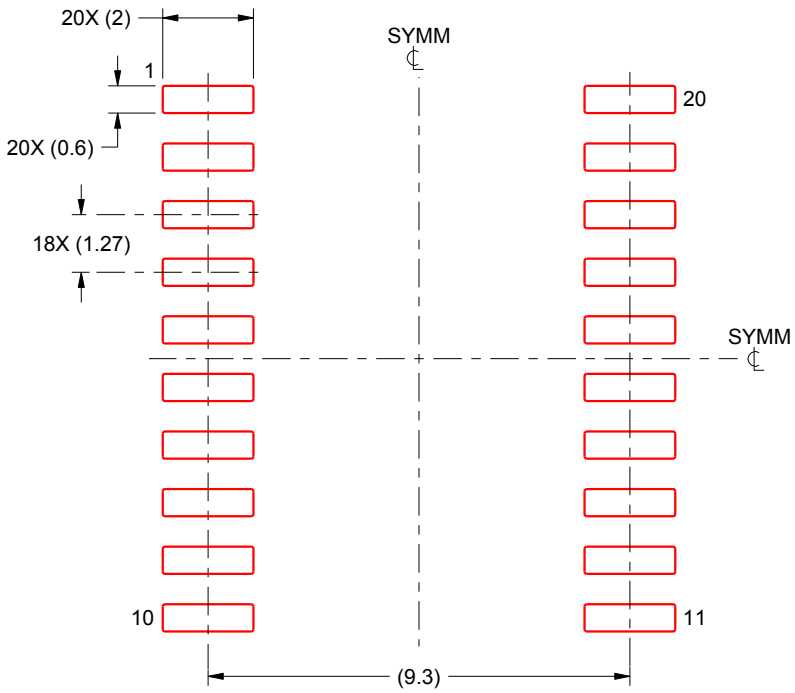


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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