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FAIRCHILD

July 2014

FCH170N60

N-Channel SuperFET® II MOSFET

600 V, 22 A, 170 mΩ

Features

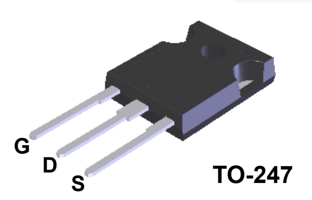
- 650 V @T_J = 150°C
- Typ. $R_{DS(on)}$ = 150 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 42 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 190 pF)
- 100% Avalanche Tested
- RoHS Compliant

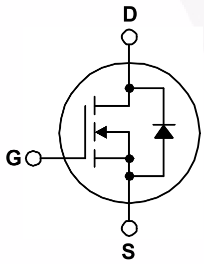
Applications

- Telecom / Sever Power Supplies
- Industrial Power Supplies
- AC-DC Power Supply

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is suitable for various AC/DC power conversion for system miniaturization and higher efficiency.





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FCH170N60	Unit
V_{DSS}	Drain to Source Voltage		600	V
V_{GSS}	Gate to Source Voltage	- DC	±20	V
		- AC	±30	
I_D	Drain Current	- Continuous (T_C = 25°C)	22	A
		- Continuous (T_C = 100°C)	14	
I_{DM}	Drain Current	- Pulsed (Note 1)	66	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		525	mJ
I_{AR}	Avalanche Current (Note 1)		5	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		2.27	mJ
dv/dt	MOSFET dv/dt (Note 3)		100	V/ns
	Peak Diode Recovery dv/dt		20	
P_D	Power Dissipation	(T_C = 25°C)	227	W
		- Derate above 25°C	1.82	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FCH170N60	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.55	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCH170N60	FCH170N60	TO-247	-	-	30

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 10 mA, V_{GS} = 0 V, T_J = 25°C	600	-	-	V
		I_D = 10 mA, V_{GS} = 0 V, T_J = 150°C	650	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, Referenced to 25°C	-	0.67	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V	-	-	1	μA
		V_{DS} = 480 V, V_{GS} = 0 V, T_C = 125°C	-	1.2	-	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, I_D = 250 μA	2.5	-	3.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 11 A	-	150	170	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 11 A	-	17	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 380 V, V_{GS} = 0 V f = 1 MHz	-	2150	2860	pF
C_{oss}	Output Capacitance		-	60	80	pF
C_{rss}	Reverse Transfer Capacitance		-	2.65	-	pF
$C_{oss\ (eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	-	190	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 380 V, I_D = 11 A, V_{GS} = 10 V (Note 4)	-	42	55	nC
Q_{gs}	Gate to Source Gate Charge		-	9	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	11	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	0.95	-	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 380 V, I_D = 11 A, V_{GS} = 10 V, R_g = 4.7 Ω (Note 4)	-	21	50	ns
t_r	Turn-On Rise Time		-	12	35	ns
$t_{d(off)}$	Turn-Off Delay Time		-	55	120	ns
t_f	Turn-Off Fall Time		-	3.8	18	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	22	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	66	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 11 A	-	-	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 11 A, dI_F/dt = 100 A/μs	-	346	-	ns
Q_{rr}	Reverse Recovery Charge		-	6.2	-	μC

Notes:

1. Repetitive rating: pulse width limited by maximum junction temperature
2. I_{AS} = 5 A, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 11 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 380 V, Starting T_J = 25°C
4. Essentially independent of operating temperature typical characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

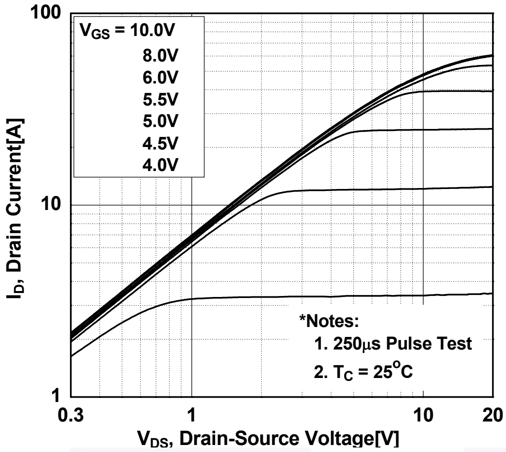


Figure 2. Transfer Characteristics

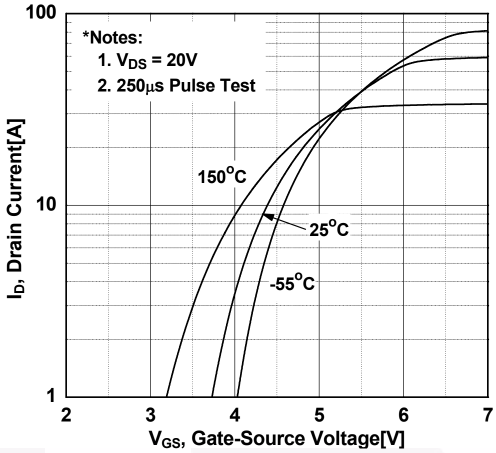


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

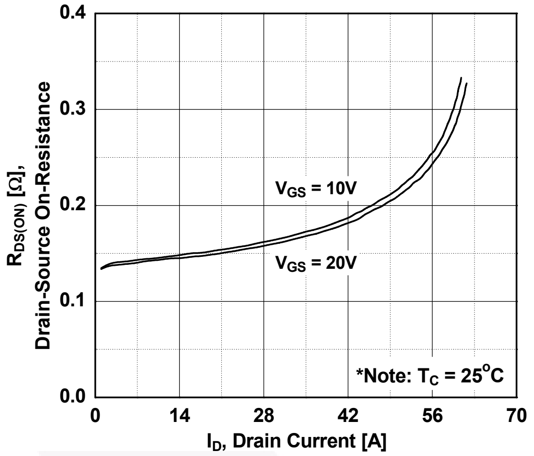


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

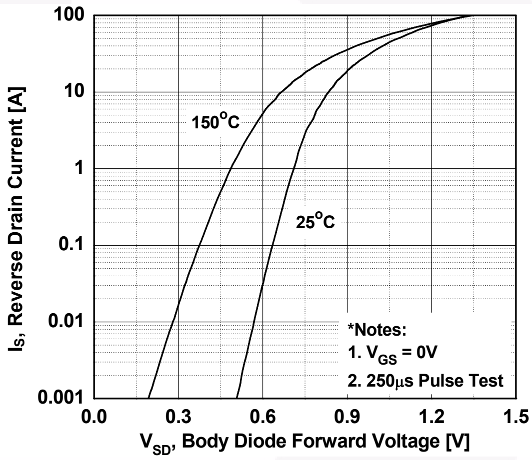


Figure 5. Capacitance Characteristics

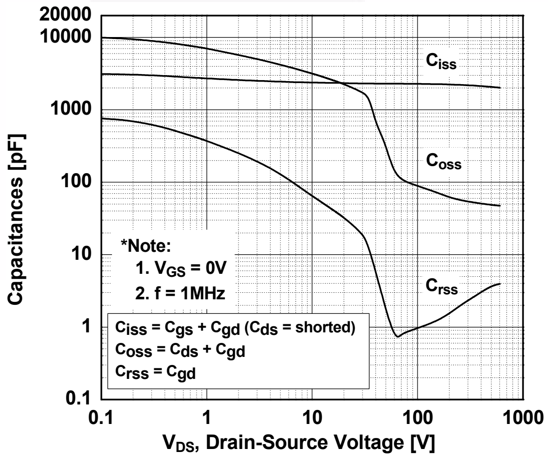
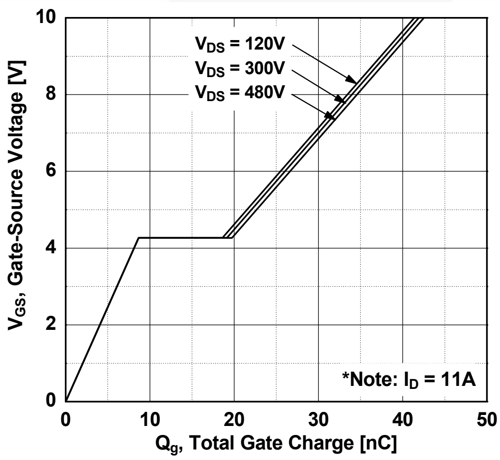


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

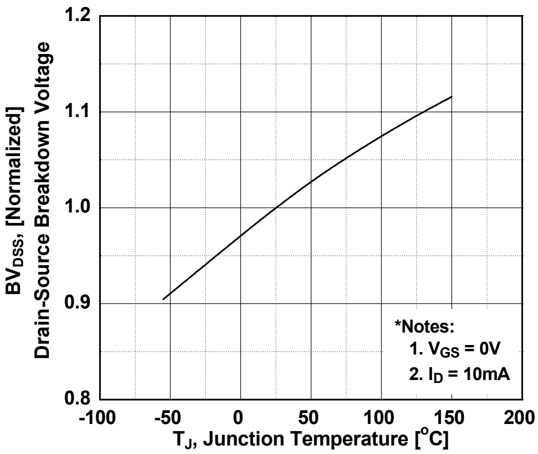


Figure 8. On-Resistance Variation vs. Temperature

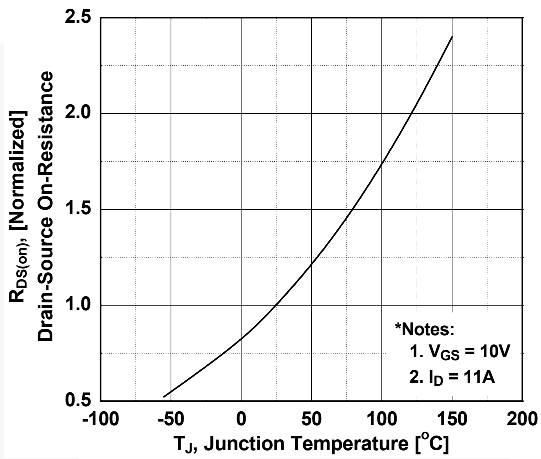


Figure 9. Maximum Safe Operating Area

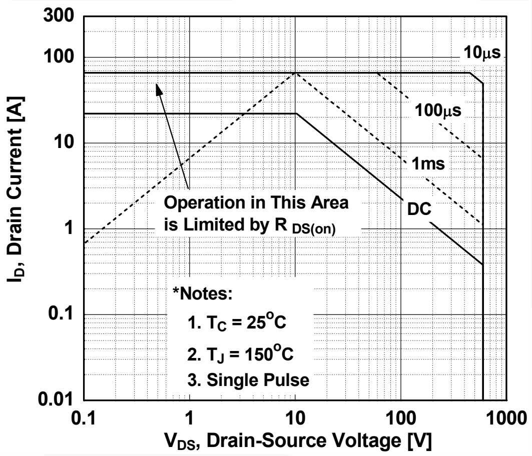


Figure 10. Maximum Drain Current vs. Case Temperature

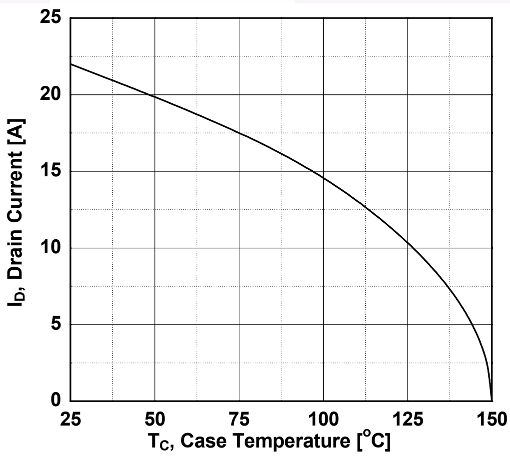
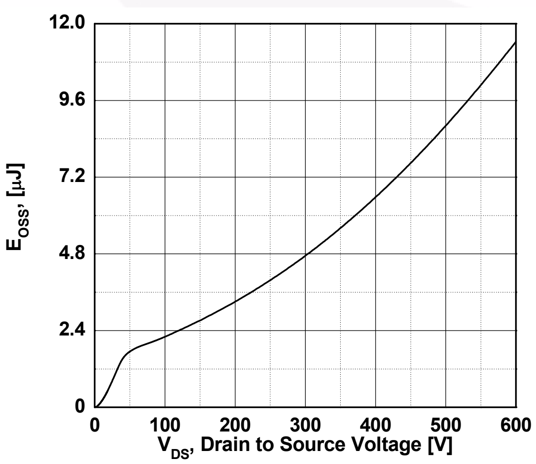
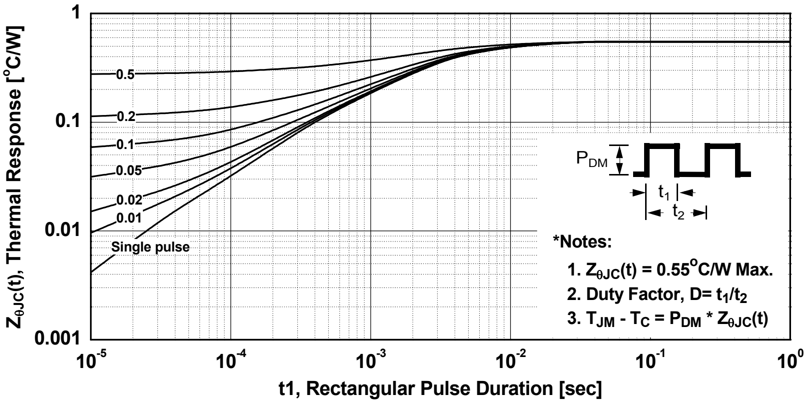


Figure 11. Eoss vs. Drain to Source Voltage



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



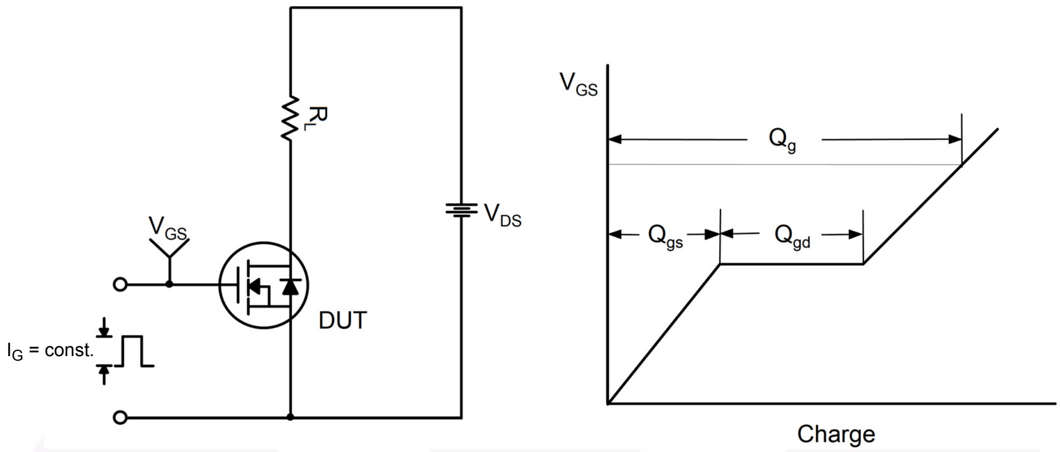


Figure 13. Gate Charge Test Circuit & Waveform

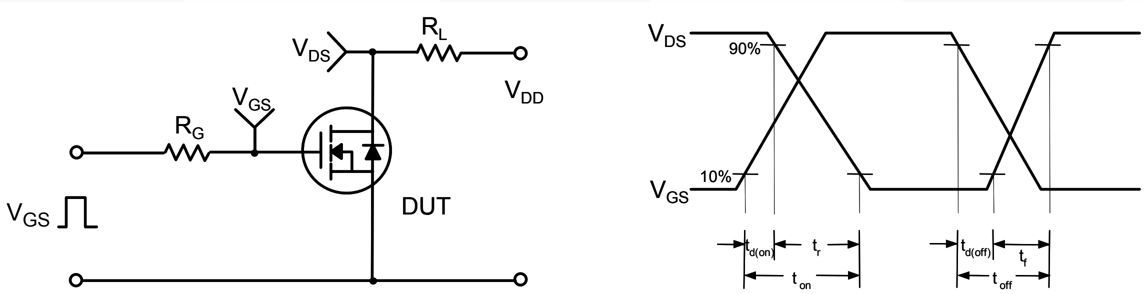


Figure 14. Resistive Switching Test Circuit & Waveforms

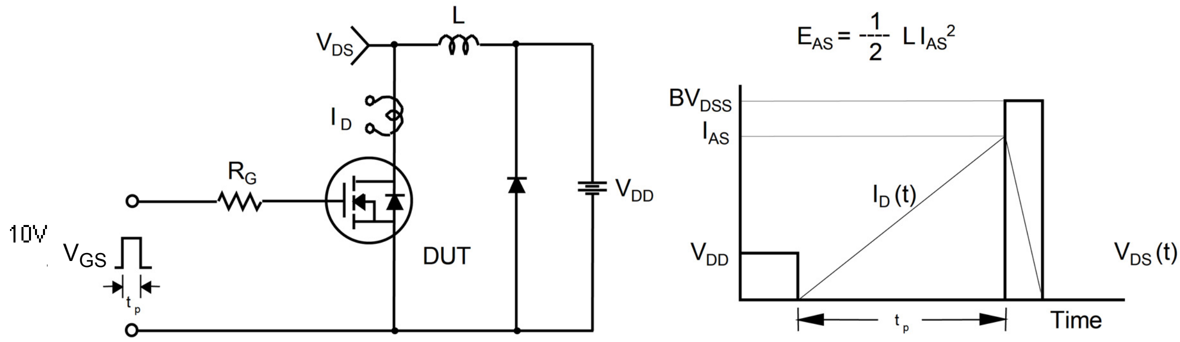


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

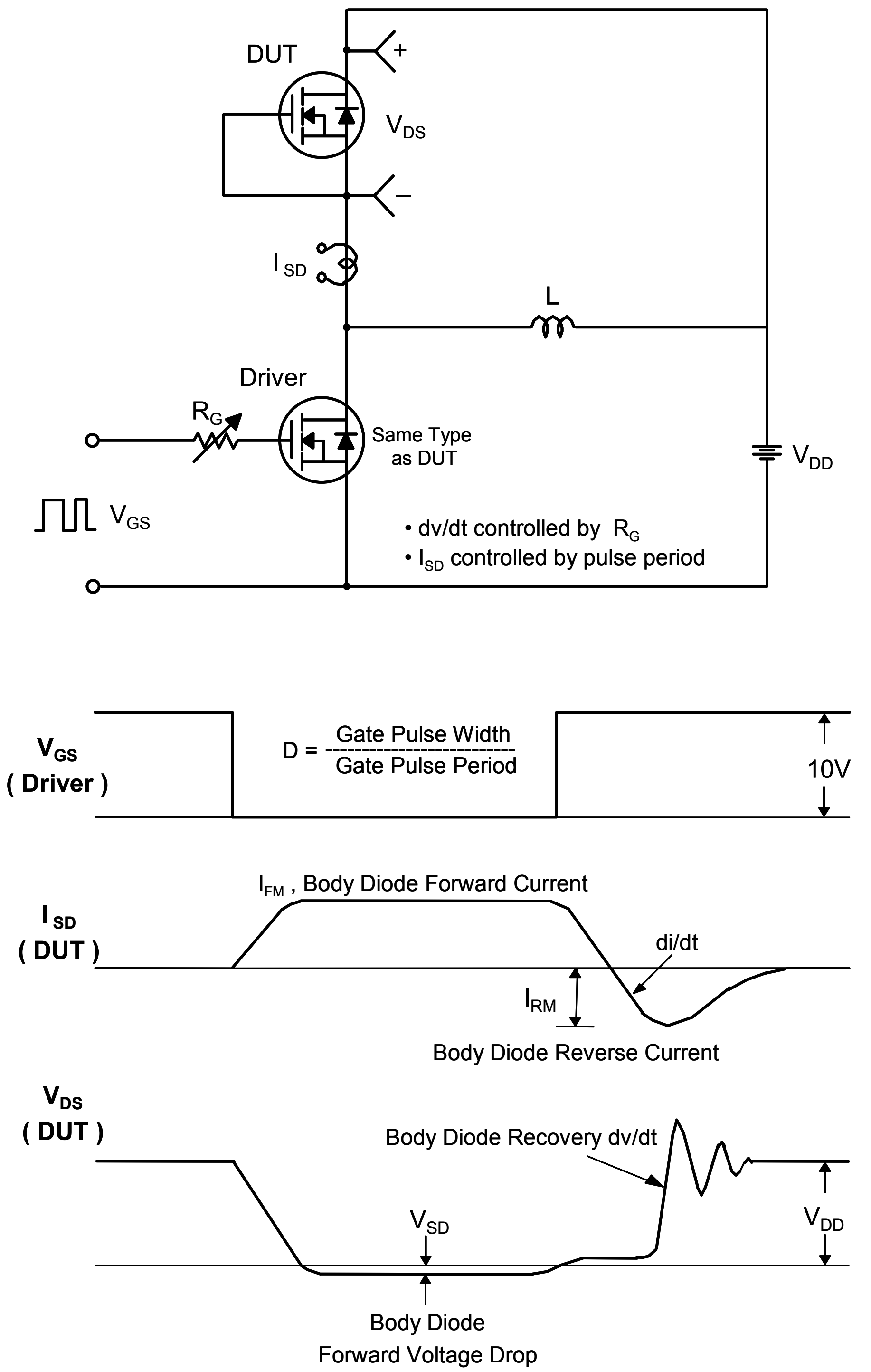


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

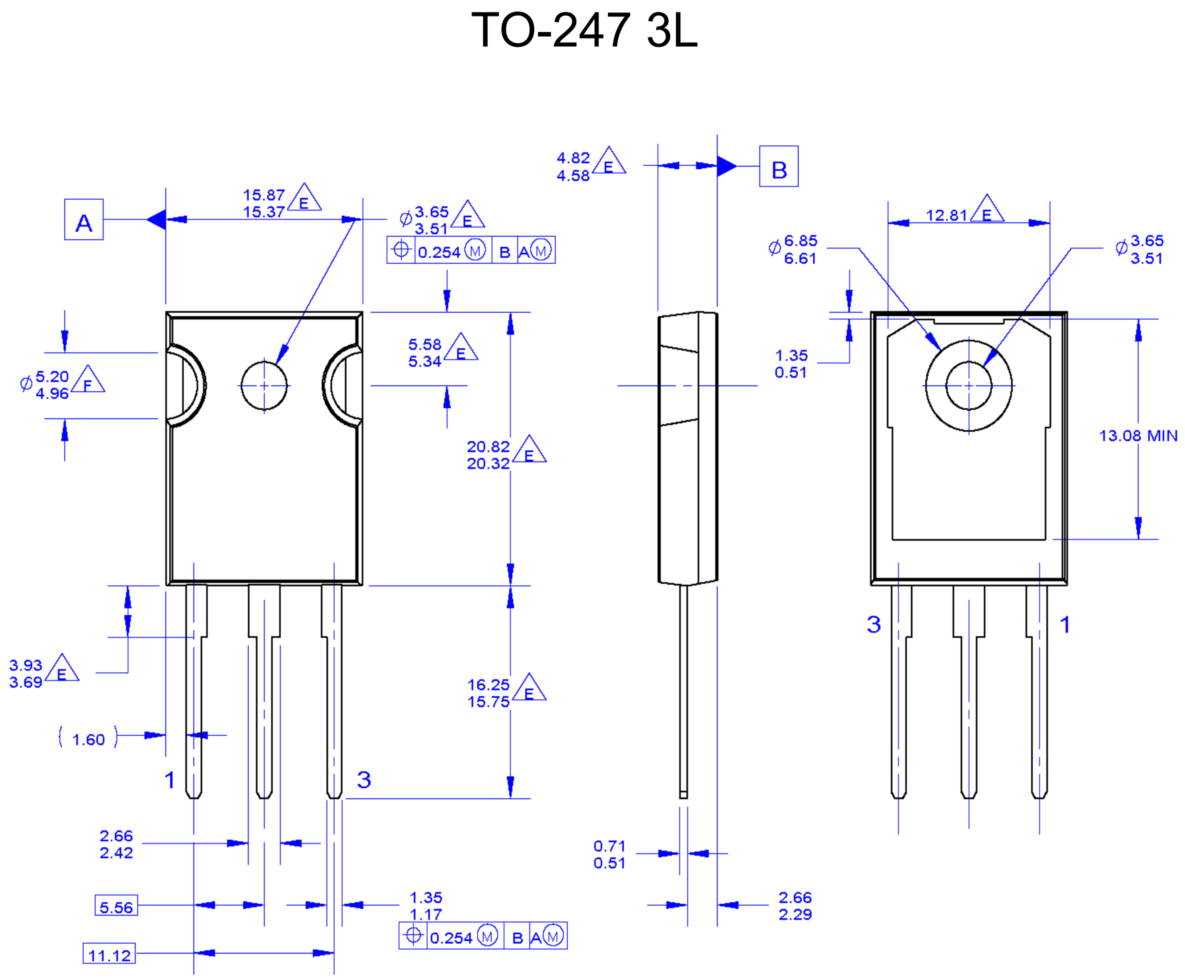


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Figure 17. TO-247,Molded, 3 Lead, Jedec Variation AB

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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