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November 2013

FQP34N20

N-Channel QFET[®] MOSFET 200 V, 31 A, 75 m Ω

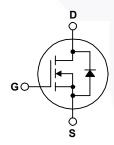
Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 31 A, 200 V, $R_{DS(on)}$ = 75 m Ω (Max.) @ V_{GS} = 10 V, I_D = 15.5 A
- Low Gate Charge (Typ. 60 nC)
- Low Crss (Typ. 55 pF)
- · 100% Avalanche Tested





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter	FQP34N20	Unit	
V_{DSS}	Drain-Source Voltage		200	V
I _D	Drain Current - Continuous (T _C = 25°C) - Continuous (T _C = 100°C)		31	А
			20	А
I _{DM}	Drain Current - Pulsed	(Note 1)	124	Α
V _{GSS}	Gate-Source Voltage		± 30	V
E _{AS}	Single Pulsed Avalanche Energy	(Note 2)	640	mJ
I _{AR}	Avalanche Current	(Note 1)	31	Α
E _{AR}	Repetitive Avalanche Energy	(Note 1)	18	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		5.5	V/ns
P_{D}	Power Dissipation (T _C = 25°C)	180	W	
	- Derate above 25°C	1.43	W/°C	
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T _L	Maximum Lead Temperature for Solderin 1/8" from Case for 5 seconds	300	°C	

Thermal Characteristics

Symbol	Parameter	FQP34N20	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.7	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	°C/W

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP34N20	FQP34N20	TO-220	Tube	N/A	N/A	50 units

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Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Off Cha	aracteristics					
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	200			V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		0.2		V/°C
I _{DSS}	Zara Oata Vallana Busin Ourset	V _{DS} = 200 V, V _{GS} = 0 V			1	μΑ
	Zero Gate Voltage Drain Current	V _{DS} = 160 V, T _C = 125°C			10	μА
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
On Cha	aracteristics					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	3.0		5.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 15.5 A		0.06	0.075	Ω
9 _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 15.5 A		25		S
C _{iss}	Input Capacitance Output Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz		2400 430	3100 560	pF pF
	·	7 50				
C _{rss}	Reverse Transfer Capacitance	1.00 mm/2		55	70	pF
Cwitchi	ing Characteristics					
t _{d(on)}	ing Characteristics Turn-On Delay Time			40	90	ns
t _r	Turn-On Rise Time	$V_{DD} = 100 \text{ V}, I_D = 34 \text{ A},$		280	570	ns
	Turn-Off Delay Time	$R_G = 25 \Omega$		125	260	ns
t _{d(off)}	Turn-Off Fall Time	1		115	240	ns
Q _g	Total Gate Charge	V _{DS} = 160 V, I _D = 34 A,		60	78	nC
Q _{gs}	Gate-Source Charge	$V_{DS} = 160 \text{ V}, I_D = 34 \text{ A},$ $V_{GS} = 10 \text{ V}$	//	17		nC
Q _{gd}	Gate-Drain Charge	VGS - 10 V		27		nC
gu						
Drain-S	Source Diode Characteristics a	nd Maximum Ratings				
I _S	Maximum Continuous Drain-Source Diode Forward Current				31	Α
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current				124	Α
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 31 A			1.5	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 34 A,		150		ns
Q _{rr}	Reverse Recovery Charge	dl _F / dt = 100 A/μs		0.95		μС

- **Notes:** 1. Repetitive Rating : Pulse width limited by maximum junction temperature. 2. L = 1.0 mH, I $_{AS}$ = 31 A, V $_{DD}$ = 50 V, R $_{G}$ = 25 Ω , starting T $_{J}$ = 25°C. 3. I $_{SD}$ ≤ 34 A, di/dt ≤ 300 A/ $_{IS}$, V $_{DD}$ ≤ BV $_{DSS}$, starting T $_{J}$ = 25°C. 4. Essentially independent of operating temperature.

Typical Characteristics

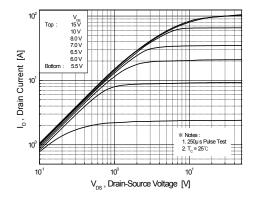
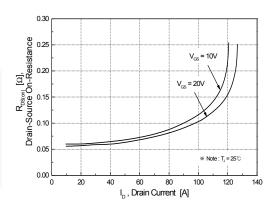


Figure 1. On-Region Characteristics





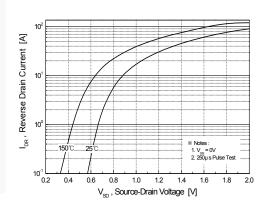
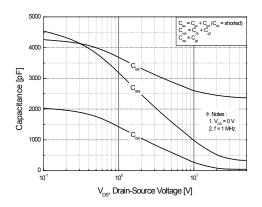


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature



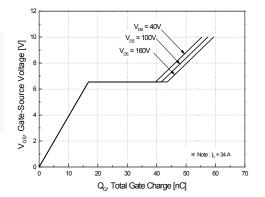
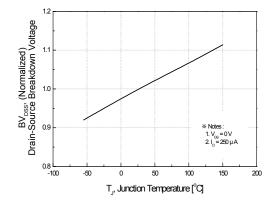


Figure 5. Capacitance Characteristics

Figure 6. Gate Charge Characteristics

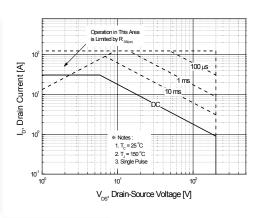
Typical Characteristics (continued)



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Figure 7. Breakdown Voltage Variation vs. Temperature

Figure 8. On-Resistance Variation vs. Temperature



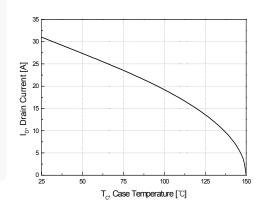


Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs. Case Temperature

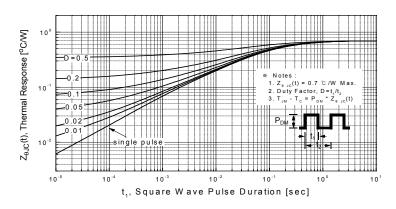


Figure 11. Transient Thermal Response Curve

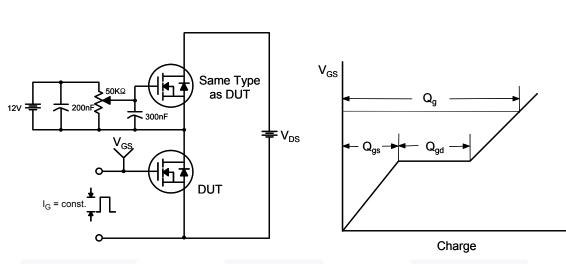


Figure 12. Gate Charge Test Circuit & Waveform

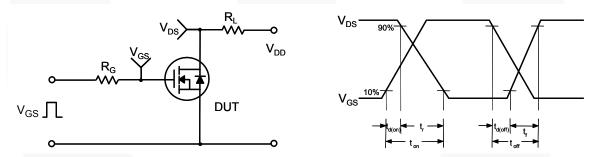


Figure 13. Resistive Switching Test Circuit & Waveforms

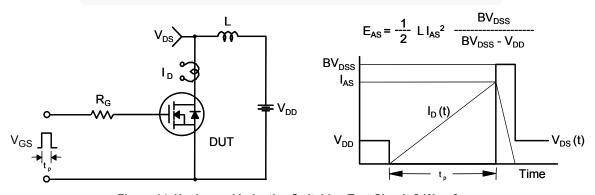
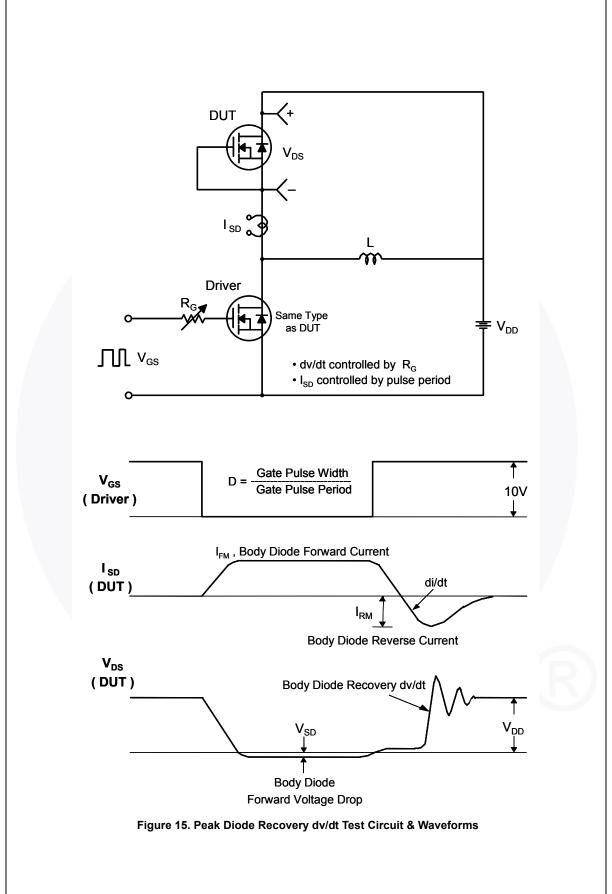
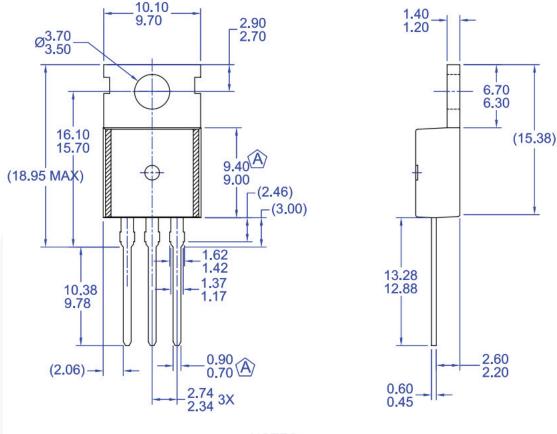


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Mechanical Dimensions



4.70 10.20 9.80

NOTES:

- (A) CONFORMS TO JEDEC TO-220 VARIATION AB EXCEPT WHERE NOTED
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D) DRAWING FILE/REVISION: MKT-TO220Y03REV1

Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB

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