LM4929 Boomer™ Audio Power Amplifier Series Stereo 40mW Low Noise Headphone Amplifier with OCL Output

Check for Samples: LM4929

FEATURES

- **OCL outputs — No DC Blocking Capacitors**
- **External Gain-Setting Capability**
- **Available in Space-Saving VSSOP Package**
- **Ultra Low Current Shutdown Mode**
- **2V - 5.5V Operation**
- **Ultra Low Noise**

APPLICATIONS

- **Portable CD players**
- **PDAs**
- **Portable Electronics Devices**

KEY SPECIFICATIONS

- **PSRR at 217Hz and 1kHz**
- **Output Power at 1kHz with V_{DD} = 2.4V, 1% THD+N into a 16Ω load, 65dB (Typ)**
- **Output Power at 1kHz with V_{DD} = 3V, 1% THD+N into a 16Ω load, 25 mW (Typ)**
- **Shutdown current, 40 mW (Typ), 2.0µA (Max)**
- **Output Voltage change on release from Shutdown V_{DD} = 2.4V, R_L = 16Ω, 1mV (Max)**

DESCRIPTION

The LM4929 is an stereo audio power amplifier capable of delivering 40mW per channel of continuous average power into a 16Ω load or 25mW per channel into a 32Ω load at 1% THD+N from a 3V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. Since the LM4929 does not require bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems. The LM4929 is configured for OCL (Output Capacitor-Less) outputs, operating with no DC blocking capacitors on the outputs.

The LM4929 features a low-power consumption shutdown mode with a faster turn on time. Additionally, the LM4929 features an internal thermal shutdown protection mechanism.

The LM4929 is unity gain stable and may be configured with external gain-setting resistors.

Block Diagram

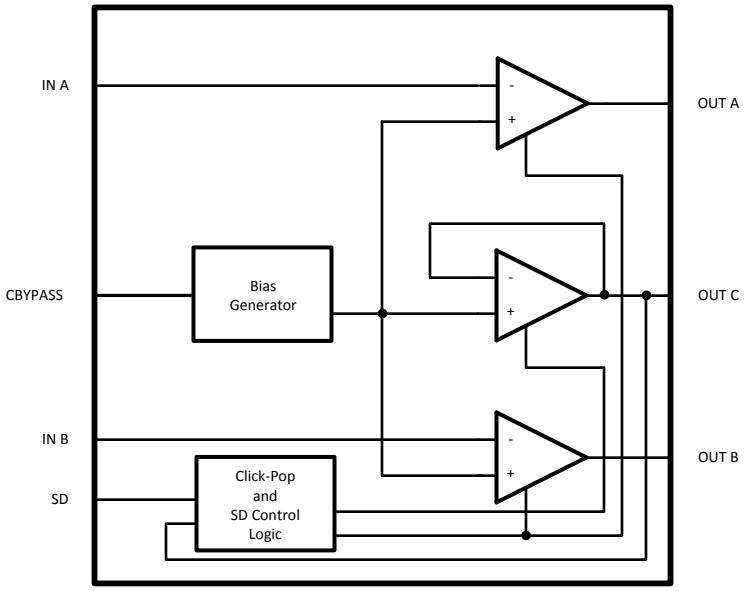


Figure 1. Block Diagram

Typical Application

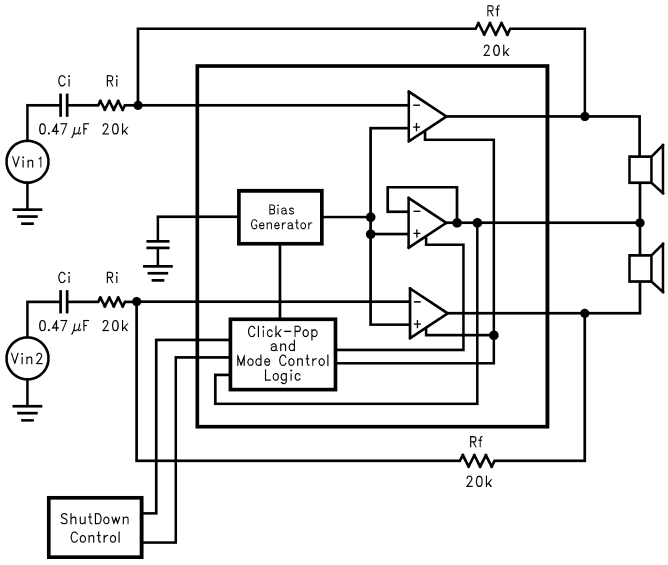


Figure 2. Typical OCL Output Configuration Circuit

Connection Diagram

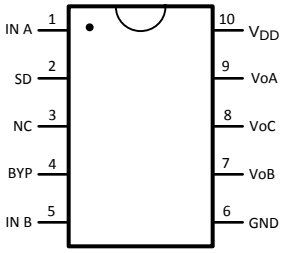


Figure 3. VSSOP Package
Top View
See NS Package Number DGS

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

Supply Voltage		6.0V
Storage Temperature		−65°C to +150°C
Input Voltage(4)		-0.3V to V_{DD} + 0.3V
Power Dissipation(5)		Internally Limited
ESD Susceptibility(6)		2000V
ESD Susceptibility(7)		200V
Junction Temperature		150°C
Thermal Resistance	θ_{JC} (VSSOP)	56°C/W
	θ_{JA} (VSSOP)	190°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Datasheet min/max specification limits are ensured by design, test, or statistical analysis.
(4) 10Ω Terminated input.
(5) The maximum power dissipation must be derated at elevated temperatures and is dictated by TJMAX, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/ \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4929, see power derating currents for more information.
(6) Human body model, 100pF discharged through a 1.5kΩ resistor.
(7) Machine Model, 220pF-240pF discharged through all pins.

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le 85°C$
Supply Voltage		$2V \le V_{DD} \le 5.5V$

Electrical Characteristics V_{DD} = 5V(1)(2)

The following specifications apply for V_{DD} = 5V, R_L = 16Ω, and C_B = 4.7µF unless otherwise specified. Limits apply to T_A = 25°C. Pin 3 connected to GND(3).

Symbol	Parameter	Conditions	LM4929		Units (Limits)
			Typ(4)	Limit(5)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A	2	5	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = GND	0.1	2.0	µA(max)
V_{SDIH}	Shutdown Voltage Input High		1.8		V
V_{SDIL}	Shutdown Voltage Input Low		0.4		V
P_O	Output Power	THD = 1%; f = 1 kHZ			mW
		R_L= 16Ω	80		
		R_L = 32Ω	80		
V_{NO}	Output Noise Voltage	BW = 20Hz to 20kHz, A-weighted	10		µV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV sine p-p	65		dB

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Pin 3 (NC) should be connected to GND for proper part operation.
(4) Typicals are measured at 25°C and represent the parametric norm.
(5) Limits are specified to Texas Instruments' AOQL (Average Outgoing Quality Level).

Electrical Characteristics V_{DD} = 3.0V(1)(2)

The following specifications apply for V_{DD} = 3.0V, R_L = 16Ω, and C_B = 4.7µF unless otherwise specified. Limits apply to T_A = 25°C. Pin 3 connected to GND(3).

Symbol	Parameter	Conditions	LM4929		Units (Limits)
			Typ(4)	Limit(5)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A	1.5	3.5	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = GND	0.1	2.0	µA(max)
P_O	Output Power	THD = 1%; f = 1kHz			mW
		R = 16Ω	40		
		R = 32Ω	25		
V_{NO}	Output Noise Voltage	BW = 20 Hz to 20kHz, A-weighted	10		µV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV sine p-p	65		dB

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Pin 3 (NC) should be connected to GND for proper part operation.
(4) Typicals are measured at 25°C and represent the parametric norm.
(5) Limits are specified to Texas Instruments' AOQL (Average Outgoing Quality Level).

Electrical Characteristics V_{DD} = 2.4V(1)(2)

The following specifications apply for V_{DD} = 2.4V, R_L = 16Ω, and C_B = 4.7µF unless otherwise specified. Limits apply to T_A = 25°C. Pin 3 connected to GND(3).

Symbol	Parameter	Conditions	LM4929		Units (Limits)
			Typ(4)	Limit(5)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A	1.5	3	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = GND	0.1	2.0	µA(max)
P_O	Output Power	THD = 1%; f = 1kHz			mW
		R = 16Ω	25		
		R = 32Ω	12		
V_{NO}	Output Noise Voltage	BW = 20 Hz to 20kHz, A-weighted	10		µV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV sine p-p	65		dB
T_{WU}	Wake Up Time from Shutdown	OCL	0.5		s

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Pin 3 (NC) should be connected to GND for proper part operation.
(4) Typicals are measured at 25°C and represent the parametric norm.
(5) Limits are specified to Texas Instruments' AOQL (Average Outgoing Quality Level).

External Components Description

See Figure 2

Components		Functional Description
1.	R_I	Inverting input resistance which sets the closed-loop gain in conjunction with R_f. This resistor also forms a high-pass filter with C_i at $f_c = 1/(2\pi R_i C_i)$.
2.	C_I	Input coupling capacitor which blocks the DC voltage at the amplifier's input terminals. Also creates a high-pass filter with R_i at $f_c = 1/(2\pi R_i C_i)$. Refer to the section PROPER SELECTION OF EXTERNAL COMPONENTS for an explanation of how to determine the value of C_i.
3.	R_f	Feedback resistance which sets the closed-loop gain in conjunction with R_i.
4.	C_S	Supply bypass capacitor which provides power supply filtering. Refer to the POWER SUPPLY BYPASSING section for information concerning proper placement and selection of the supply bypass capacitor.
5.	C_B	Bypass pin capacitor which provides half-supply filtering. Refer to the section, PROPER SELECTION OF EXTERNAL COMPONENTS, for information concerning proper placement and selection of C_B

Typical Performance Characteristics

THD+N vs Frequency

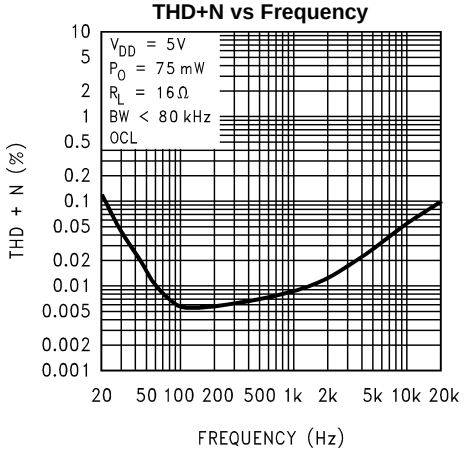


Figure 4.

THD+N vs Frequency

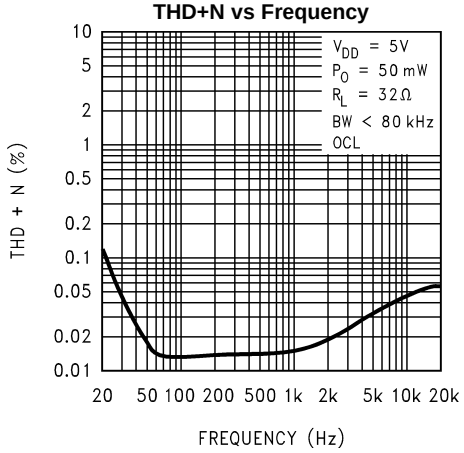


Figure 5.

THD+N vs Frequency

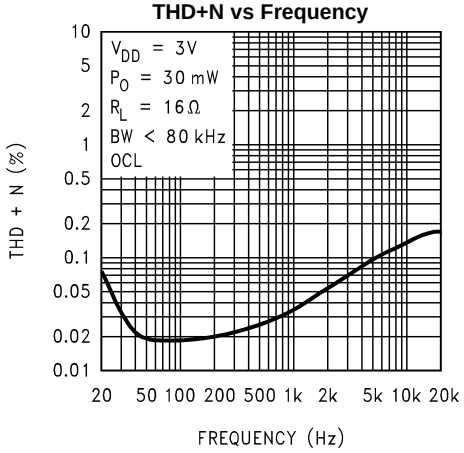


Figure 6.

THD+N vs Frequency

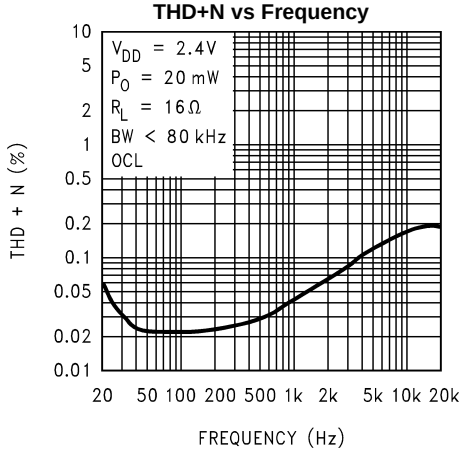


Figure 7.

THD+N vs Frequency

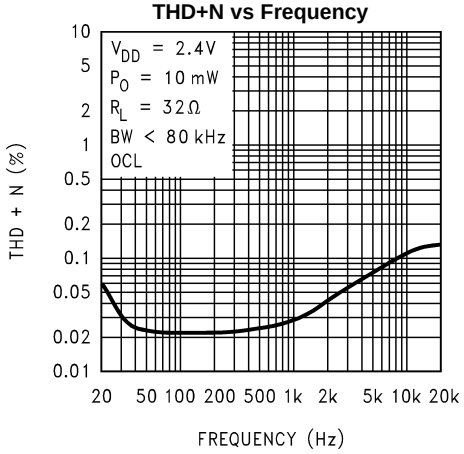


Figure 8.

THD+N vs Frequency

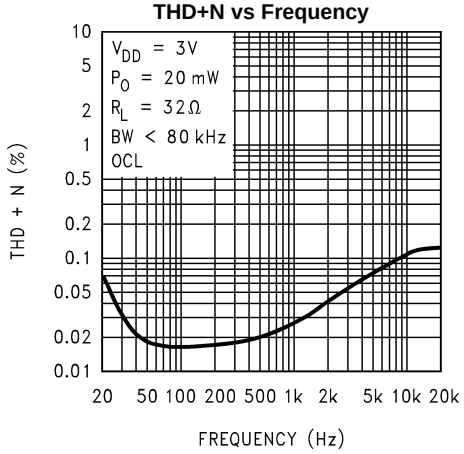


Figure 9.

Typical Performance Characteristics (continued)

THD+N vs Output Power

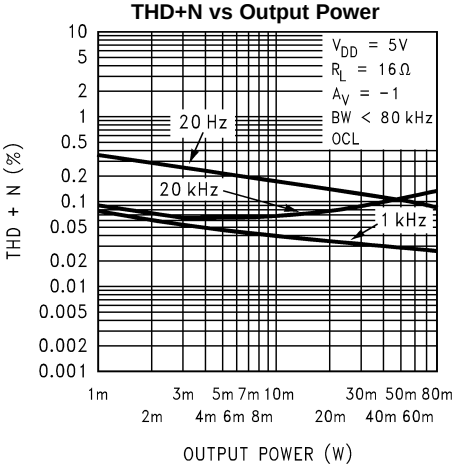


Figure 10.

THD+N vs Output Power

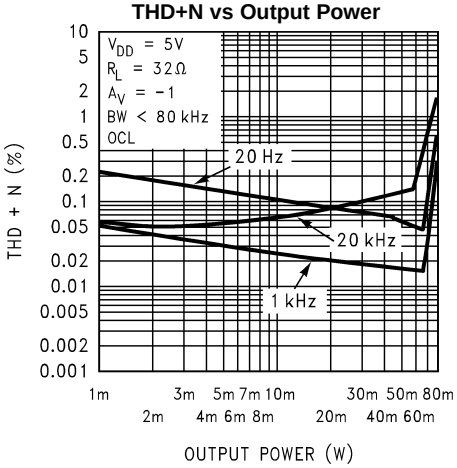


Figure 11.

Output Power vs Load Resistance

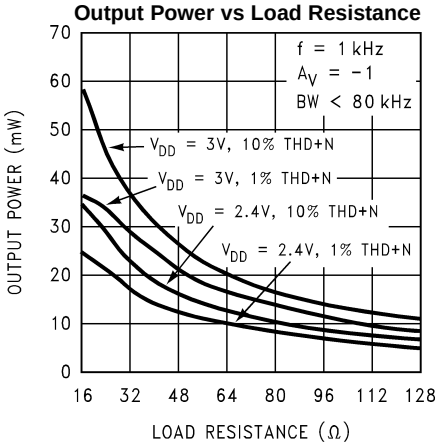


Figure 12.

Output Power vs Supply Voltage

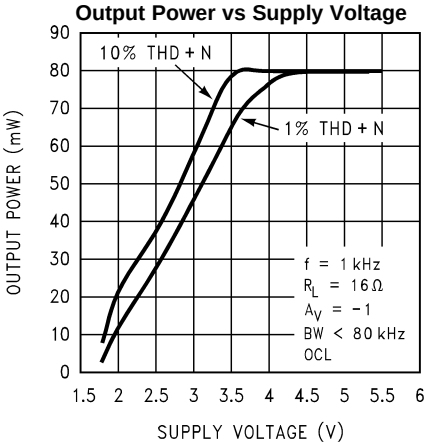


Figure 13.

Output Power vs Supply Voltage

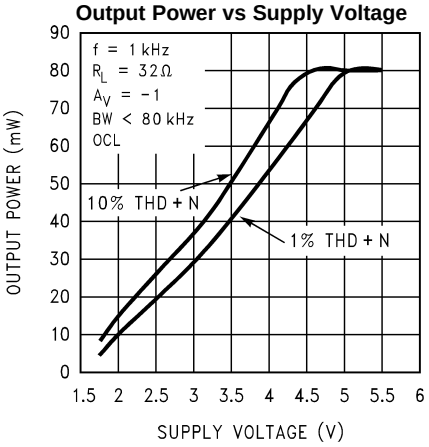


Figure 14.

Output Power vs Load Resistance

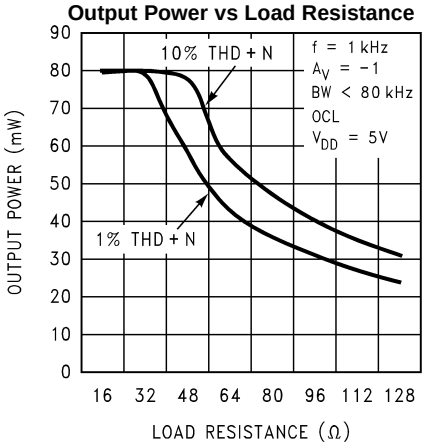


Figure 15.

Typical Performance Characteristics (continued)

Power Supply Rejection Ratio

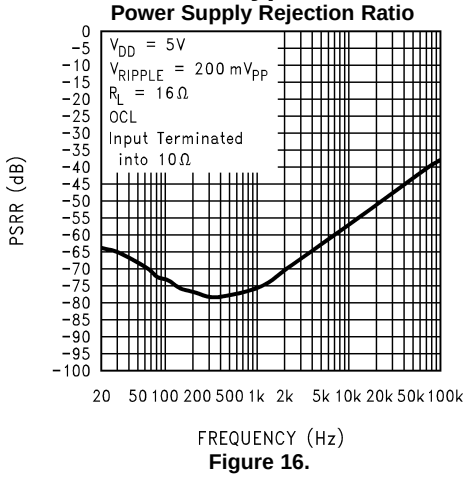


Figure 16.

Power Supply Rejection Ratio

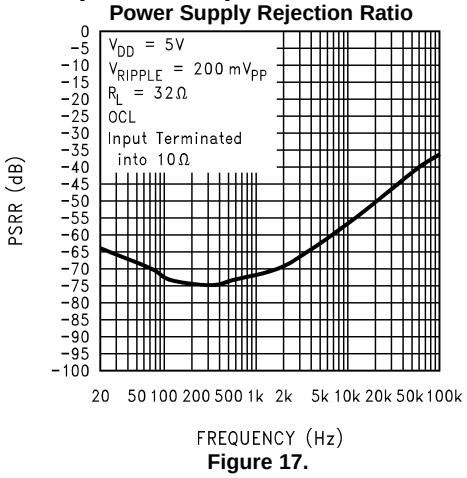


Figure 17.

Frequency Response vs Input Capacitor Size

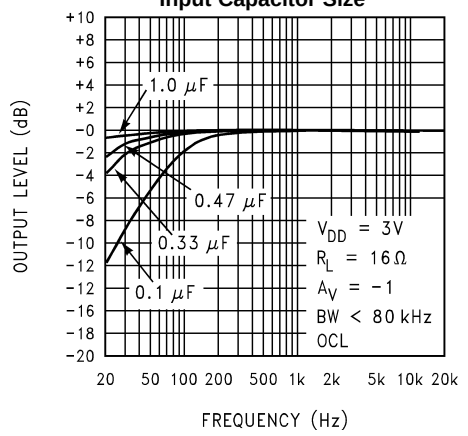


Figure 18.

Open Loop Frequency Response

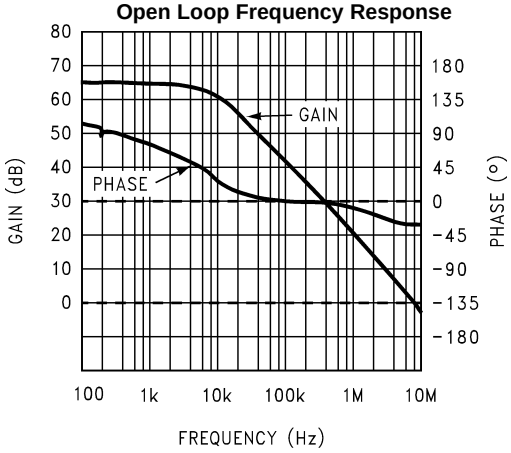


Figure 19.

Supply Voltage vs Supply Current

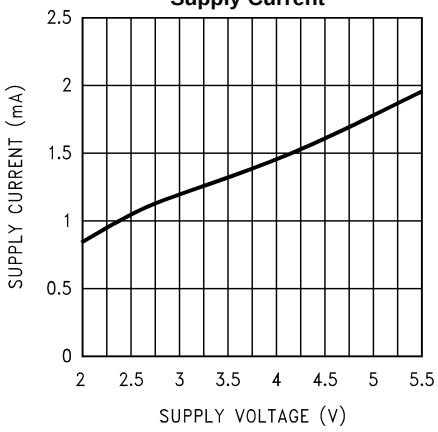


Figure 20.

Clipping Voltage vs Supply Voltage

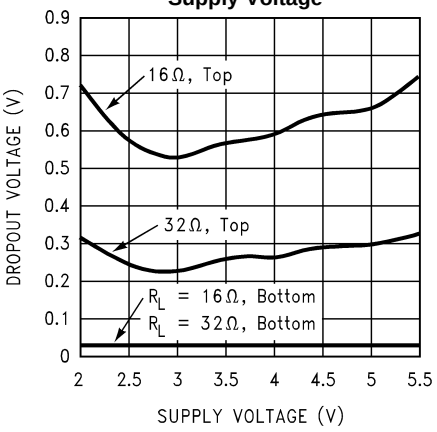


Figure 21.

Typical Performance Characteristics (continued)

Shutdown Hysteresis Voltage, V_{DD} = 5V

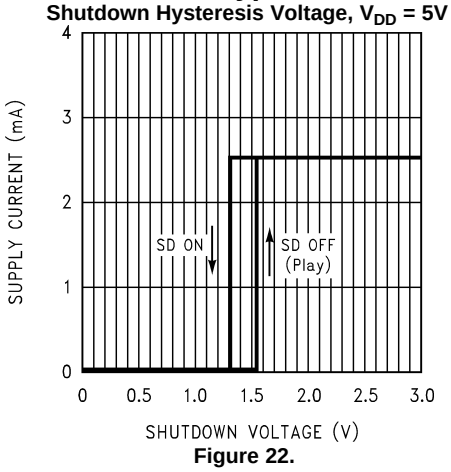


Figure 22.

Shutdown Hysteresis Voltage, V_{DD} = 3V

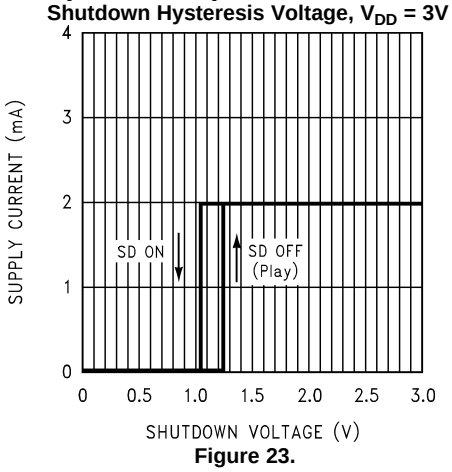


Figure 23.

Power Dissipation vs Output Power
V_{DD} = 5V

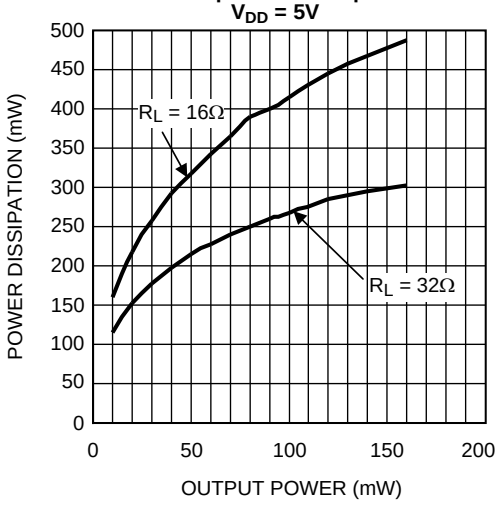


Figure 24.

Power Dissipation vs Output Power
V_{DD} = 3V

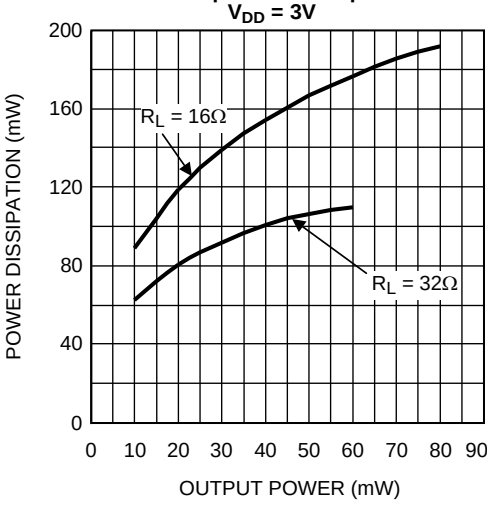


Figure 25.

Power Dissipation vs Output Power
V_{DD} = 2.4V

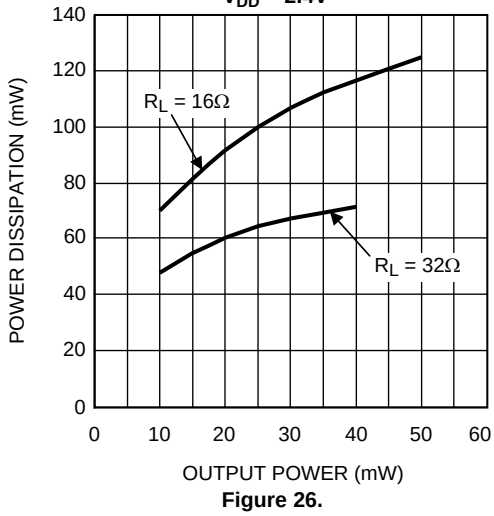


Figure 26.

THD+N vs Output Power
V_{DD} = 3V, R_L = 32Ω

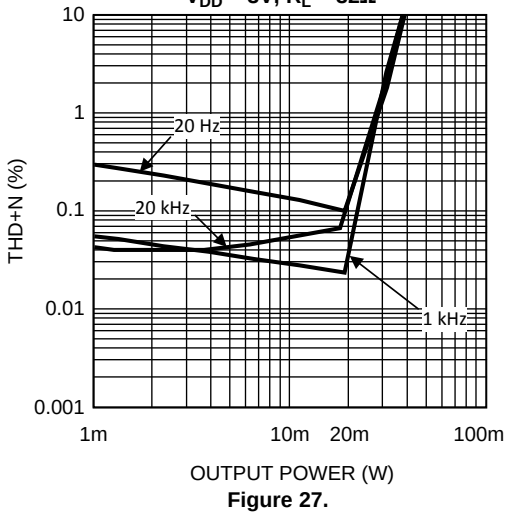


Figure 27.

Typical Performance Characteristics (continued)

THD+N vs Output Power
V_{DD} = 2.4V, R_L = 32Ω

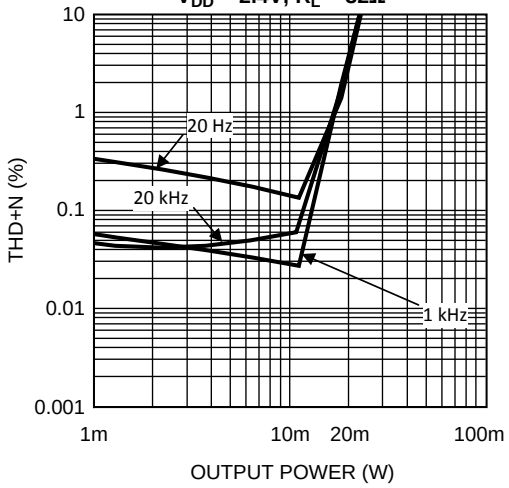


Figure 28.

THD+N vs Output Power
V_{DD} = 3V, R_L = 16Ω

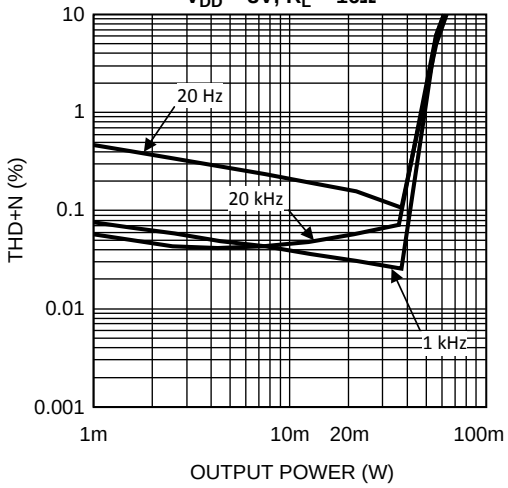


Figure 29.

THD+N vs Output Power
V_{DD} = 2.4V, R_L = 16Ω

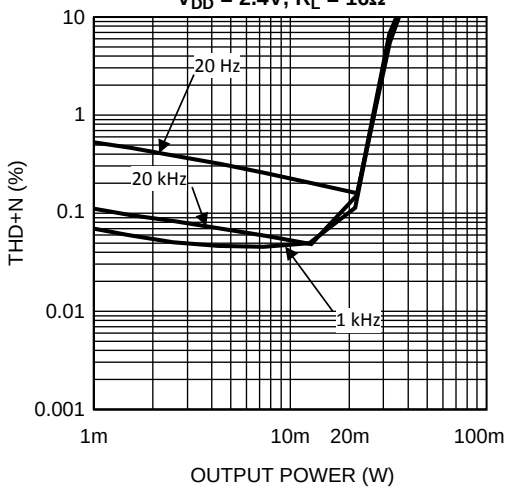


Figure 30.

Power Derating Curve

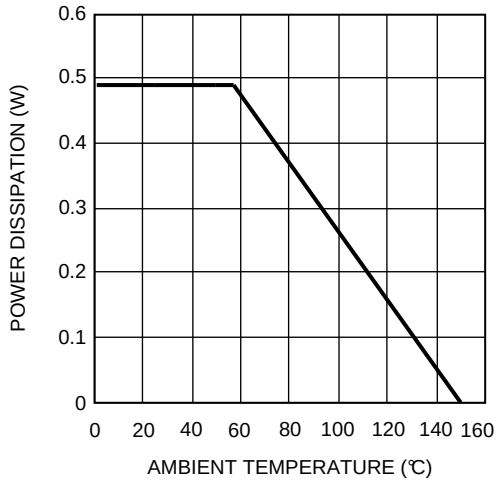


Figure 31.

APPLICATION INFORMATION

AMPLIFIER CONFIGURATION EXPLANATION

As shown in Figure 1, the LM4929 has three operational amplifiers internally. Two of the amplifier's have externally configurable gain while the other amplifier is internally fixed at the bias point acting as a unity-gain buffer. The closed-loop gain of the two configurable amplifiers is set by selecting the ratio of R_f to R_i. Consequently, the gain for each channel of the IC is

$$A_{VD} = -(R_f / R_i) \quad (1)$$

By driving the loads through outputs V_oA and V_oB with V_oC acting as a buffered bias voltage the LM4929 does not require output coupling capacitors. The classical single-ended amplifier configuration where one side of the load is connected to ground requires large, expensive output coupling capacitors.

A configuration such as the one used in the LM4929 has a major advantage over single supply, single-ended amplifiers. Since the outputs V_oA, V_oB, and V_oC are all biased at 1/2 V_{DD}, no net DC voltage exists across each load. This eliminates the need for output coupling capacitors which are required in a single-supply, single-ended amplifier configuration. Without output coupling capacitors in a typical single-supply, single-ended amplifier, the bias voltage is placed across the load resulting in both increased internal IC power dissipation and possible loudspeaker damage.

The LM4929 eliminates these output coupling capacitors by running in OCL mode. Unless shorted to ground, VoC is internally configured to apply a 1/2 V_{DD} bias voltage to a stereo headphone jack's sleeve. This voltage matches the bias voltage present on VoA and VoB outputs that drive the headphones. The headphones operate in a manner similar to a bridge-tied load (BTL). Because the same DC voltage is applied to both headphone speaker terminals this results in no net DC current flow through the speaker. AC current flows through a headphone speaker as an audio signal's output amplitude increases on the speaker's terminal.

The headphone jack's sleeve is not connected to circuit ground when used in OCL mode. Using the headphone output jack as a line-level output will place the LM4929's 1/2 V_{DD} bias voltage on a plug's sleeve connection. This presents no difficulty when the external equipment uses capacitively coupled inputs. For the very small minority of equipment that is DC coupled, the LM4929 monitors the current supplied by the amplifier that drives the headphone jack's sleeve. If this current exceeds 500mAPK, the amplifier is shutdown, protecting the LM4929 and the external equipment.

POWER DISSIPATION

Power dissipation is a major concern when using any power amplifier and must be thoroughly understood to ensure a successful design. When operating in capacitor-coupled mode, Equation 2 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \quad (2)$$

Since the LM4929 has three operational amplifiers in one package, the maximum power dissipation increases due to the use of the third amplifier as a buffer and is given in Equation 3:

$$P_{DMAX} = 4(V_{DD})^2 / (2\pi^2 R_L) \quad (3)$$

The maximum power dissipation point obtained from Equation 3 must not be greater than the power dissipation that results from Equation 4:

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} \quad (4)$$

For package DGS, θ_{JA} = 190°C/W. T_{JMAX} = 150°C for the LM4929. Depending on the ambient temperature, T_A, of the system surroundings, Equation 4 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 3 is greater than that of Equation 4, then either the supply voltage must be decreased, the load impedance increased or T_A reduced. For the typical application of a 3V power supply, with a 32Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 144°C provided that device operation is around the maximum power dissipation point. Thus, for typical applications, power dissipation is not an issue. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature may be increased accordingly. Refer to the Typical Performance Characteristics for power dissipation information for lower output powers.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is important for low noise performance and high power supply rejection. The capacitor location on the power supply pins should be as close to the device as possible.

Typical applications employ a 3V regulator with 10mF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM4929. A bypass capacitor value in the range of 0.1µF to 1µF is recommended for C_S.

MICRO POWER SHUTDOWN

The voltage applied to the SHUTDOWN pin controls the LM4929's shutdown function. Activate micro-power shutdown by applying a logic-low voltage to the SHUTDOWN pin. When active, the LM4929's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The trigger point varies depending on supply voltage and is shown in the Shutdown Hysteresis Voltage graphs in the Typical Performance Characteristics section. The low 0.1µA(typ) shutdown current is achieved by applying a voltage that is as near as ground as possible to the SHUTDOWN pin. A voltage that is higher than ground may increase the shutdown current. There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external 100kΩ pull-up resistor between the SHUTDOWN pin and V_{DD}. Connect the switch between the SHUTDOWN pin and ground. Select normal amplifier operation by opening the switch. Closing the switch connects the SHUTDOWN pin to ground, activating micro-power shutdown.

The switch and resistor ensure that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the pull-up resistor.

Shutdown enable/disable times are controlled by a combination of C_B and V_{DD}. Larger values of C_B results in longer turn on/off times from Shutdown. Smaller V_{DD} values also increase turn on/off time for a given value of C_B. Longer shutdown times also improve the LM4929's resistance to click and pop upon entering or returning from shutdown. For a 2.4V supply and C_B = 4.7µF, the LM4929 requires about 2 seconds to enter or return from shutdown. This longer shutdown time enables the LM4929 to have virtually zero pop and click transients upon entering or release from shutdown.

Smaller values of C_B will decrease turn-on time, but at the cost of increased pop and click and reduced PSRR. Since shutdown enable/disable times increase dramatically as supply voltage gets below 2.2V, this reduced turn-on time may be desirable if extreme low supply voltage levels are used as this would offset increases in turn-on time caused by the lower supply voltage. This technique is not recommended for OCL mode since shutdown enable/disable times are very fast (0.5s) independent of supply voltage.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4929 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The LM4929 is unity-gain stable which gives the designer maximum system flexibility. The LM4929 should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than $1V_{rms}$ are available from sources such as audio codecs. Very large values should not be used for the gain-setting resistors. Values for R_i and R_f should be less than 1MΩ. Please refer to the section, AUDIO POWER AMPLIFIER DESIGN, for a more complete explanation of proper gain selection

Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in Figure 2. The input coupling capacitor, C_i, forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response and turn-on time.

SELECTION OF INPUT CAPACITOR SIZE

Amplifying the lowest audio frequencies requires a high value input coupling capacitor, C_i. A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the headphones used in portable systems have little ability to reproduce signals below 60Hz. Applications using headphones with this limited frequency response reap little improvement by using a high value input capacitor.

In addition to system cost and size, turn on time is affected by the size of the input coupling capacitor C_i. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage. This charge comes from the output via the feedback Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on time can be minimized. A small value of C_i (in the range of 0.1µF to 0.39µF), is recommended.

AUDIO POWER AMPLIFIER DESIGN

A 25mW/32Ω AUDIO AMPLIFIER

Given:	
Power Output	25mWrms
Load Impedance	32Ω
Input Level	1Vrms
Input Impedance	20kΩ

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the Typical Performance Characteristics section, the supply rail can be easily found.

3V is a standard voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the LM4929 to reproduce peak in excess of 25mW without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the POWER DISSIPATION section.

Once the power dissipation equations have been addressed, the required gain can be determined from Equation 5.

$$A_V \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (5)$$

From Equation 5, the minimum A_V is 0.89; use A_V = 1. Since the desired input impedance is 20kΩ, and with a A_V gain of 1, a ratio of 1:1 results from Equation 1 for R_f to R_i. The values are chosen with R_i = 20kΩ and R_f = 20kΩ. The final design step is to address the bandwidth requirements which must be stated as a pair of -3dB frequency points. Five times away from a -3dB point is 0.17dB down from passband response which is better than the required ± 0.25dB specified.

f_L = 100Hz/5 = 20Hz

f_H = 20kHz * 5 = 100kHz

As stated in the **External Components** section, R_i in conjunction with C_i creates a

$C_i \geq 1 / (2\pi * 20k\Omega * 20Hz) = 0.397\mu F$; use 0.39µF.

The high frequency pole is determined by the product of the desired frequency pole, f_H, and the differential gain, A_V. With an A_V = 1 and f_H = 100kHz, the resulting GBWP = 100kHz which is much smaller than the LM4929 GBWP of 10MHz. This figure displays that is a designer has a need to design an amplifier with higher differential gain, the LM4929 can still be used without running into bandwidth limitations.

Figure 32 shows an optional resistor connected between the amplifier output that drives the headphone jack sleeve and ground. This resistor provides a ground path that supressed power supply hum. Thishum may occur in applications such as notebook computers in a shutdown condition and connected to an external powered speaker. The resistor's 100Ω value is a suggested starting point. Its final value must be determined based on the tradeoff between the amount of noise suppression that may be needed and minimizing the additional current drawn by the resistor (25mA for a 100Ω resistor and a 5V supply).

ESD PROTECTION

As stated in the Absolute Maximum Ratings, the LM4929 has a maximum ESD susceptibility rating of 2000V. For higher ESD voltages, the addition of a PCDN042 dual transil (from California Micro Devices), as shown in Figure 32, will provide additional protection.

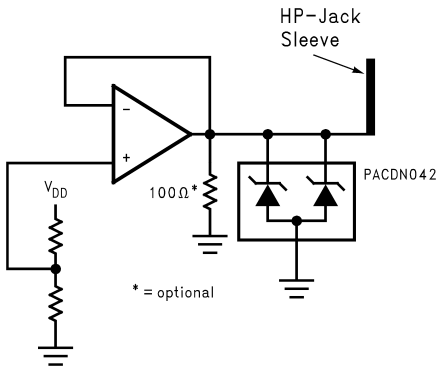


Figure 32. The PCDN042 provides additional ESD protection beyond the 2000V shown in the Absolute Maximum Ratings for the V_OC output

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4929MMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	GB9	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

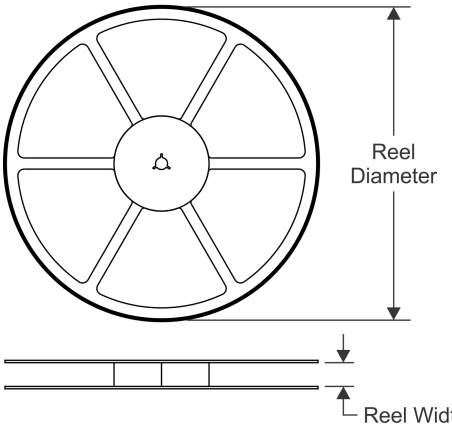
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

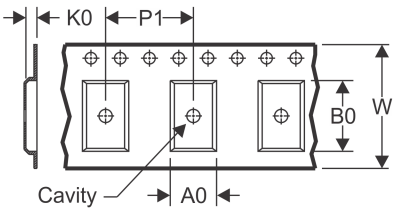
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

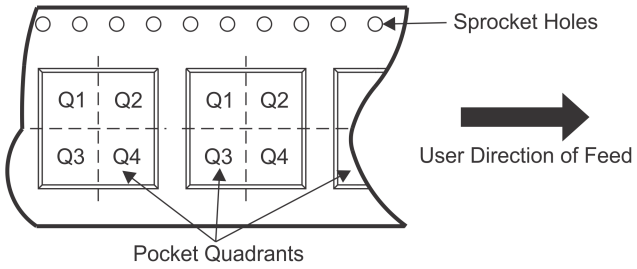


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

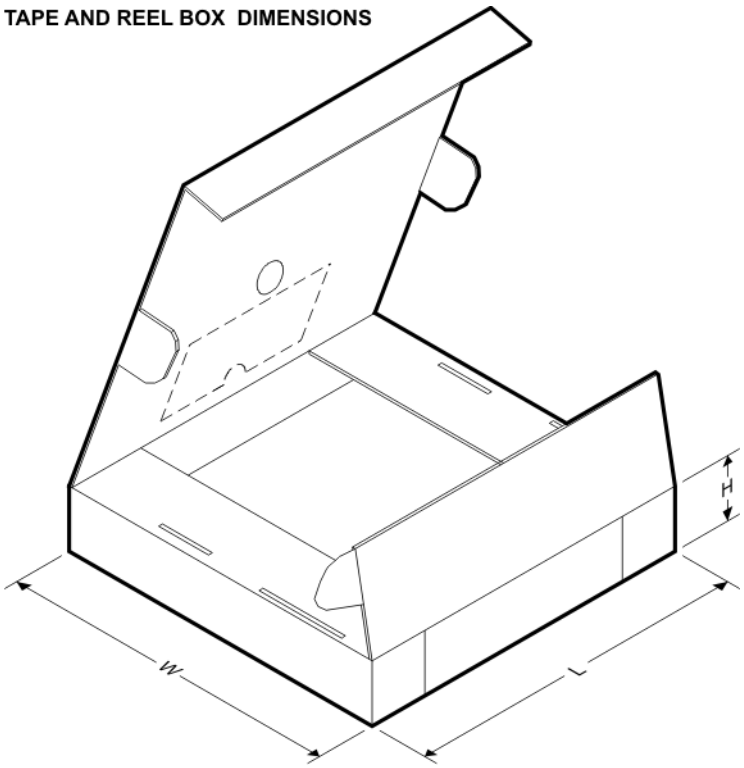
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4929MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

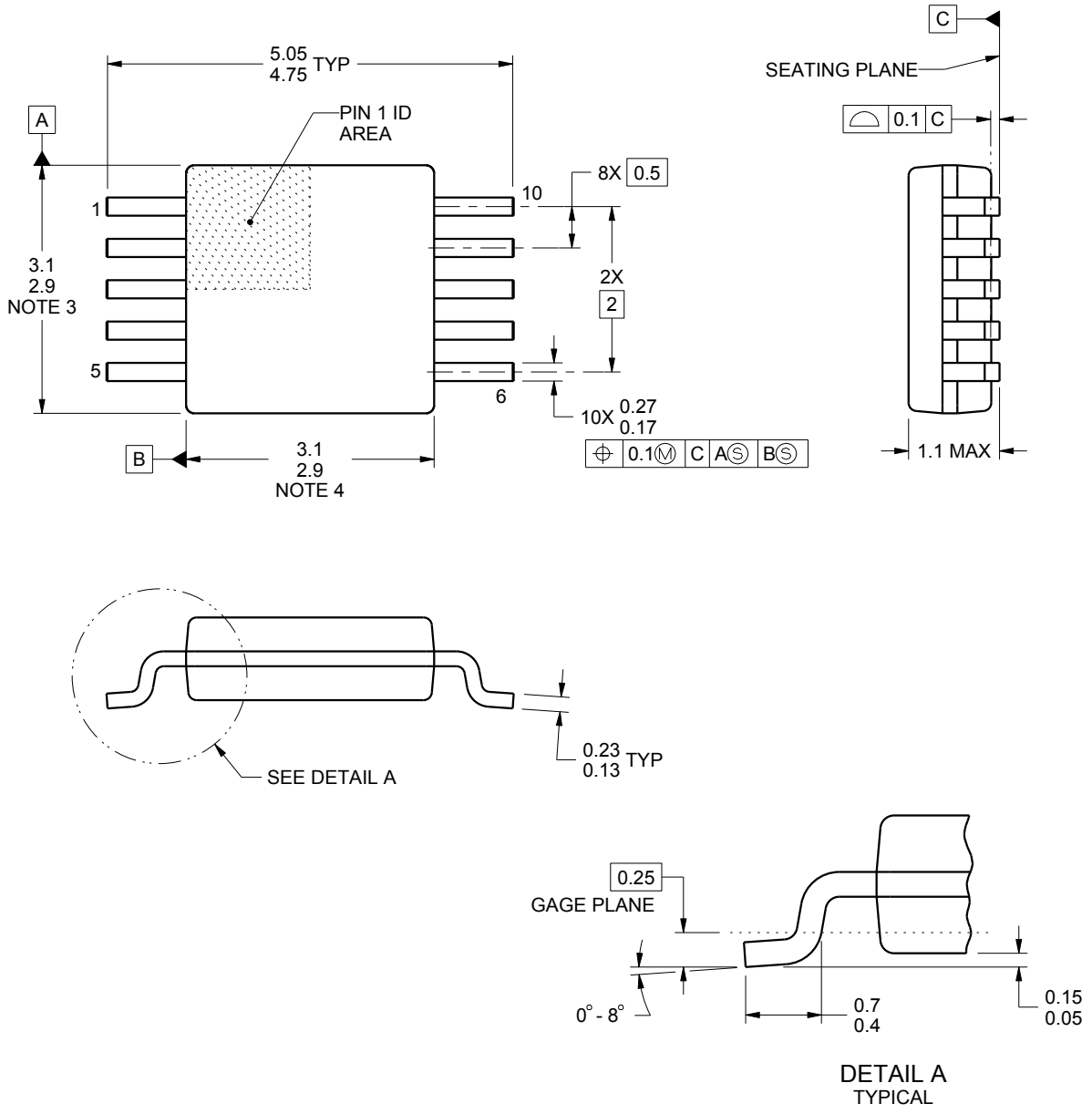
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4929MMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0

PACKAGE OUTLINE

DGS0010A

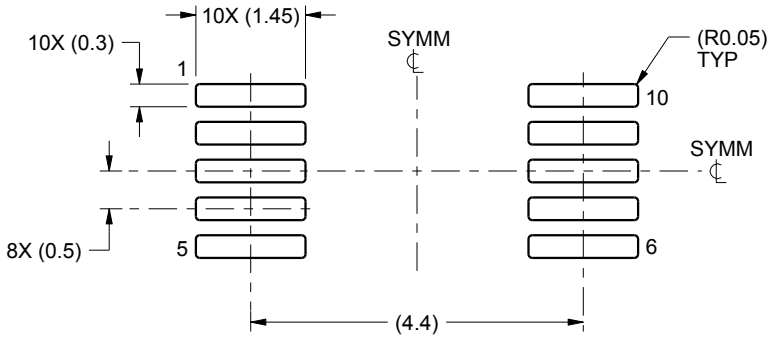
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

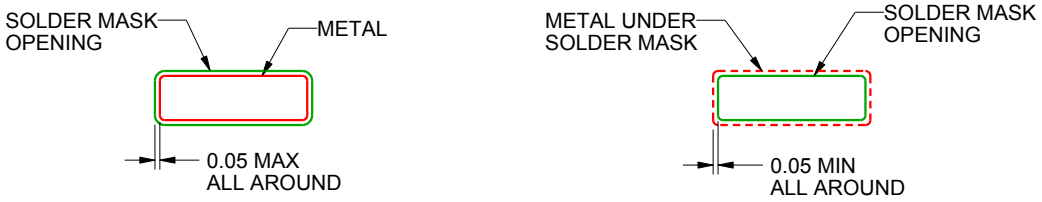


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

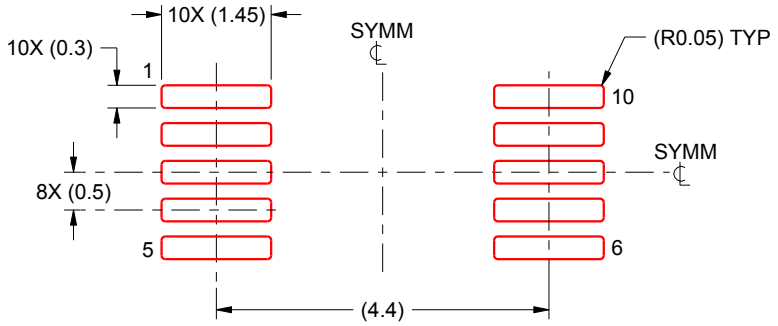


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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