- **Two independent VCOs in a 16-Pin Package**

- **Output Frequency Set by Single External Component:**
  Capacitor for Fixed- or Variable-Frequency Operation

- **Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Output Circuitry**

- **Highly Stable Operation over Specified Temperature and/or Supply Voltage Ranges**

- **Typical f_{max}** . . . . **85 MHz**
  Typical Power Dissipation . . . . . . **525 mW**
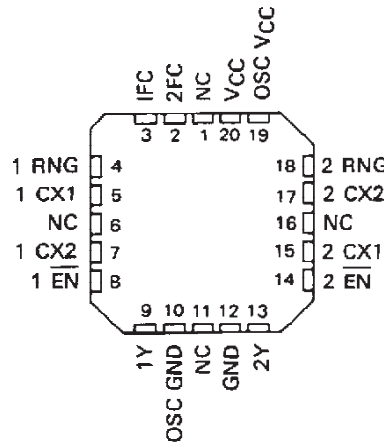
- **Frequency Spectrum . . . 1 Hz to 60 MHz**

description

The 'S124 features two independent voltage-controlled oscillators (VCO) in a single monolithic chip. The output frequency of each VCO is established by an external capacitor in combination with two voltage-sensitive inputs, one for frequency range and one for frequency control. These inputs can be used to vary the output frequency as shown under typical characteristics. These highly stable oscillators can be set to operate at any frequency typically between 0.12 hertz and 85 megahertz. '

SN54S124 . . . J OR W PACKAGE
SN74S124 . . . D OR N PACKAGE
(TOP VIEW)

2FC	1	16	V_{CC}
1FC	2	15	OSC V_{CC}
1 RNG	3	14	2 RNG
1 CX1	4	13	2 CX2
1 CX2	5	12	2 CX1
1 $\overline{EN}$	6	11	2 $\overline{EN}$
1Y	7	10	2Y
OSC GND	8	9	GND
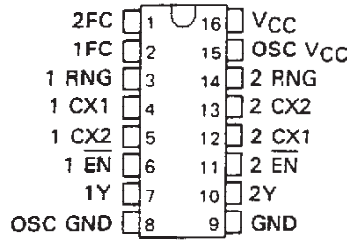
SN54S124 . . . FK PACKAGE
(TOP VIEW)

1 RNG	4	18	2 RNG
1 CX1	5	17	2 CX2
NC	6	16	NC
1 CX2	7	15	2 CX1
1 $\overline{EN}$	8	14	2 $\overline{EN}$

Top pins (3 2 1 20 19): IFC, 2FC, NC, V_{CC}, OSC V_{CC}

Bottom pins (9 10 11 12 13): 1Y, OSC GND, NC, GND, 2Y

NC – No internal connection

While the enable input is low, the output is enabled.
While the enable input is high, the output is high.

These devices can operate from a single 5-volt supply. However, one set of supply-voltage and ground pins (V_{CC} and GND) is provided for the enable, synchronization-gating, and output sections, and a separate set ($\ominus V_{CC}$ and $\ominus$ GND) is provided for the oscillator and associated frequency-control circuits so that effective isolation can be accomplished in the system.

The enable input of these devices starts or stops the output pulses when it is low or high, respectively. The internal oscillator of the 'S124 is started and stopped by the enable input. The enable input is one standard load; it and the buffered output operate at standard Schottky-clamped TTL levels.

The pulse synchronization-gating section ensures that the first output pulse is neither clipped nor extended. Duty cycle of the square-wave output is fixed at approximately 50 percent.

The SN54S124 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74S124 is characterized for operation from 0°C to 70°C.

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logic symbol†
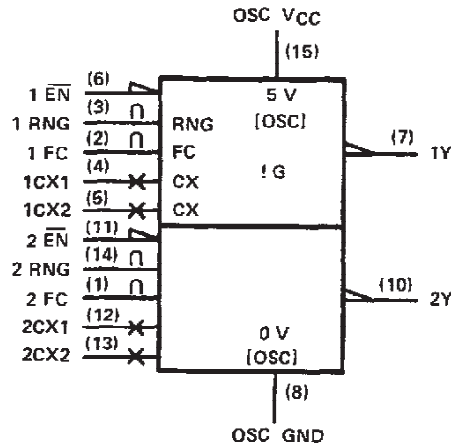
†This symbol is in accordance with ANSI/IEEE Std 91-1984
 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs

EQUIVALENT OF EACH ENABLE INPUT	EQUIVALENT OF EACH FREQUENCY CONTROL OR RANGE INPUT	TYPICAL OF BOTH OUTPUTS
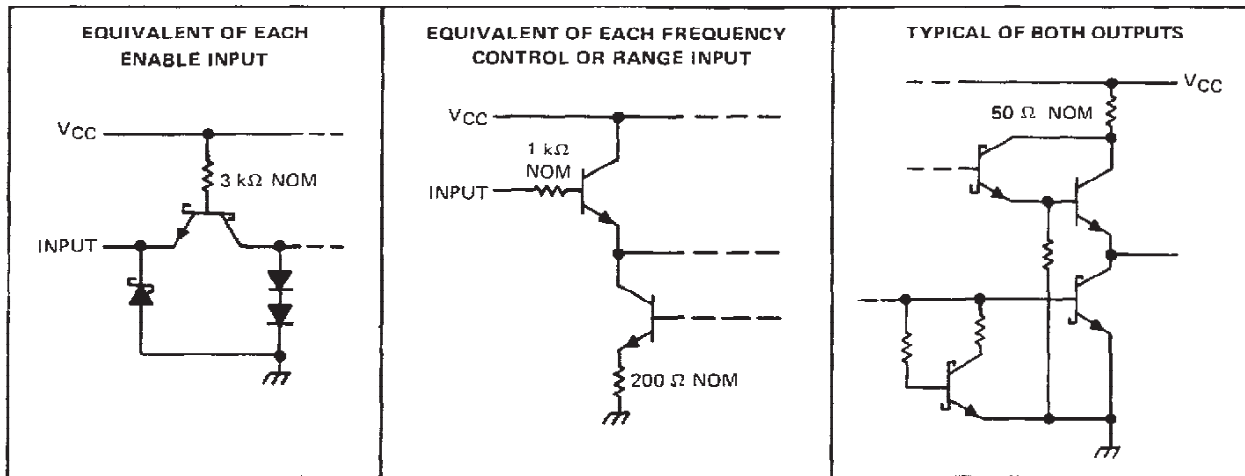
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Notes 1 and 2) 7V
Input voltage . . . . 5.5 V
Operating free-air temperature range: SN54S124 . . . . −55°C to 125°C
                                       SN74S124 . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to the appropriate ground terminal.
        2. Throughout this data sheet, the symbol V_{CC} is used for the voltage applied to both the V_{CC} and ⊙V_{CC} terminals, unless other-
           wise noted.

recommended operating conditions

	SN54S124			SN74S124			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
Input voltage at frequency control or range input, $V_{I(freq)}$ or $V_{I(rng)}$	1		5	1		5	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Output frequency (enabled), f_o	1			1			Hz
			60			60	MHz
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIONS[†]		MIN	TYP[‡]	MAX	UNIT
V_{IH}	High-level input voltage at enable				2			V
V_{IL}	Low-level input voltage at enable						0.8	V
V_{IK}	Input clamp voltage at enable		$V_{CC} = $ MIN, $I_I = −18$ mA				−1.2	V
V_{OH}	High-level output voltage		$V_{CC} = $ MIN, $V_{IH} = 2$ V, $I_{OH} = −1$ mA	SN54S′	2.5	3.4		V
				SN74S′	2.7	3.4		
V_{OL}	Low-level output voltage		$V_{CC} = $ MIN, $V_{IL} = 0.8$ V, $I_{OL} = 20$ mA				0.5	V
I_I	Input current	Freq control or range	$V_{CC} = $ MAX	$V_I = 5$ V		10	50	μA
				$V_I = 1$ V		1	15	
I_I	Input current at maximum input voltage	Enable	$V_{CC} = $ MAX, $V_I = 5.5$ V				1	mA
I_{IH}	High-level input current	Enable	$V_{CC} = $ MAX, $V_I = 2.7$ V				50	μA
I_{IL}	Low-level input current	Enable	$V_{CC} = $ MAX, $V_I = 0.5$ V				−2	mA
I_{OS}	Short-circuit output current[§]		$V_{CC} = $ MAX		−40		−100	mA
I_{CC}	Supply current, total into V_{CC} and ⊖ V_{CC}		$V_{CC} = $ MAX, See Note 3			105	150	mA
			$V_{CC} = $ MAX, $T_A = 125$°C, See Note 3	W package only			110	

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡]All typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.
[§]Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTE 3: I_{CC} is measured with the outputs disabled and open.

switching characteristics, $V_{CC} = 5$ V, $R_L = 280 \ \Omega$, $C_L = 15$ pF, $T_A = 25$°C (see note 4)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_o	Output frequency	$C_{ext} = 2$ pF	$V_{I(freq)} = 4$ V, $V_{I(rng)} = 1$ V	60	85		MHz
			$V_{I(freq)} = 1$ V, $V_{I(rng)} = 5$ V	25	40		
	Output duty cycle	$C_{ext} = 8.3$ pF to 500 μF			50%		
t_{PHL}	Propagation delay time, high-to-low-level output from enable	$f_o = 1$ Hz to 20 MHz			$\dfrac{1.4}{f_{o(Hz)}}$		s
		$f_o > 20$ MHz			70		ns

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

TYPICAL CHARACTERISTICS

BASE OUTPUT FREQUENCY
vs
EXTERNAL CAPACITANCE

FIGURE 1

NORMALIZED OUTPUT FREQUENCY
vs
INPUT VOLTAGE

FIGURE 2
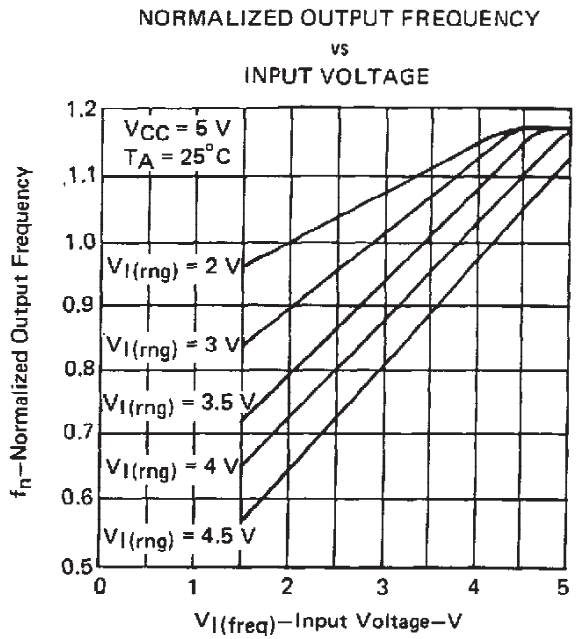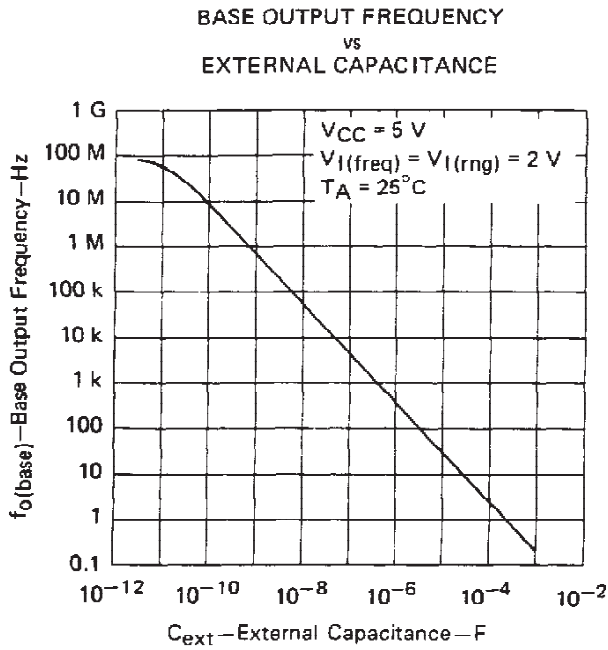
NOTE: $f_o = f_n \times f_{o(base)}$

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN54S124J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54S124J	Samples
SN74S124D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	S124	Samples
SN74S124N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74S124N	Samples
SN74S124NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74S124N	Samples
SNJ54S124J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S124J	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54S124, SN74S124 :

- Catalog : SN74S124

- Military : SN54S124

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74S124D	D	SOIC	16	40	507	8	3940	4.32
SN74S124N	N	PDIP	16	25	506	13.97	11230	4.32
SN74S124N	N	PDIP	16	25	506	13.97	11230	4.32
SN74S124NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74S124NE4	N	PDIP	16	25	506	13.97	11230	4.32

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80)
△C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) △D

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
        △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
        △D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
          E. Reference JEDEC MS−012 variation AC.

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D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

14x1,27

16x0,55

14x1,27

16x1,50

5,40

5.40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0,07

All Around

4211283−4/E   08/12

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC−7351 is recommended for alternate designs.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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J (R−GDIP−T**)   CERAMIC DUAL IN−LINE PACKAGE
14 LEADS SHOWN

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

0.065 (1,65)
0.045 (1,14)

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°−15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package is hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E. Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

N (R–PDIP–T**)   PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E   12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
         D.   The 20 pin end lead shoulder width is a vendor option, either half or full width.

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