

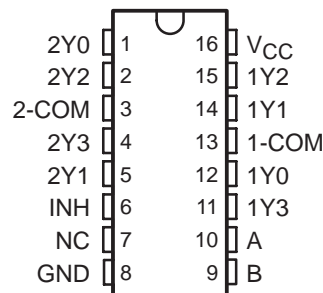
# SN74HC4852

## DUAL 4-TO-1 CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH INJECTION-CURRENT EFFECT CONTROL

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- Injection Current Cross-Coupling <math><1\text{mV}/\text{mA}</math> (see Figure 1)
- Low Crosstalk Between Switches
- Pin Compatible with SN74HC4052, SN74LV4052A, and CD4052B
- 2-V to 6-V  $V_{CC}$  Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

D, DGV, N, OR PW PACKAGE  
(TOP VIEW)



NC – No internal connection

### description/ordering information

This dual 4-to-1 CMOS analog multiplexer/demultiplexer is pin compatible with the 4052 function and also features injection-current effect control. This feature has excellent value in automotive applications where voltages in excess of normal supply voltages are common.

The injection-current effect control allows signals at disabled analog input channels to exceed the supply voltage without affecting the signal of the enabled analog channel. This eliminates the need for external diode/resistor networks typically used to keep the analog channel signals within the supply voltage range.

### ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	PDIP – N	Tube	SN74HC4852N	SN74HC4852N
	SOIC – D	Tube	SN74HC4852D	HC4852
		Tape and reel	SN74HC4852DR	
	TSSOP – PW	Tube	SN74HC4852PW	HC4852
		Tape and reel	SN74HC4852PWR	
	TVSOP – DGV	Tape and reel	SN74HC4852DGV	HC4852

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### FUNCTION TABLE

INPUTS			ON CHANNEL
INH	B	A	
L	L	L	1Y0, 2Y0
L	L	H	1Y1, 2Y1
L	H	L	1Y2, 2Y2
L	H	H	1Y3, 2Y3
H	X	X	None



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



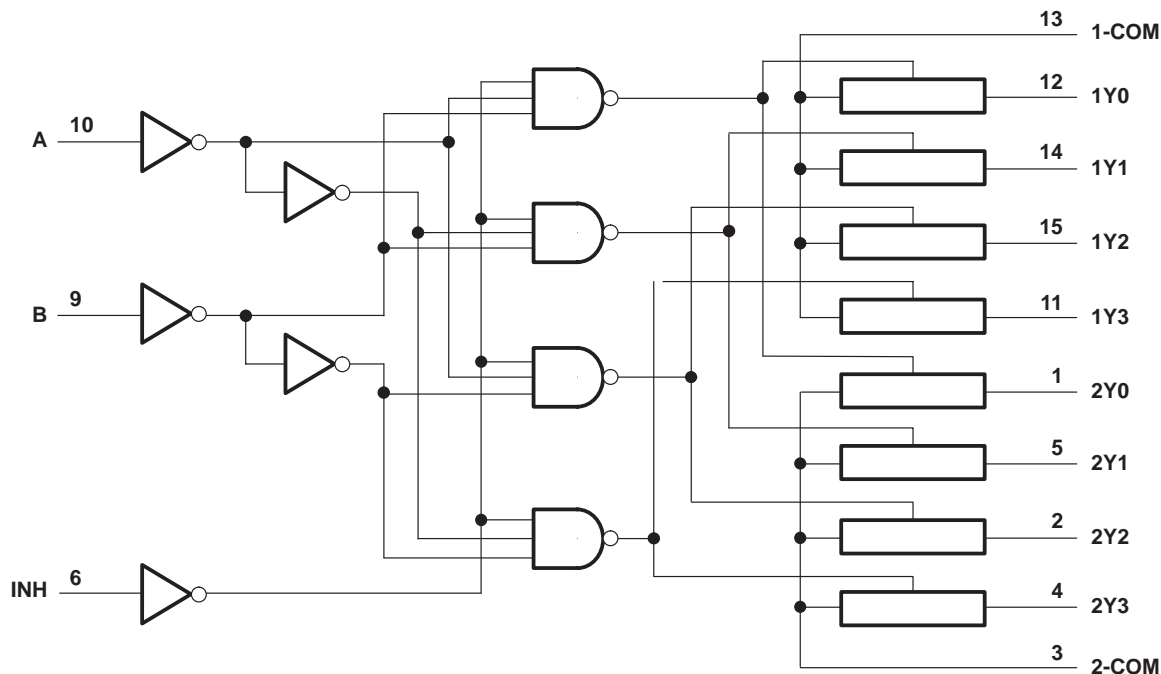
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**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$	-0.5 V to 7.0 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Switch I/O voltage range, $V_{IO}$ (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	$\pm 20$ mA
I/O diode current, $I_{IOK}$ ( $V_{IO} < 0$ or $V_{IO} > V_{CC}$ )	$\pm 20$ mA
Switch through current, $I_S$ ( $V_{IO} = 0$ to $V_{CC}$ )	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND	$\pm 50$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3):	
D package	73°C/W
DGV package	120°C/W
N package	67°C/W
PW package	108°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. This value is limited to 5.5 V maximum.  
 3. The package thermal impedance is calculated in accordance with JESD 51-7.



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**recommended operating conditions (see Note 4)**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	6	V
V <sub>IH</sub>	High-level input voltage, control inputs	V <sub>CC</sub> = 2 V	1.5	V
		V <sub>CC</sub> = 3 V	2.1	
		V <sub>CC</sub> = 3.3 V	2.3	
		V <sub>CC</sub> = 4.5 V	3.15	
		V <sub>CC</sub> = 6 V	4.2	
V <sub>IL</sub>	Low-level input voltage, control inputs	V <sub>CC</sub> = 2 V	0.5	V
		V <sub>CC</sub> = 3 V	0.9	
		V <sub>CC</sub> = 3.3 V	1	
		V <sub>CC</sub> = 4.5 V	1.35	
		V <sub>CC</sub> = 6 V	1.8	
V <sub>I</sub>	Control input voltage	0	V <sub>CC</sub>	V
V <sub>IO</sub>	Input/output voltage	0	V <sub>CC</sub>	V
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 2 V	1000	ns
		V <sub>CC</sub> = 3 V	800	
		V <sub>CC</sub> = 3.3 V	700	
		V <sub>CC</sub> = 4.5 V	500	
		V <sub>CC</sub> = 6 V	400	
T <sub>A</sub>	Operating free-air temperature	-40	125	°C

NOTE 4: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			-40 TO 85°C		-40 TO 125°C		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
r <sub>on</sub> On-state switch resistance	I <sub>S</sub> ≤ 2 mA V <sub>I</sub> = V <sub>CC</sub> to GND, V <sub>INH</sub> = V <sub>IL</sub> (see Figure 5)	2. V		500	650		670		700	Ω	
		3 V		215	280		320		360		
		3.3 V		210	270		305		345		
		4.5 V		160	210		240		270		
		6 V		150	195		220		250		
Δr <sub>on</sub> Difference in on-state resistance between switches	I <sub>S</sub> ≤ 2 mA V <sub>I</sub> = V <sub>CC</sub> /2 V <sub>INH</sub> = V <sub>IL</sub>	2. V		4	18		22		24	Ω	
		3 V		2	12		14		16		
		3.3 V		2	12		14		16		
		4.5 V		2	8		12		16		
		6 V		3	9		13		18		
I <sub>I</sub> Control input current	V <sub>I</sub> = V <sub>CC</sub> or GND	6 V			±0.1		±0.1		±1	μA	
I <sub>S(off)</sub> Off-state switch leakage current (any one channel)	V <sub>I</sub> = V <sub>CC</sub> or GND V <sub>INH</sub> = V <sub>IH</sub> (see Figure 6)	6 V			±0.1		±0.5		±1	μA	
	V <sub>I</sub> = V <sub>CC</sub> or GND V <sub>INH</sub> = V <sub>IH</sub> (see Figure 7)				±0.2		±2		±4		
I <sub>S(on)</sub> On-state switch leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>INH</sub> = V <sub>IL</sub> (see Figure 8)	6 V			±0.1		±0.5		±1	μA	
I <sub>CC</sub> Supply current	V <sub>I</sub> = V <sub>CC</sub> or GND	6 V			2		5		10	μA	
C <sub>IC</sub> Control input capacitance	A, B, INH				3.5	10		10		10	pF
C <sub>IS</sub> Common terminal capacitance	Switch off				22	40		40		40	pF
C <sub>OS</sub> Switch terminal capacitance	Switch off				6.7	15		15		15	pF

### injection-current coupling specifications, T<sub>A</sub> = -40°C to 125°C (see Figure 1)

PARAMETER	V <sub>CC</sub>	TEST CONDITIONS	TYP†	MAX	UNIT
V <sub>Δout</sub> Maximum shift of output voltage of enabled analog channel	3.3 V	I <sub>I</sub> ‡ ≤ 1 mA, R <sub>S</sub> ≤ 3.9 kΩ	0.05	1	mV
	5 V		0.1	1	
	3.3 V	I <sub>I</sub> ‡ ≤ 10 mA, R <sub>S</sub> ≤ 3.9 kΩ	0.345	5	
	5 V		0.067	5	
	3.3 V	I <sub>I</sub> ‡ ≤ 1 mA, R <sub>S</sub> ≤ 20 kΩ	0.05	2	
	5 V		0.11	2	
	3.3 V	I <sub>I</sub> ‡ ≤ 10 mA, R <sub>S</sub> ≤ 20 kΩ	0.05	20	
	5 V		0.024	20	

† Typical values are measured at T<sub>A</sub> = 25°C.

‡ I<sub>I</sub> = total current injected into all disabled channels.



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**DUAL 4-TO-1 CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER  
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switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 2 V, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figures 9–14)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			–40 TO 85°C		–40 TO 125°C		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time	COM or Y <sub>n</sub>	Y <sub>n</sub> or COM	14.5	19.5	33	12	34	11	35	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time	Channel Select	COM or Y <sub>n</sub>	19.6	24.5	38	15.4	40	13.8	42	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Enable delay time	INH	COM or Y <sub>n</sub>	19.4	23.6	47.5	15.8	52.5	14.5	57.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Disable delay time	INH	COM or Y <sub>n</sub>	39.5	48.4	100	39.3	105	39	115	ns

switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 3 V, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figures 9–14)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			–40 TO 85°C		–40 TO 125°C		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time	COM or Y <sub>n</sub>	Y <sub>n</sub> or COM	8.6	12	16.5	6.5	18	5.8	19.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time	Channel Select	COM or Y <sub>n</sub>	12.4	14.6	20	9.3	21.5	8.2	23	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Enable delay time	INH	COM or Y <sub>n</sub>	12.1	13.8	45	9.2	50	8.5	55	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Disable delay time	INH	COM or Y <sub>n</sub>	35.2	44.5	90	35.5	100	35	110	ns

switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 3.3 V, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figures 9–14)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			–40 TO 85°C		–40 TO 125°C		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time	COM or Y <sub>n</sub>	Y <sub>n</sub> or COM	7.9	11	15	5.8	16.5	5	18.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time	Channel Select	COM or Y <sub>n</sub>	11.4	13.5	17.5	8.5	19	7.5	22	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Enable delay time	INH	COM or Y <sub>n</sub>	11.2	12.7	42.5	8.4	47.5	7.4	52.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Disable delay time	INH	COM or Y <sub>n</sub>	34.6	43.9	85	34.6	95	34.5	105	ns

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switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 4.5\text{ V}$ ,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figures 9–14)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			$-40\text{ TO }85^\circ\text{C}$		$-40\text{ TO }125^\circ\text{C}$		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time	COM or Y <sub>n</sub>	Y <sub>n</sub> or COM	6.3	8.6	11.6	4.6	12.5	4.5	13.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time	Channel Select	COM or Y <sub>n</sub>	9.3	11	14	6.5	15	5.6	17	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Enable delay time	INH	COM or Y <sub>n</sub>	8	9.9	40	5.3	45	4.4	50	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Disable delay time	INH	COM or Y <sub>n</sub>	28.5	41.4	80	28.2	90	28	100	ns

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 6\text{ V}$ ,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figures 9–14)

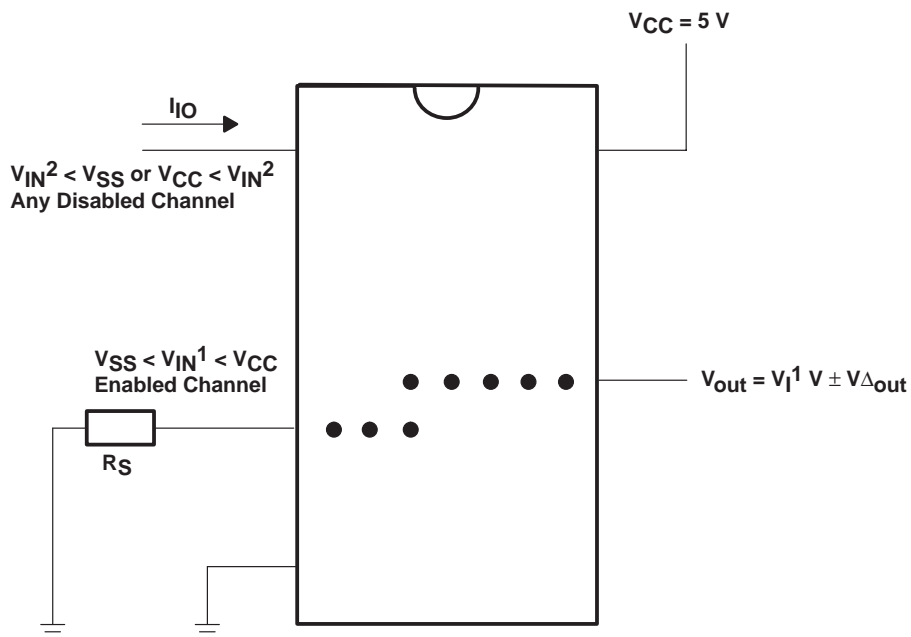
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			$-40\text{ TO }85^\circ\text{C}$		$-40\text{ TO }125^\circ\text{C}$		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time	COM or Y <sub>n</sub>	Y <sub>n</sub> or COM	5.5	8	10.2	4.1	11	3.6	12	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time	Channel Select	COM or Y <sub>n</sub>	7.4	9.5	12.6	4.7	14.5	3.8	16.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Enable delay time	INH	COM or Y <sub>n</sub>	6.8	8.4	39	4.8	40	3.8	40	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Disable delay time	INH	COM or Y <sub>n</sub>	14.4	38	78	13.5	80	13	80	ns

operating characteristics,  $T_A = 25^\circ\text{C}$  (see Figure 15)

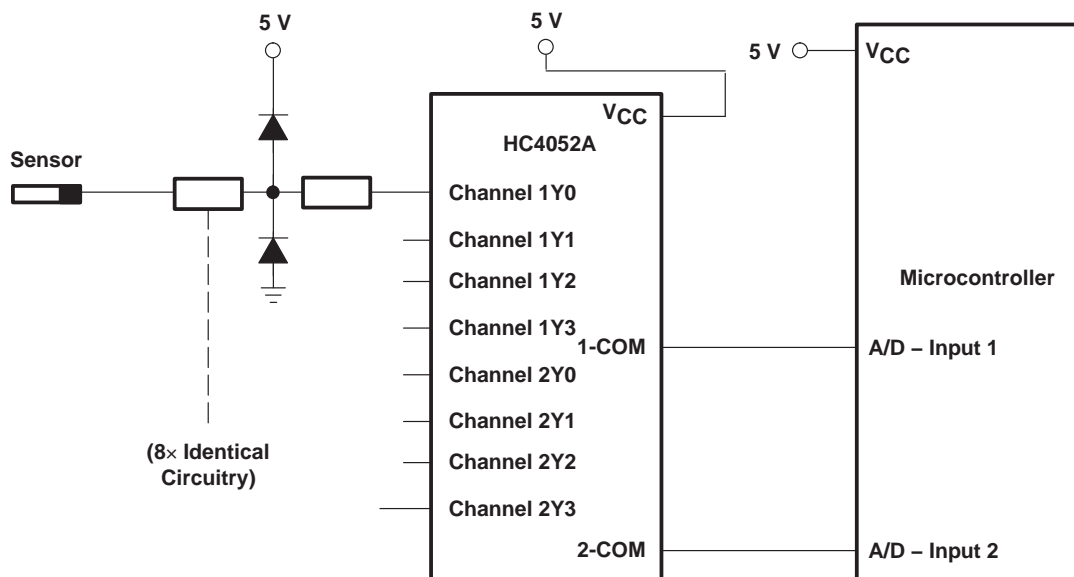
PARAMETER		$V_{CC}$	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	3.3 V	No load	48	pF
		5 V		60	



**APPLICATION INFORMATION**



**Figure 1. Injection-Current Coupling Specification**

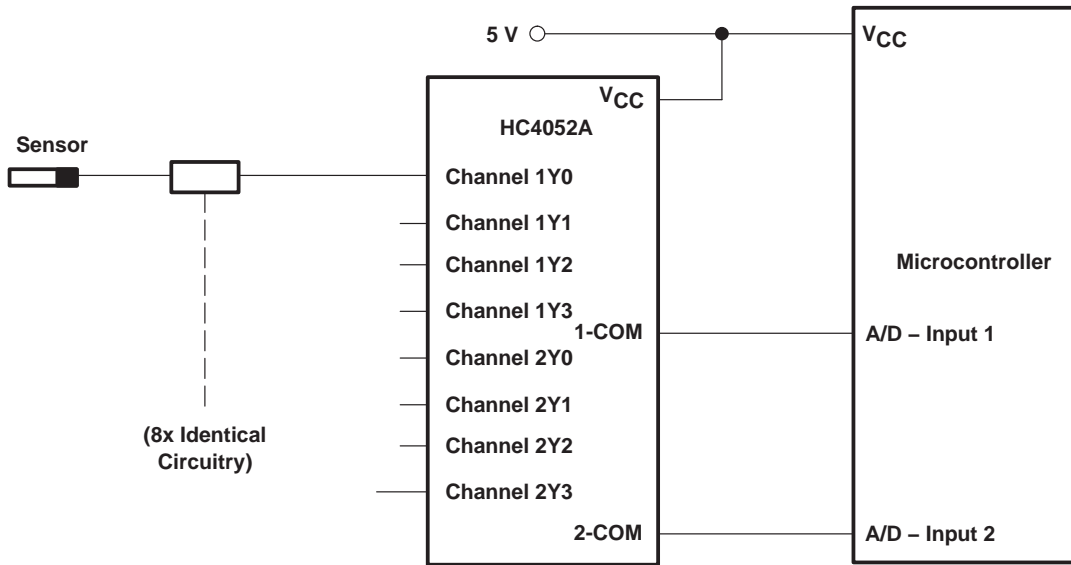


**Figure 2. Actual Technology Requires 32 Passive Components and One Extra 6-V Regulator to Suppress Injection Current Into a Standard HC4052 Multiplexer**

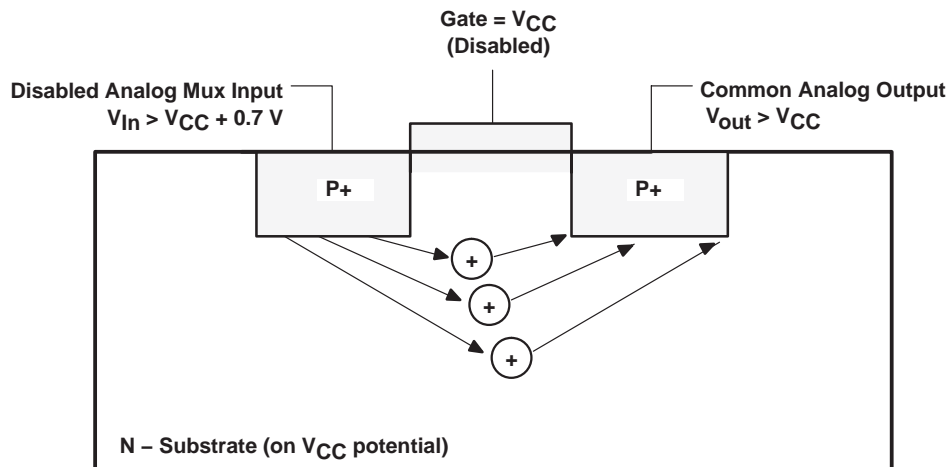
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**APPLICATION INFORMATION**



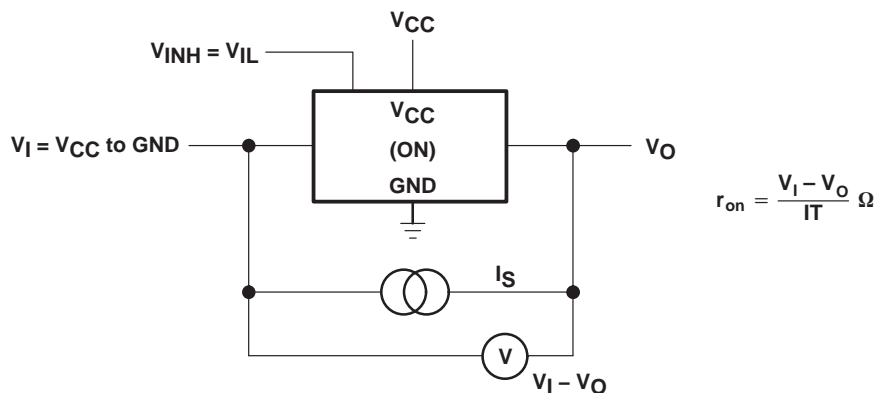
**Figure 3. Solution by Applying the HC4852 Multiplexer**



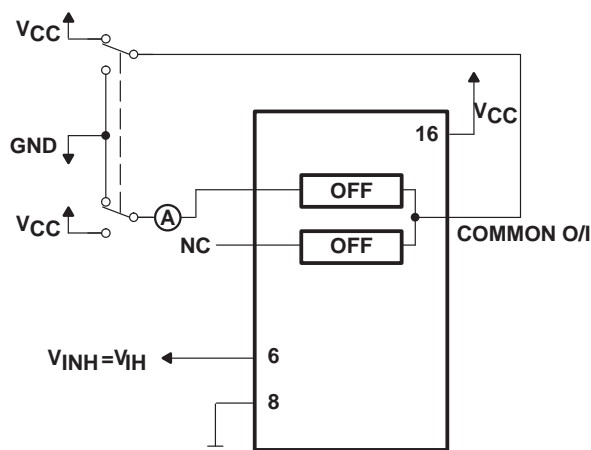
**Figure 4. Diagram of Bipolar Coupling Mechanism**  
**(Appears if  $V_{In}$  Exceeds  $V_{CC}$ , Driving Injection Current Into the Substrate)**



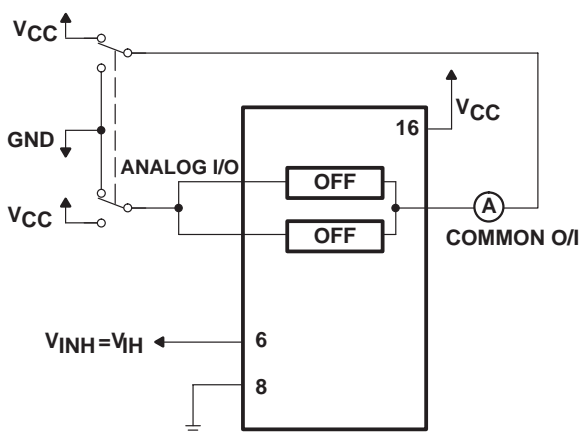
**PARAMETER MEASUREMENT INFORMATION**



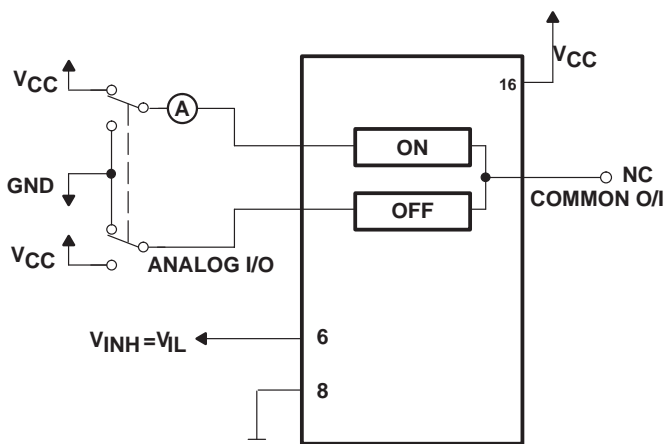
**Figure 5. On-State Resistance Test Circuit**



**Figure 6. Maximum Off-Channel Leakage Current, Any One Channel, Test Setup**



**Figure 7. Maximum Off-Channel Leakage Current, Common Channel, Test Setup**

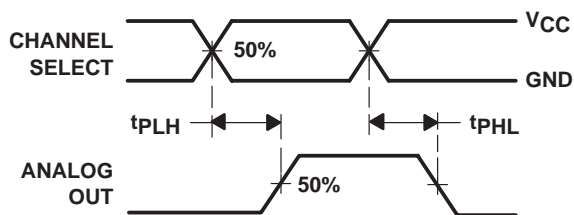


**Figure 8. Maximum On-Channel Leakage Current, Channel to Channel, Test Setup**

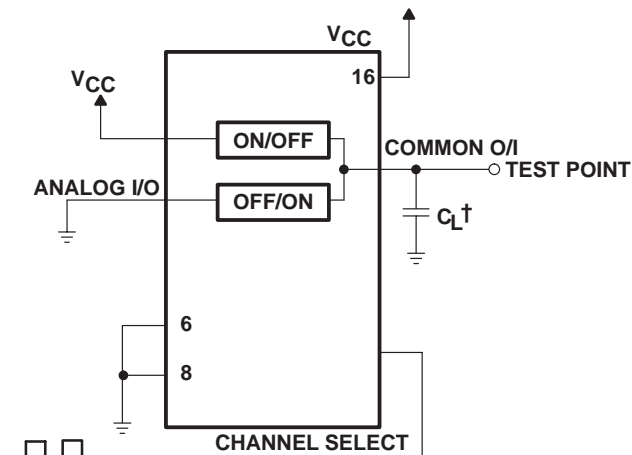
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**PARAMETER MEASUREMENT INFORMATION**

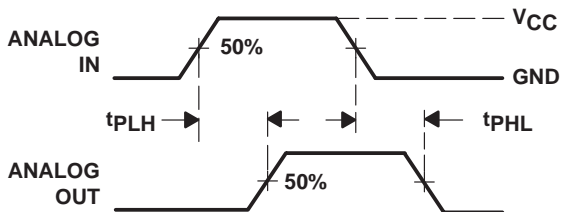


**Figure 9. Propagation Delays, Channel Select to Analog Out**

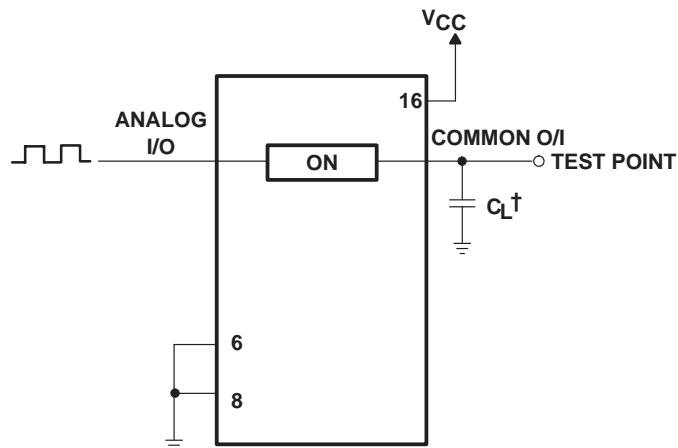


† Includes all probe and jig capacitance

**Figure 10. Propagation Delay, Channel Select to Analog Out, Test Setup**



**Figure 11. Propagation Delays, Analog In to Analog Out**



† Includes all probe and jig capacitance

**Figure 12. Propagation Delay, Analog In to Analog Out, Test Setup**

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### PARAMETER MEASUREMENT INFORMATION

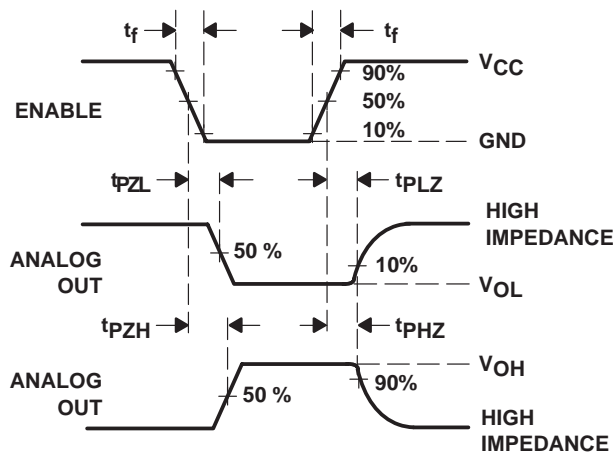


Figure 13. Propagation Delays, Enable to Analog Out

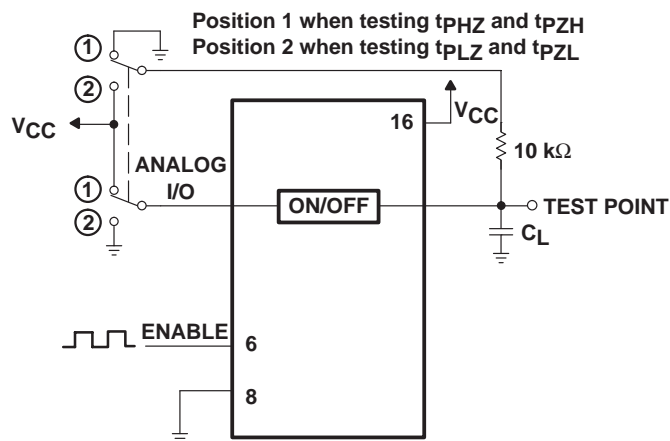


Figure 14. Propagation Delay, Enable to Analog Out, Test Setup

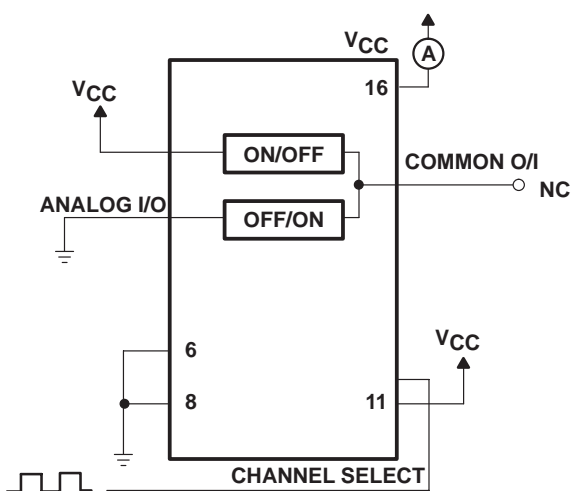


Figure 15. Power-Dissipation Capacitance, Test Setup

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC4852D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4852	<a href="#">Samples</a>
SN74HC4852DGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4852	<a href="#">Samples</a>
SN74HC4852DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4852	<a href="#">Samples</a>
SN74HC4852DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4852	<a href="#">Samples</a>
SN74HC4852N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 125	SN74HC4852N	<a href="#">Samples</a>
SN74HC4852PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4852	<a href="#">Samples</a>
SN74HC4852PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4852	<a href="#">Samples</a>
SN74HC4852PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4852	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74HC4852 :**

- Automotive: [SN74HC4852-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC4852DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74HC4852DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC4852PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC4852DGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74HC4852DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74HC4852PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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