

## SN74LVC1GX04 Crystal Oscillator Driver

### 1 Features

- Available in Texas Instruments NanoStar™ and NanoFree™ Packages
- Supports 5-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 5.5 V
- One Unbuffered Inverter (SN74LVC1GU04) and One Buffered Inverter (SN74LVC1G04)
- Suitable for Commonly Used Clock Frequencies:
  - 15 kHz, 3.58 MHz, 4.43 MHz, 13 MHz, 25 MHz, 26 MHz, 27 MHz, 28 MHz
- Maximum  $t_{pd}$  of 2.4 ns at 3.3 V
- Low Power Consumption, 10- $\mu$ A Maximum  $I_{CC}$
- $\pm 24$ -mA Output Drive at 3.3 V
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

### 2 Applications

- Crystal Oscillators
- Clock Generation

### 3 Description

The SN74LVC1GX04 device is designed for 1.65-V to 5.5-V  $V_{CC}$  operation. This device incorporates the SN74LVC1GU04 (inverter with unbuffered output) and the SN74LVC1G04 (inverter) functions into a single device. The LVC1GX04 is optimized for use in crystal oscillator applications.

X1 and X2 can be connected to a crystal or resonator in oscillator applications. The device provides an additional buffered inverter (Y) for signal conditioning (see Figure 5). The additional buffered inverter improves the signal quality of the crystal oscillator output by making it rail to rail.

NanoStar and NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

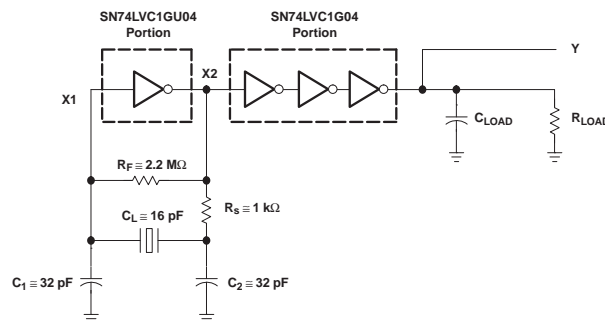
This device is fully specified for partial-power-down applications using  $I_{off}$  (Y output only). The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC1GX04DB V	SOT-23 (6)	2.90 mm x 1.60 mm
SN74LVC1GX04DC K	SC70 (6)	2.00 mm x 1.25 mm
SN74LVC1GX04DR L	SOT (6)	1.60 mm x 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Functional Block Diagram



SN74LVC1GX04 includes both dotted portions



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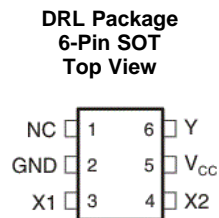
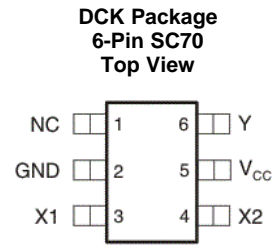
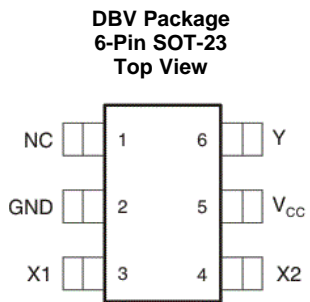
## 4 Revision History

### Changes from Revision C (December 2013) to Revision D

Page

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ..... **1**

## 5 Pin Configuration and Functions



See mechanical drawings for dimensions.

NC – No internal connection.

### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2	–	Ground
NC	1	–	No internal connection
VCC	5	–	Supply power
X1	3	I	Amplifier input
X2	4	O	Amplifier output
Y	6	O	Main output to other logic

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	6.5	V
V <sub>I</sub>	Input voltage <sup>(2)</sup>	-0.5	6.5	V
V <sub>O</sub>	Voltage applied to Y output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	6.5	V
V <sub>O</sub>	Voltage applied to any output in the high or low state <sup>(2)</sup> <sup>(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	-50	mA
I <sub>O</sub>	Continuous output current		±50	mA
	Continuous current through V <sub>CC</sub> or GND		±100	mA
T <sub>J</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V<sub>CC</sub> is provided in the recommended operating conditions table.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per AEC Q100-011	±1000

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	Operating	1.65	5.5
		Data retention only	1.5	
		Crystal oscillator use	2	
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 5.5 V	0.75 × V <sub>CC</sub>	V
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 5.5 V	0.25 × V <sub>CC</sub>	V
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>O</sub>	Output voltage	X2, Y	0	V <sub>CC</sub>
		Y output only, Power-down mode, V <sub>CC</sub> = 0 V	0	5.5
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V		-4
		V <sub>CC</sub> = 2.3 V		-8
		V <sub>CC</sub> = 3 V		-16
		V <sub>CC</sub> = 4.5 V		-24
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V		4
		V <sub>CC</sub> = 2.3 V		8
		V <sub>CC</sub> = 3 V		16
		V <sub>CC</sub> = 4.5 V		24

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

**Recommended Operating Conditions<sup>(1)</sup> (continued)**

			MIN	MAX	UNIT
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}, 2.5\text{ V} \pm 0.2\text{ V}$		20	ns/V
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		10	
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		10	
$T_A$	Operating free-air temperature		-40	125	°C

**6.4 Thermal Information**

THERMAL METRIC <sup>(1)</sup>	SN74LVC1GX04			UNIT	
	DBV (SOT-23)	DCK (SC70)	DRL (SOT)		
	6 PINS	6 PINS	6 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165	259	142	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

**6.5 Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$V_{CC}$	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
$V_{OH}$		$I_{OH} = -100\ \mu\text{A}$ $I_{OH} = -4\ \text{mA}$ $I_{OH} = -8\ \text{mA}$ $I_{OH} = -16\ \text{mA}$ $I_{OH} = -24\ \text{mA}$ $I_{OH} = -32\ \text{mA}$	$V_I = 5.5\ \text{V or GND}$	$T_A = -40^\circ\text{C to } 125^\circ\text{C}$	1.65 V to 5.5 V	$V_{CC} - 0.1$		V	
					1.65 V	1.2			
					2.3 V	1.9			
					3 V	2.4			
						2.3			
					4.5 V	3.8			
$V_{OL}$		$I_{OL} = 100\ \mu\text{A}$ $I_{OL} = 4\ \text{mA}$ $I_{OL} = 8\ \text{mA}$ $I_{OL} = 16\ \text{mA}$ $I_{OL} = 24\ \text{mA}$ $I_{OL} = 32\ \text{mA}$	$V_I = 5.5\ \text{V or GND}$	$T_A = -40^\circ\text{C to } 125^\circ\text{C}$	1.65 V to 5.5 V		0.1	V	
					1.65 V		0.45		
					2.3 V		0.3		
					$T_A = -40^\circ\text{C to } 125^\circ\text{C}$	3 V			0.4
					$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	3 V			0.55
					$T_A = -40^\circ\text{C to } 125^\circ\text{C}$				0.63
					$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	4.5 V			0.55
					$T_A = -40^\circ\text{C to } 125^\circ\text{C}$				0.7
$I_I$	X1	$V_I = 5.5\ \text{V or GND}$	$T_A = -40^\circ\text{C to } 125^\circ\text{C}$	0 to 5.5 V			$\pm 5$	$\mu\text{A}$	
$I_{off}$	X1, Y	$V_I$ or $V_O = 5.5\ \text{V}$	$T_A = -40^\circ\text{C to } 125^\circ\text{C}$	0			$\pm 10$	$\mu\text{A}$	
$I_{CC}$		$V_I = 5.5\ \text{V or GND}, I_O = 0$	$T_A = -40^\circ\text{C to } 125^\circ\text{C}$	1.65 V to 5.5 V			10	$\mu\text{A}$	
$C_i$		$V_I = V_{CC}$ or GND		3.3 V		7		pF	

(1) All typical values are at  $V_{CC} = 3.3\ \text{V}$ ,  $T_A = 25^\circ\text{C}$ .

## SN74LVC1GX04

SCES581D – JULY 2004 – REVISED OCTOBER 2015

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### 6.6 Switching Characteristics, SN74LVC1GX04

over recommended operating free-air temperature range,  $C_L = 15$  pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEMPERATURE	$V_{CC}$	MIN	MAX	UNIT
$t_{pd}$	X1	X2	–40°C to 85°C	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	1	4	ns
				$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	0.8	2.6	
				$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	0.6	2.4	
				$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	0.5	2	
		Y <sup>(1)</sup>	–40°C to 85°C	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	3.5	10	
				$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	2.2	6	
				$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	2	5	
				$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	1.5	3.5	

(1) X2 – no external load

### 6.7 Switching Characteristics, SN74LVC1GX04

over recommended operating free-air temperature range,  $C_L = 30$  pF or 50 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEMPERATURE	$V_{CC}$	MIN	MAX	UNIT
$t_{pd}$	X1	X2	–40°C to 85°C	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	1.1	7	ns
				$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	0.8	4	
				$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	0.8	3.7	
				$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	0.8	3	
		Y <sup>(1)</sup>	–40°C to 85°C	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	3.8	18	
				$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	2	7.4	
				$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	2	7.8	
				$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	2	5	

(1) X2 – no external load

### 6.8 Switching Characteristics, SN74LVC1GX04

over recommended operating free-air temperature range,  $C_L = 30$  pF or 50 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEMPERATURE	$V_{CC}$	MIN	MAX	UNIT
$t_{pd}$	X1	X2	–40°C to 125°C	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	1.1	8	ns
				$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	0.8	5	
				$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	0.8	4.3	
				$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	0.8	3.5	
		Y <sup>(1)</sup>	–40°C to 125°C	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	3.8	20	
				$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	2	8.4	
				$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	2	8.8	
				$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	2	5.5	

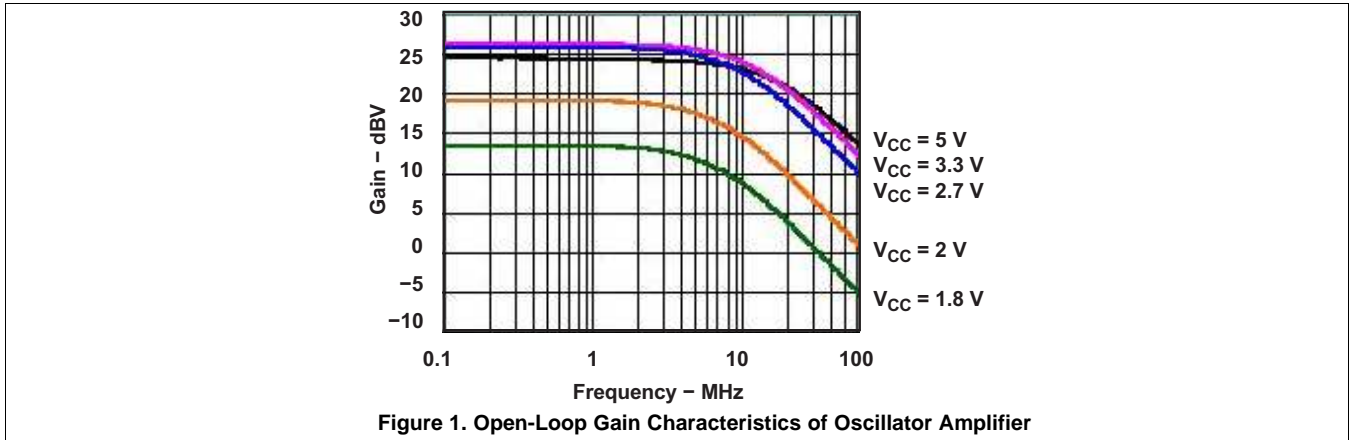
(1) X2 – no external load

### 6.9 Operating Characteristics

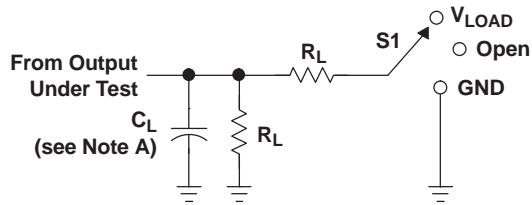
$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$f = 10\text{ MHz}$	$V_{CC} = 1.8\text{ V}$	22	pF
		$V_{CC} = 2.5\text{ V}$	22	
		$V_{CC} = 3.3\text{ V}$	24	
		$V_{CC} = 5\text{ V}$	35	

## 6.10 Typical Characteristics

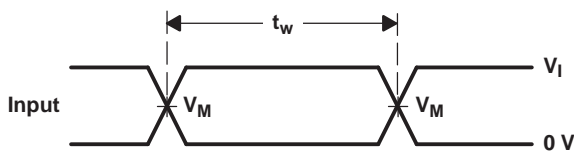
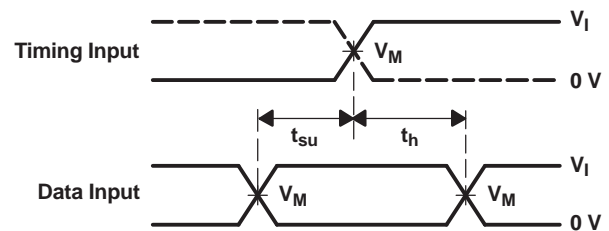
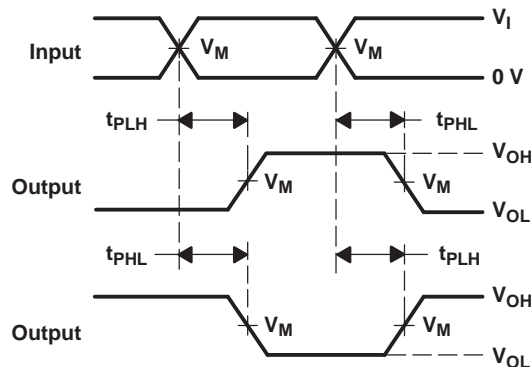
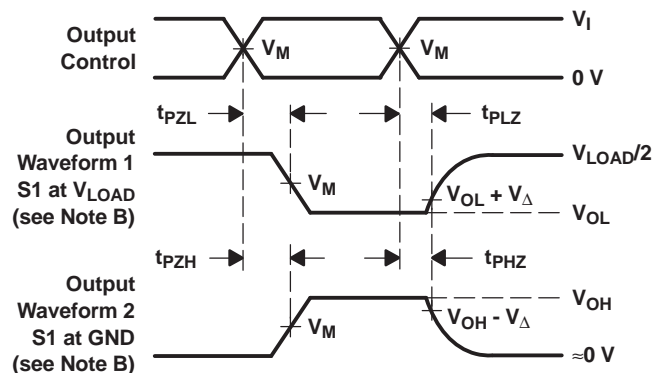


## 7 Parameter Measurement Information


**LOAD CIRCUIT**

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	0.3 V

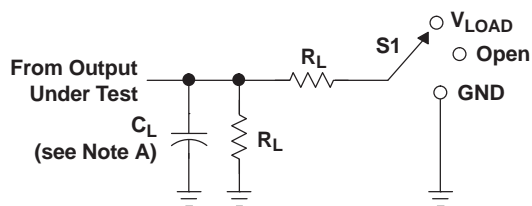

**VOLTAGE WAVEFORMS  
PULSE DURATION**

**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING**

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

**Figure 2. Load Circuit and Voltage Waveforms**



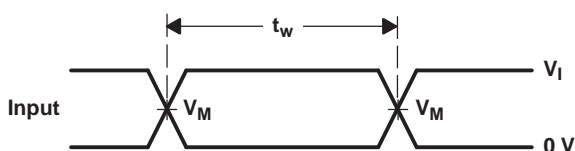
Parameter Measurement Information (continued)



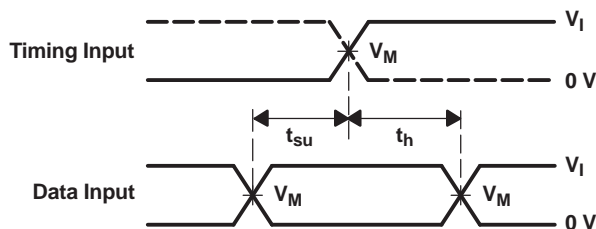
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

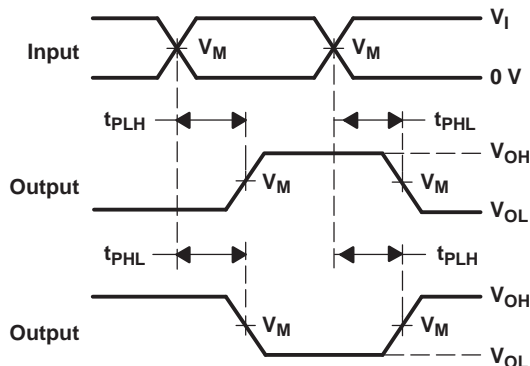
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V



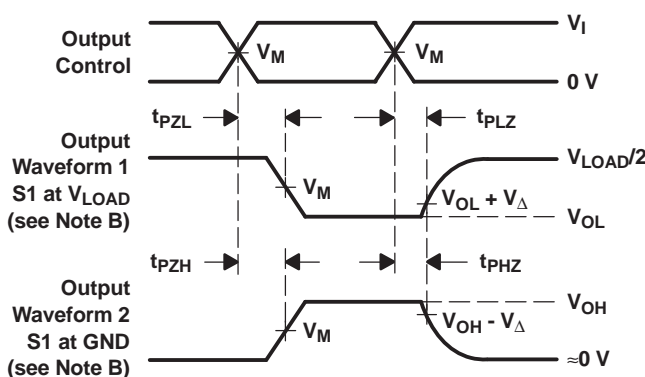
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

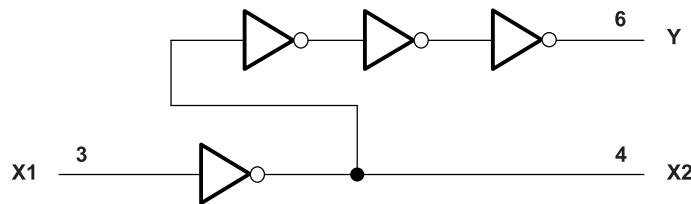
Figure 3. Load Circuit and Voltage Waveforms

## 8 Detailed Description

### 8.1 Overview

The SN74LVC1GX04 is optimized for creating a crystal oscillator circuit with a buffered square-wave output. This device is fully specified for partial-power-down applications using  $I_{off}$  (Y output only). The  $I_{off}$  circuitry disables the outputs, preventing damaging current back-flow through the device when it is powered down.

### 8.2 Functional Block Diagram



**Figure 4. Logic Diagram (Positive Logic)**

### 8.3 Feature Description

The first inverter is used as a linear amplifier for crystal oscillator.

The last three inverters ensure a fast edge square-wave at the Y output.

### 8.4 Device Functional Modes

The only intended device use is to generate a square-wave output using a crystal to set the operating frequency.

**Table 1. Function Table**

INPUT X1	OUTPUTS	
	X2	Y
H	L	H
L	H	L

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74LVC1GX04 contains a buffered and unbuffered inverter for the specific purpose of creating a crystal oscillator and driver with limited external components.

### 9.2 Typical Application

Figure 5 shows a typical application of the SN74LVC1GX04 in a Pierce oscillator circuit. The buffered inverter (SN74LVC1G04 portion) produces a rail-to-rail voltage waveform. The recommended load for the crystal shown in this example is 16 pF. The value of the recommended load ( $C_L$ ) can be found in the crystal manufacturer's data sheet.

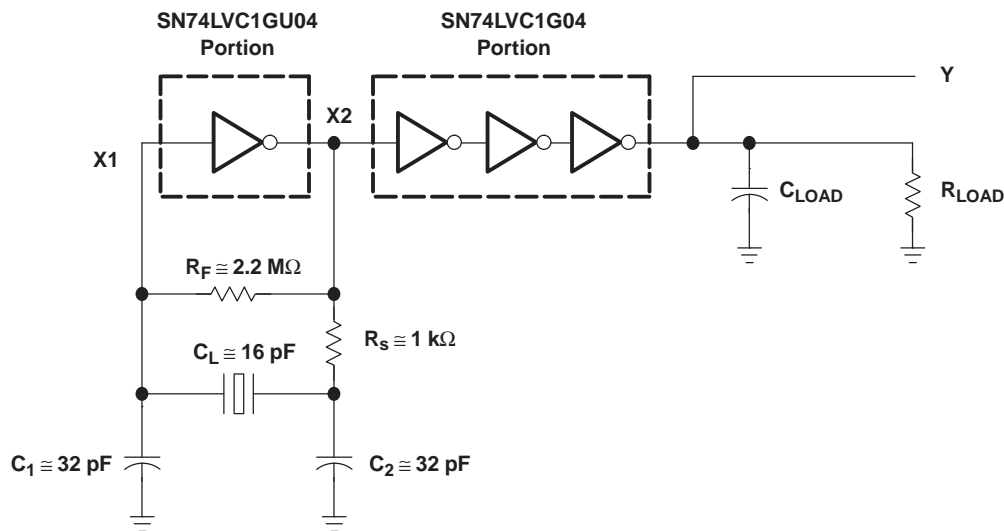
Values of  $C_1$  and  $C_2$  are chosen to calculate  $C_L$  in Equation 1 where  $C_1 \equiv C_2$ .

$$C_L = \frac{C_1 C_2}{C_1 + C_2} \quad (1)$$

$R_s$  is the current-limiting resistor, and the value depends on the maximum power dissipation of the crystal. Generally, the recommended value of  $R_s$  is specified in the crystal manufacturer's data sheet and, usually, this value is approximately equal to the reactance of  $C_2$  at resonance frequency, that is seen in Equation 2.

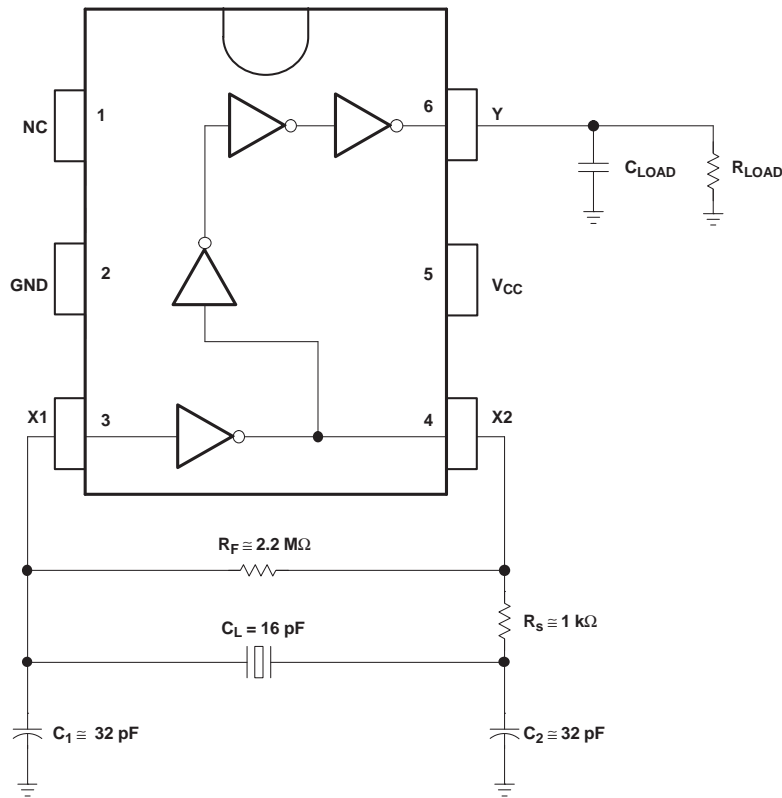
$$R_s = X_{C_2} \quad (2)$$

$R_F$  is the feedback resistor that is used to bias the inverter in the linear region of operation. Usually, the value is chosen to be within 1 M $\Omega$  to 10 M $\Omega$ .



a) Logic Diagram View

Figure 5. Oscillator Circuit

**Typical Application (continued)**


b) Oscillator Circuit in DBV or DCK Pinout

**Figure 6. Oscillator Circuit (Continued)**
**9.2.1 Design Requirements**

The open-loop gain of the unbuffered inverter decreases as power-supply voltage decreases. This decreases the closed-loop gain of the oscillator circuit. The value of  $R_S$  can be decreased to increase the closed-loop gain, while maintaining the power dissipation of the crystal within the maximum limit.

$R_S$  and  $C_2$  form a low-pass filter and reduce spurious oscillations. Component values can be adjusted, based on the desired cutoff frequency.

$C_2$  can be increased over  $C_1$  to increase the phase shift and help in start-up of the oscillator. Increasing  $C_2$  may affect the duty cycle of the output voltage.

At high frequency, phase shift due to  $R_S$  becomes significant. In this case,  $R_S$  can be replaced by a capacitor to reduce the phase shift.

**9.2.2 Detailed Design Procedure**

After the selection of proper component values, the oscillator circuit should be tested using these components. To ensure that the oscillator circuit performs within the *Recommended Operating Conditions*<sup>(1)</sup>, follow these steps:

1. Without a crystal, the oscillator circuit should not oscillate. To check this, the crystal can be replaced by its equivalent parallel-resonant resistance.
2. When the power-supply voltage drops, the closed-loop gain of the oscillator circuit reduces. Ensure that the circuit oscillates at the appropriate frequency at the lowest  $V_{CC}$  and highest  $V_{CC}$ .
3. Ensure that the duty cycle, start-up time, and frequency drift over time is within the system requirements.

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

Typical Application (continued)

9.2.3 Application Curve

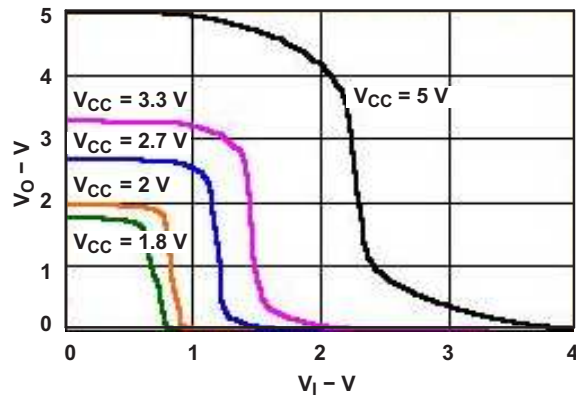


Figure 7.  $V_O$  vs  $V_I$  Characteristics of Oscillator Amplifier

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in [Recommended Operating Conditions<sup>\(1\)</sup>](#) table.

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu$ F capacitor is recommended. If there are multiple  $V_{CC}$  terminals then 0.01- $\mu$ F or 0.022- $\mu$ F capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

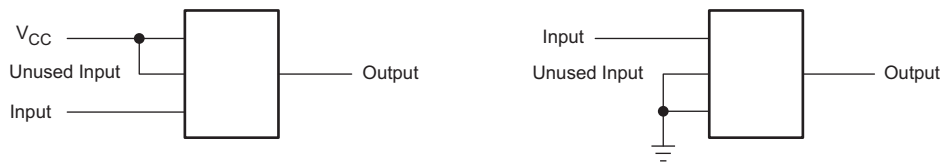
## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 8](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient.

### 11.2 Layout Example



**Figure 8. Layout Diagram**

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation, see the following:

*Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

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### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74LVC1GX04DCKTG4	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(D25, D2R)	<a href="#">Samples</a>
SN74LVC1GX04DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CX45, CX4R)	<a href="#">Samples</a>
SN74LVC1GX04DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CX45, CX4R)	<a href="#">Samples</a>
SN74LVC1GX04DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(D25, D2J, D2K, D2R)	<a href="#">Samples</a>
SN74LVC1GX04DCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(D25, D2J, D2R)	<a href="#">Samples</a>
SN74LVC1GX04DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(1K6, D27, D2R)	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LVC1GX04 :**

- Enhanced Product : [SN74LVC1GX04-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC1GX04DCKTG4	SC70	DCK	6	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1GX04DBVR	SOT-23	DBV	6	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1GX04DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1GX04DBVT	SOT-23	DBV	6	250	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1GX04DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1GX04DCKR	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1GX04DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74LVC1GX04DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1GX04DCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74LVC1GX04DCKT	SC70	DCK	6	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1GX04DCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1GX04DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1GX04DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC1GX04DCKTG4	SC70	DCK	6	250	183.0	183.0	20.0
SN74LVC1GX04DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC1GX04DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74LVC1GX04DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
SN74LVC1GX04DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74LVC1GX04DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1GX04DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74LVC1GX04DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1GX04DCKT	SC70	DCK	6	250	202.0	201.0	28.0
SN74LVC1GX04DCKT	SC70	DCK	6	250	180.0	180.0	18.0
SN74LVC1GX04DCKT	SC70	DCK	6	250	180.0	180.0	18.0
SN74LVC1GX04DRLR	SOT-5X3	DRL	6	4000	202.0	201.0	28.0
SN74LVC1GX04DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0

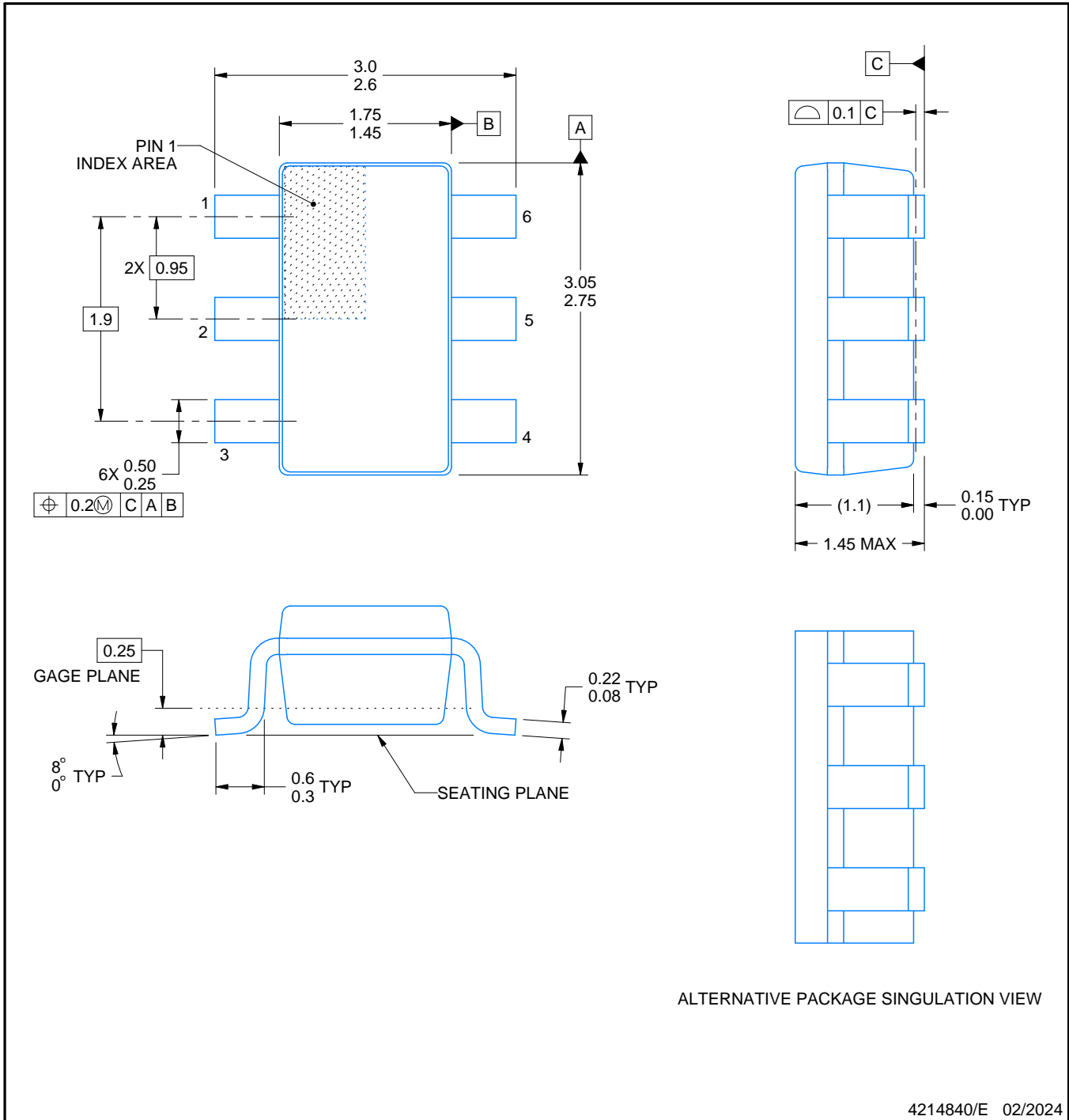
# DBV0006A



# PACKAGE OUTLINE

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

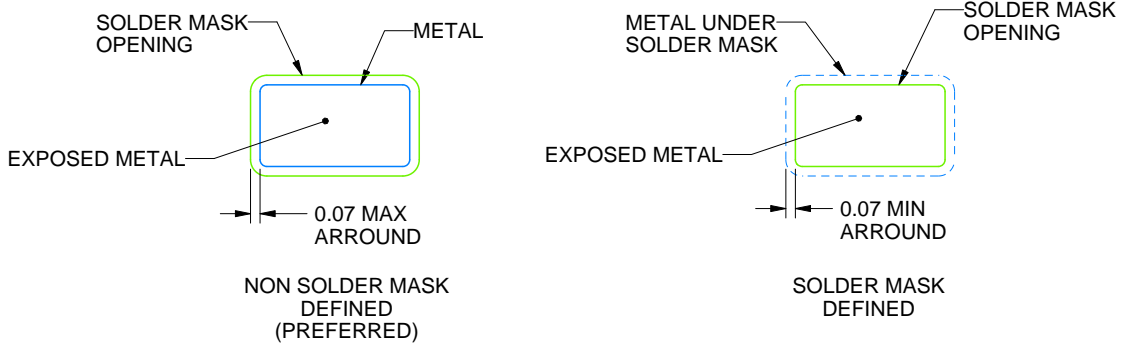
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/E 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

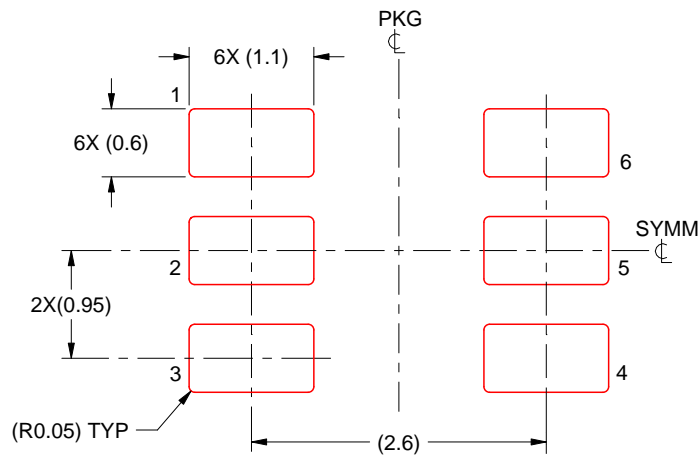
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214840/E 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

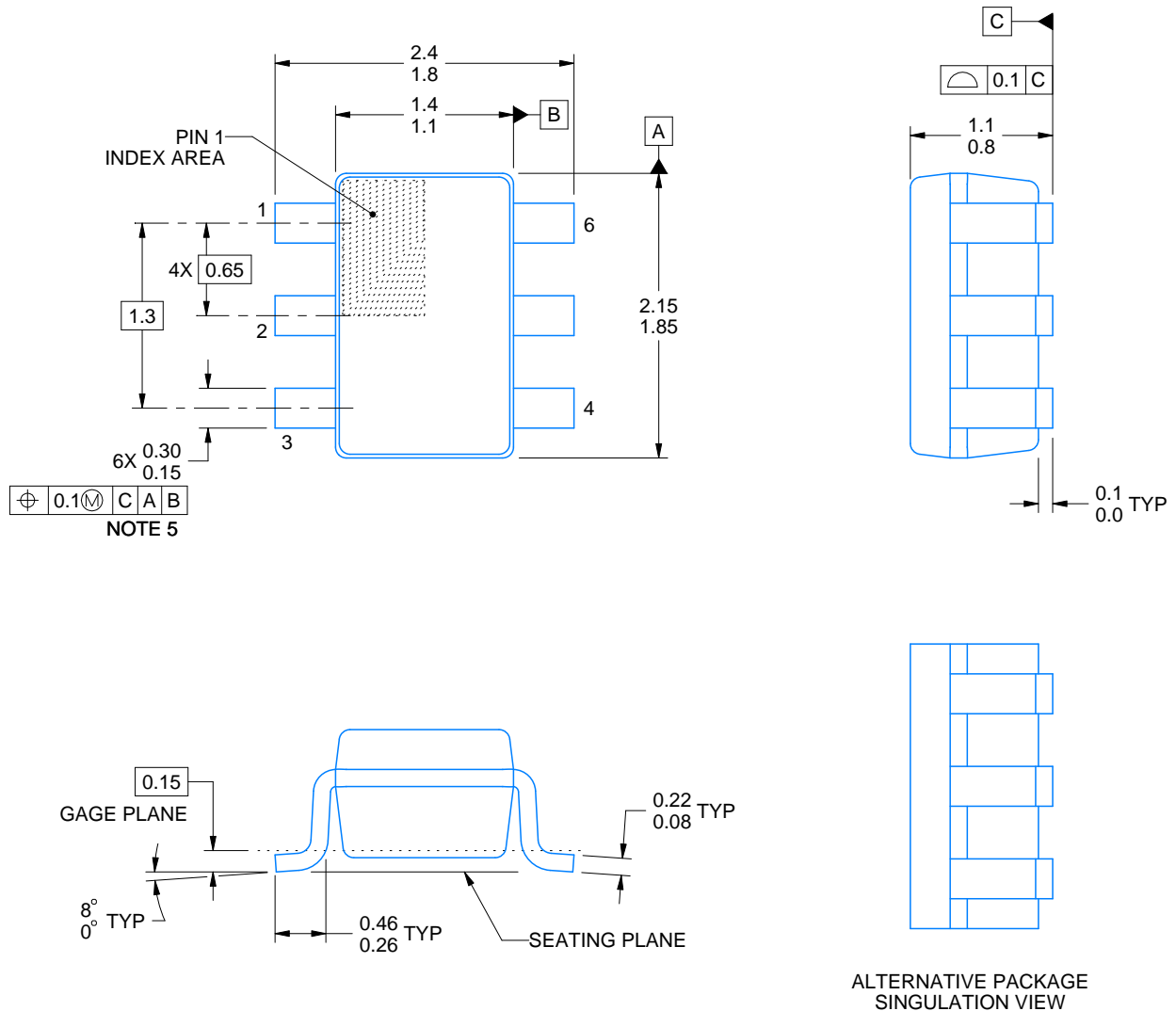
# DCK0006A



# PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR

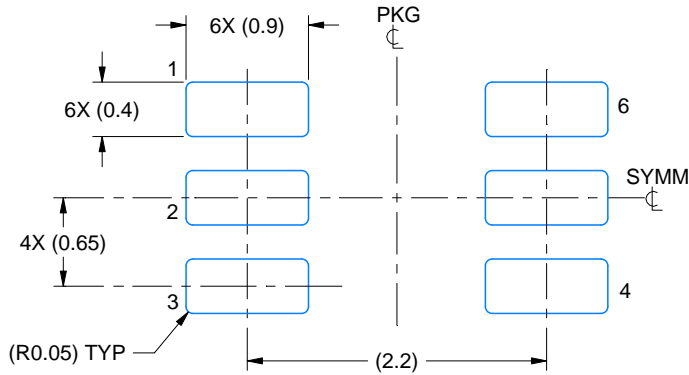


4214835/B 04/2024

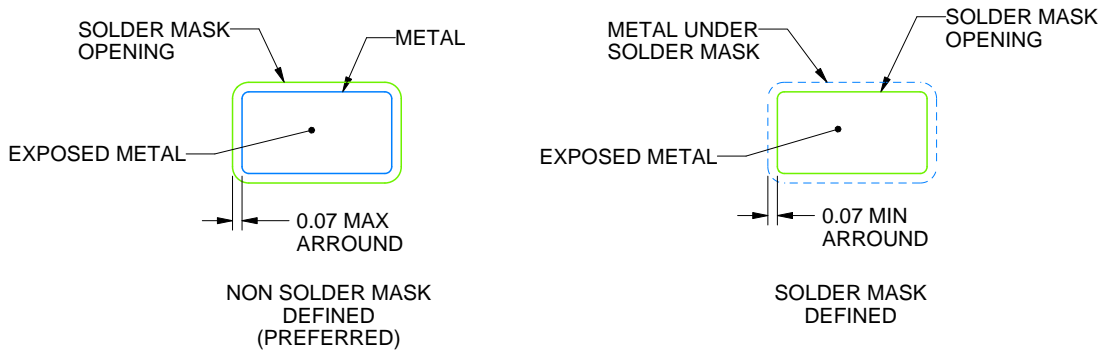
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.





LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4214835/B 04/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



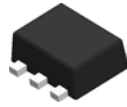
SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

4214835/B 04/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

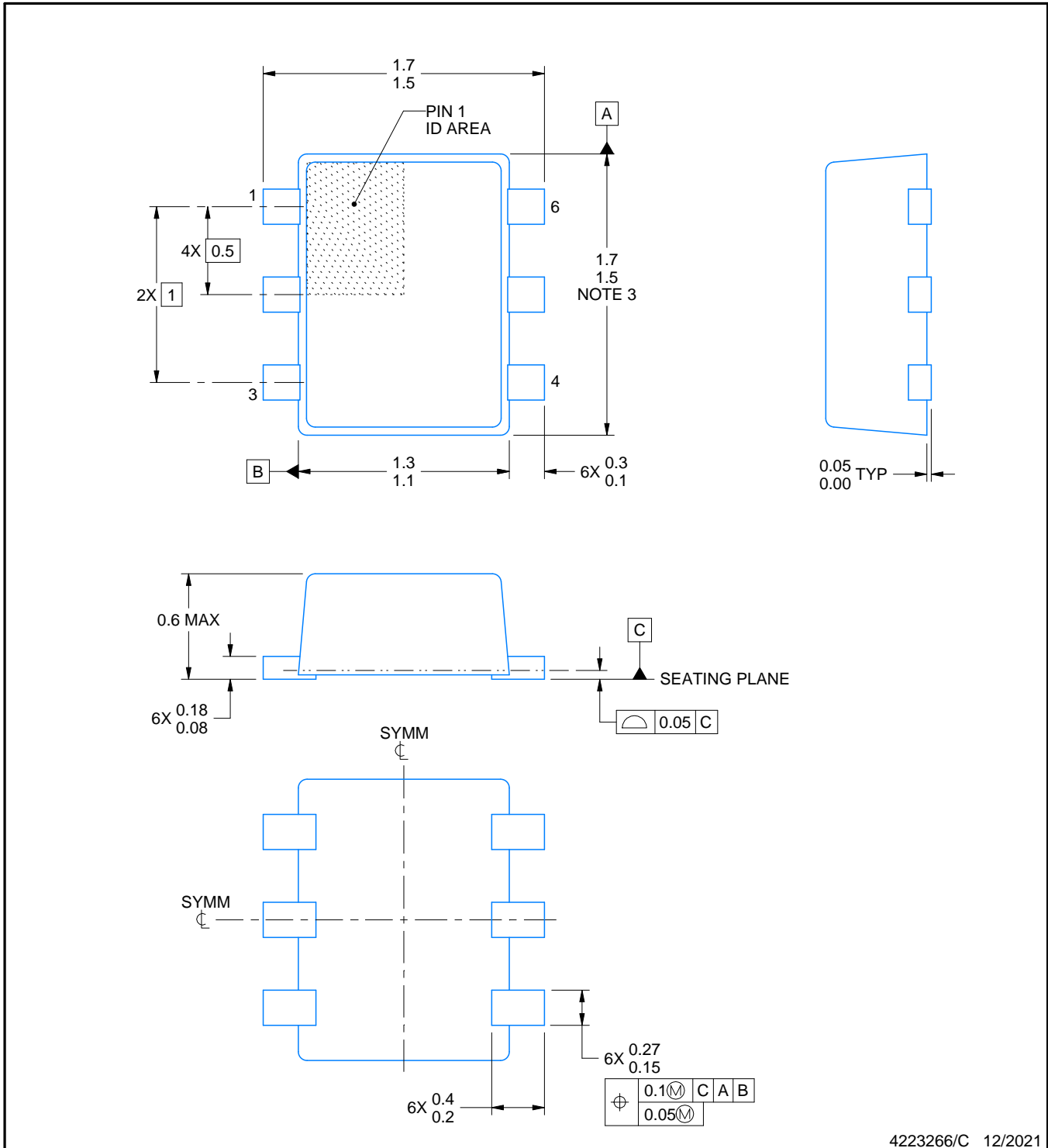
# DRL0006A



# PACKAGE OUTLINE

## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4223266/C 12/2021

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

# EXAMPLE BOARD LAYOUT

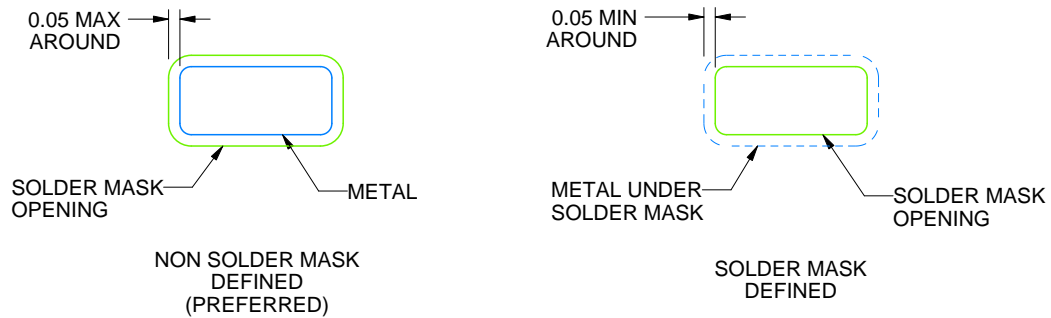
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDERMASK DETAILS

4223266/C 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

# EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4223266/C 12/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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