DS89C387 Twelve Channel CMOS Differential Line Driver

Check for Samples: DS89C387

FEATURES

- **Low Power I_{CC}: 1.5 mA Maximum**
- **Meets TIA/EIA-422-B (RS-422)**
- **Ensured AC Parameters:**
  - **Maximum Driver Skew −3 ns**
  - **Maximum Transition Time −10 ns**
- **Available in SSOP Packaging:**
  - **Requires 30% Less PCB Space than 3 DS34C87TMs**

DESCRIPTION

The DS89C387 is a high speed twelve channel CMOS differential driver that meets the requirements of TIA/EIA-422-B. The DS89C387 features a low I_{CC} specification of 1.5 mA maximum, which makes it ideal for battery powered and power conscious applications. The device replaces three DS34C87s and offers a PC board space savings up to 30%. The twelve channel driver is available in a SSOP package. The device is ideal for wide parallel bus applications.

Each TRI-STATE enable (EN) allows the driver outputs to be active or in a HI-impedance off state. Each enable is common to only two drivers for flexibility and control. The drivers may be disabled to turn off load current and to save power when data is not being transmitted.

The driver's input (DI) is compatible with both TTL and CMOS signal levels.

Connection Diagrams

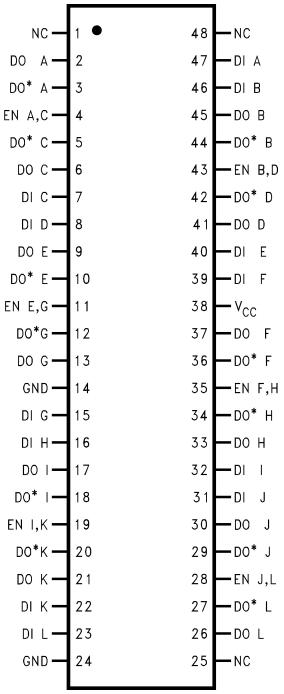
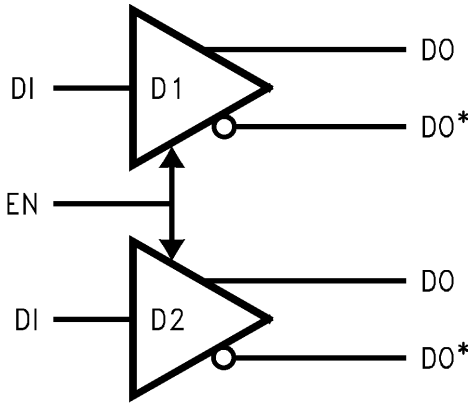


Figure 1. 48-Pin SSOP Package
See Package Number DL0048A



1/6 of package

Figure 2. Functional Diagram

Truth Table

Enable	Input	Outputs	
EN	DI	DO	DO*
L	X	Z	Z
H	H	H	L
H	L	L	H

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

Supply Voltage (V_{CC})	−0.5 to 7.0V
DC Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to 7V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±150 mA
DC V_{CC} or GND Current (I_{CC})	±500 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Junction Temperature	+150°C
Maximum Power Dissipation (P_D) @ 25°C(4)	
SSOP Package	1359 mW
Thermal Resistance	
θ_{JA}	81.7°C/W
θ_{JC}	31.7°C/W
Lead Temperature (T_L)	
(Soldering 4 sec.)	260°C
This device does not meet 2000V ESD rating.(5)	

(1) Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive; all currents out of device pins are negative.
(2) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be specified. They are not meant to imply that the device should be operated at these limits. The table of “Electrical Characteristics” provide conditions for actual device operation.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Ratings apply to ambient temperature at 25°C. Above this temperature derate SSOP (MEA) Package 10.9 mW/°C.
(5) ESD Rating: HBM (1.5 kΩ, 100 pF) Inputs ≥ 1500V Outputs ≥ 1000V EIAJ (0Ω, 200 pF) All Pins ≥ 350V

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
DS89C387T	−40	+85	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics(1)(2)

V_{CC} = 5V ±10% (unless otherwise specified)

Parameter		Test Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{OH}	High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = −20 mA	2.5	3.4		V
V_{OL}	Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 48 mA		0.3	0.5	V

(1) Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive; all currents out of device pins are negative.
(2) Unless otherwise specified, min/max limits apply across the −40°C to 85°C temperature range. All typicals are given for V_{CC} = 5V and T_A = 25°C.

DC Electrical Characteristics[1][2] (continued)

V_{CC} = 5V ±10% (unless otherwise specified)

Parameter		Test Conditions		Min	Typ	Max	Units
V_T	Differential Output Voltage	R_L = 100Ω See[3]		2.0	3.1		V
$\|V_T\|-\|\overline{V}_T\|$	Difference In Differential Output	R_L = 100Ω See[3]				0.4	V
V_{OS}	Common Mode Output Voltage	R_L = 100Ω See[3]			2.0	3.0	V
$\|V_{OS}-\overline{V}_{OS}\|$	Difference In Common Mode Output	R_L = 100Ω See[3]				0.4	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, V_{IH}, or V_{IL}				±1.0	µA
I_{CC}	Quiescent Supply Current	I_{OUT} = 0 µA, V_{IN} = V_{CC} or GND			600	1500	µA
		V_{IN} = 2.4V or 0.5V[4]			0.8	2.0	mA
I_{OZ}	TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND Control = V_{IL}			±0.5	±5.0	µA
I_{SC}	Output Short Circuit Current	V_{IN} = V_{CC} or GND See[3] and [5]		−30	−115	−150	mA
I_{OFF}	Power Off Output Leakage Current	V_{CC} = 0V See[6]	V_{OUT} = 6V			100	µA
			V_{OUT} = −0.25V			−100	µA

(3) See TIA/EIA-422-B for exact test conditions.
(4) Measured per input. All other inputs at V_{CC} or GND.
(5) This is the current sourced when a high output is shorted to ground. Only one output at a time should be shorted.
(6) See TIA/EIA-422-B for exact test conditions.

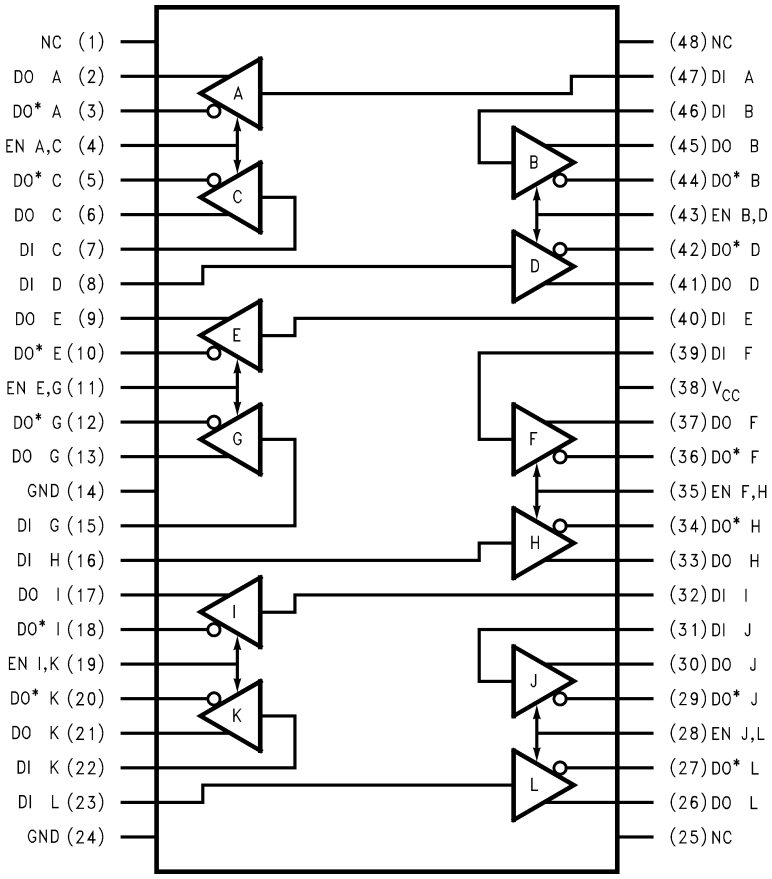
Switching Characteristics [1]

V_{CC} = 5V ±10%, t_r, t_f ≤ 6 ns (Figure 3, Figure 4, Figure 5, and Figure 6)

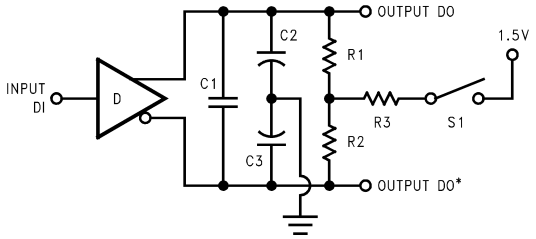
Parameter		Test Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	S1 Open	2	6	11	ns
Skew	See[2]	S1 Open	0	0.5	3	ns
t_{TLH}, t_{THL}	Differential Output Rise And Fall Times	S1 Open		6	10	ns
t_{PZH}	Output Enable Time	S1 Closed		12	25	ns
t_{PZL}	Output Enable Time	S1 Closed		13	26	ns
t_{PHZ}	Output Disable Time[3]	S1 Closed		4	8	ns
t_{PLZ}	Output Disable Time[3]	S1 Closed		6	12	ns
C_{PD}	Power Dissipation Capacitance[4]			100		pF
C_{IN}	Input Capacitance			6		pF

(1) Unless otherwise specified, min/max limits apply across the −40°C to 85°C temperature range. All typicals are given for V_{CC} = 5V and T_A = 25°C.
(2) Skew is defined as the difference in propagation delays between complementary outputs at the crossing point.
(3) Output disable time is the delay from the control input being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.
(4) C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V^2CC\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

Logic Diagram



Parameter Measurement Information



C1 = C2 = C3 = 40 pF (including Probe and Jig Capacitance), R1 = R2 = 50Ω, R3 = 500Ω

Figure 3. AC Test Circuit

Parameter Measurement Information (continued)

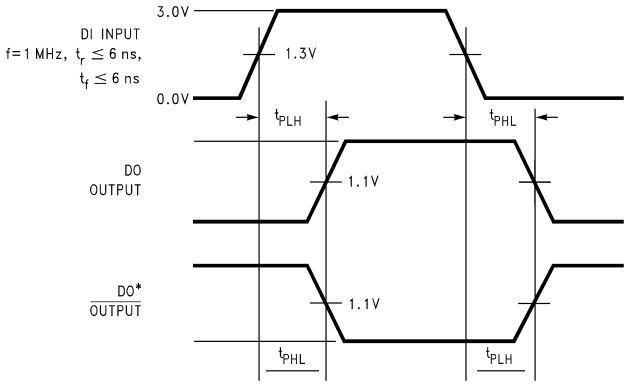


Figure 4. Propagation Delays

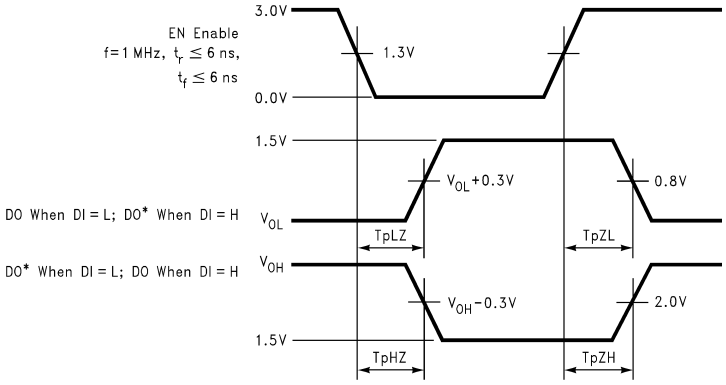
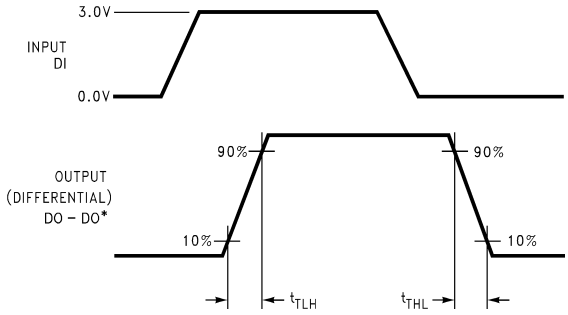


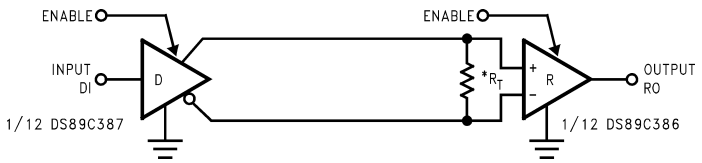
Figure 5. Enable and Disable Times



Input pulse; f = 1 MHz, 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns

Figure 6. Differential Rise and Fall Times

Typical Application



* R_T is optional although highly recommended to reduce reflection.

Figure 7. Two-Wire Balanced System, RS-422

APPLICATION INFORMATION

SKEW

Skew may be thought of in a lot of different ways, the next few paragraphs should clarify what is represented by "Skew" in the datasheet and how it is determined. Skew, as used in this databook, is the absolute value of a mathematical difference between two propagation delays. This is commonly accepted throughout the semiconductor industry. However, there is no standardized method of measuring propagation delay, from which skew is calculated, of differential line drivers. Elucidating, the voltage level, at which propagation delays are measured, on both input and output waveforms are not always consistant. Therefore, skew calculated in this datasheet, may not be calculated the same as skew defined in another. This is important to remember whenever making a skew comparison.

Skew may be calculated for the DS89C387, from many different propagation delay measurements. They may be classified into three categories, single-ended, differential, and complementry. Single-ended skew is calculated from t_{PHL} and t_{PLH} measurements (see Figure 9 and Figure 11). Differential skew is calculated from t_{PHLD} and t_{PLHD} measurements (see Figure 12 and Figure 13). Complementry skew is calculated from t_{PHL} and t_{PLH} measurements (see Figure 14 and Figure 15).

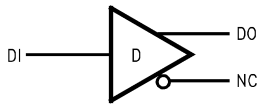


Figure 8. (Circuit 1) – Circuits for Measuring Single-Ended Propagation Delays (See Figure 11)

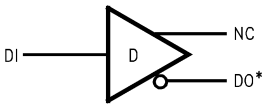


Figure 9. (Circuit 2) – Circuits for Measuring Single-Ended Propagation Delays (See Figure 11)

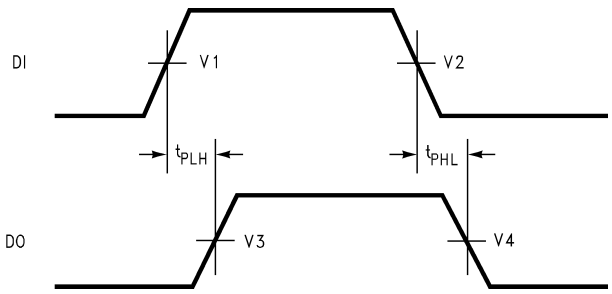


Figure 10. Waveforms for Circuit 1 – Propagation Delay Waveforms for Circuit 1 and Circuit 2 (See Figure 9)

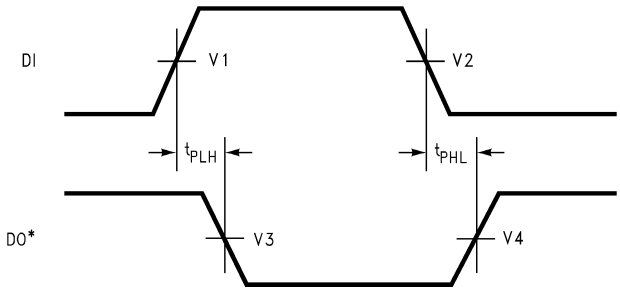


Figure 11. Waveforms for Circuit 2 – Propagation Delay Waveforms for Circuit 1 and Circuit 2 (See Figure 9)

In Figure 4, VX, where X is a number, is the waveform voltage level at which the propagation delay measurement either starts or stops. Furthermore, V1 and V2 are normally identical. The same is true for V3 and V4. However, as mentioned before, these levels are not standardized and may vary, even with similar devices from other companies. Also note, NC (no connection) in Figure 3 means the pin is not used in propagation delay measurement for the corresponding circuit.

The single-ended skew provides information about the pulse width distortion of the output waveform. The lower the skew, the less the output waveform will be distorted. For best case, skew would be zero, and the output duty cycle would be 50%, assuming the input has a 50% duty cycle.

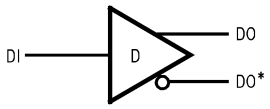


Figure 12. (Circuit 3) – Circuit for Measuring Differential Propagation Delays (See Figure 13)

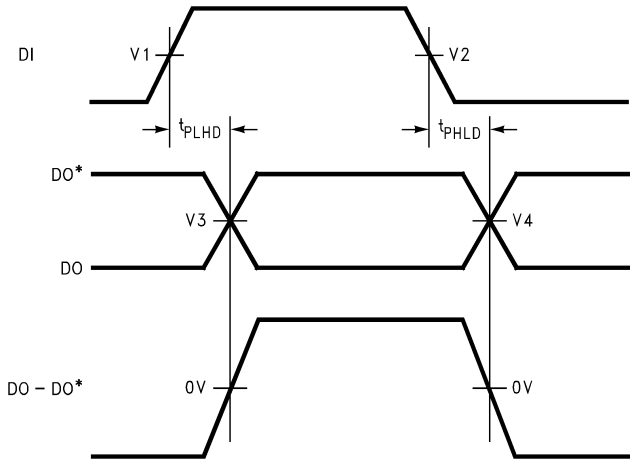


Figure 13. Waveforms for Circuit 3 – Propagation Delay Waveforms for Circuit 3 (See Figure 12)

For differential propagation delays, V1 should equal V2. Furthermore, the crossing point of DO and DO* corresponds to zero volts on the differential waveform (see bottom waveform in Figure 13). This is true whether V3 equals V4 or not. However, if V3 and V4 are specified voltages, then V3 and V4 are less likely to be equal to the crossing point voltage. Thus, the differential propagation delays will not be measured to zero volts on the differential waveform.

The differential skew also provides information about the pulse width distortion of the differential output waveform relative to the input waveform. The higher the skew, the greater the distortion of the differential output waveform. Assuming the input has a 50% duty cycle, the differential output will have a 50% duty cycle if skew equals zero and less than a 50% duty cycle if skew is greater than zero.

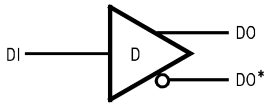


Figure 14. (Circuit 4) – Circuit for Measuring Complementary Skew (See Figure 15)

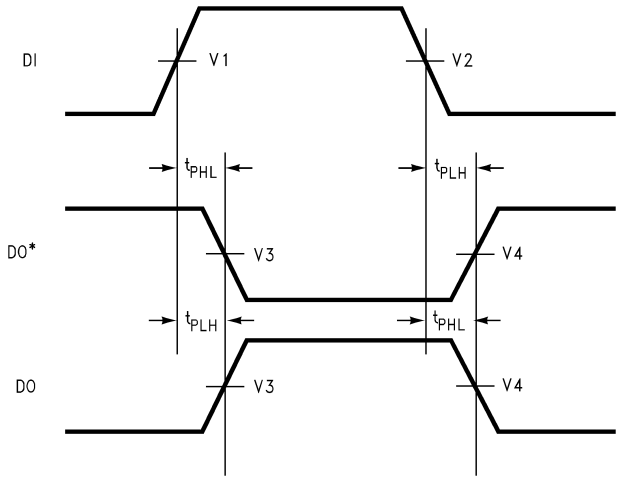


Figure 15. Waveforms for Circuit 4 – Waveforms for Circuit 4 (See Figure 14)

Complementary skew is calculated from single-ended propagation delay measurements on complementary output signals, DO and DO*. Note, when V3 and V4 are absolute values, they are identical on DO and DO*; but vary whenever they are relative values.

The complementary skew reveals information about the contour of the rising and falling edge of the differential output signal of the driver. This is important information because the receiver will interpret the differential output signal. If the differential transitions do not continuously ascend or decend through the receivers threshold region, errors may occur. Errors may also occur if the transitions are too slow.

In addition, complementary skew provides information about the common mode modulation of the driver. The common mode voltage is represented by (DO–DO*)/2. This information may be used as a means for determining EMI affects.

Only “Skew” is specified in this datasheet for the DS89C387. It refers to the complementary skew of the driver. Complementary skew is measured at both V3 and V4 (see Figure 15).

More information can be calculated from the propagation delays. The channel to channel and device to device skew may be calculated in addition to the types of skew mentioned previously. These parameters provide timing performance information beneficial when designing. The channel to channel skew is calculated from the variation in propagation delay from receiver to receiver within one package. The device to device skew is calculated from the variation in propagation delay from one DS89C387 to another DS89C387.

For the DS89C387, the maximum channel to channel skew is 9 ns (t_p max–t_p min) where t_p is the low to high or high to low propagation delay. The minimum channel to channel skew is 0 ns since it is possible for all 12 drivers to have identical propagation delays. Note, this is best and worst case calculations used whenever Skew (channel) is not independently characterized and specified in the datasheet. The device to device skew may be calculated in the same way and the results are the same. Therefore, the device to device skew is 9 ns and 0 ns maximum and minimum respectively.

Table 1. DS89C387 Skew Table

Parameter	Min	Typ	Max	Units
Skew (comp.)	0	0.5	3	ns
Skew (channel)	0		9	ns
Skew (device)	0		9	ns

Note Skew (comp.) in Table 1 is the same as “Skew” in the datasheet. Also Skew (channel) and Skew (device) are calculations, but are specified by the propagation delay tests. Both Skew (channel) and Skew (device) would normally be tighter whenever specified from characterization data.

The information in this section of the datasheet is to help clarity how skew is defined in this datasheet. This should help when designing the DS89C387 into most applications.

DS89C387 Equivalent Input/Output Circuits

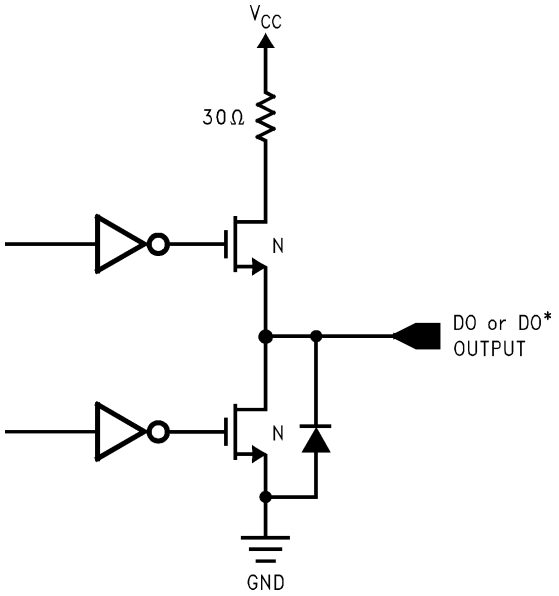


Figure 16. Driver Output Equivalent Circuit

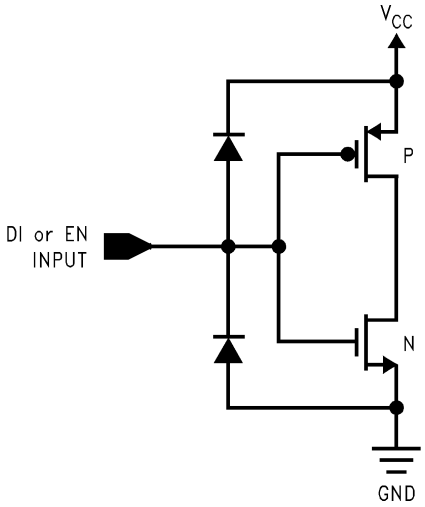


Figure 17. Driver Input or Driver Enable Equivalent Circuit

Table 2. Pin Descriptions

Pin No.	Pin Name	Pin Description
7, 8, 15, 16, 22, 23, 31, 32, 39, 40, 46, 47	DI	TTL/CMOS Compatible Driver Input
2, 6, 9, 13, 17, 21, 26, 30, 33, 37, 41, 45	DO	Non-Inverting Driver Output Pin
3, 5, 10, 12, 18, 20, 27, 29, 34, 36, 44, 44	DO*	Inverting Driver Output Pin
4, 11, 19, 28, 35, 43	EN	Active High Dual Driver Enabling Pin
38	V_{CC}	Positive Power Supply Pin +5 ±10%
14, 24	GND	Device Ground Pin
1, 25, 48	NC	Unused Pin (NOT CONNECTED)

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS89C387TMEA/NOPB	NRND	SSOP	DL	48	29	Pb-Free (RoHS)	CU SN	Level-2A-260C-4 WEEK	-40 to 85	DS89C387T MEA	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

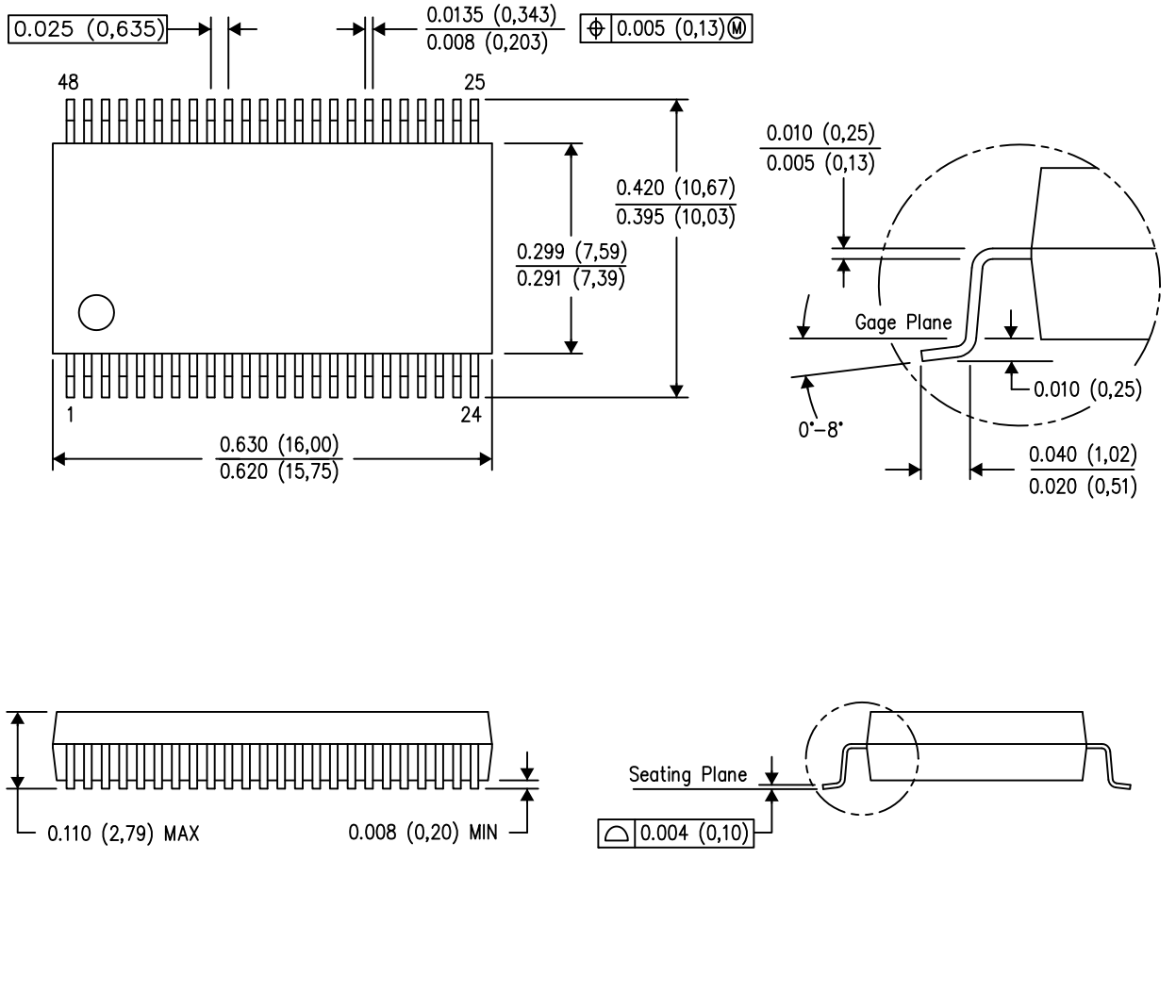
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

DL (R–PDSO–G48) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

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