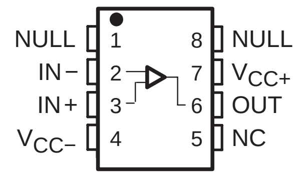
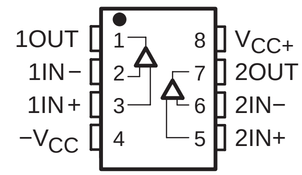
- **High Speed**
  - **180 MHz Bandwidth (G = 1, −3 dB)**
  - **400 V/μs Slew Rate**
  - **40-ns Settling Time (0.1%)**
- **High Output Drive, I_O = 115 mA (typ)**
- **Excellent Video Performance**
  - **75 MHz 0.1 dB Bandwidth (G = 1)**
  - **0.02% Differential Gain**
  - **0.02° Differential Phase**
- **Very Low Distortion**
  - **THD = −72 dBc at f = 1 MHz**
- **Wide Range of Power Supplies**
  - **V_{CC} = ±5 V to ±15 V**
- **Available in Standard SOIC, MSOP PowerPAD™, JG, or FK Package**
- **Evaluation Module Available**

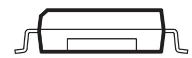
THS4061
JG, D AND DGN PACKAGE
(TOP VIEW)



THS4062
D AND DGN PACKAGE
(TOP VIEW)

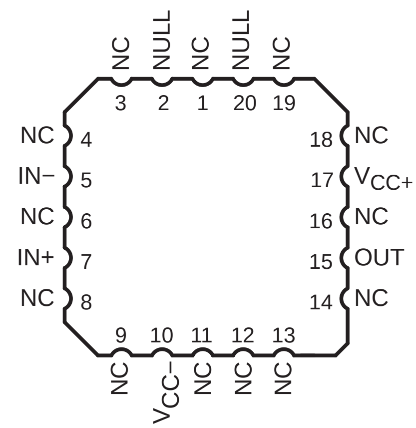


NC − No internal connection



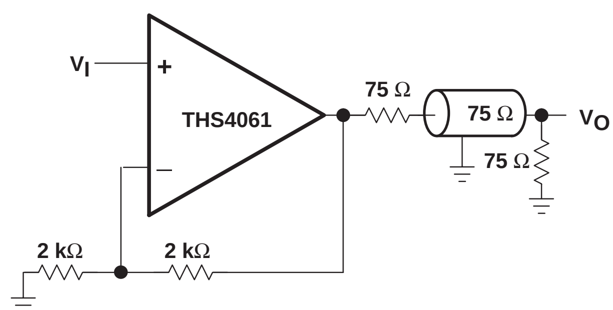
Cross-Section View Showing PowerPAD Option (DGN)

THS4061
FK PACKAGE
(TOP VIEW)



description

The THS4061 and THS4062 are general-purpose, single/dual, high-speed voltage feedback amplifiers ideal for a wide range of applications including video, communication, and imaging. The devices offer very good ac performance with 180-MHz bandwidth, 400-V/μs slew rate, and 40-ns settling time (0.1%). The THS4061/2 are stable at all gains for both inverting and noninverting configurations. These amplifiers have a high output drive capability of 115 mA and draw only 7.8 mA supply current per channel. Excellent professional video results can be obtained with the low differential gain/phase errors of 0.02%/0.02° and wide 0.1 db flatness to 75 MHz. For applications requiring low distortion, the THS4061/2 is ideally suited with total harmonic distortion of −72 dBc at f = 1 MHz.



LINE DRIVER (G = 2)

CAUTION: The THS4061 and THS4062 provide ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality

RELATED DEVICES

DEVICE	DESCRIPTION
THS4011/2	290-MHz Low Distortion High-Speed Amplifiers
THS4031/2	100-MHz Low Noise High Speed-Amplifiers
THS4061/2	180-MHz High-Speed Amplifiers

AVAILABLE OPTIONS

T_A	NUMBER OF CHANNELS	PACKAGED DEVICES				MSOP SYMBOL	EVALUATION MODULES
		PLASTIC SMALL OUTLINE† (D)	PLASTIC MSOP† (DGN)	CERAMIC DIP (JG)	CHIP CARRIER (FK)		
0°C to 70°C	1	THS4061CD	THS4061CDGN	—	—	TIABS	THS4061EVM
	2	THS4062CD	THS4062CDGN	—	—	TIABM	THS4062EVM
−40°C to 85°C	1	THS4061ID	THS4061IDGN	—	—	TIABT	—
	2	THS4062ID	THS4062IDGN	—	—	TIABN	—
−55°C to 125°C	1	—	—	THS4061MJG	THS4061MFK	—	—

† The D and DGN packages are available taped and reeled. Add an R suffix to the device type (i.e., THS4061CDGNR).

functional block diagram

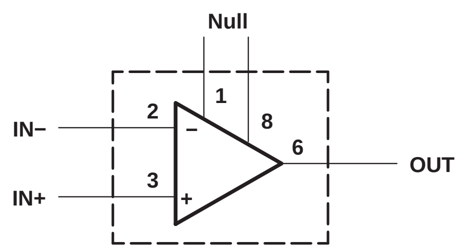


Figure 1. THS4061 − Single Channel

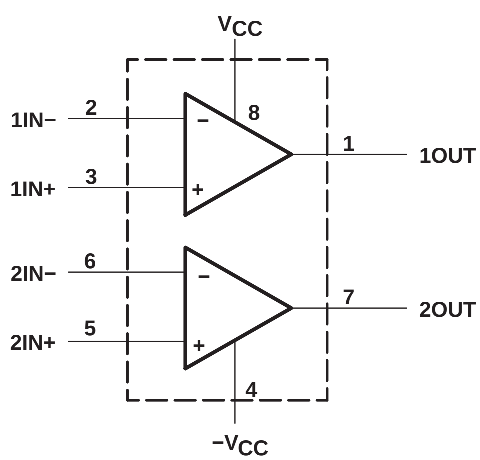


Figure 2. THS4062 − Dual Channel

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, $V_{CC}+$ to $V_{CC}-$ . . . . . 33 V
Input voltage, V_I . . . . . $\pm V_{CC}$
Output current, I_O . . . . . 150 mA
Differential input voltage, V_{IO} . . . . . ±4 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Maximum junction temperature, T_J . . . . . 150°C
Operating free-air temperature, T_A: C-suffix . . . . . 0°C to 70°C
I-suffix . . . . . −40°C to 85°C
M-suffix . . . . . −55°C to 125°C
Storage temperature, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, D and DGN package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds, JG package . . . . . 300°C
Case temperature for 60 seconds, FK package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	740 mW	6 mW/°C	475 mW	385 mW	—
DGN‡	2.14 W	17.1 mW/°C	1.37 W	1.11 W	—
JG	1057 mW	8.4 mW/°C	627 mW	546 mW	210 mW
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW

‡ The DGN package incorporates a PowerPAD on the underside of the device. This acts as a heatsink and must be connected to a thermal dissipation plane for proper power dissipation. Failure to do so can result in exceeding the maximum specified junction temperature, which could permanently damage the device.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}+$ and $V_{CC}-$	Dual supply	±4.5		±16	V
	Single supply	9		32	
Operating free-air temperature, T_A	C-suffix	0		70	°C
	I-suffix	−40		85	
	M-suffix	−55		125	

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS†		THS4061C/I, THS4062C/I MIN	TYP	MAX	UNIT
BW	Dynamic performance small-signal bandwidth (−3 dB)	V_{CC} = ±5 V	Gain = 1		180		MHz
		V_{CC} = ±15 V	Gain = −1		50		MHz
		V_{CC} = ±5 V			50		
	Bandwidth for 0.1 dB flatness	V_{CC} = ±15 V	Gain = 1		75		MHz
		V_{CC} = ±5 V			20		
SR	Slew rate	V_{CC} = ±15 V	Gain = −1		400		V/µs
		V_{CC} = ±5 V			350		
t_s	Settling time to 0.1%	V_{CC} = ±15 V, 5-V step (0 V to 5 V)	Gain = −1		40		ns
		V_{CC} = ±5 V, V_O = −2.5 V to 2.5 V,			40		
	Settling time to 0.01%	V_{CC} = ±15 V, 5-V step (0 V to 5 V)	Gain = −1		140		ns
		V_{CC} = ±5 V, V_O = −2.5 V to 2.5 V,			150		

† Full range = 0°C to 70°C for C suffix and −40°C to 85°C for I suffix

noise/distortion performance

PARAMETER		TEST CONDITIONS†		THS4061C/I, THS4062C/I MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	f = 1 MHz			−72		dBc
V_n	Input voltage noise	f = 10 kHz, V_{CC} = ±5 V or ±15 V			14.5		nV/√Hz
I_n	Input current noise	f = 10 kHz, V_{CC} = ±5 V or ±15 V			1.6		pA/√Hz
	Differential gain error	Gain = 2, NTSC, 40 IRE modulation	V_{CC} = ±15 V		0.02 %		
			V_{CC} = ±5 V		0.02 %		
	Differential phase error	Gain = 2, NTSC, 40 IRE modulation	V_{CC} = ±15 V		0.02°		
			V_{CC} = ±5 V		0.06°		
	Channel-to-channel crosstalk (THS4062 only)	V_{CC} = ±5 V or ±15 V, f = 1 MHz			65		dB

† Full range = 0°C to 70°C for C suffix and −40°C to 85°C for I suffix

dc performance

PARAMETER		TEST CONDITIONS†		THS4061C/I, THS4062C/I MIN	TYP	MAX	UNIT
	Open loop gain	V_{CC} = ±15 V, V_O = ±10 V, R_L = 1 kΩ	T_A = 25°C	5	15		V/mV
			T_A = full range	4			
		V_{CC} = ±5 V, V_O = ±2.5 V, R_L = 1 kΩ	T_A = 25°C	2.5	8		V/mV
			T_A = full range	2			
V_{OS}	Input offset voltage	V_{CC} = ±5 V or ±15 V	T_A = full range		2.5	8	mV
	Offset drift	V_{CC} = ±5 V or ±15 V			15		µV/°C
I_{IB}	Input bias current	V_{CC} = ±5 V or ±15 V	T_A = full range		3	6	µA
I_{OS}	Input offset current	V_{CC} = ±5 V or ±15 V	T_A = full range		75	250	nA
	Offset current drift	T_A = full range			0.3		nA/°C

† Full range = 0°C to 70°C for C suffix and −40°C to 85°C for I suffix

electrical characteristics at $T_A = 25°C$, $V_{CC} = ±15$ V, $R_L = 150\ \Omega$ (unless otherwise noted) (continued)

input characteristics

PARAMETER		TEST CONDITIONS†			THS4061C/I, THS4062C/I MIN	TYP	MAX	UNIT
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V			±13.8	±14.1		V
		V_{CC} = ±5 V			±3.8	±4.3		
CMRR	Common mode rejection ratio	V_{CC} = ±15 V,	V_{ICR} = ±12 V	T_A = full range	70	110		dB
		V_{CC} = ±5 V,	V_{ICR} = ±2.5 V		70	95		
R_I	Input resistance					1		MΩ
C_i	Input capacitance					2		pF

† Full range = 0°C to 70°C for C suffix and −40°C to 85°C for I suffix

output characteristics

PARAMETER		TEST CONDITIONS†		THS4061C/I, THS4062C/I MIN	TYP	MAX	UNIT
V_O	Output voltage swing	V_{CC} = ±15 V	R_L = 250 Ω	±11.5	±12.5		V
		V_{CC} = ±5 V	R_L = 150 Ω	±3.2	±3.5		
		V_{CC} = ±15 V	R_L = 1 kΩ	±13	±13.5		V
		V_{CC} = ±5 V		±3.5	±3.7		
I_O	Output current	V_{CC} = ±15 V	R_L = 20 Ω	80	115		mA
		V_{CC} = ±5 V		50	75		
I_{SC}	Short-circuit current	V_{CC} = ±15 V			150		mA
R_O	Output resistance	Open loop			12		Ω

† Full range = 0°C to 70°C for C suffix and −40°C to 85°C for I suffix

power supply

PARAMETER		TEST CONDITIONS†		THS4061C/I, THS4062C/I MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage operating range	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Quiescent current (per amplifier)	V_{CC} = ±15 V	T_A = full range		7.8	10.5	mA
		V_{CC} = ±5 V			7.3	10	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = 25°C	70	78		dB
			T_A = full range	68			

† Full range = 0°C to 70°C for C suffix and −40°C to 85°C for I suffix

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS†		THS4061M MIN	THS4061M TYP	THS4061M MAX	UNIT
BW	Unity-gain bandwidth	Closed loop, R_L = 1 kΩ	V_{CC} = ±15 V	*140	180		MHz
	Dynamic performance small-signal bandwidth (−3 dB)	V_{CC} = ±15 V	Gain = 1		180		MHz
		V_{CC} = ±5 V			180		
		V_{CC} = ±15 V	Gain = −1		50		MHz
		V_{CC} = ±5 V			50		
	Bandwidth for 0.1 dB flatness	V_{CC} = ±15 V	Gain = 1		75		MHz
		V_{CC} = ±5 V			20		
SR	Slew rate	V_{CC} = ±15 V R_L = 1 kΩ		*400	500		V/µs
t_s	Settling time to 0.1%	V_{CC} = ±15 V, 5-V step (0 V to 5 V)	Gain = −1		40		ns
		V_{CC} = ±5 V, V_O = −2.5 V to 2.5 V,			40		
	Settling time to 0.01%	V_{CC} = ±15 V, 5-V step (0 V to 5 V)	Gain = −1		140		ns
		V_{CC} = ±5 V, V_O = −2.5 V to 2.5 V,			150		

† Full range = −55°C to 125°C for M suffix
*This parameter is not tested.

noise/distortion performance

PARAMETER		TEST CONDITIONS†		THS4061M MIN	THS4061M TYP	THS4061M MAX	UNIT
THD	Total harmonic distortion	f = 1 MHz			−72		dBc
V_n	Input voltage noise	f = 10 kHz, V_{CC} = ±5 V or ±15 V			14.5		nV/√Hz
I_n	Input current noise	f = 10 kHz, V_{CC} = ±5 V or ±15 V			1.6		pA/√Hz
	Differential gain error	Gain = 2, NTSC, 40 IRE Modulation	V_{CC} = ±15 V		0.02		%
			V_{CC} = ±5 V		0.02		
	Differential phase error	Gain = 2, NTSC, 40 IRE Modulation	V_{CC} = ±15 V		0.02°		
			V_{CC} = ±5 V		0.06°		

† Full range = −55°C to 125°C for M suffix

dc performance

PARAMETER		TEST CONDITIONS†		THS4061M MIN	THS4061M TYP	THS4061M MAX	UNIT
	Open loop gain	V_{CC} = ±15 V, V_O = ±10 V, R_L = 1 kΩ	T_A = full range	5	9		V/mV
		V_{CC} = ±5 V, V_O = ±2.5 V, R_L = 1 kΩ		2.5	6		
V_{IO}	Input offset voltage	V_{CC} = ±5 V or ±15 V R_L = 1 kΩ	T_A = 25°C		2.5	8	mV
			T_A = full range			9	mV
	Offset drift	V_{CC} = ±5 V or ±15 V R_L = 1 kΩ	T_A = full range		15		µV/°C
I_{IB}	Input bias current	V_{CC} = ±5 V or ±15 V R_L = 1 kΩ	T_A = full range		3	6	µA
I_{IO}	Input offset current	V_{CC} = ±5 V or ±15 V R_L = 1 kΩ	T_A = full range		75	250	nA
	Offset current drift	V_{CC} = ±5 V or ±15 V R_L = 1 kΩ	T_A = full range		0.3		nA/°C

† Full range = −55°C to 125°C for M suffix

electrical characteristics at T_A = full range, V_{CC} = ±15 V, R_L = 1 kΩ (unless otherwise noted) (continued)

input characteristics

PARAMETER		TEST CONDITIONS†		THS4061M			UNIT
				MIN	TYP	MAX	
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V		±13.8	±14.1		V
		V_{CC} = ±5 V		±3.8	±4.3		
CMRR	Common mode rejection ratio	V_{CC} = ±15 V,	V_{ICR} = ±12 V	70	86		dB
		V_{CC} = ±5 V,	V_{ICR} = ±2.5 V	80	90		
R_I	Input resistance				1		MΩ
C_i	Input capacitance				2		pF

† Full range = −55°C to 125°C for M suffix

output characteristics

PARAMETER		TEST CONDITIONS†		THS4061M			UNIT
				MIN	TYP	MAX	
V_O	Output voltage swing	V_{CC} = ±15 V	R_L = 250 Ω	±12	±13.1		V
		V_{CC} = ±5 V	R_L = 150 Ω	±3.2	±3.5		
		V_{CC} = ±15 V	R_L = 1 kΩ	±13	±13.5		V
		V_{CC} = ±5 V		±3.5	±3.7		
I_O	Output current	V_{CC} = ±15 V	R_L = 20 Ω	70	115		mA
		V_{CC} = ±5 V		50	75		
I_{SC}	Short-circuit current	V_{CC} = ±15 V	T_A = 25°C		150		mA
R_O	Output resistance	Open loop			12		Ω

† Full range = −55°C to 125°C for M suffix

power supply

PARAMETER		TEST CONDITIONS†		THS4061M			UNIT
				MIN	TYP	MAX	
V_{CC}	Supply voltage operating range	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Quiescent current	V_{CC} = ±15 V	T_A = 25°C		7.8	9	mA
		V_{CC} = ±5 V			7.3	8.5	
		V_{CC} = ±15 V	T_A = full range			11	
		V_{CC} = ±5 V				10.5	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = 25°C	76	80		dB
			T_A = full range	74	78		

† Full range = −55°C to 125°C for M suffix

TYPICAL CHARACTERISTICS

			FIGURE
I_{IB}	Input bias current	vs Free-air temperature	3
V_{IO}	Input offset voltage	vs Free-air temperature	4
	Open-loop gain	vs Frequency	5
	Phase	vs Frequency	5
	Differential gain	vs Number of loads	6, 8
	Differential phase	vs Number of loads	7, 9
	Closed-loop gain	vs Frequency	10, 11
	Output amplitude	vs Frequency	12, 13
CMRR	Common-mode rejection ratio	vs Frequency	14
PSRR	Power supply rejection ratio	vs Frequency	15
		vs Free-air temperature	16
$V_{O(PP)}$	Output voltage swing	vs Supply voltage	17
I_{CC}	Supply current	vs Free-air temperature	18
E_{nv}	Noise spectral density	vs Frequency	19
THD	Total harmonic distortion	vs Frequency	20, 21
	Crosstalk	vs Frequency	22, 23

TYPICAL CHARACTERISTICS

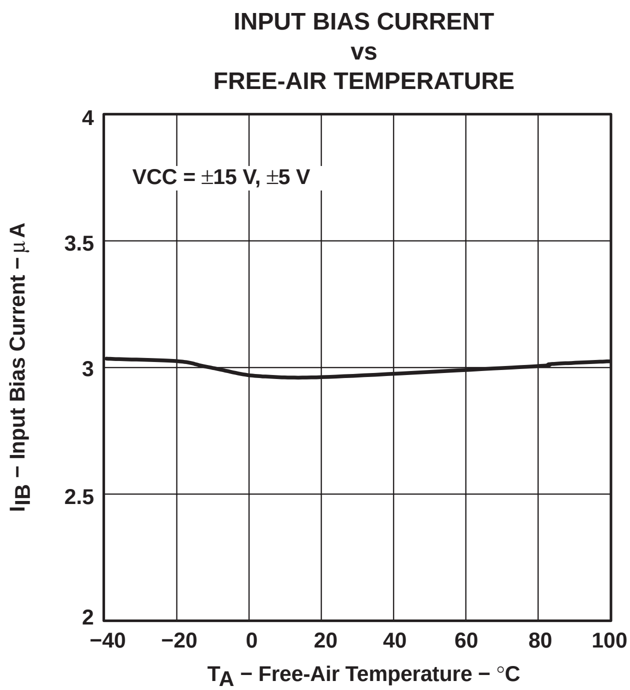


Figure 3

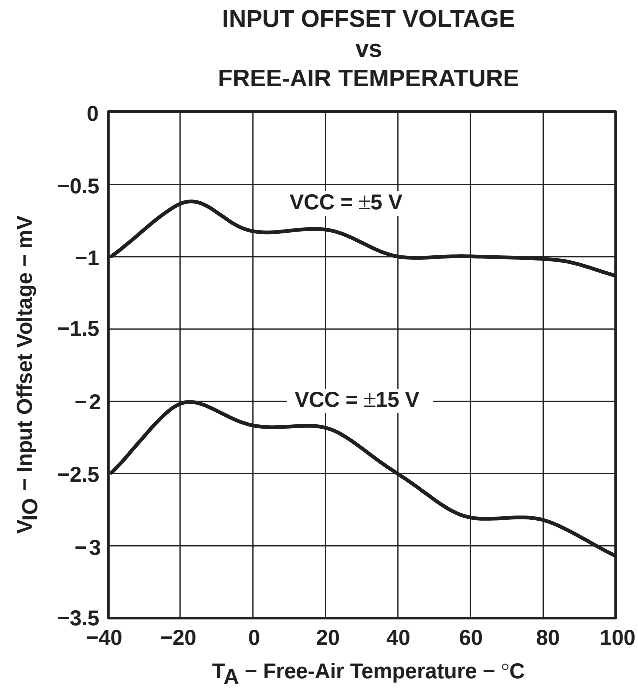


Figure 4

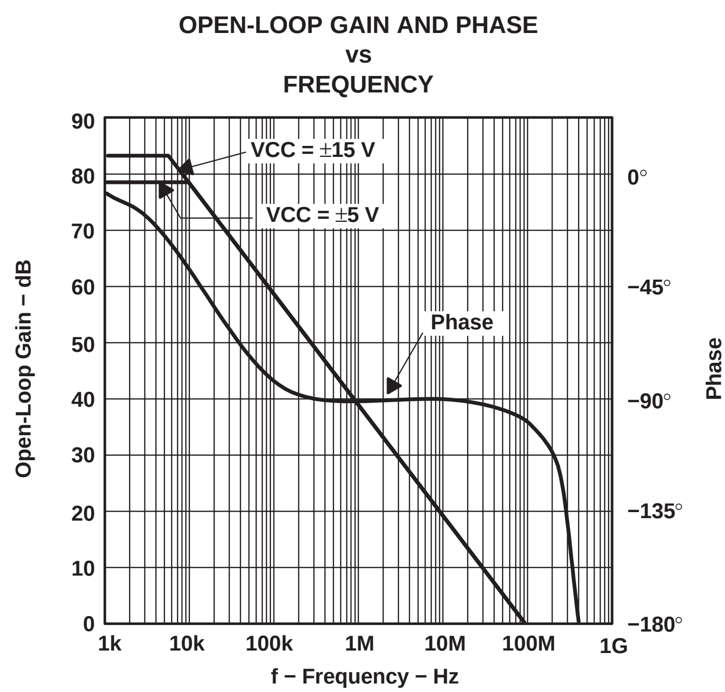


Figure 5

TYPICAL CHARACTERISTICS

DIFFERENTIAL GAIN vs NUMBER OF LOADS

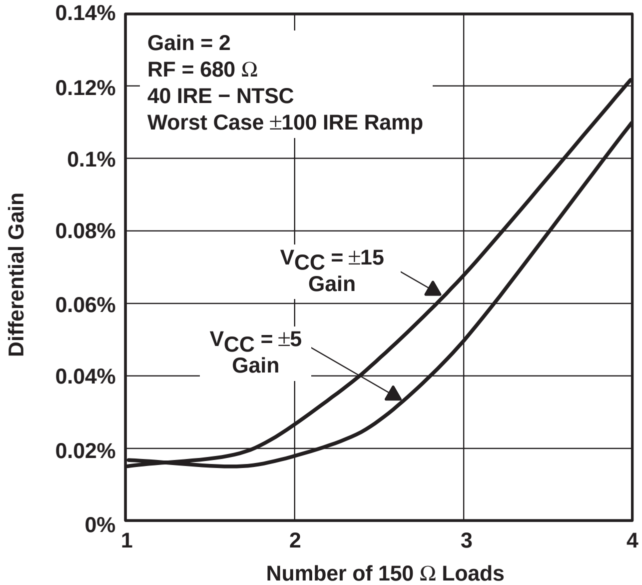


Figure 6

DIFFERENTIAL PHASE vs NUMBER OF LOADS

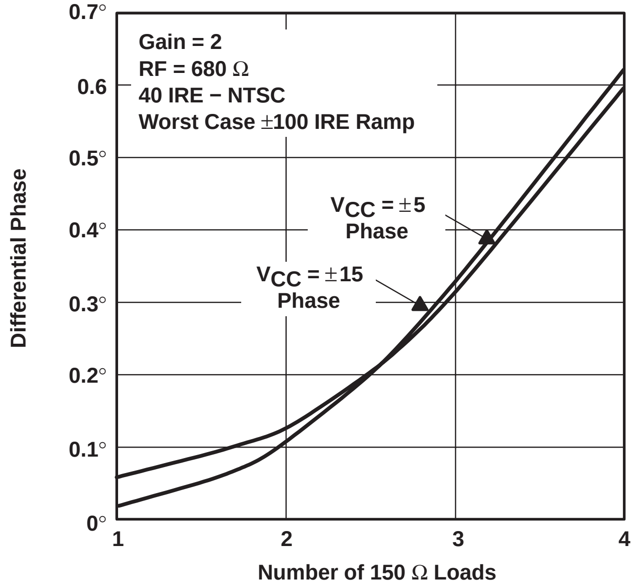


Figure 7

DIFFERENTIAL GAIN vs NUMBER OF LOADS

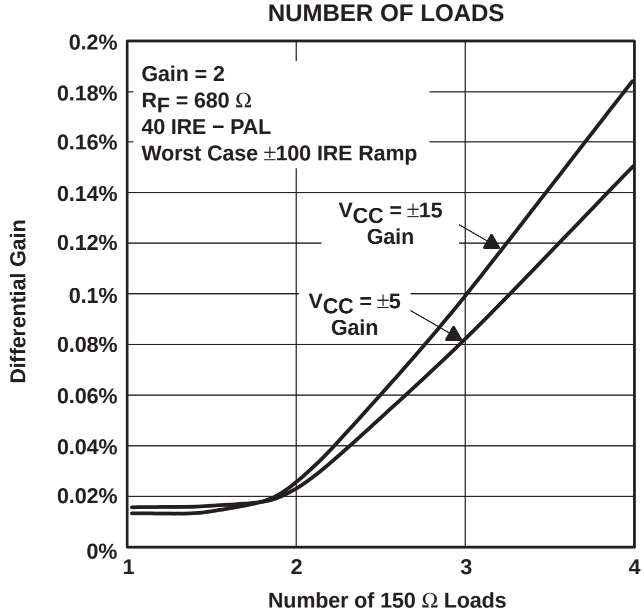


Figure 8

DIFFERENTIAL PHASE vs NUMBER OF LOADS

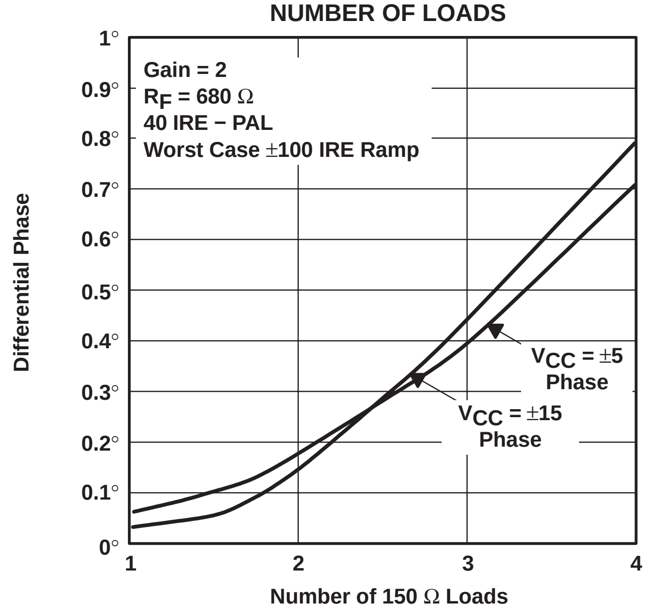


Figure 9

TYPICAL CHARACTERISTICS

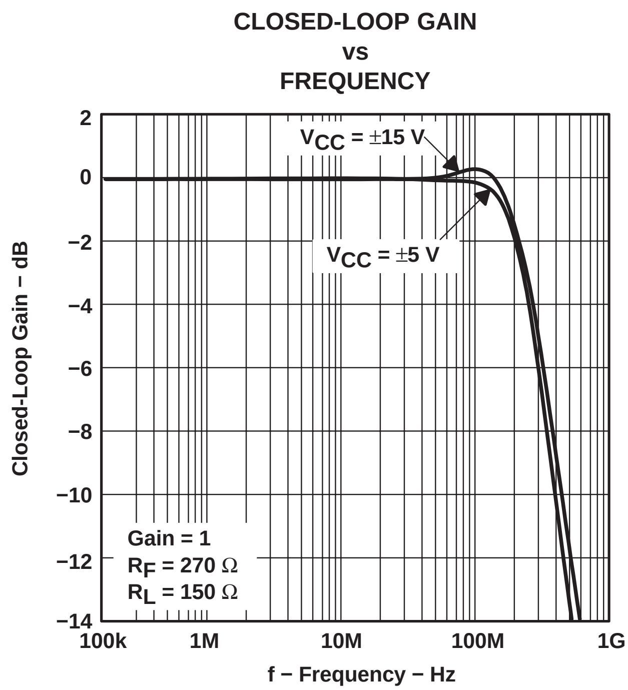


Figure 10

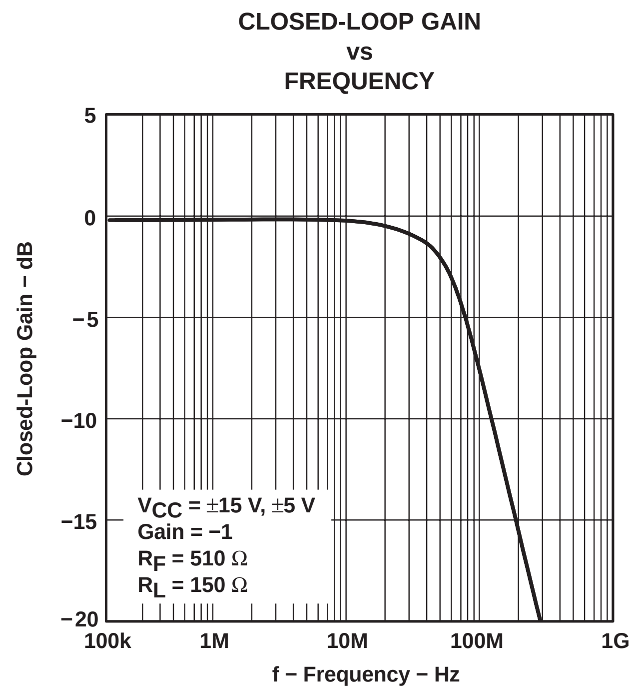


Figure 11

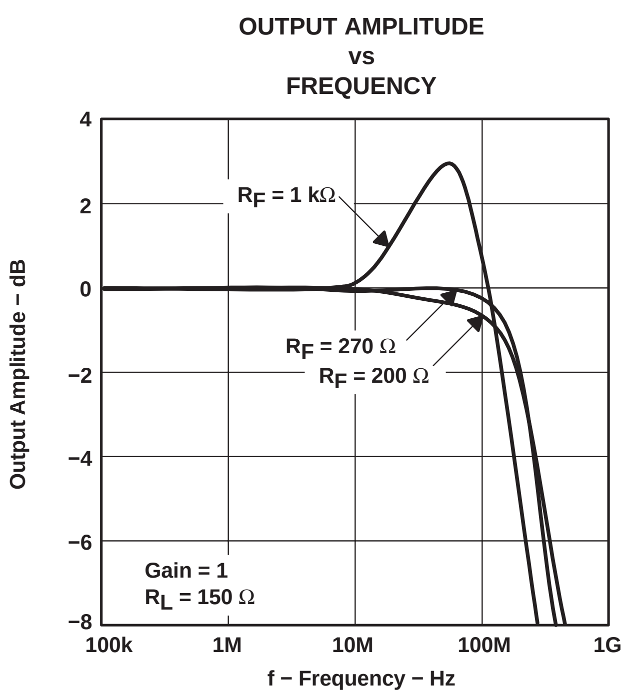


Figure 12

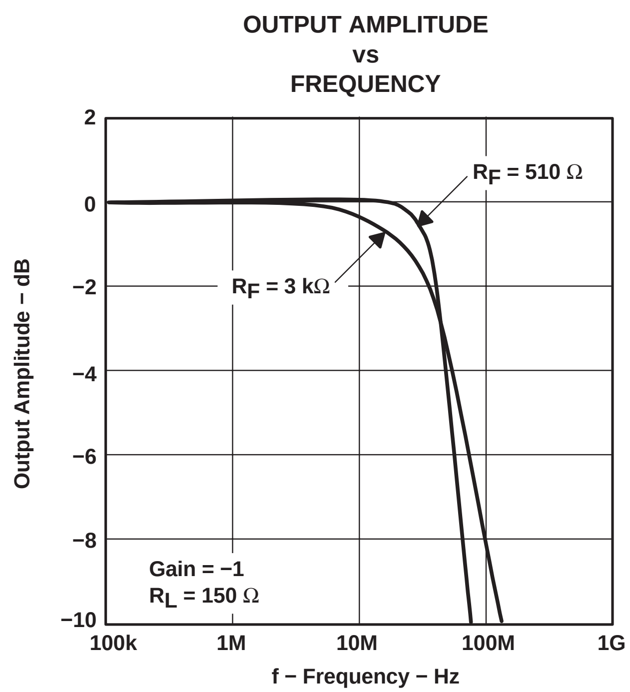


Figure 13

TYPICAL CHARACTERISTICS

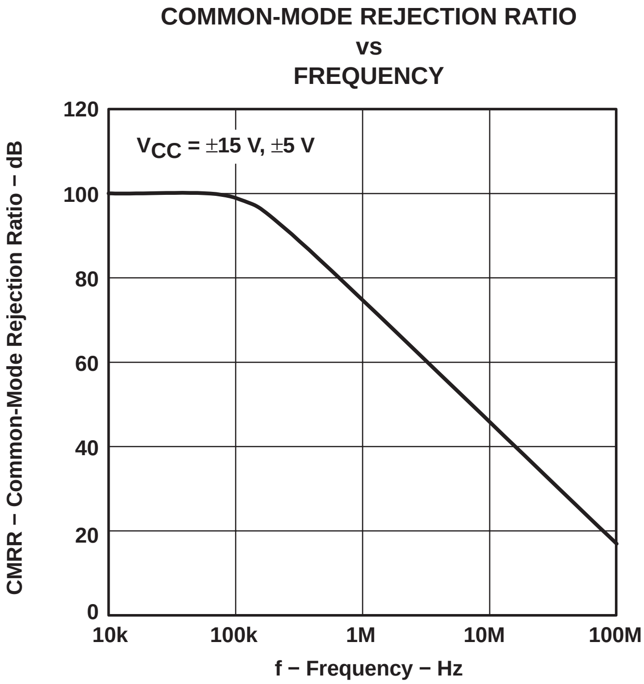


Figure 14

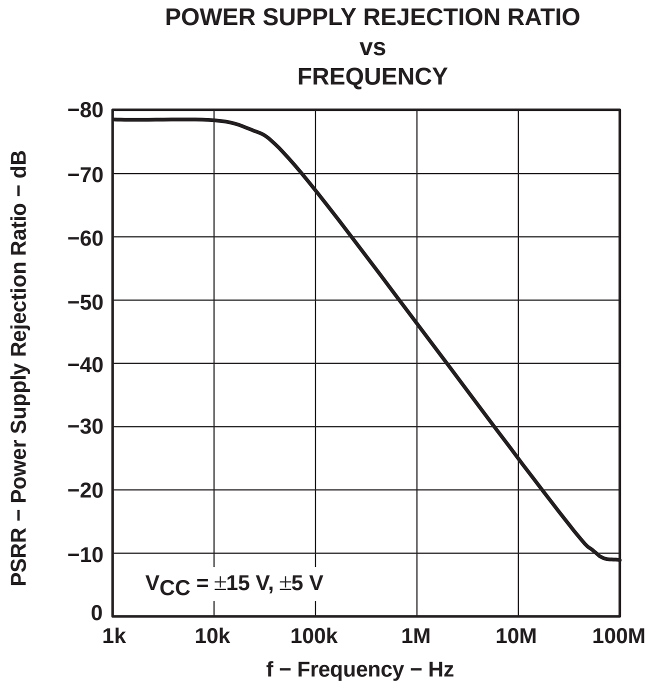


Figure 15

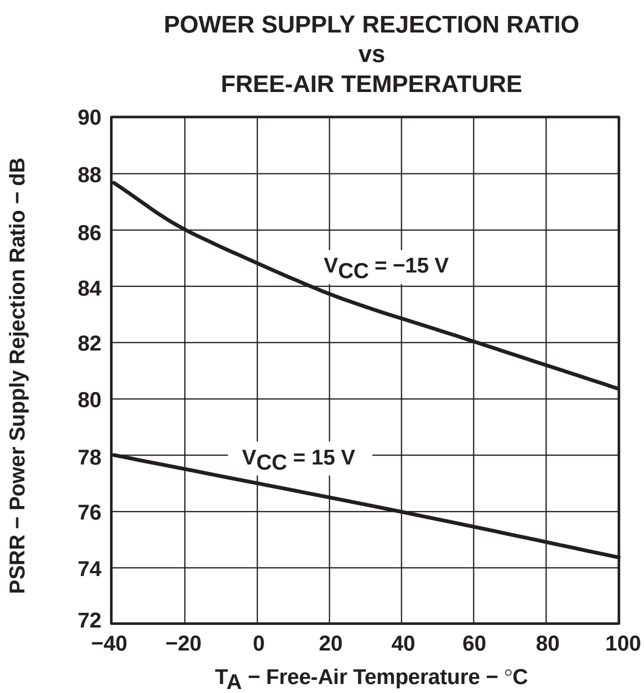


Figure 16

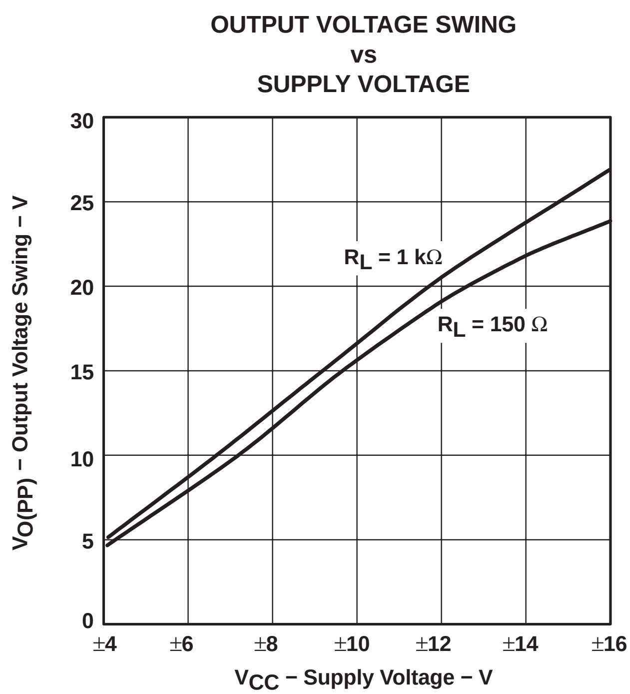


Figure 17

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

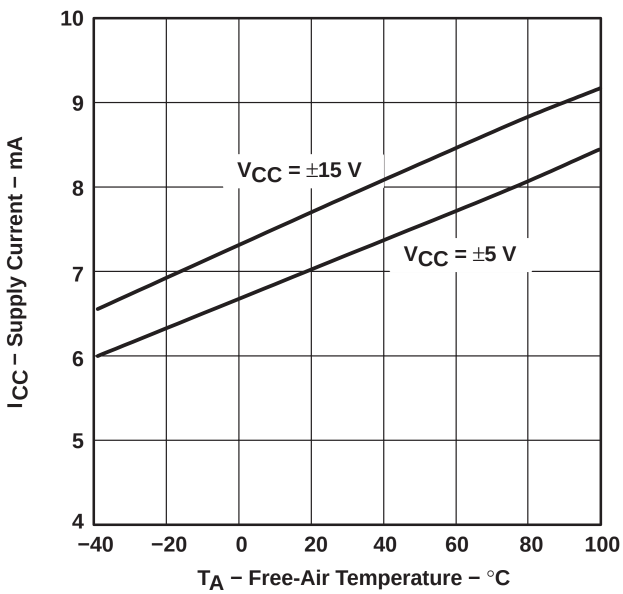


Figure 18

NOISE SPECTRAL DENSITY vs FREQUENCY

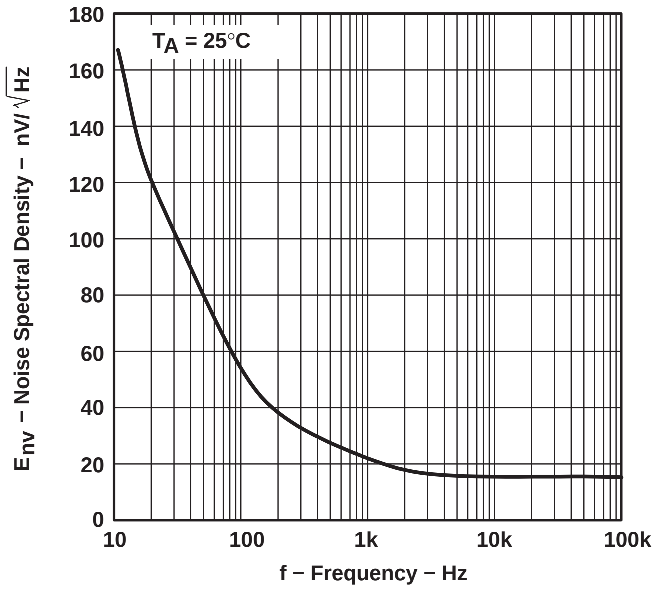


Figure 19

TOTAL HARMONIC DISTORTION vs FREQUENCY

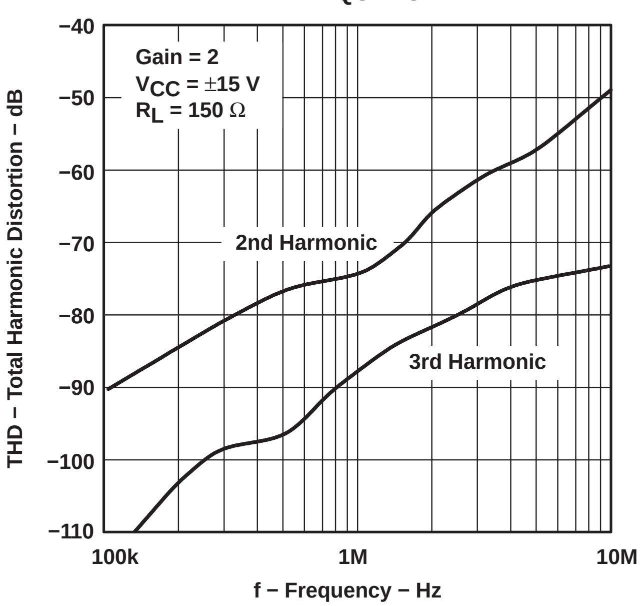


Figure 20

TOTAL HARMONIC DISTORTION vs FREQUENCY

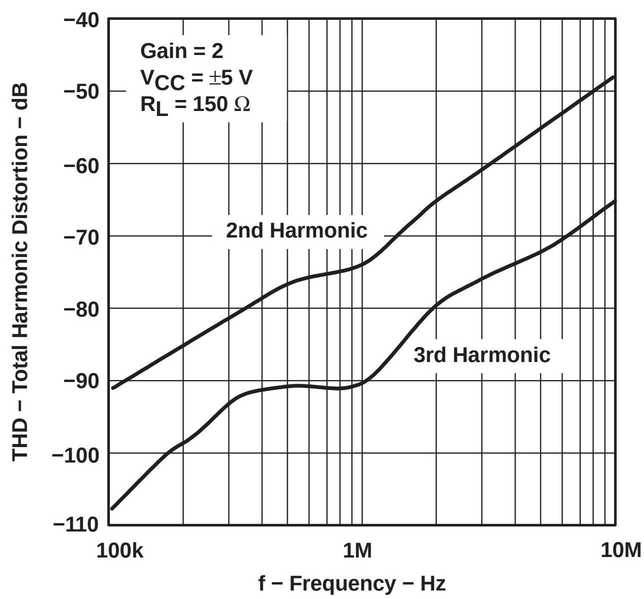


Figure 21

TYPICAL CHARACTERISTICS

CROSSTALK
vs
FREQUENCY

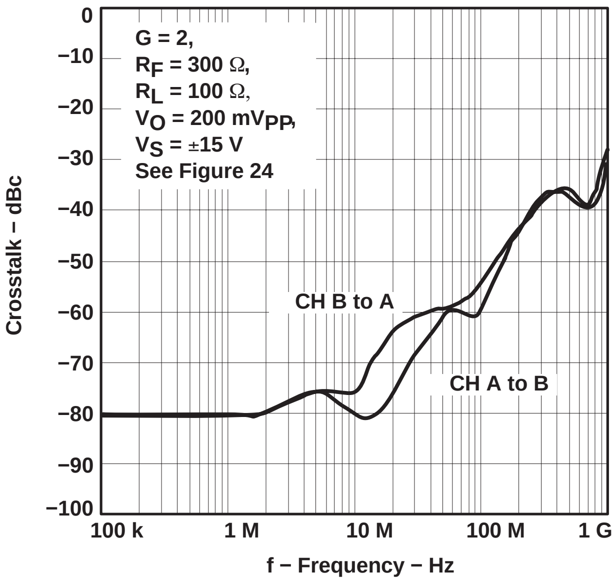


Figure 22

CROSSTALK
vs
FREQUENCY

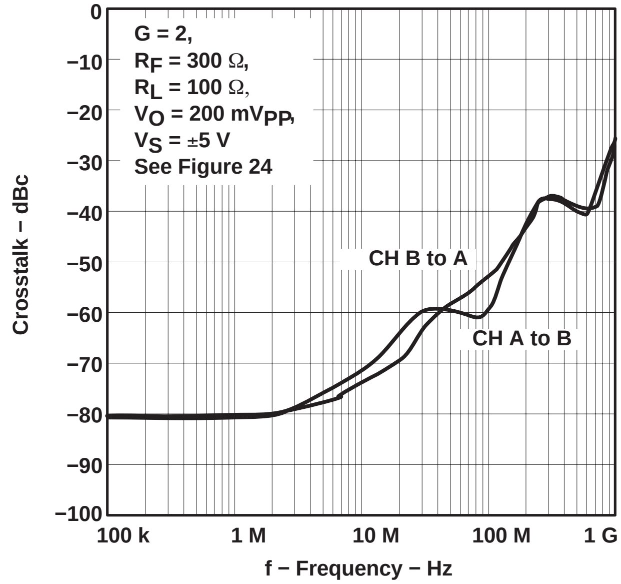


Figure 23

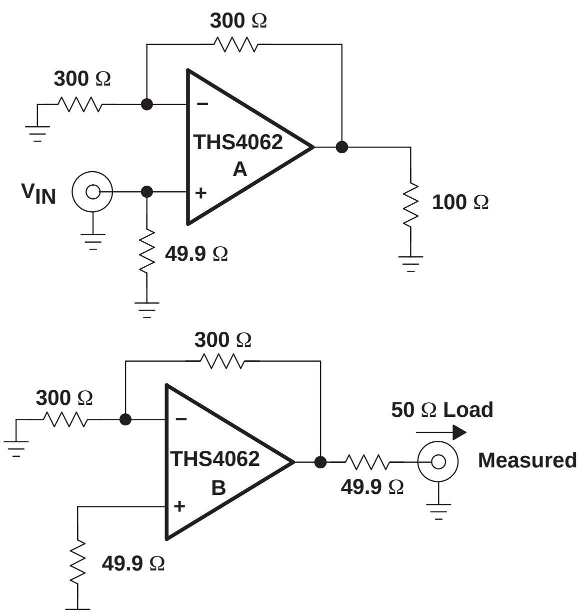


Figure 24. Test Circuits

APPLICATION INFORMATION

theory of operation

The THS406x is a high speed, operational amplifier configured in a voltage feedback architecture. It is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This results in an exceptionally high performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 25.

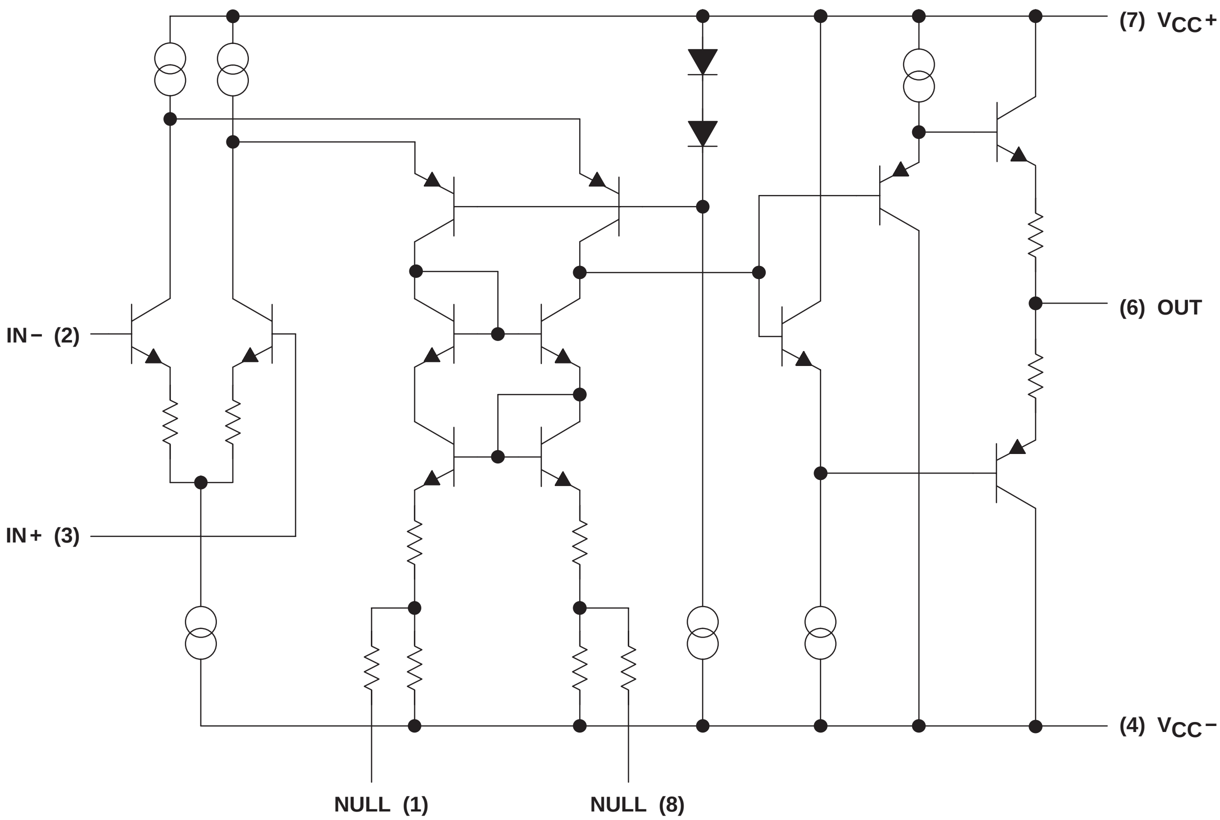


Figure 25. THS4061 Simplified Schematic

APPLICATION INFORMATION

offset nulling

The THS4061 has very low input offset voltage for a high-speed amplifier. However, if additional correction is required, an offset nulling function has been provided. By placing a potentiometer between terminals 1 and 8 and tying the wiper to the negative supply, the input offset can be adjusted. This is shown in Figure 26.

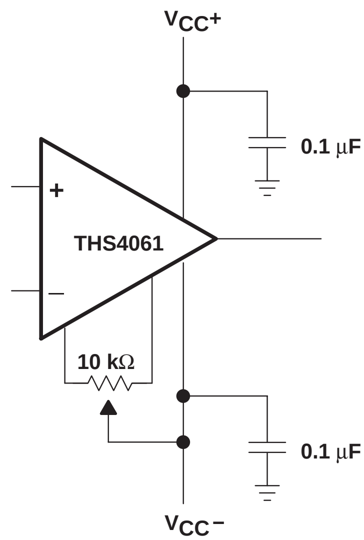


Figure 26. Offset Nulling Schematic

optimizing unity gain response

Internal frequency compensation of the THS406x was selected to provide very wideband performance yet still maintain stability when operated in a noninverting unity gain configuration. When amplifiers are compensated in this manner there is usually peaking in the closed loop response and some ringing in the step response for very fast input edges, depending upon the application. This is because a minimum phase margin is maintained for the G=+1 configuration. For optimum settling time and minimum ringing, a feedback resistor of 270 Ω should be used as shown in Figure 27. Additional capacitance can also be used in parallel with the feedback resistance if even finer optimization is required.

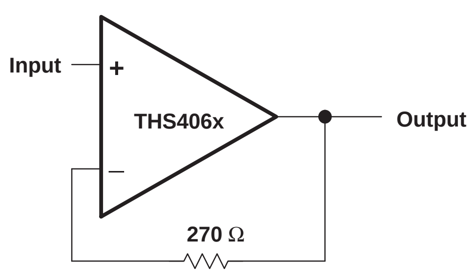


Figure 27. Noninverting, Unity Gain Schematic

APPLICATION INFORMATION

driving a capacitive load

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS406x has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 28. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

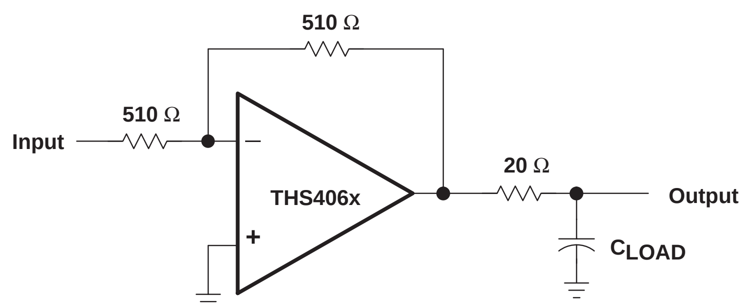


Figure 28. Driving a Capacitive Load

circuit layout considerations

In order to achieve the levels of high frequency performance of the THS406x, it is essential that proper printed-circuit board high frequency design techniques be followed. A general set of guidelines is given below. In addition, a THS406x evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes − It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling − Use a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-µF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor should be placed as close as possible to the supply terminal. As this distances increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets − Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements − Optimum high frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This helps to minimize stray capacitance at the input of the amplifier.

APPLICATION INFORMATION

circuit layout considerations (continued)

- Surface-mount passive components − Using surface-mount passive components is recommended for high-frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout, thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

evaluation board

An evaluation board is available for the THS4061 (literature number SLOP226) and THS4062 (literaure number SLOP235). This board has been configured for very low parasitic capacitance in order to realize the full performance of the amplifier. A schematic of the evaluation board is shown in Figure 29. The circuitry has been designed so that the amplifier may be used in either an inverting or noninverting configuration. To order the evaluation board contact your local TI sales office or distributor. For more detailed information, refer to the *THS4061 EVM User's Manual* (literature number SLOU038) or the *THS4062 EVM User's Manual* (literature number SLOU040)

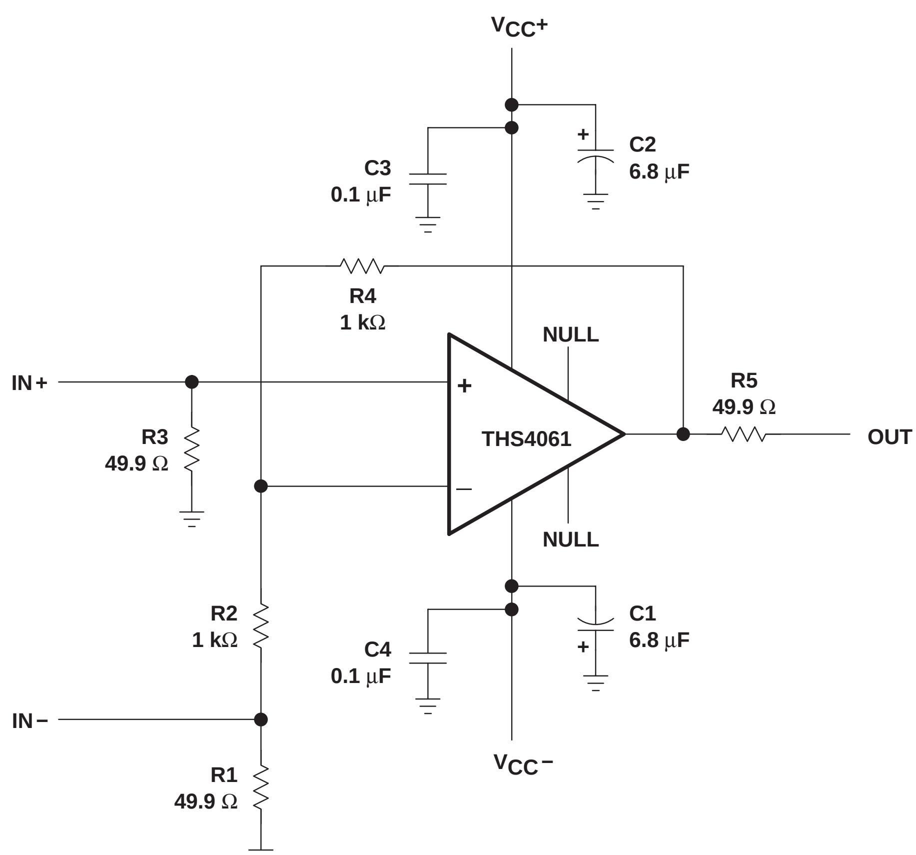


Figure 29. THS4061 Evaluation Board Schematic

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9960101Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9960101Q2A THS4061MFKB	Samples
5962-9960101QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9960101QPA THS4061M	Samples
THS4061CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4061C	Samples
THS4061CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4061C	Samples
THS4061CDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ABS	Samples
THS4061CDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ABS	Samples
THS4061CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4061C	Samples
THS4061ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4061I	Samples
THS4061IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4061I	Samples
THS4061IDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT	Samples
THS4061IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4061I	Samples
THS4061IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4061I	Samples
THS4061MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9960101Q2A THS4061MFKB	Samples
THS4061MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	THS4061MJG	Samples
THS4061MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9960101QPA THS4061M	Samples
THS4062CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4062C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4062CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4062C	Samples
THS4062CDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ABM	Samples
THS4062CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4062C	Samples
THS4062CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	4062C	Samples
THS4062ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4062I	Samples
THS4062IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	4062I	Samples
THS4062IDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABN	Samples
THS4062IDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABN	Samples
THS4062IDGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF THS4061, THS4061M :

- Catalog: THS4061

- Military: THS4061M

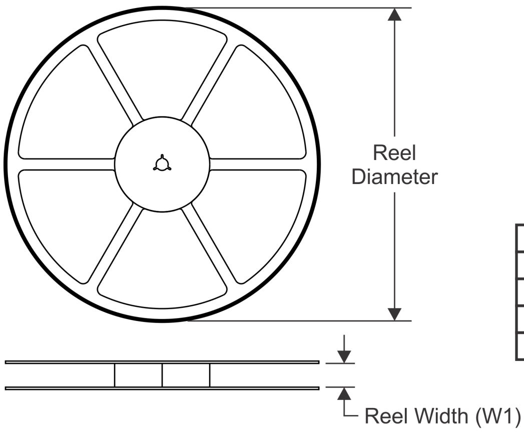
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

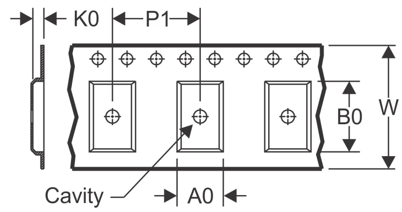
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

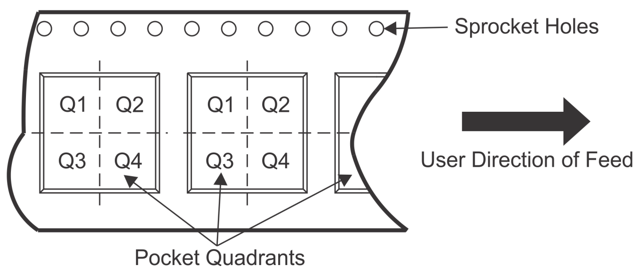


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

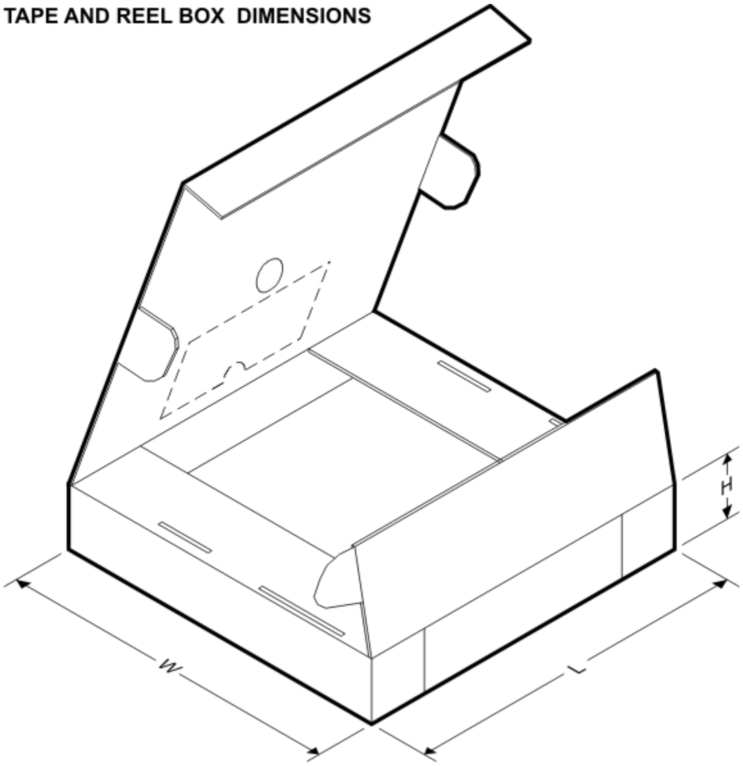
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4061CDGNR	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4061CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4061IDGNR	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4061IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4062CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4062IDGNR	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

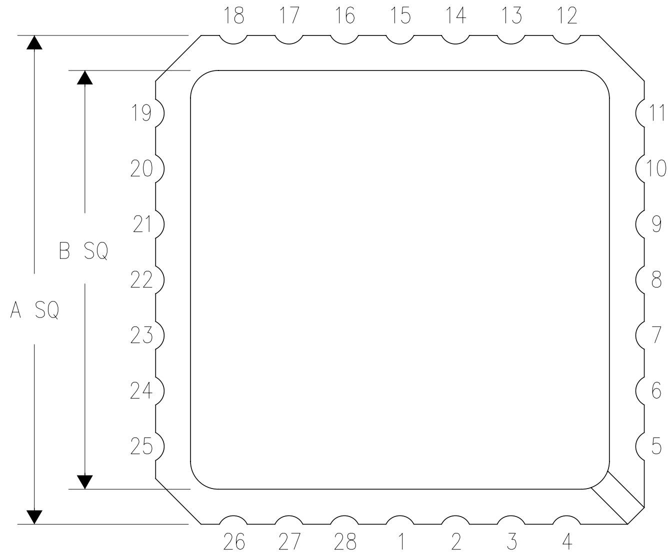


*All dimensions are nominal

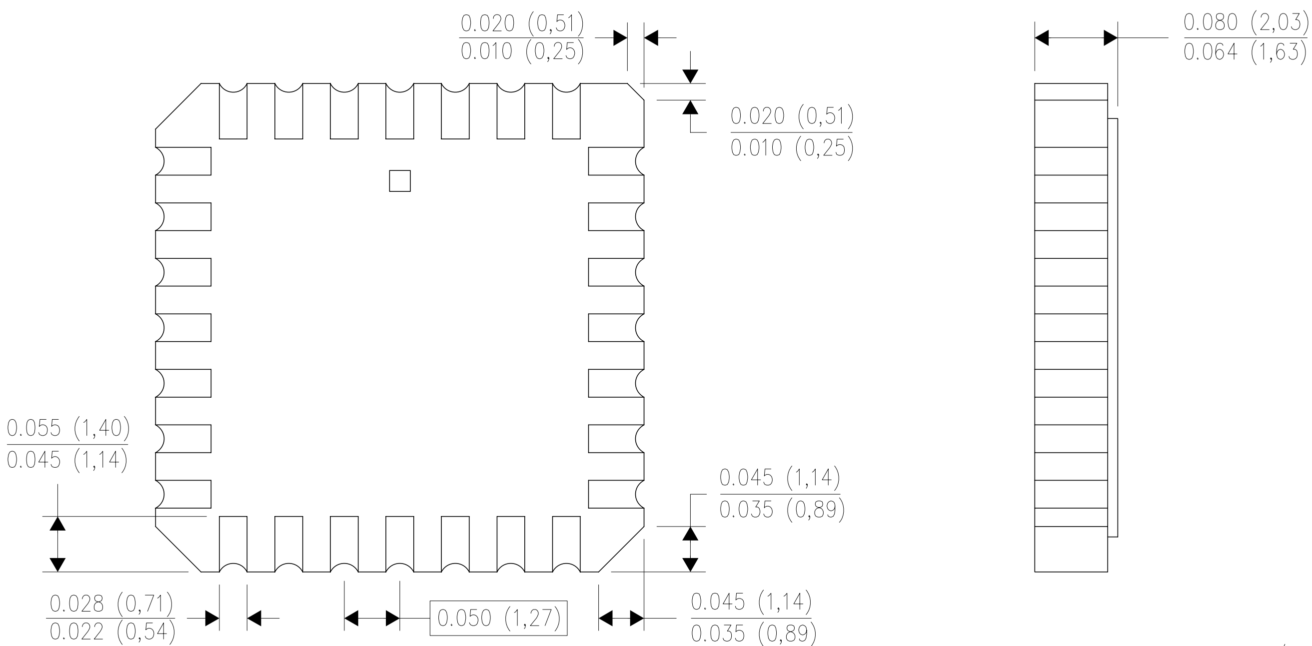
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4061CDGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
THS4061CDR	SOIC	D	8	2500	350.0	350.0	43.0
THS4061IDGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
THS4061IDR	SOIC	D	8	2500	350.0	350.0	43.0
THS4062CDR	SOIC	D	8	2500	350.0	350.0	43.0
THS4062IDGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0

FK (S-CQCC-N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

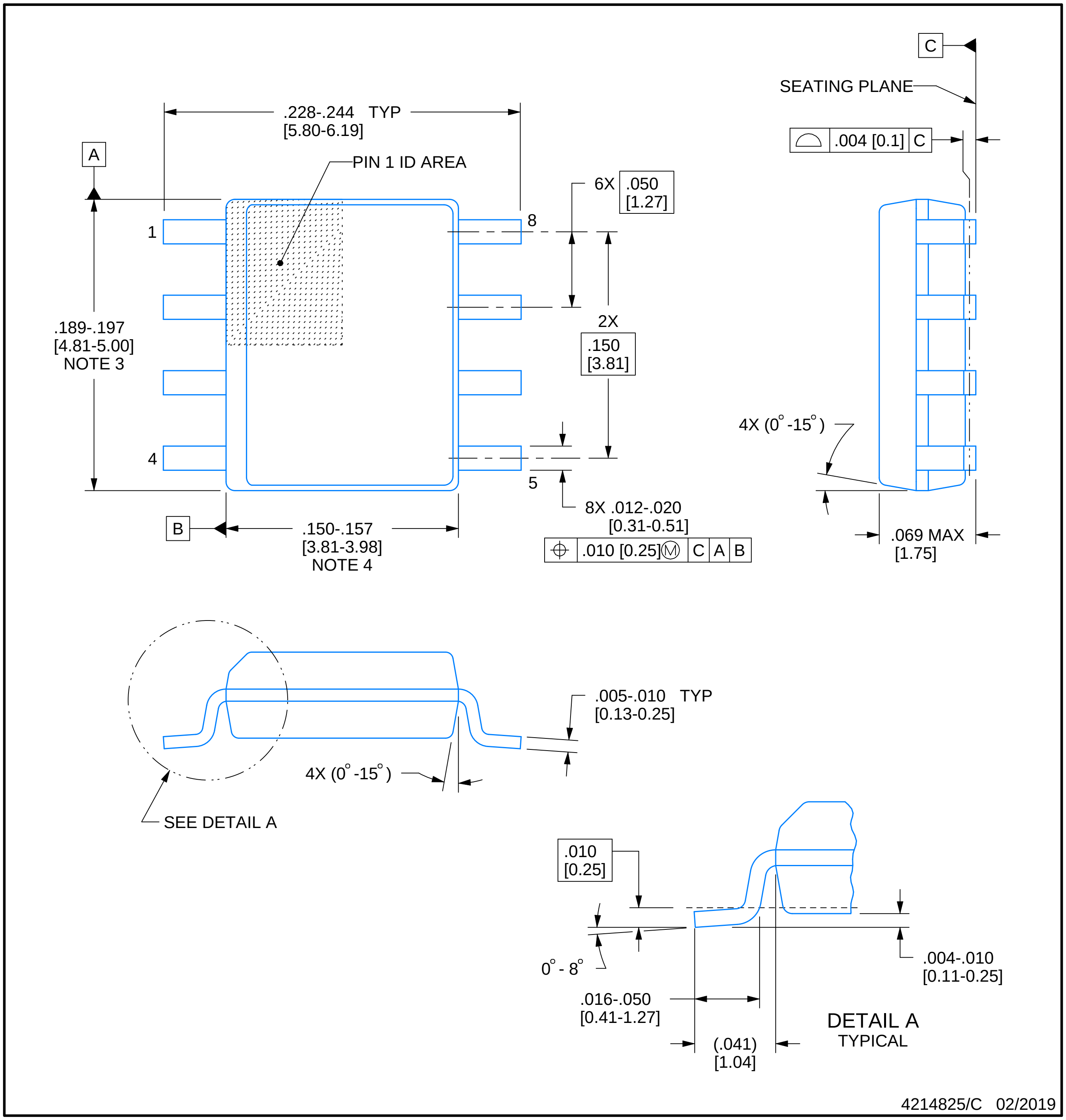


NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



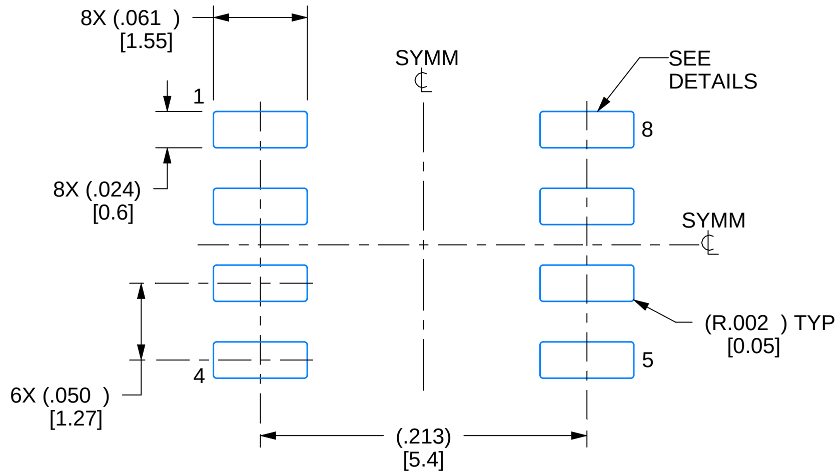
4040140/D 01/11

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

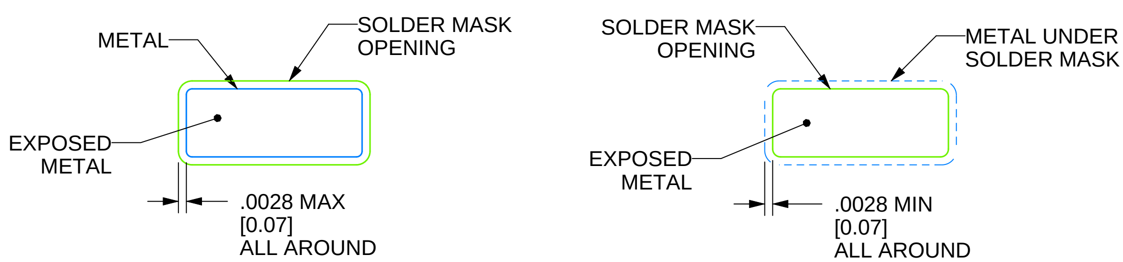


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

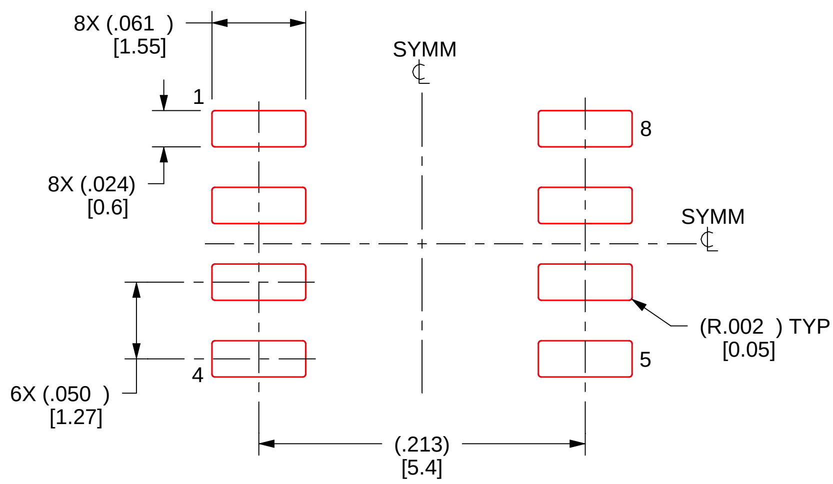
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



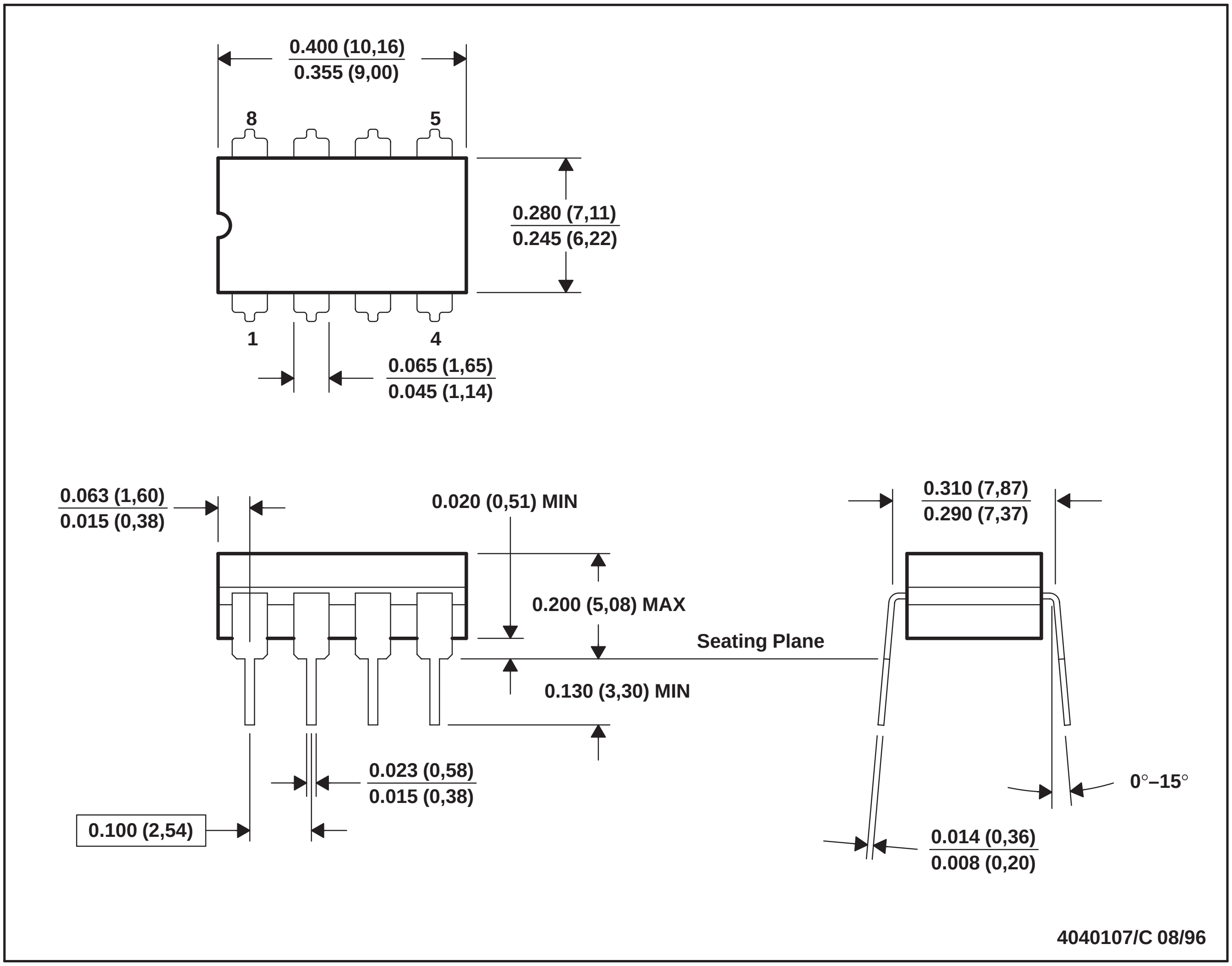
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

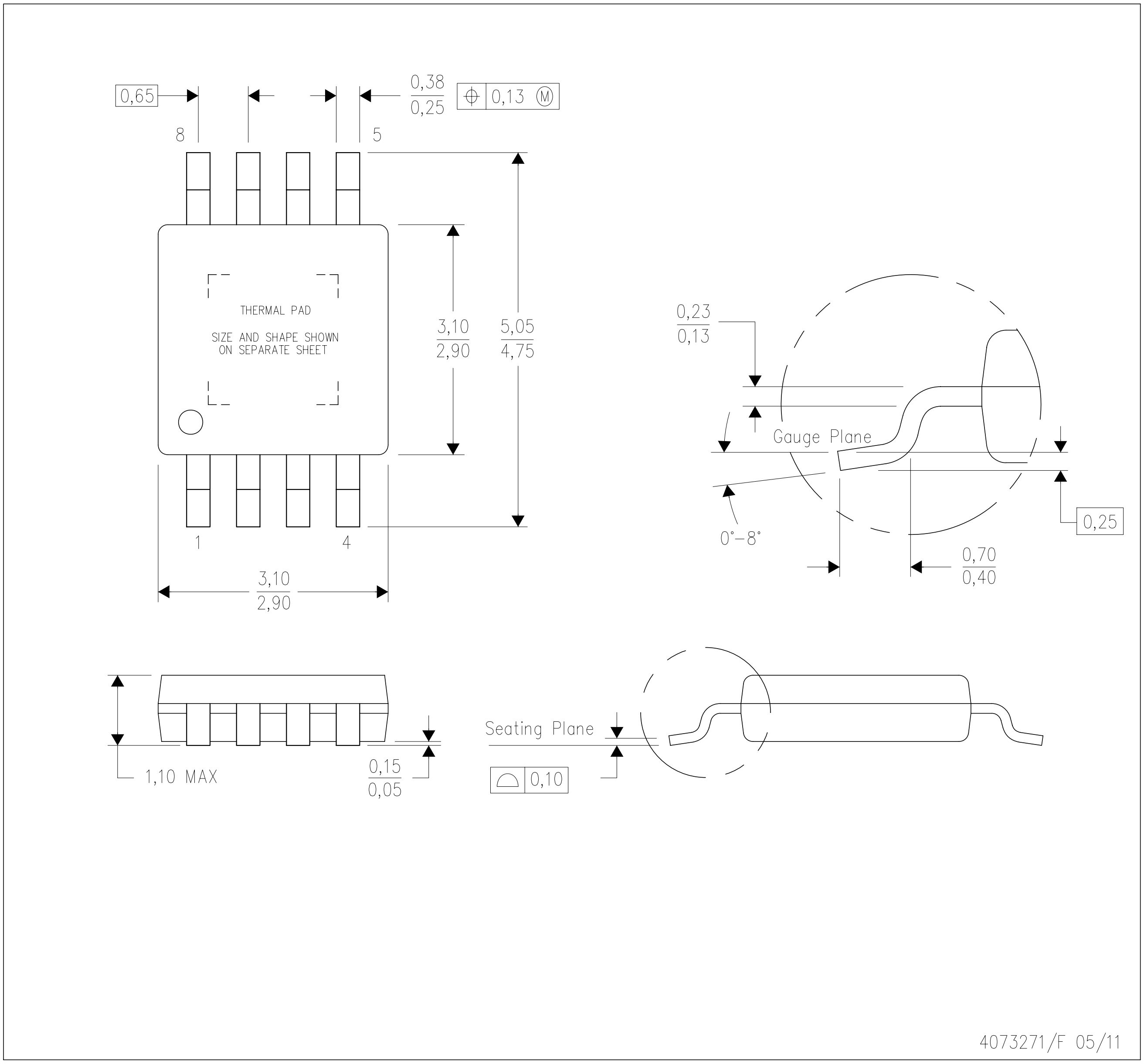
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

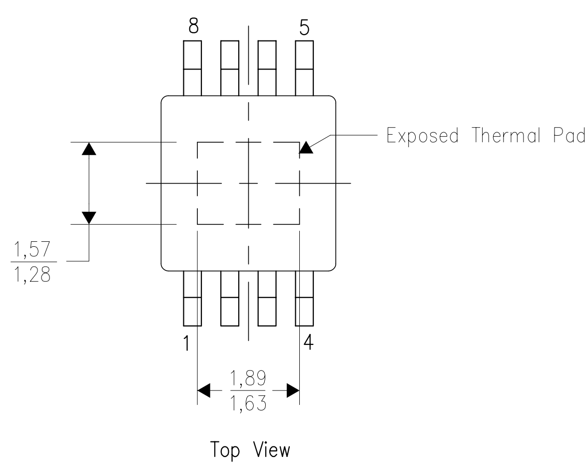
DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



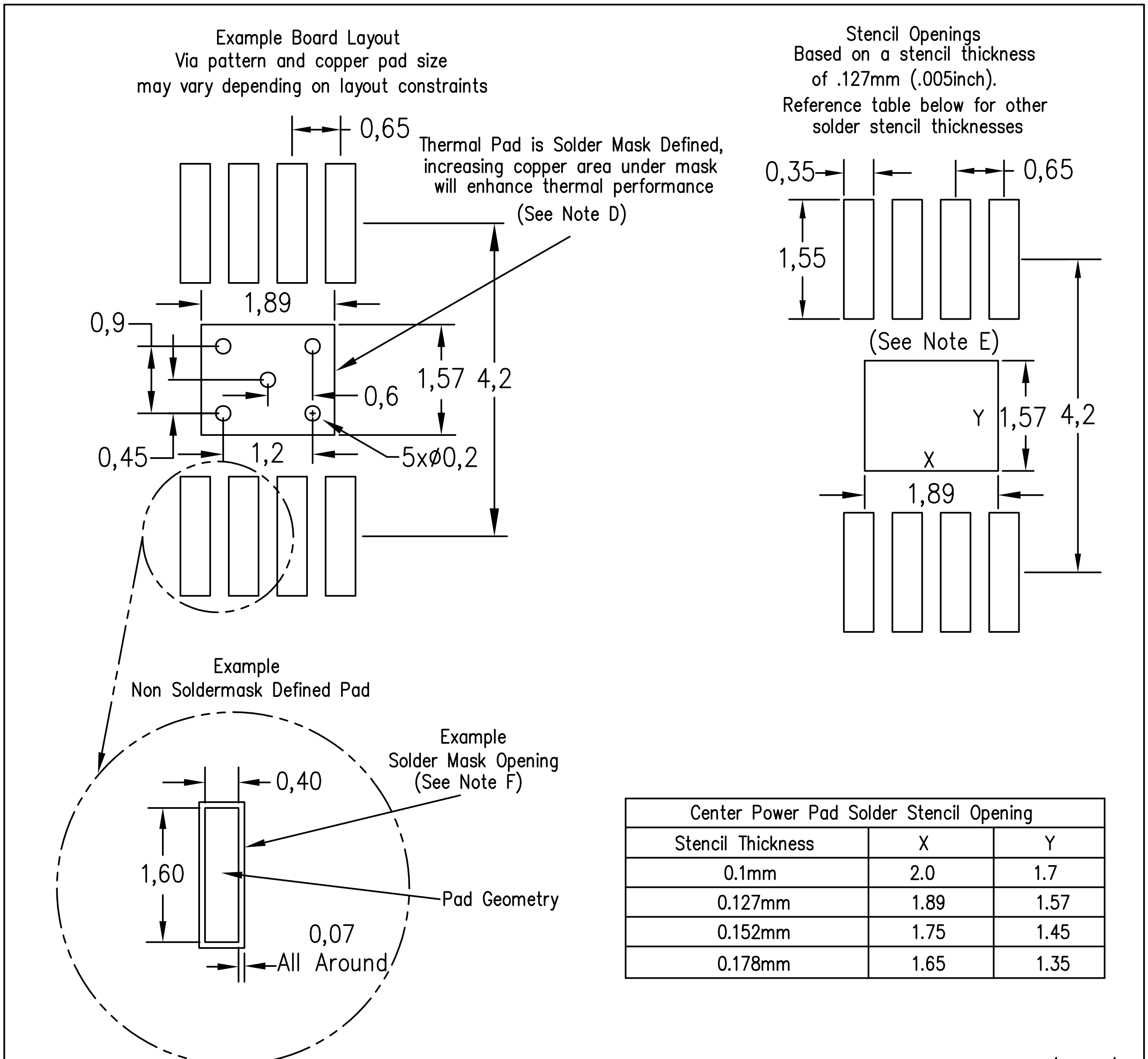
Exposed Thermal Pad Dimensions

4206323-2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

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NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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