# 8-Channel Variable-Gain Amplifier (VGA) With Octal High-Speed ADC

**Check for Samples: AFE5801**

## FEATURES

- **Eight Variable-Gain Amplifiers (VGA)**
  - **Eight Differential Buffered Inputs With 2Vpp Maximum Swing**
  - **5.5nV/√Hz VCA Input Noise (31dB Gain)**
  - **Variable Gain, –5dB to 31dB With 0.125dB or 1dB Steps**
  - **Digital Gain Control**
- **Third-Order Antialiasing Filter With Programmable Cutoff Frequency (7.5, 10, or 14MHz)**
- **Clamping**
- **Analog-to-Digital Converter (ADC)**
  - **Octal Channel, 12Bit, 65MSPS**
  - **Internal and External Reference Support**
  - **No External Decoupling Required for References**
  - **Serial LVDS Outputs**
- **1.8V and 3.3V Supplies**
- **50mW Total Power per Channel at 30MSPS**
- **58mW Total Power per Channel at 50MSPS**
- **64QFN Package (9mm × 9mm)**

## APPLICATIONS

- **Imaging: Ultrasound, PET**

## RELATED DEVICES

- **AFE5851: 16-Channel VGA + ADC, 32.5MSPS/Channel**

## DESCRIPTION

The AFE5801 is an analog front end, targeting applications where the power and level of integration are critical. The device contains eight variable-gain amplifiers (VGA), each followed by a high-speed (up to 65MSPS) ADC, for a total of eight ADCs per device.

Each of the eight differential inputs is buffered, accepts up to 2Vpp maximum input swing, and is followed by a VGA with a gain range from –5dB to 31dB. The VGA gain is digitally controlled, and the gain curves versus time can be stored in memory integrated within the device using the serial interface.

A selectable clamping and antialias low-pass filter (with 3dB attenuation at 7.5, 10, or 14MHz) is also integrated between VGA and ADC, for every channel.

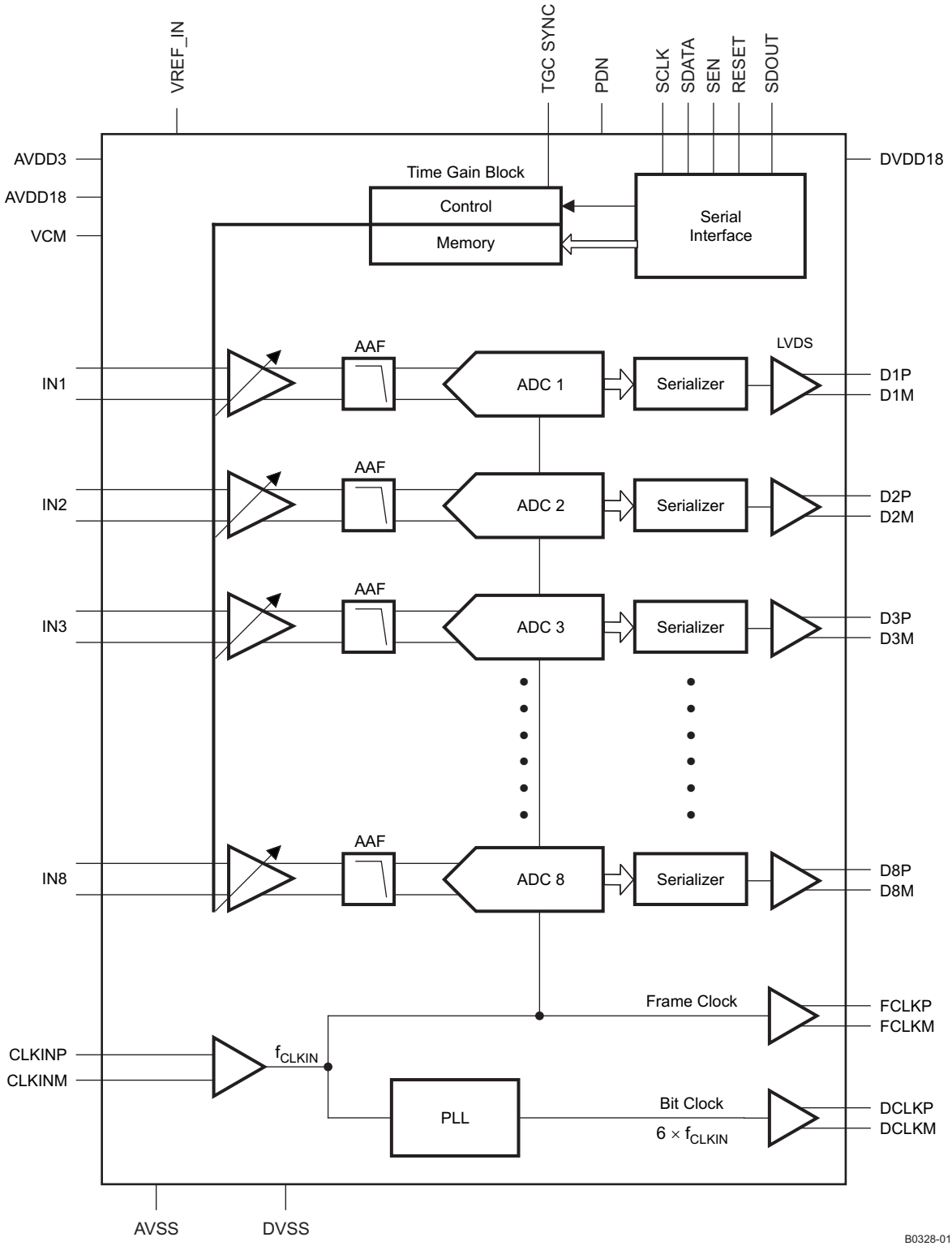
The VGA/antialias filter outputs are differential (limited to 2Vpp) and drive the onboard 12bit, 65MSPS ADC. The ADC also scales down its power consumption should a lower sampling rate be selected. The ADC outputs are serialized in LVDS streams, which further minimizes power and board area.

The AFE5801 is available in a 64-pin QFN package (9mm × 9mm) and is specified over the full industrial temperature range (–40°C to 85°C).

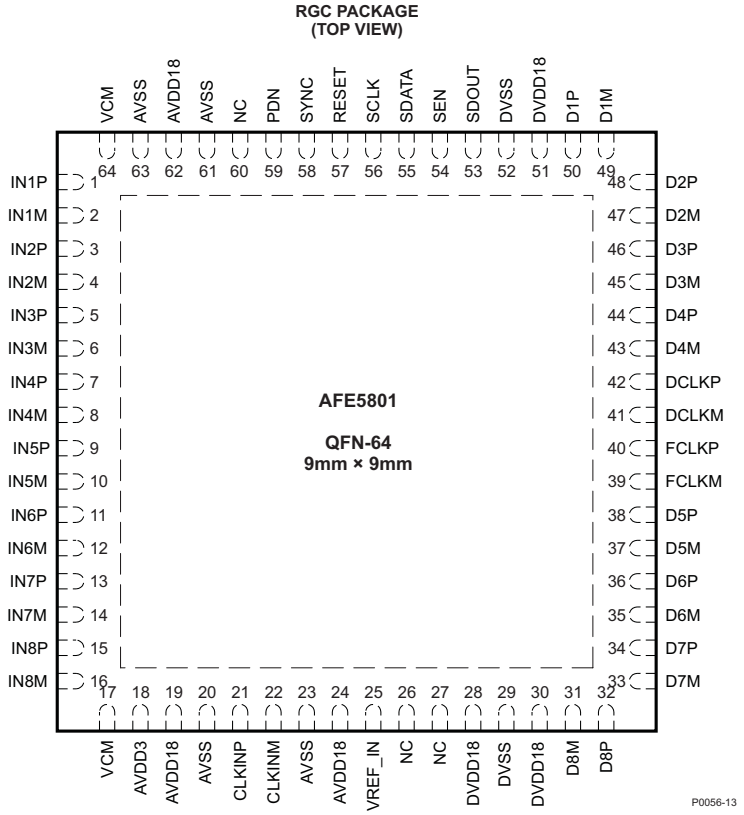
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## BLOCK DIAGRAM



## PINOUT




## TERMINAL FUNCTIONS

| Name | NUMBER | DESCRIPTION |
|---|---|---|
| AVSS | 20, 23, 61, 63 | Analog ground |
| AVDD18 | 19, 24, 62 | 1.8V analog supply voltage |
| AVDD3 | 18 | 3.3V analog supply voltage |
| CLKINP, CLKINM | 21, 22 | Differential clock input pins. Single-ended clock is also supported. See the *Clock Inputs* section. |
| D1P/M–D8P/M | 50–43, 38–31 | LVDS outputs for channels 1 to 8 |
| DCLKM, DCLKP | 41, 42 | LVDS bit clock output |
| DVSS | 29, 52 | Digital ground |
| DVDD18 | 28(1), 30, 51 | 1.8V LVDS buffer supply voltage |
| FCLKM, FCLKP | 39, 40 | LVDS frame clock output |
| IN1P/M–IN8P/M | 1–16 | Differential analog input pins for channels 1 to 8 |
| NC | 26, 27, 60 | Do not connect |
| PDN | 59 | Global power-down control input (active-high). 100kΩ pulldown resistor |
| RESET | 57 | Hardware reset pin (active-high). 100kΩ pulldown resistor |
| SCLK | 56 | Serial interface clock input. 100kΩ pulldown resistor |
| SDATA | 55 | Serial interface data input. 100kΩ pulldown resistor |
| SDOUT | 53 | Serial interface data readout |
| $\overline{\text{SEN}}$ | 54 | Serial interface enable. 100kΩ pullup resistor |
| SYNC | 58 | TGC/VGA synchronization signal input. 100kΩ pulldown resistor |
| VCM | 17, 64 | Common-mode output pins for possible bias of the analog input signals |
| VREF_IN | 25 | Reference input in the external reference mode |
| Thermal pad | Bottom of package | Connect to AVSS |

(1) Pin 28 can be connected to the 1.8V or 3.3V supply, whichever is easier for user. It does not affect the performance.

## PACKAGING/ORDERING INFORMATION(1)

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|---|---|---|---|---|---|---|
| AFE5801 | QFN-64(2) | RGC | –40°C to 85°C | AFE5801 | AFE5801IRGCT | Tape/reel, 250 |
| AFE5801 | QFN-64(2) | RGC | –40°C to 85°C | AFE5801 | AFE5801IRGCR | Tape/reel, 2000 |

(1) For the most-current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) For the thermal pad size on the package, see the mechanical drawings at the end of this document.

## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | VALUE | UNIT |
|---|---|---|---|
| | AVDD3 to AVSS | –0.3 to 3.8 | V |
| | AVDD18 to AVSS | –0.3 to 2.2 | V |
| | DVDD18 to DVSS | –0.3 to 2.2 | V |
| | Voltage between AVSS and DVSS | –0.3 to 0.3 | V |
| | Analog input pins ($IN_iP$, $IN_iM$) to AVSS | –0.3V to MIN (3.6V, AVDD3 + 0.3V) | V |
| | VREF_IN to AVSS | –0.3 to 2.2 | V |
| | $V_{CLKP}$, $V_{CLKM}$ to AVSS | –0.3 to 2.2 | V |
| | Digital control pins to DVSS: PDN, RESET, SCLK, SDATA, $\overline{SEN}$, SYNC | –0.3 to 3.6 | V |
| $T_J$ | Maximum operating junction temperature | 125 | °C |
| $T_{stg}$ | Storage temperature range | –60 to 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## THERMAL CHARACTERISTICS

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|
| $\theta_{JA}$ | 0 LFM air flow | 23.17 | °C/W |
| $\theta_{JC}$ | 2-oz. (0.071-mm thick) copper trace and pad soldered directly to a JEDEC-standard four-layer 3-in. × 3-in. (7.62-cm ×7.62-cm) PCB. | 22.1 | °C/W |

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $T_A$ | Ambient temperature | –40 | | 85 | °C |
| **SUPPLIES** | | | | | |
| AVDD3 | Analog supply voltage (VGA) | 3 | 3.3 | 3.6 | V |
| AVDD18 | Analog supply voltage (ADC) | 1.7 | 1.8 | 1.9 | V |
| DVDD18 | Digital supply voltage (ADC, LVDS) | 1.7 | 1.8 | 1.9 | V |
| **ANALOG INPUTS** | | | | | |
| $IN_iP$, $IN_iM$ | Input voltage range to AVSS | VCM – 0.5 | | VCM + 0.5 | V |
| | VREF_IN in external reference mode | 1.35 | 1.4 | 1.45 | V |
| | VCM load | | 3 | | mA |

## RECOMMENDED OPERATING CONDITIONS (continued)

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **CLOCK INPUT** | | | | | |
| $f_{CLKIN}$ | Input clock frequency | 5 | | 65 | MSPS |
| | Input clock duty cycle | 40% | 50% | 60% | |
| $V_{CLKP-CLKM}$ | Sine wave, ac-coupled | 0.5 | | | Vpp |
| | LVPECL, ac-coupled | | 1.6 | | Vpp |
| | LVDS, ac-coupled | 0.25 | 0.7 | | Vpp |
| $V_{CLKP}$ | LVCMOS, single-ended, $V_{CLKM}$ to AVSS | | 1.8 | | Vpp |
| $V_{IH}$ | High-level input voltage | 0.75 × AVDD18 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.25 × AVDD18 | V |
| **DIGITAL OUTPUT** | | | | | |
| $C_{LOAD}$ | External load capacitance from each output pin to DVSS | | 5 | | pF |
| $R_{LOAD}$ | Differential load resistance (external) between the LVDS output pairs | | 100 | | Ω |

## ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, MIN and MAX values are across the full temperature range of $T_{min}$ = –40°C to $T_{max}$ = 85°C, AVDD3 = 3.3V, AVDD18 = 1.8V, DVDD18 = 1.8V, –1dBFS analog input ac-coupled with 0.1µF, internal reference mode, maximum-rated sampling frequency (65MSPS), LVCMOS (single-ended) clock, 50% duty cycle, antialiasing filter set at 14MHz (3dB corner), output clamp disabled(1) and analog high-pass filter enabled, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **VARIABLE GAIN AMPLIFIER (VGA)** | | | | | | | |
| | Maximum input voltage swing | Linear operation, from INP to INM | | | 2 | | Vpp |
| VCM | Common-mode voltage | | | | 1.6 | | V |
| | Gain range | Maximum gain – minimum gain | | | 36 | | dB |
| | Maximum gain | | | 29.5 | 31 | 32.5 | dB |
| | Gain resolution | | | | 0.125 or 1 | | dB |
| | Input resistance | From each input to dc bias level | | | 5 | | kΩ |
| | Input capacitance | Differential between the inputs | | | 2 | | pF |
| **ANTIALIAS FILTER (AAF)** | | | | | | | |
| | AAF cutoff frequency | 7.5MHz filter selected | –3dB | | 7.5 | | MHz |
| | | 10MHz filter selected | | | 10 | | |
| | | 14MHz filter selected | | | 14 | | |
| | AAF stop-band attenuation | 7.5MHz filter selected | –6dB | | 10 | | MHz |
| | | 10MHz filter selected | | | 14 | | |
| | | 14MHz filter selected | | | 20 | | |
| | | 7.5MHz filter selected | –12dB | | 18 | | MHz |
| | | 10MHz filter selected | | | 24 | | |
| | | 14MHz filter selected | | | 30 | | |
| | In-band attenuation | 7.5MHz filter selected | At 3.2MHz | | 1.2 | | dB |
| | | 10MHz filter selected | | | 0.5 | | |
| | | 14MHz filter selected | | | 0.2 | | |

(1) Enabling clamping increases distortion values at high swings by about 2dB.

## ELECTRICAL CHARACTERISTICS (continued)

Typical values are at 25°C, MIN and MAX values are across the full temperature range of $T_{min}$ = –40°C to $T_{max}$ = 85°C, AVDD3 = 3.3V, AVDD18 = 1.8V, DVDD18 = 1.8V, –1dBFS analog input ac-coupled with 0.1μF, internal reference mode, maximum-rated sampling frequency (65MSPS), LVCMOS (single-ended) clock, 50% duty cycle, antialiasing filter set at 14MHz (3dB corner), output clamp disabled (1) and analog high-pass filter enabled, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **FULL-CHANNEL CHARACTERISTICS** | | | | | | |
| | Gain matching | Across channels and parts | | 0.1 | 0.6 | dB |
| | Gain error | –5dB to 28dB gain | –1.2 | ±0.3 | 1.2 | dB |
| | | Gain > 28dB | –1.8 | ±0.5 | 1.8 | |
| | Offset error | 31dB gain | –50 | | 50 | LSB |
| | Input-referred noise voltage | 5MHz, 31dB VGA gain, low-noise mode | | 5 | 6.5 | nV/√Hz |
| | | 5MHz, 31dB VGA gain, default noise mode | | 5.5 | | nV/√Hz |
| SNR | Signal-to-noise ratio | –1dBFS ADC input, 6dB gain | | 66 | | dBc |
| HD2 | Second-harmonic distortion | –1dBFS ADC input, 17dB gain, $f_{in}$ = 2MHz | | –75 | –60 | dBc |
| | | –1dBFS ADC input, 31dB gain, $f_{in}$ = 2MHz | | –75 | –60 | |
| HD3 | Third-harmonic distortion | –1dBFS ADC input, 17dB gain, $f_{in}$ = 2MHz | | –65 | –55 | dBc |
| | | –1dBFS ADC input, 31dB gain, $f_{in}$ = 2MHz | | –60 | –52 | |
| SFDR | Spurious-free dynamic range | –1dBFS ADC input, 17dB gain, $f_{in}$ = 2MHz | | 65 | | dBc |
| THD | Total harmonic distortion | –1dBFS ADC input, 17dB gain, $f_{in}$ = 2MHz | | 64 | | dBc |
| IMD | Intermodulation distortion | $f_{in1}$ = 1MHz, $f_{in2}$ = 2MHz, $A_{in1, in2}$ = –7dBFS, 30dB VGA gain | | –70 | | dBFS |
| | Group delay variation | f = 100kHz to 14MHz, across gain settings and channels | | ±3.5 | | ns |
| | | f = 100kHz to 14MHz, across channels | | ±1.5 | | |
| | Input overload recovery | ≤ 6dB overload to within 1% | | 1 | | Clock cycle |
| | Clamp level | After amplification. Clamp enabled by default | | 3 | | dB |
| | ADC number of bits | | | 12 | | |
| | Crosstalk | Aggressor: $f_{in}$ = 3MHz, 1dB below ADC full-scale Victims (channel next to aggressor channel): 50Ω differential (between $IN_iP$ and $IN_iM$) | | 92 | | dB |
| **POWER** | | | | | | |
| | Total power dissipation | Default noise mode | | 522 | 600 | mW |
| | | Low-noise mode | | 561 | 636 | |
| $I_{AVDD3}$ | AVDD3 current consumption | | | 6 | 9 | mA |
| $I_{AVDD18}$ | AVDD18 current consumption | Default noise mode | | 198 | 222 | mA |
| | | Low-noise mode | | 220 | 244 | |
| $I_{DVDD18}$ | DVDD18 current consumption | See (2) | | 81 | 100 | mA |
| | Power down | Standby mode | | 64 | | mW |
| | | Full power-down mode | | 8 | 25 | mW |
| AC PSRR | Power-supply rejection ratio | | | 30 | | dBc |

(2) Using digital modes like averaging, digital gain, digital HPF, etc., (see the *Application Information* section) might increase the DVDD18 current by about 60mA.

## DIGITAL CHARACTERISTICS(1)

The dc specifications refer to the condition where the digital outputs are not switching, but permanently at a valid logic level 0 or 1. Typical values are at 25°C, min and max values are across the full temperature range of $T_{min}$ = –40°C to $T_{max}$ = 85°C, AVDD3 = 3.3V, AVDD18 = 1.8V, DVDD18 = 1.8V, external differential load resistance between the LVDS output pair $R_{LOAD}$ = 100Ω.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **DIGITAL INPUTS (PDN, RESET, SCLK, SDATA, $\overline{SEN}$, SYNC)** | | | | | |
| High-level input voltage | | 1.4 | | 3.6 | V |
| Low-level input voltage | | | | 0.8 | V |
| High-level input current | | | 10 | | µA |
| Low-level input current | | | 10 | | µA |
| Input capacitance | | | 4 | | pF |
| **DIGITAL OUTPUTS ($D_iP$, $D_iM$)** | | | | | |
| High-level output voltage | | | 1375 | | mV |
| Low-level output voltage | | | 1025 | | mV |
| Output differential voltage $\|V_{OD}\|$ | | 270 | 380 | 490 | mV |
| Output offset voltage $V_{OS}$ | Common-mode voltage of $D_iP$ and $D_iM$ | 0.9 | 1.15 | 1.5 | V |
| Output capacitance | Output capacitance inside the device, from either output to DVSS. | | 2 | | pF |
| **DIGITAL OUTPUTS (SDOUT)** | | | | | |
| High-level output voltage | | 1.6 | 1.8 | | V |
| Low-level output voltage | | | 0 | 0.2 | V |
| Output impedance | | | 50 ±25% | | Ω |

(1) All LVDS specifications have been characterized but not tested at production. For clock input levels, see the *Recommended Operating Conditions* table.

## OUTPUT INTERFACE TIMING

Typical values are at 25°C, AVDD3 = 3.3V, AVDD18 = DVDD = 1.8V, LVCMOS (single ended) clock, $C_{LOAD}$ = 5pF, $R_{LOAD}$ = 100Ω, $I_O$ = 3.5mA, unless otherwise noted. Minimum and maximum values are across the full temperature range $T_{MIN}$ = –40°C to $T_{MAX}$ = 85°C.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_a$ | Aperture delay | The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs | 0.7 | 3 | | ns |
| | Aperture delay matching | Across channels within the same device | | ±150 | | ps |
| $t_j$ | Aperture jitter | | | 450 | | fs rms |
| | Wake-up time | Time to valid data after coming out of STANDBY mode | | 10 | 50 | µs |
| | | Time to valid data after coming out of PDN GLOBAL mode | | 50 | 200 | |
| | | Time to valid data after stopping and restarting the input clock | | 30 | 200 | |
| | ADC latency | Default, after reset | | 11 | | Input clock cycles |
| $t_{delay}$ | Data and frame clock delay | Input clock rising edge (zero cross) to frame clock rising edge (zero cross) minus half the input clock period (T). | 3 | 4.7 | 6.4 | ns |
| $\Delta t_{delay}$ | Delay variation | At fixed supply and 20°C T difference | –1 | | 1 | ns |
| $t_{RISE}$<br>$t_{FALL}$ | Data rise time<br>Data fall time | Rise time measured from –100mV to 100mV<br>Fall time measured from 100mV to –100mV<br>10MHz < $f_{CLKIN}$ < 65MHz | 0.1 | 0.25 | 0.4 | ns |
| $t_{FCLKRISE}$<br>$t_{FCLKFALL}$ | Frame clock rise time<br>Frame clock fall time | Rise time measured from –100mV to 100mV<br>Fall time measured from 100mV to –100mV<br>10MHz < $f_{CLKIN}$ < 65MHz | 0.1 | 0.25 | 0.4 | ns |
| | Frame clock duty cycle | Zero crossing of the rising edge to zero crossing of the falling edge | 48% | 50% | 52% | |
| $t_{DCLKRISE}$<br>$t_{DCLKFALL}$ | Bit clock rise time<br>Bit clock fall time | Rise time measured from –100mV to 100mV<br>Fall time measured from 100mV to –100mV<br>10MHz < $f_{CLKIN}$ < 65MHz | 0.1 | 0.2 | 0.35 | ns |
| | Bit clock duty cycle | Zero crossing of the rising edge to zero crossing of the falling edge<br>10MHz < $f_{CLKIN}$ < 65MHz | 44% | 50% | 56% | |

## Output Interface Timing(1)

| $f_{CLKIN}$, Input Clock Frequency | Period (T) | Setup Time ($t_{su}$), ns | | | Hold Time ($t_h$), ns | | | $t_{pdi}$ = 0.5 × T + $t_{delay}$, ns | | |
|---|---|---|---|---|---|---|---|---|---|---|
| MHz | ns | Zero-Cross Data to Zero-Cross Clock (both edges) | | | Zero-Cross Clock to Zero-Cross Data (both edges) | | | Input Clock Zero-Cross (rising edge) to Frame Clock Zero-Cross (rising edge) | | |
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX |
| 65 | 15 | 0.35 | 0.6 | | 0.3 | 0.6 | | | 12.3 | |
| 50 | 20 | 0.5 | 0.8 | | 0.5 | 0.8 | | | 14.6 | |
| 40 | 25 | 0.75 | 1 | | 0.75 | 1 | | | 17 | |
| 30 | 33 | 1 | 1.4 | | 1 | 1.4 | | | 21.2 | |
| 20 | 50 | 1.7 | 2.1 | | 1.7 | 2.1 | | | 29.5 | |
| 10 | 100 | 3.8 | 4.2 | | 3.8 | 4.2 | | | 54.7 | |

(1) FCLK timing is the same as for the output data lines. It has the same relation to DCLK as the data pins. Setup and hold are the same for the data and the frame clock.

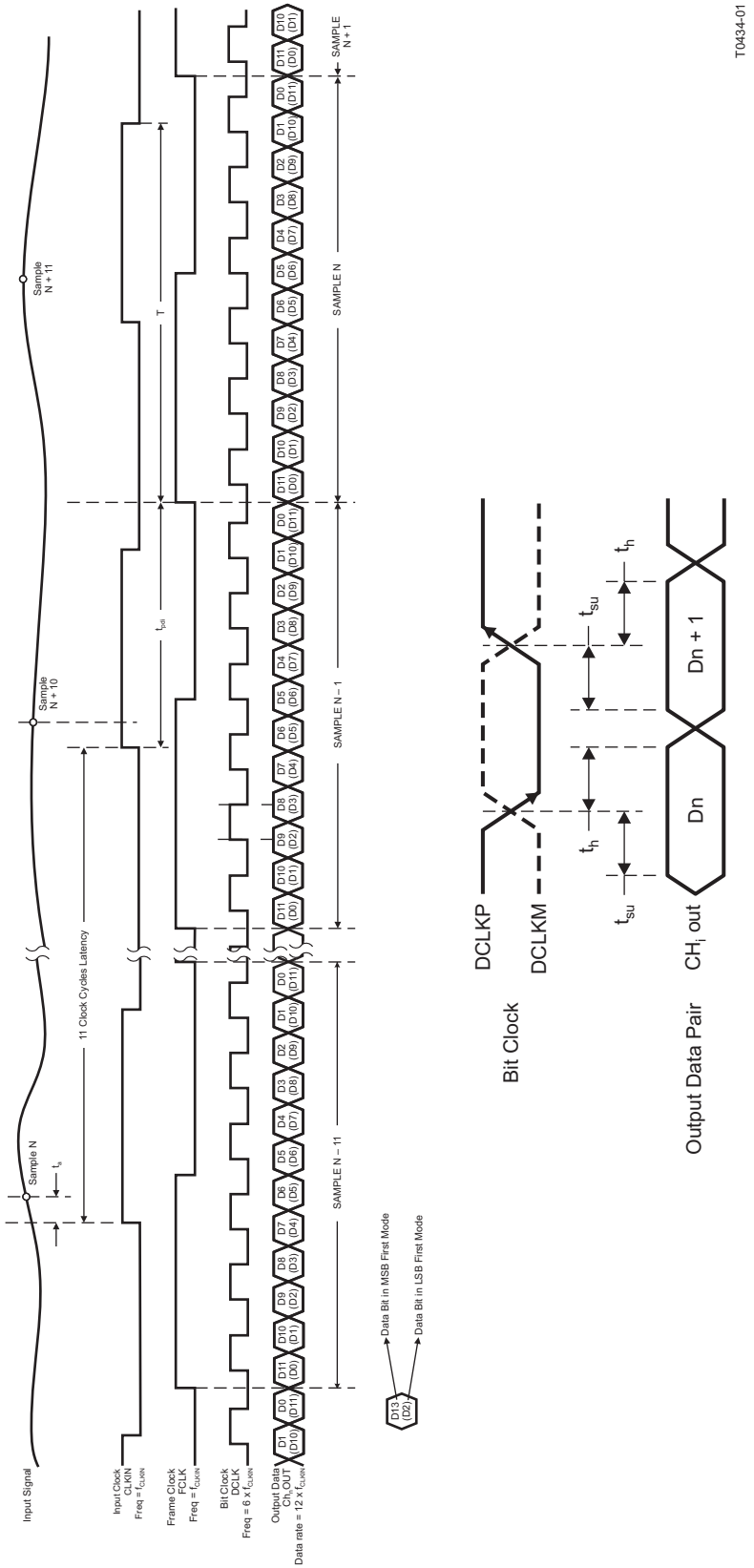



**Figure 1. Timing Diagram**

## TYPICAL CHARACTERISTICS

All graphs are at 25°C, AVDD3 = 3.3V, AVDD18 = DVDD18 = 1.8V, –1dBFS analog input AC coupled with 0.1μF, internal reference mode, maximum rated channel sampling frequency (65MSPS), LVCMOS (single-ended) clock, 50% duty cycle, $f_{IN}$ = 2MHz, anti-aliasing filter set at 14MHz (3dB corner), output clamp disable and analog high-pass filter enabled.

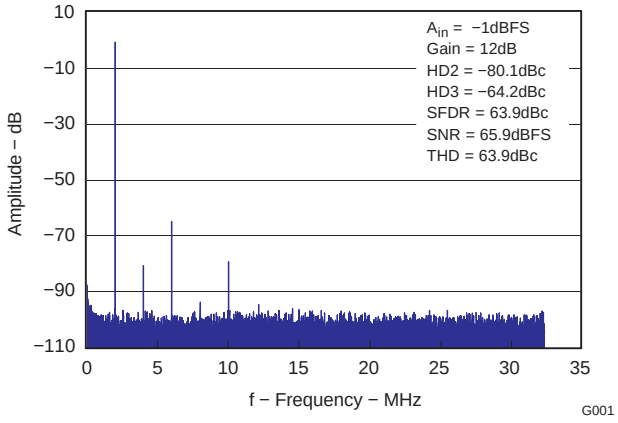



**Figure 2. FFT for 2MHz Input Signal and 12dB Gain**

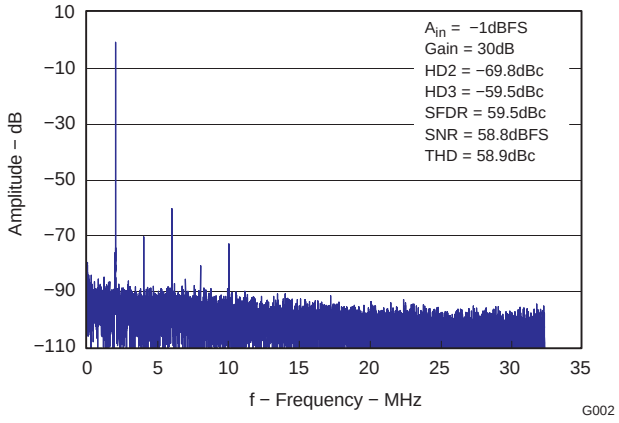



**Figure 3. FFT for 2MHz Input Signal and 30dB Gain**

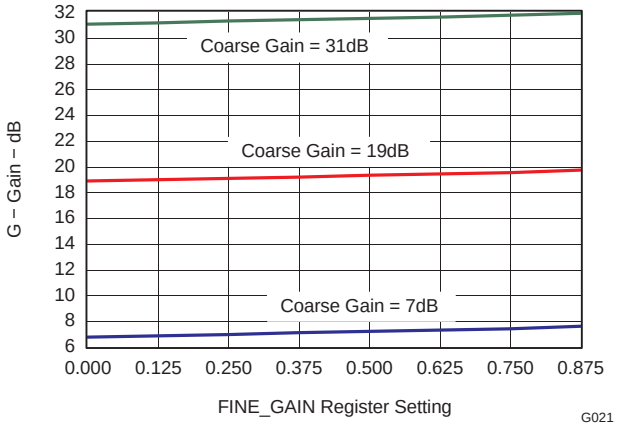



**Figure 4. Fine Gain vs Gain Code**

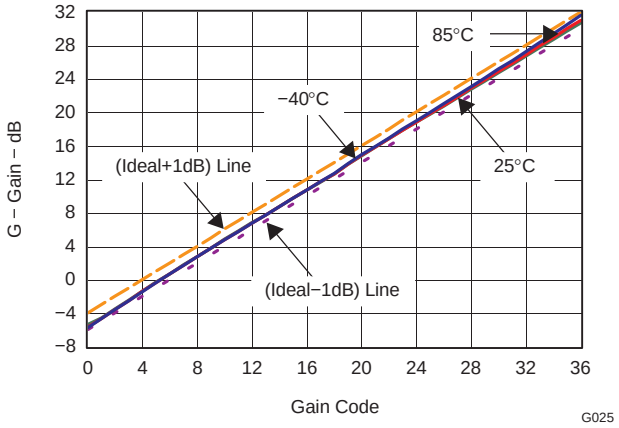



**Figure 5. Gain vs Gain Code and Temperature**

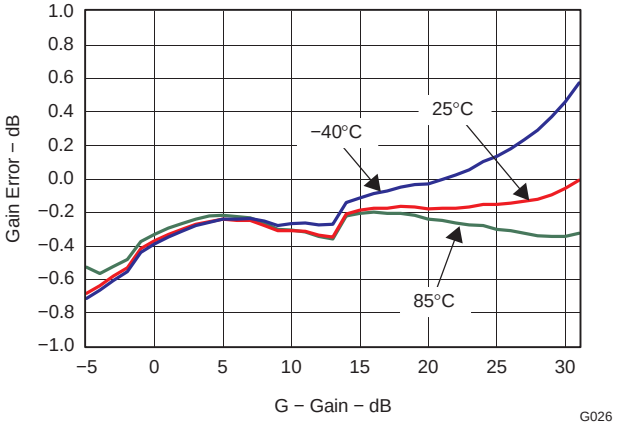



**Figure 6. Gain Error vs Gain Code and Temperature**

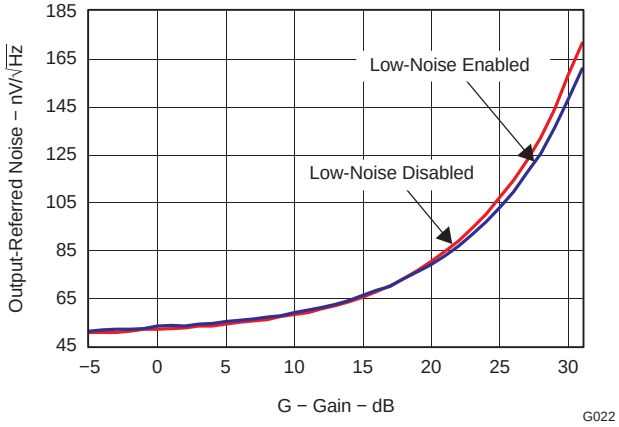



**Figure 7. Output-Referred Noise vs Gain**

## TYPICAL CHARACTERISTICS (continued)

All graphs are at 25°C, AVDD3 = 3.3V, AVDD18 = DVDD18 = 1.8V, –1dBFS analog input AC coupled with 0.1μF, internal reference mode, maximum rated channel sampling frequency (65MSPS), LVCMOS (single-ended) clock, 50% duty cycle, $f_{IN}$ = 2MHz, anti-aliasing filter set at 14MHz (3dB corner), output clamp disable and analog high-pass filter enabled.

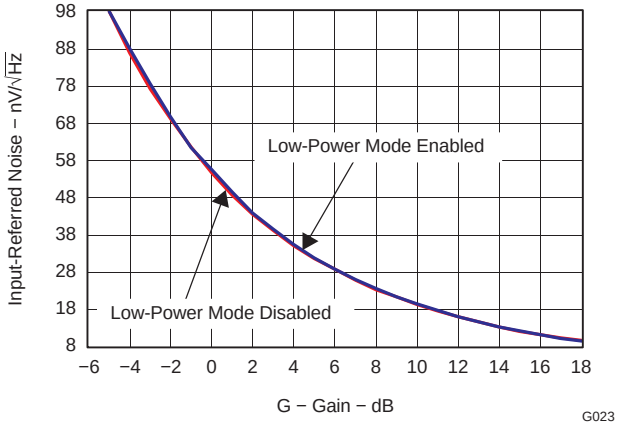



**Figure 8. Input-Referred Noise for Low Gains**

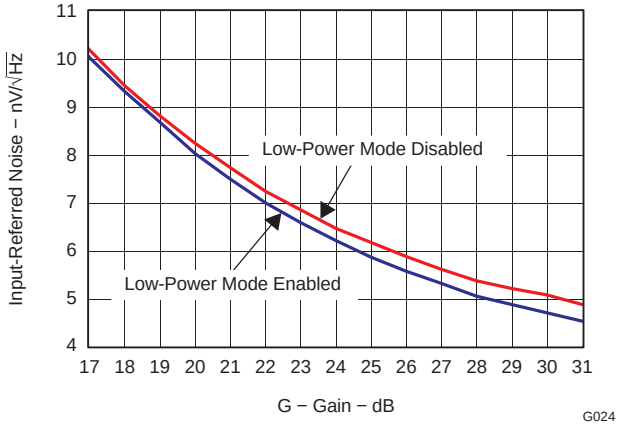



**Figure 9. Input-Referred Noise for High Gains**

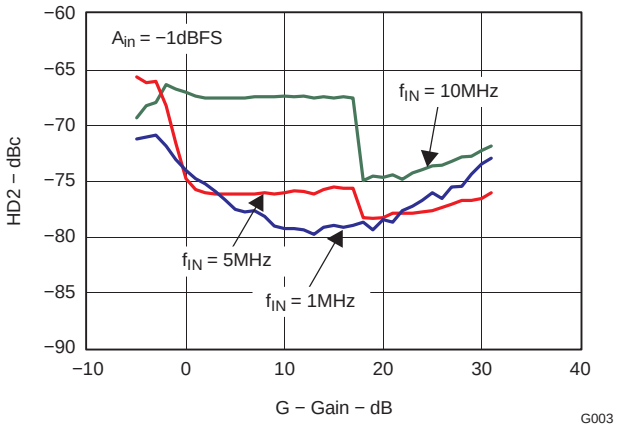



**Figure 10. HD2 Across Coarse Gain and Three $f_{IN}$ (–1dBFS)(1)**

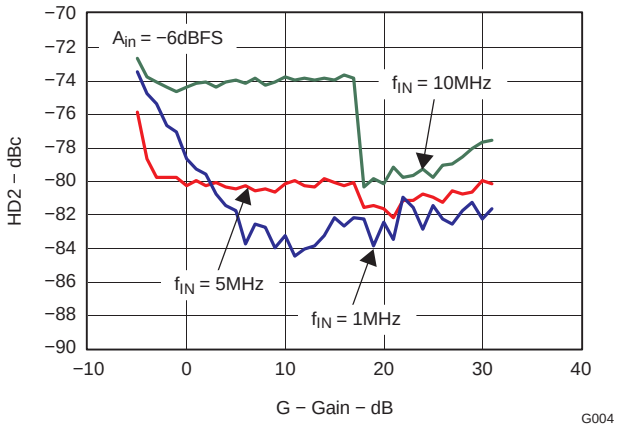



**Figure 11. HD2 Across Coarse Gain and Three $f_{IN}$ (–6dBFS)(2)**

(1) For gains ≥5dB, the input amplitude is adjusted to give –1dBFS. At 5dB gain, input amplitude is 4dBm (corresponding to –1dBFS). For gains less than 5dB, the input is kept constant at 4dBm.
(2) For gains ≥0dB, the input amplitude is adjusted to give –6dBFS. At 0dB gain, input amplitude is 4dBm (corresponding to –6dBFS). For gains less than 0dB, the input is kept constant at 4dBm.

## TYPICAL CHARACTERISTICS (continued)

All graphs are at 25°C, AVDD3 = 3.3V, AVDD18 = DVDD18 = 1.8V, –1dBFS analog input AC coupled with 0.1µF, internal reference mode, maximum rated channel sampling frequency (65MSPS), LVCMOS (single-ended) clock, 50% duty cycle, $f_{IN}$ = 2MHz, anti-aliasing filter set at 14MHz (3dB corner), output clamp disable and analog high-pass filter enabled.

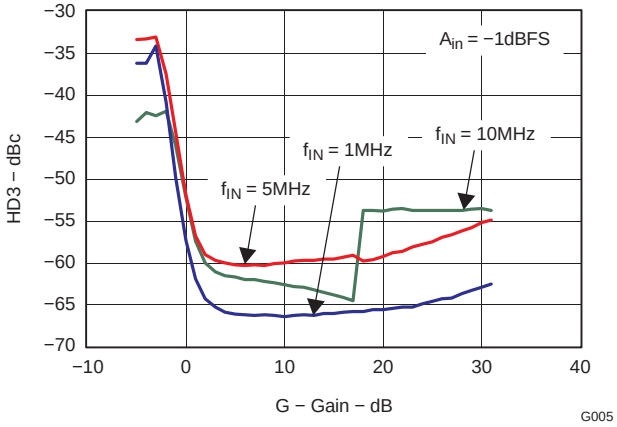



**Figure 12. HD3 Across Coarse Gain and Three $f_{IN}$ (–1dBFS)(1)**

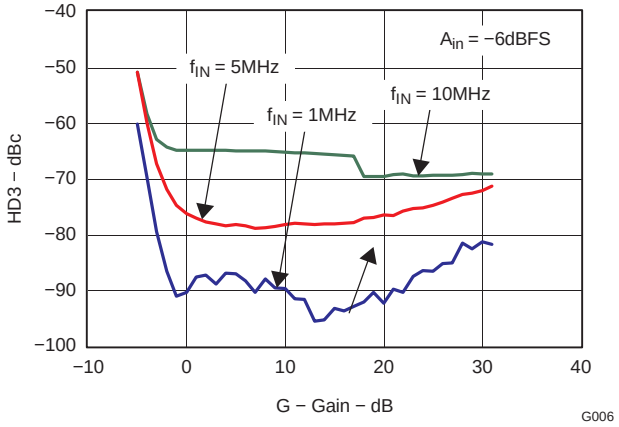



**Figure 13. HD3 Across Coarse Gain and Three $f_{IN}$ (–6dBFS)(2)**

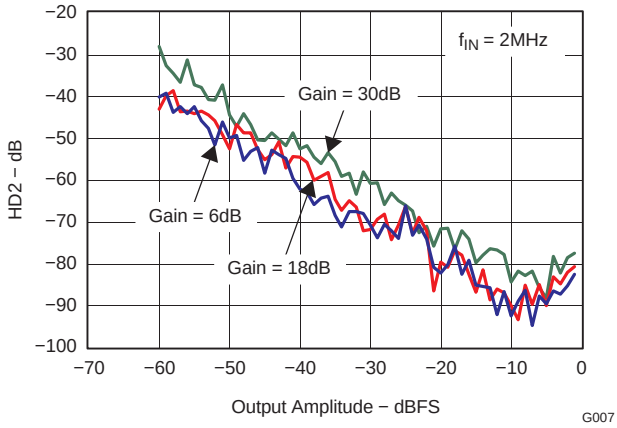



**Figure 14. HD2 vs Output Amplitude**

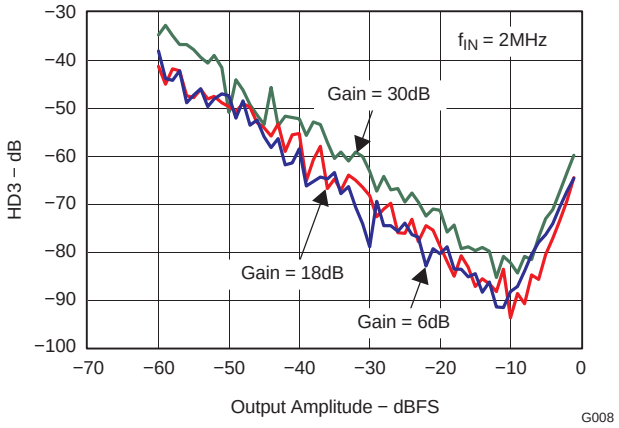



**Figure 15. HD3 vs Output Amplitude**

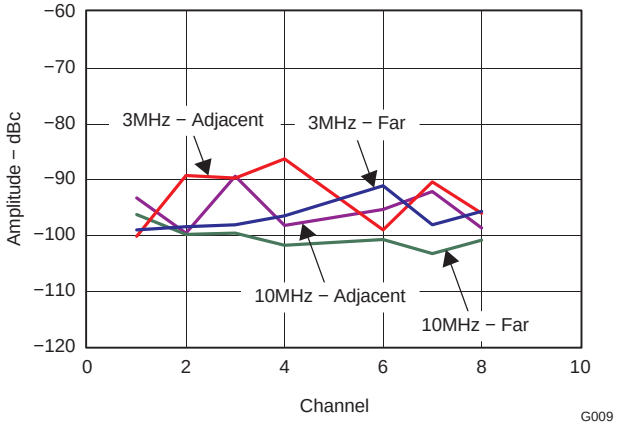



**Figure 16. Crosstalk(3)**

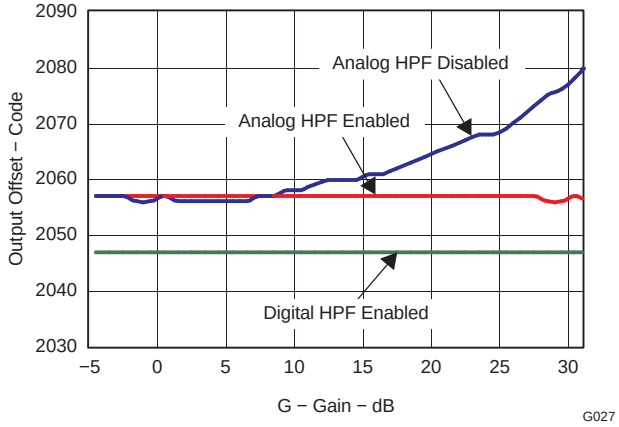



**Figure 17. Output Offset vs Gain**

(3) –1dB signal applied on one channel at a time and output is observed on:
1. Adjacent channel - channel next to the aggressor channel, but not a shared channel
2. Far channel - all other channels (neither shared or adjacent)

## TYPICAL CHARACTERISTICS (continued)

All graphs are at 25°C, AVDD3 = 3.3V, AVDD18 = DVDD18 = 1.8V, –1dBFS analog input AC coupled with 0.1μF, internal reference mode, maximum rated channel sampling frequency (65MSPS), LVCMOS (single-ended) clock, 50% duty cycle, $f_{IN}$ = 2MHz, anti-aliasing filter set at 14MHz (3dB corner), output clamp disable and analog high-pass filter enabled.

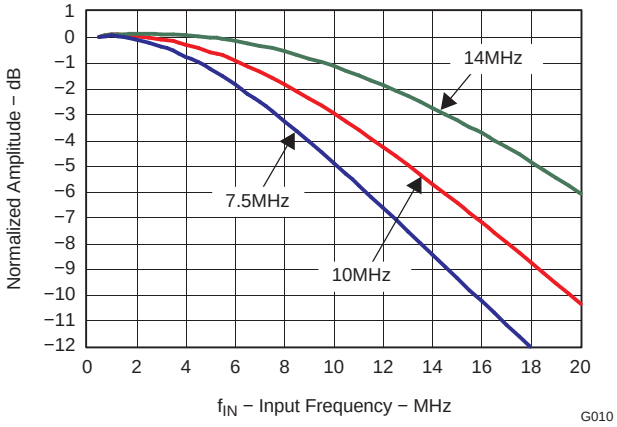



**Figure 18. Antialiasing Filter Frequency Response**

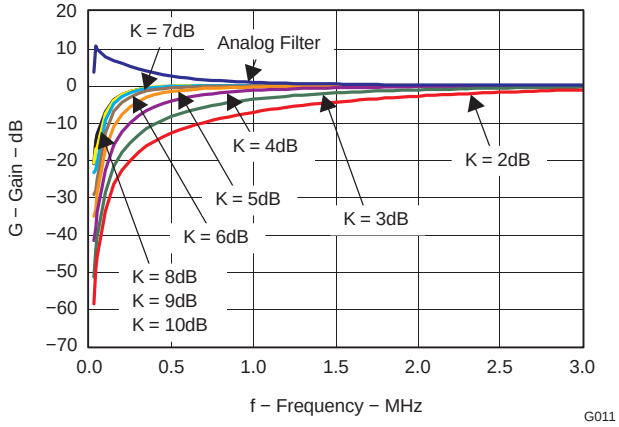



**Figure 19. High-Pass Filter Options**

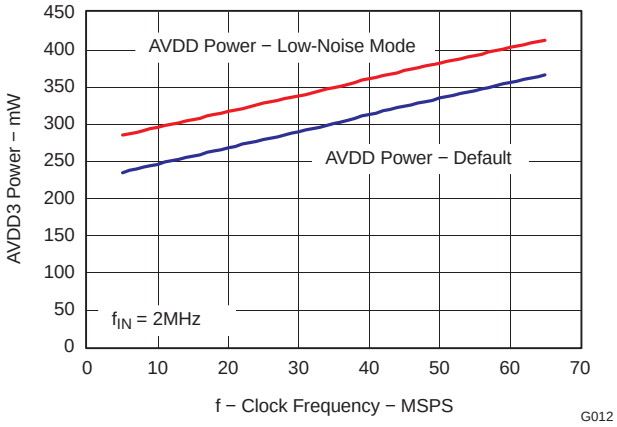



**Figure 20. Analog Power vs Input-Clock Frequency**

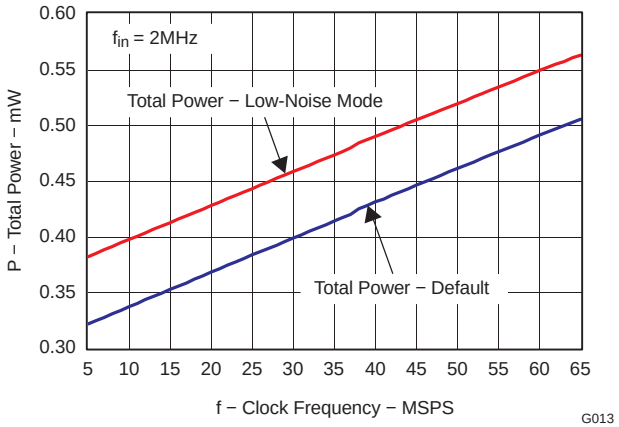



**Figure 21. Total Power vs Input-Clock Frequency**

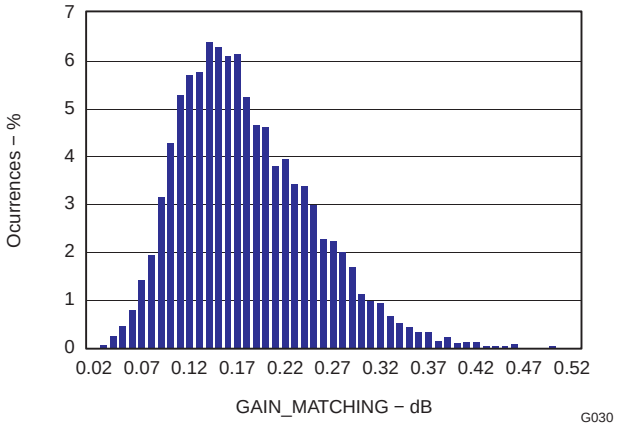



**Figure 22. Gain Matching Measured at a Single Gain (30 dB) as Peak-to-Peak Variation of Gain Across Channels on Every Device and Measured at Three Temperatures. Every Device at Each Temperature Counted as One Event**

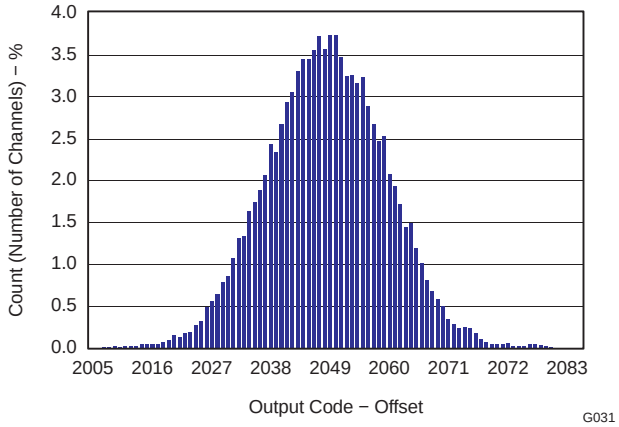



**Figure 23. Offset (Average Code) With Signal. Every Channel Counted as One Event**

## TYPICAL CHARACTERISTICS (continued)

All graphs are at 25°C, AVDD3 = 3.3V, AVDD18 = DVDD18 = 1.8V, –1dBFS analog input AC coupled with 0.1μF, internal reference mode, maximum rated channel sampling frequency (65MSPS), LVCMOS (single-ended) clock, 50% duty cycle, $f_{IN}$ = 2MHz, anti-aliasing filter set at 14MHz (3dB corner), output clamp disable and analog high-pass filter enabled.

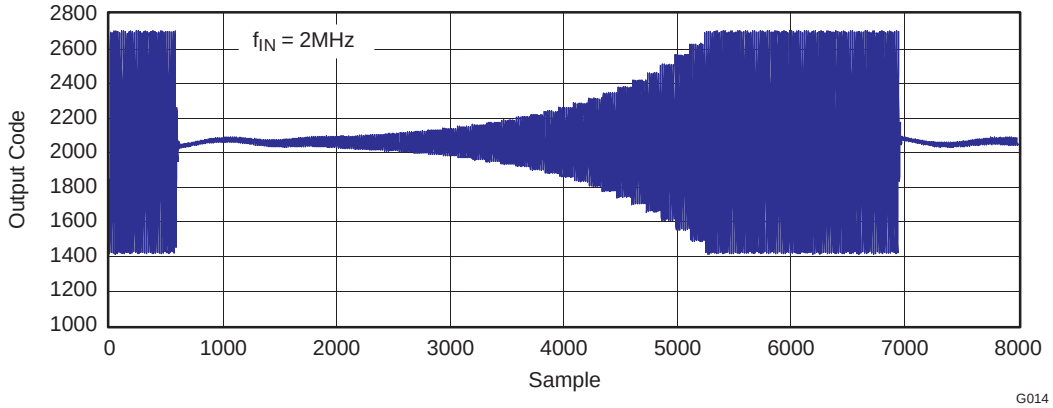



**Figure 24. TGC Sweep With Interpolation Disabled and High-Pass Filter Enabled**

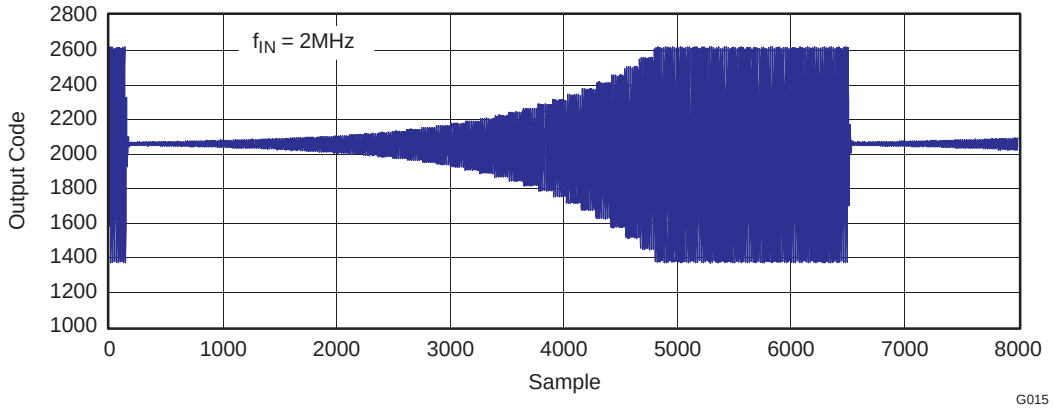



**Figure 25. TGC Sweep With Interpolation Disabled and High-Pass Filter Disabled**

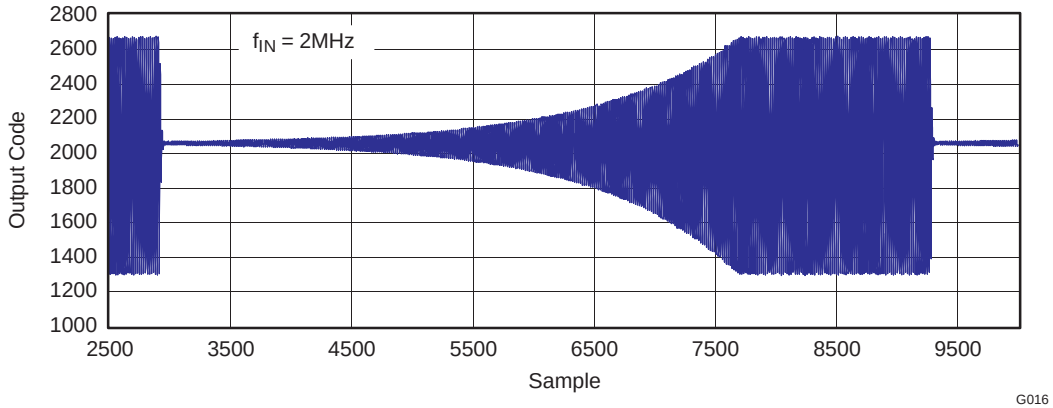



**Figure 26. TGC Sweep With Interpolation Enabled and High-Pass Filter Disabled**

## TYPICAL CHARACTERISTICS (continued)

All graphs are at 25°C, AVDD3 = 3.3V, AVDD18 = DVDD18 = 1.8V, –1dBFS analog input AC coupled with 0.1µF, internal reference mode, maximum rated channel sampling frequency (65MSPS), LVCMOS (single-ended) clock, 50% duty cycle, $f_{IN}$ = 2MHz, anti-aliasing filter set at 14MHz (3dB corner), output clamp disable and analog high-pass filter enabled.

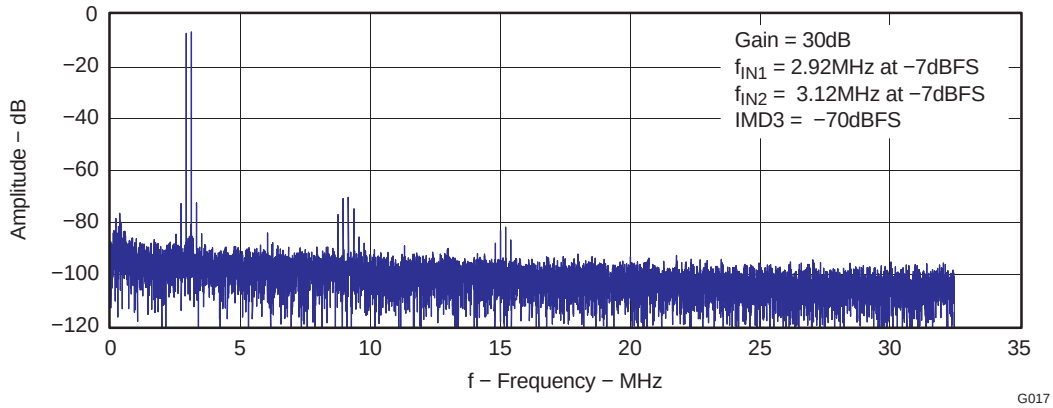



**Figure 27. Intermodulation Distortion**

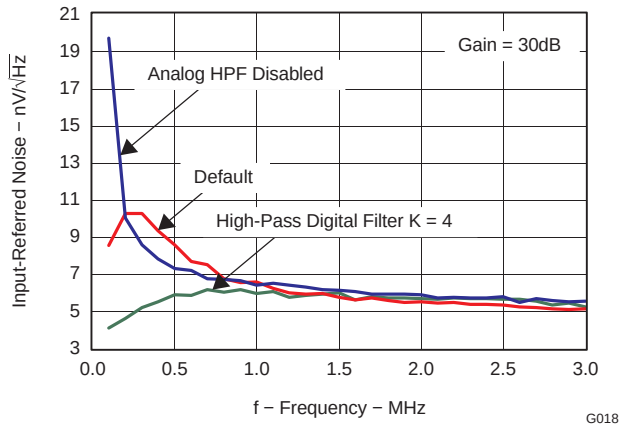



**Figure 28. Input-Referred Noise vs Frequency**

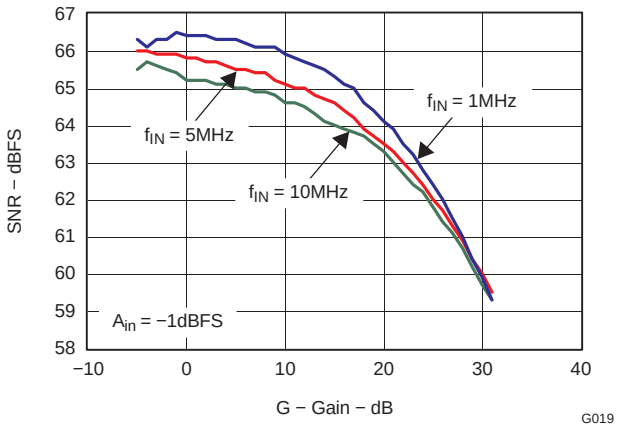



**Figure 29. SNR vs Gain, Three $f_{IN}$ (–1dBFS)**

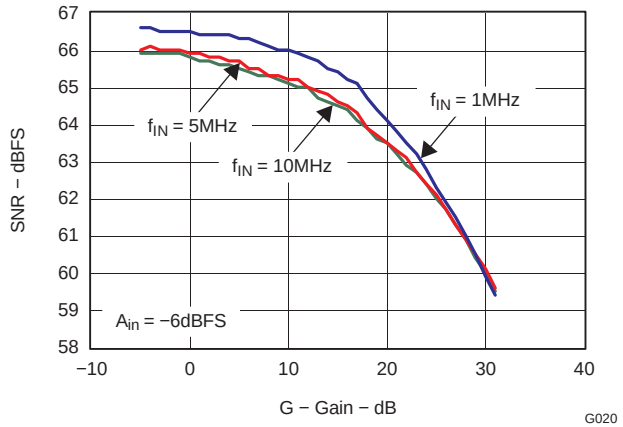



**Figure 30. SNR vs Gain Three $f_{IN}$ (–6dBFS)**

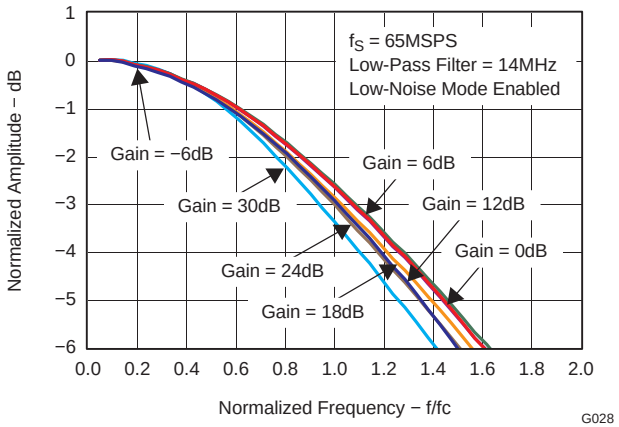



**Figure 31. LPF Response Across Coarse Gain**

## TYPICAL CHARACTERISTICS (continued)

All graphs are at 25°C, AVDD3 = 3.3V, AVDD18 = DVDD18 = 1.8V, –1dBFS analog input AC coupled with 0.1µF, internal reference mode, maximum rated channel sampling frequency (65MSPS), LVCMOS (single-ended) clock, 50% duty cycle, $f_{IN}$ = 2MHz, anti-aliasing filter set at 14MHz (3dB corner), output clamp disable and analog high-pass filter enabled.

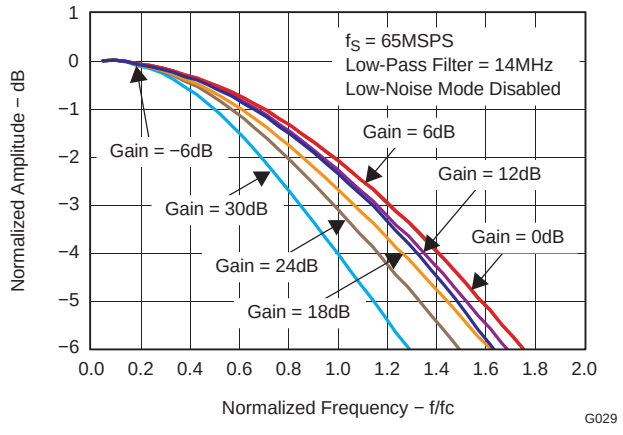



**Figure 32. LPF Response Across Coarse Gain**

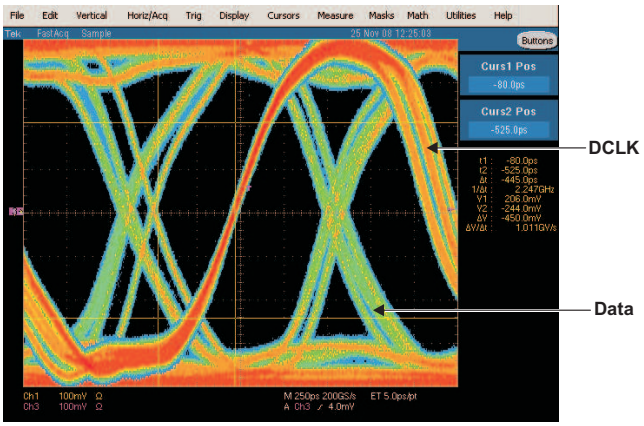



**Figure 33. LVDS Eye Pattern**

# APPLICATION INFORMATION

## THEORY OF OPERATION

The AFE5801 is a very low-power CMOS monolithic analog front end which includes an eight-channel variable-gain amplifier (VGA) followed by an eight-channel, 12bit, high-speed pipeline analog-to-digital convereter (ADC) based on switched-capacitor architecture.

Each of the eight VGA differential inputs is buffered and accepts a maximum swing of 2Vpp centered at a dc level (VCM) of about 1.6V.

Each VGA has a gain range from –5dB to 31dB, and the gain is digitally controlled, with a resolution of 0.125dB. Using the serial interface, the gain curves (common to all VGAs) versus time can be stored in the memory integrated within the device.

A hardware sync input pin is available (SYNC). When a pulse is applied to this pin, all the VGAs in the device start stepping through the selected time-gain curve at the same clock cycle. This sync can also be initiated by software using the serial interface.

A selectable anti-alias low-pass filter (AAF) with 3dB attenuation at 7.5MHz, 10MHz, or 14MHz is also integrated, together with clamping (which can be disabled).

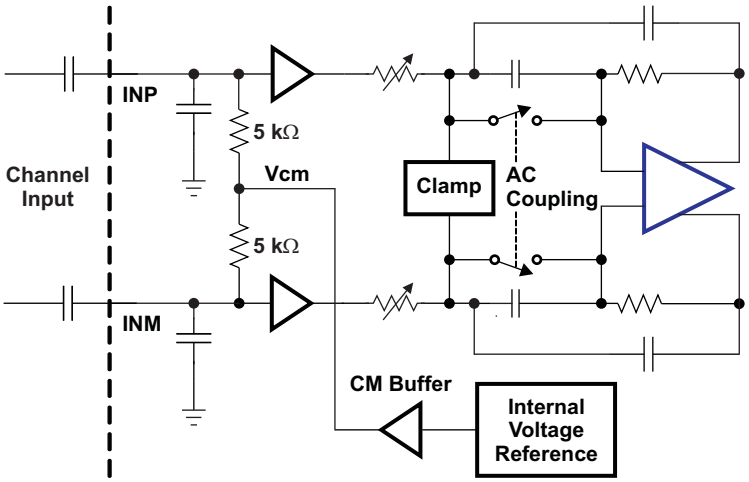
The VGA/AAF can output 2Vpp differential swing without degradation in the specified linearity and can drive an onboard 12bit ADC. After the input signals are captured by the sample-and-hold circuit, at the rising edge of the clock, the samples are sequentially converted by a series of low-resolution stages. The outputs of the stages are combined in a digital correction logic block to form the final 12bit word with a latency of 11 clock cycles, without taking into account the delays introduced by the optional digital signal-processing functions. These functions are, in this order, offset correction, channel averaging, digital gain, and high-pass filtering (see *General-Purpose Register Map* for more details). The 12bit words of each channel are serialized and output as LVDS levels. For slower operation speeds, the AFE5801 offers the possibility of multiplexing up to two input channels into one LVDS output stream, reducing even further the power consumption and routing area. In addition to the data streams, a bit clock and frame clock are also output. The frame clock is aligned with the 12bit word boundary.

Notice that for the correct operation of the device (see the *Serial Interface* section), a positive pulse must be applied to the RESET pin. This sets the internal control registers to zero. There is, nevertheless, no need for any type of power-up sequencing.

## INPUT CONFIGURATION

The analog input for the AFE5801, Figure 34, consists of a differential analog buffer which has inputs biased to 1.6V (usually refered as common-mode voltage, $V_{CM}$). The biasing is done with two internal resistors of 5kΩ. For proper operation, the input signal should be either ac-coupled or have a commn-mode value equal to $V_{CM}$. In the case of ac coupling, the external input capacitors form a high-pass filter with the internal bias resistors (5kΩ), so, the value of the capacitors should allow the lowest frequency of interest to pass with minimum attenuation. For the typical frequencies used in ultrasound (>1MHz) a value of 10nF or bigger is recommended. If dc coupling is preferred, the user can tap the $V_{CM}$ output pins to set the common-mode level of the input signal. The $V_{CM}$ output should be connected to high-input-impedance circuits, as its driving capability is limited. Regardless of the choosen input configuration, a capacitor of 100nF should be connected on each $V_{CM}$ input to AVSS.

For proper operation, the input signal should be in the recommended input range. The maximum input swing is limited to 2Vpp before saturation/distortion fo the input stage occurs. As the input common mode (VCM) is about 1.6V, each input of the buffer should stay between 1.1V and 2.1V.




NOTE: Dashed area denotes one of eight channels.

**Figure 34. Common-Mode Biasing of Input Pins**

The maximum input swing is limited to 2Vpp before distortion/saturation of the input stage occurs. As the input dc level (VCM) is about 1.6V, this means that each input of the VGA typically stays between 1.1V and 2.1V.

To drive the AFE5801 with a single-ended signal, the signal should be connected to one of the inputs ($IN_iP$, in principle, to keep the polarity) and the other connected to AVSS through a 100nF capacitor. In fact, all the AFE5801 inputs that must be connected to ground can be shorted together and connected to ground through a single 100nF capacitor. The input is limited to 1Vpp (from 1.1V to 2.1V) and the performance is similar to that of the AFE5851. Every channel on the AFE5851 is similar to a channel on the AFE5801 where the other input has been shorted internally to VCM. See the *AFE5851 16 Channel Variable Gain Amplifier (VGA) With Octal High Speed ADC* data sheet (SLOS574) for more information.

## SERIAL INTERFACE

### Register Initialization

After power up, the internal registers must be initialized to the default value (zero). Initialization can be done in one of two ways:

- Through a hardware reset, by applying a positive pulse in the RESET pin
- Through a software reset, using the serial interface, by setting the SOFTWARE RESET bit to high. Setting this bit initializes the internal registers to the respective default values (all zeros) and then self-resets the SOFTWARE RESET bit to low. In this case, the RESET pin can stay low (inactive).

  It is important to notice that after power up and before the device is reset to its default state, the power consumption could be up to 2× the specified maximum, due to the unknown setting of the internal registers. In order to prevent the initial increased power consumption, a potential solution is to connect the RESET pin to either 1.8V or 3.3V supply with a 10kΩ resistor, so that the device is reset while powering up. For the reset to take effect, the power must be up on DVDD18. Notice that there is no damage to the part by applying voltage to the RESET pin while the device power is off.

  Notice also that the reset only affects the digital registers, putting the part in its default state. It does not act as a power down and as such, everything internal just keeps running. As the internal registers change their values, the effects on the data propagate through the pipe. At the same time, there may be some glitches on the output due to the transition of the registers values if any of the output controlling modes, for instance, change. As the reset is level-sensitive and asynchronous with the input clock, it should be inactive in order to write into the internal registers. Although it takes only 10ns after the reset rising edge to change the registers, the output data may take, in the worst case, up to 20 clock cycles to be considered stable. Notice that the output clocks (data and frame) are independent of the RESET and tight to the input clock, avoiding any loss of synchronization.

### *Reset Timing*

Typical values at 25°C, min and max values across the full temperature range $T_{MIN}$ = –40°C to $T_{MAX}$ = 85°C, AVDD3 = 3.3V, AVDD18 = DVDD18 = 1.8V, unless otherwise noted.

| PARAMATER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_1$ | Power-on delay time | Delay from power-up of AVDD and LVDD to RESET pulse active | 5 | | | ms |
| $t_2$ | Reset pulse width | Pulse width of active RESET signal | 10 | | | ns |
| $t_3$ | Register write delay time | Delay from RESET disable to $\overline{SEN}$ active | 25 | | | ns |
| $t_{PO}$ | Power-up delay time | Delay from power-up of AVDD and LVDD to output stable | | 6.5 | | ms |

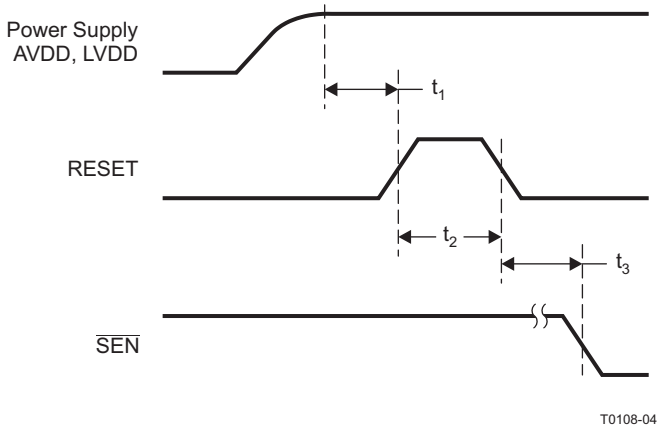



**Figure 35. Reset Timing**

Programming of different modes can be done through the serial interface formed by pins $\overline{SEN}$ (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data) and RESET. SCLK and SDATA have a 100kΩ pulldown resistor to ground, and $\overline{SEN}$ has a 100kΩ pullup resistor to DVDD18. Serial shift of bits into the device is enabled when $\overline{SEN}$ is low. Serial data SDATA is latched at every rising edge of SCLK when $\overline{SEN}$ is active (low). The serial data is loaded into the register at every 24th SCLK rising edge when $\overline{SEN}$ is low. In case the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24bit words within a single active $\overline{SEN}$ pulse (there is an internal counter that counts groups of 24 clocks after the falling edge of $\overline{SEN}$). The interface can work with SCLK frequency from 20MHz down to very low speeds (a few Hertz) and even with a non-50% duty-cycle SCLK.

The data is divided in two main portions: a register address (8 bits) and the data itself, to load on the addressed register (16 bits). When writing to a register with unused bits, these should be set to 0. Also, when writing, the SDOUT signal outputs zeros. The following timing diagram illustrates this process.

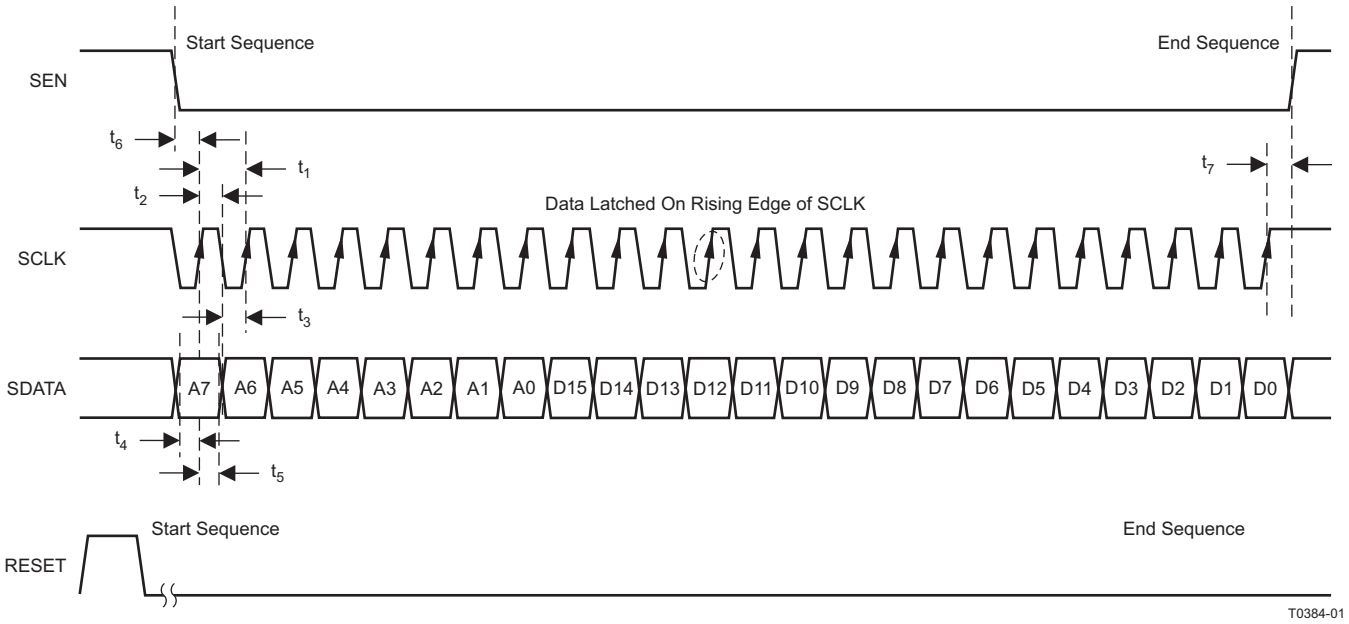



**Figure 36. Serial Interface Register Write**

Minimum values across full temperature range $T_{MIN}$ = –40°C to $T_{MAX}$ = 85°C, AVDD3 = 3.3V, AVDD18 = DVDD18 = 1.8V.

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_1$ | SCLK period | 50 | | | ns |
| $t_2$ | SCLK high time | 20 | | | ns |
| $t_3$ | SCLK low time | 20 | | | ns |
| $t_4$ | Data setup time | 5 | | | ns |
| $t_5$ | Data hold time | 5 | | | ns |
| $t_6$ | $\overline{SEN}$ fall to SCLK rise | 8 | | | ns |
| $t_7$ | Time between last SCLK rising edge to $\overline{SEN}$ rising edge | 8 | | | ns |

## GENERAL-PURPOSE REGISTER MAP

The internal registers can be divided in two groups, a group of registers to control all the general functions and settings of the device, and a bank of registers to control the TGC/gain curves operation. Those two sets of registers overlap in all the address space, except for the address 0, which holds the control of the register bank. One of the bits of this register, TGC_REG_WREN (see following table) is used to access one set of registers or the other. Its default value is zero and gives access to the general-purpose registers (which are also by default zero). The TGC control registers (described after the general-purpose registers) can be accessed by writing 1 to TGC_REG_WREN.

The following table describes the function of the registers when TGC_REGISTER_WREN = 0 (default). The address format is *address[bit of the register]*.

| ADDRESS | FUNCTION | DESCRIPTION |
|---|---|---|
| 0[2] | TGC_REGISTER_WREN | 0: Access to general-purpose registers. 1: Access to TGC registers |
| 0[1] | REGISTER_READOUT_ENABLE | 1: Enables readout of the registers |
| 0[0] | SOFTWARE_RESET | 1: Resets the device and self-resets the bit to zero |
| 1[14] | OUTPUT_RATE_2X | 0: 1× rate (one ADC per LVDS stream). 1: 2× rate (2 ADCs per LVDS stream) |
| 1[13] | EXTERNAL_REFERENCE | 0: Internal reference. 1: External reference |
| 1[11] | LOW_FREQUENCY_NOISE_SUPRESSION | 0: No supression. 1: Supresses noise at low frequencies and pushes it to $f_S/2$ |

| ADDRESS | FUNCTION | DESCRIPTION |
|---|---|---|
| 1[10] | STDBY | 0: Power up. 1: Standby (fast power-up mode) |
| 1[9:2] | PDN CHANNEL<7:0> | PDN for each individual channel (VCA+ADC). LVDS outputs logic 0. |
| 1[1] | OUTPUT_DISABLE | 0: Ouptut enabled. 1: Output disabled |
| 1[0] | GLOBAL_PDN | 0: Power up. 1: Global power down (slow power-up mode) |
| 2[15:13] | PATTERN_MODES | Pattern modes for serial LVDS. 000: No pattern. 001: Sync. 010: Deskew. 011: Custom reg. 100: All 1s. 101: toggle. 110: All 0s. 111: Ramp |
| 2[11] | AVERAGING_ENABLE | 0: Default (no averaging). 1: Average two channels to increase SNR. |
| 2[10:3] | PDN_LVDS | Power down the eight data-output LVDS pairs. |
| 3[14:13] | SERIALIZED_DATA_RATE | Serialization factor. 00: 12×. 01: 10×. 10: 16×. 11: 14× |
| 3[12] | DIGITAL_GAIN_ENABLE | 0: Default (no gain). 1: Apply digital gain set by the following registers. |
| 3[8] | REGISTER_OFFSET_SUBTRACTION_ ENABLE | 0: Default (no subtraction). 1: Subtract offset value set in the corresponding registers. |
| 4[3] | DFS | Data format select. 0: 2s complement. 1: Offset binary |
| 5[13:0] | CUSTOM_PATTERN | Custom pattern data for LVDS (PATTERN_MODES = 011) |
| 7[10] | VCA_LOW_NOISE_MODE_(INCREASE_ POWER) | 0: Low power. 1: Low noise, at the expense of increased power (5mW/channel) |
| 7[8:7] | SELF_TEST | 00 or 10: No self-test. 01: Self-test enabled. 100 mV dc applied to the input of the channels. 11: Self-test enabled. 150 mV dc applied to the input of the channels. NOTE: DC applied before the input buffer. Test does not work if input is dc-shorted to a different potential. Also notice that the INTERNAL_AC_COUPLING bit is automatically set to 1 when entering this mode, and reset back to whatever value it had before, when leaving this mode. |
| 7[3:2] | FILTER_BW | 00: 14MHz. 01: 10MHz. 10: 7.5MHz. 11: Not used. |
| 7[1] | INTERNAL_AC_COUPLING | VGA coupling. 0: AC-coupled. 1: DC-coupled |
| 13[15:11] | DIG_GAIN1 | 0dB to 6dB in steps of 0.2dB |
| 13[9:2] | OFFSET_CH1 | Value to be subtracted from channel 1 |
| 15[15:11] | DIG_GAIN2 | 0dB to 6dB in steps of 0.2dB |
| 15[9:2] | OFFSET_CH2 | Value to be subtracted from channel 2 |
| 17[15:11] | DIG_GAIN3 | 0dB to 6dB in steps of 0.2dB |
| 17[9:2] | OFFSET_CH3 | Value to be subtracted from channel 3 |
| 19[15:11] | DIG GAIN4 | 0dB to 6dB in steps of 0.2dB |
| 19[9:2] | OFFSET_CH4 | Value to be subtracted from channel 4 |
| 21[4:1] | DIGITAL_HIGH_PASS_FILTER_CORNER_ FREQ_FOR_CHANNELS-1–4 | Sets k for the high-pass filter as desribed in *General-Purpose Register Description* (k from 2 to 10). |
| 21[0] | DIGITAL_HIGH_PASS_FILTER_ENABLE_ FOR_CHANNELS_1–4 | 0: No high-pass filter. 1: High-pass filter enabled |
| 25[15:11] | DIG_GAIN8 | 0dB to 6dB in steps of 0.2dB |
| 25[9:2] | OFFSET_CH8 | Value to be subtracted from channel 5 |
| 27[15:11] | DIG_GAIN7 | 0dB to 6dB in steps of 0.2dB |
| 27[9:2] | OFFSET_CH7 | Value to be subtracted from channel 6 |
| 29[15:11] | DIG_GAIN6 | 0dB to 6dB in steps of 0.2dB |
| 29[9:2] | OFFSET_CH6 | Value to be subtracted from channel 7 |
| 31[15:11] | DIG_GAIN5 | 0dB to 6dB in steps of 0.2dB |
| 31[9:2] | OFFSET_CH5 | Value to be subtracted from channel 8 |
| 33[4:1] | DIGITAL_HIGH_PASS_FILTER_CORNER_ FREQ_FOR_CHANNELS_5–8 | Sets k for the high-pass filter as desribed in *General-Purpose Register Description* (k from 2 to 10). |
| 33[0] | DIGITAL_HIGH_PASS_FILTER_ENABLE_ FOR_CHANNELS_5–8 | 0: No high-pass filter. 1: High-pass filter enabled |
| 70[14] | CLAMP_DISABLE | 0: Enabled. 1: Disabled |

## GENERAL-PURPOSE REGISTER DESCRIPTION

### AVERAGING_ENABLE

Address: 2[11]

When set to 1, two samples, corresponding to two consecutive channels, are averaged (channel 1 with 2, 3 with 4, 5 with 6, and 7 with 8). If both channels receive the same input, the net effect is an improvement in SNR. The averaging is performed as:

- Channel 1 + channel 2 comes out on channel 3.
- Channel 3 + channel 4 comes out on channel 4.
- Channel 5 + channel 6 comes out on channel 5.
- Channel 7 + channel 8 comes out on channel 6.

### DFS

Address: 4[3]

DFS stands for data format select. The ADC output, by default, is in 2s-complement mode. Programming the DFS bit to 1 inverts the MSB, and the output becomes straight-offset binary mode.

### DIGITAL_GAIN_ENABLE

Address: 3[12]

Setting this bit to 1 applies to each channel i the corresponding gain given by $DIG\_GAIN_i$<15:11>. The gain is given as 0dB + 0.2dB × $DIG\_GAIN_i$<15:11>. For instance, if $DIG\_GAIN_5$<15:11> = 3, channel 5 is increased by 0.6dB gain. $DIG\_GAIN_i$<15:11> = 31 produces the same effect as $DIG\_GAIN_i$<15:11> = 30, setting the gain of channel i to 6dB.

### DIGITAL_HIGH_PASS_FILTER_ENABLE and DIGITAL_HIGH_PASS_FILTER_CORNER_FREQ

DIGITAL_HIGH_PASS_FILTER_ENABLE (channels 1–4): Address: 21[0]
DIGITAL_HIGH_PASS_FILTER_ENABLE (channels 5–8): Address: 33[0]
DIGITAL_HIGH_PASS_FILTER_CORNER_FREQ (channels 1–4): Address: 21[4:1]
DIGITAL_HIGH_PASS_FILTER_CORNER_FREQ (channels 5–8): Address: 33[4:1]

This group of four registers controls the characteristics of a digital high-pass transfer function applied to the output data, following the formula: $y(n) = 2^k/(2^k + 1) [x(n) – x(n – 1) + y(n – 1)]$. The DIGITAL_HIGH_PASS_FILTER_CORNER_FREQ registers (one for the first four channels and one for the second group of four channels) describe the setting of k.

### EXTERNAL_REFERENCE

Address: 1[13]

The internal reference mode (default) uses approximately 3mW more power on AVDD (which is already included in all the specification tables). The AFE5801 can operate in external reference mode by programming EXTERNAL_REFERENCE to 1. In this mode, the VREF_IN pin should be driven with 1.4V. Due to the high input impedace of this pin, no special drive capabilities are required. For the same reason, no decoupling on VREF_IN is needed, although depending on the noise on the 1.4V signal, some filtering may be required. Nevertheless, when using the internal reference, there is no need to decouple VREF_IN. The advantage of using the external reference mode is that multiple AFE5801 units can be made to operate with the same external reference, thereby improving parameters such as gain matching across devices.

### FILTER_BW

Address: 7[3:2]

This bit sets the 3dB attenuation frequency for the antialiasing filter (AAF).

### GLOBAL_PDN

Address: 1[0]

The global PDN bit is ORed with the signal in the external PDN pin (59). Therefore, a 1 on this bit shuts the device down completely.

### INTERNAL_AC_COUPLING

Address: 7[1]

This bit controls an internal high-pass filter (Figure 34), set between the input buffer and the VCA. This filter removes the input offset to avoid its amplification by the TGC. An alternative method is to remove the offset effect on the digital domain, either on the device following the ADC or at the ADC output, by using the DIGITAL HIGH PASS FILTER registers described previously.

### LOW_FREQUENCY_NOISE_SUPPRESSION

Address: 1[11]

The low-frequency noise-suppression mode is specifically useful in applications where good noise performance is desired in the frequency band of 0MHz to 1MHz (around dc). Setting this mode shifts the low-frequency noise of the ADC in the AFE5801 to approximately $f_S/2$, thereby reducing the noise floor around dc to a much lower value.

### OUTPUT_DISABLE

Address: 1[1]

A 1 on this bit sets all the LVDS outputs into the high-impedance state.

### OUTPUT_RATE_2X

Address: 1[14]

The output data always uses a DDR format, with valid/different bits on the positive as well as the negative edges of the LVDS bit clock, DCLK. The output rate is set by default to 1× (OUTPUT_RATE_2X = 0), where each ADC has one LVDS stream associated with it. If the sampling rate is low enough, two ADCs can share one LVDS stream, in this way lowering the power consumption devoted to the interface. The unused outputs will output zero. To avoid consumption from those outputs, no termination should be connected to them. The distribution on the used output pairs is done in the following way:

- Channel 1 and channel 2 come out on channel 3. Channel 1 comes out first.
- Channel 3 and channel 4 come out on channel 4. Channel 3 comes out first.
- Channel 5 and channel 6 come out on channel 5. Channel 5 comes out first.
- Channel 7 and channel 8 come out on channel 6. Channel 7 comes out first.

### PATTERN_MODES and CUSTOM_PATTERN

PATTERN_MODES: Address: 2[15:13]

CUSTOM_PATTERN: Address: 5[13:0]

The AFE5801 can output a variety of test patterns on the LVDS outputs. These test patterns replace the normal ADC data output and help on debugging and synchronization, with the device reading the output of the ADC.

- PATTERN_MODE equal to 000 is the default and disables this test mode, i.e., the output data is the same as the ADC data.
- PATTERN_MODE equal to 001 (SYNC mode) replaces the normal ADC word by a fixed 1111 1100 0000 word.
- PATTERN_MODE equal to 010 sets the DESKEW mode, where the 12-bit ADC output D<11:0> is replaced with the 0101 0101 0101 word, which creates a continuous stream of 1s and 0s in the data line.
- PATTERN_MODE equal to 011 outputs a constant code set by the bits in CUSTOM_PATTERN<13:0>. Depending on the value of SERIALIZED_DATA_RATE (see following) the output bits conform to the following rules:
  - In the default case, where SERIALIZED_DATA_RATE is 00, for 12-bit ADC data at the output, the CUSTOM_PATTERN<13:2> bits are used, replacing the sampled data. These bits are still controlled by the LSB-first and MSB-first modes in the same way as normal ADC data are.
  - For SERIALIZED_DATA_RATE = 01, 10-bit output mode is selected, and the CUSTOM_PATTERN<13:4> bits are used.
  - For SERIALIZED_DATA_RATE = 10, 16-bit output mode is selected. In this case, the CUSTOM_PATTERN<13:0> bits are used for the first 14 most-significant bits, and two 0s take the place of the LSBs.
  - For SERIALIZED_DATA_RATE = 11, 14-bit mode is selected, and the CUSTOM_PATTERN<13:0> bits take the place of the output word.
- PATTERN_MODE equal to 100 makes the output always 1, whereas setting it to 110 makes the output always 0.
- PATTERN_MODE equal to 101 makes the output of the device toggle between two consecutive codes. On the nth sample clock, the data is 0000 0000 0000, and on the following one (nth + 1), it is 1111 1111 1111.
- PATTERN_MODE equal to 111 causes all the channels to output a repeating full-scale ramp pattern. The ramp increments from zero code to full-scale code in steps of 1 LSB every clock cycle. After hitting the full-scale code, it returns back to the zero code and ramps again.

### PDN_CHANNEL<7:0>

Address: 1[9:2]

Each bit controls the power down of a channel (buffer, VCA, and ADC). For example, PDN_CHANNEL<0> powers down channel 1 and the corresponding LVDS pair becomes high-impedance. DCLK and FCLK are not powered down. They become active if terminated with 100Ω.

### PDN_LVDS

Address: 2[10:3]

PDN_LVDS<7:0> selects which LVDS pairs become inactive (zero output current, i.e., high-impedance state). The frame and clock LVDS streams are powered down only when OUTPUT_DISABLE and/or GLOBAL_PDN is set.

### REGISTER_OFFSET_SUBTRACTION_ENABLE

Address: 3[8]

Setting this bit to 1 enables the substraction of the value on the corresponding OFFSET_CH$_i$<9:2> (offset for channel i) from the ADC output. The number is specified in 2s-complement format. For example,

OFFSET_CH$_i$<9:2> = 0100 0000 means substract –128. For OFFSET_CH$_i$<9:2> = 0111 1111 the effect is to substract 127. In effect, both addition and subtraction can be performed. Note that the the offset is applied before the digital gain (see DIGITAL_GAIN_ENABLE). The whole data path is 2s-complement throughout internally. Only when DFS = 1 (straight binary output format) is the 2s-complement word translated into offset binary at the end.

### REGISTER_READOUT_ENABLE

Address: 0[1]

The device includes an option where the contents of the internal registers can be read back. This may be useful as a diagnostic to verify the serial interface communication between the external controller and the AFE. First, the <REGISTER READOUT ENABLE> bit must be set to 1. Then user should initiate a serial interface cycle specifying the address of the register (A7–A0) whose content is to be read. The data bits are don't care. The device outputs the contents (D15–D0) of the selected register on the SDOUT pin. The external controller can latch the contents at the rising edge of SCLK. To enable serial register writes, set the <REGISTER READOUT ENABLE> bit back to 0. The following timing diagram shows this operation (the time specifications follow the same information provided on the table for a serial interface register write):

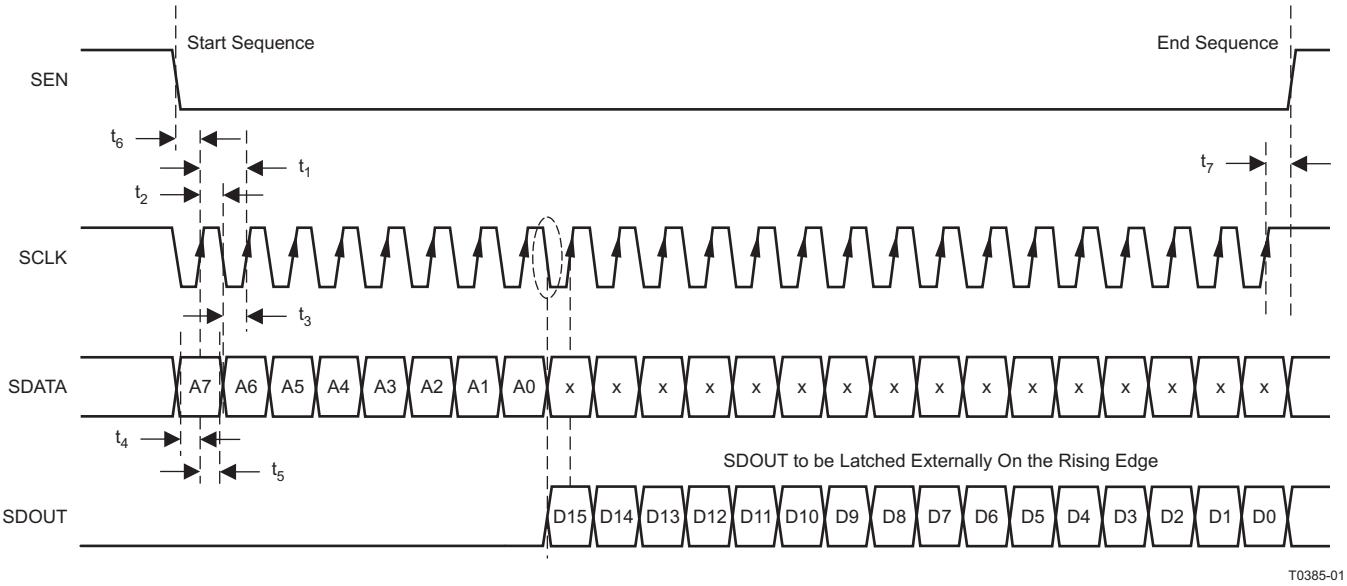



**Figure 37. Serial Interface Register Read**

Register readback is incorrect for address 0x97. See the INTERP_ENABLE section for details.

### SERIALIZED_DATA_RATE

Address: 3[14:13]

These two bits control the length of the data word, i.e., the number of DCLKs per FCLK period. It is possible, for instance, to output a 16bit data stream even with a 12bit ADC. In this case, the 4 LSBs are padded with 0s. The pass from higher resolution to lower serialization is not supported, however. I.e, it is not possible to select a 10bit stream with a 12bit ADC.

### TGC_REGISTER_WREN

Address: 0[2]

Set this bit to 1 to access the TGC table and 0 (default after reset) to access the general-purpose register table. The same address may point, this way, to one bank of registers (general purpose) or to the other (TGC control). Nevertheless, observe that register 0 of the general-purpose registers is always accessible, regardless of the value of TGC_REGISTER_WREN. The TGC table starts at address 1.

### VCA_LOW_NOISE_MODE

Address: 7[10]

Setting this bit to 1 reduces the equivalent input noise of the VCA to 5nv/√Hz (for a 51dB gain) at the expense of an increased power consumption (5mW increase per channel).

## TGC CONTROL REGISTER MAP

The TGC operation is described in the VGA/TGC Operation section that follows. This section describes the TGC control registers which can be accessed by writing 1 to TGC_REG_WREN bit. The following table describes the register map for all the registers involved in the TGC operation.

| ADDRESS | D[15:7] | D[8] | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x01...0x94 | | REG_VALUES | | | | | | | | |
| 0x95 | NOT USED | | START_INDEX | | | | | | | |
| 0x96 | | | STOP_INDEX | | | | | | | |
| 0x97 | | | INTERP_ ENABLE | 0 | START_GAIN | | | | | |
| 0x98 | | | HOLD_ GAIN _TIME | | | | | | | |
| 0x99 | | | 0 | 0 | SOFT_ SYNC | UNIFORM_ GAIN_ MODE | STATIC_ PGA | FINE_GAIN | | |
| 0x9A | | | 0 | 0 | COARSE_GAIN | | | | | |
| 0x9B | | | UNIFORM_GAIN_SLOPE | | | | | | | |

### REG_VALUE

Address: 0x01[8:0] to 0x94[8:0]

Each of these 9 bit registers (148 of them) stores the time to stay at a given gain setting, during the gain ramp. The most significant bit of each register (REG_VALUE<8>) denotes either increment or decrement gain from current gain value. The other 8 bits (REG_VALUE<7:0>) denote the time (a multiple of 8 × Tclk; Tclk being the channel sampling clock, i.e., double the period of the device input clock) for the change of the gain from the CURRENT_GAIN to CURRENT_GAIN ±1dB (depending on the REG_VALUE<8>). The fastest ramp (shortest time) for this 1dB gain change is set by REG_VALUE<7:0> equal to 0x00 and it is 8 × Tclk. The slowest ramp (longest time) for this 1dB gain change is set by REG_VALUE<7:0> equal to 0xFF, and it is 255 × 8 × Tclk (see VGA operation – described later).

### START_INDEX

Address: 0x95[7:0]

This 8 bit register specifies/points to the first REG_VALUE register of the TGC curve (i.e., where the curve starts) and can have values ranging from 1 to 148 (in decimal).

### STOP_INDEX

Address: 0x96[7:0]

This 8 bit register specifies/points to the last REG_VALUE register of the TGC curve (i.e., where the curve finishes) and can have values ranging from 1 to 148 (in decimal).

### START_GAIN

Address: 0x97[5:0]

This 6 bit register specifies the start gain value from –5dB to 31dB.

START_GAIN = [–5 + REG_VALUE ] dB

| REG_VALUE | GAIN |
|---|---|
| 0x0 | –5 dB |
| 0x1 | –4 dB |
| 0x24 | 31 dB |

### STOP_GAIN (Not a programmable register; it is an internally computed value.)

Case 1:

INTERP_ENABLE = 1,

STOP_GAIN = START_GAIN + (STOP_INDEX – START_INDEX) – ( 2 × Number of decrements) + 0.875dB.

Case 2:

INTERP_ENABLE = 0,

STOP_GAIN = START_GAIN + (STOP_INDEX – START_INDEX) – ( 2 × Number of decrements).

### HOLD_GAIN_TIME

Address: 0x98[7:0]

This 8 bit register specifies the time for holding of the STOP_GAIN, after reaching either the STOP_GAIN value as computed in the *STOP_GAIN* section or the maximum/minimum gain. After this time, the TGC starts stepping down to the START_GAIN value in 1dB steps every Tclk. The STOP_GAIN value is held for the following number of clocks:

HOLD_GAIN_TIME = [33 × REG_VALUE] Tclks

where Tclk is the channel sampling clock.

| **REG_VALUE** | **HOLD_GAIN_TIME** |
|---|---|
| 0x0 | 0 Tclks |
| 0x1 | 33 Tclks |
| 0xFF | 8415 Tclks |

### INTERP_ENABLE

Address: 0x97[7]

This 8 bit register sets the ramp rate. When INTERP_ENABLE = 1, the ramp rate is 0.125dB for every number of clocks stored in REG_VALUE:

| REG_VALUE | SLOPE |
|---|---|
| 0x0 | 0.125dB per Tclk |
| 0x1 | 0.125dB per Tclk |
| 0x2 | 0.125dB per 2 × Tclk |
| 0xFF | 0.125dB per 255 × Tclk |

When INTERP_ENABLE = 0 the ramp rate is 1dB for every 8 times the number of clocks stored in REG_VALUE:

| REG_VALUE | SLOPE |
|---|---|
| 0x0 | 1dB per 8 × Tclk |
| 0x1 | 1dB per 8 × Tclk |
| 0x2 | 1dB per 16 × Tclk |
| 0xFF | 1dB per 255× 8 × Tclk |

**NOTE**

Reading back the address 0x97 (INTERP_ENABLE) to verify its value shows the opposite value of what it actually is. For instance, after setting INTERP_ENABLE to 1 in addres 0x97 to enable interpolation, the bit shows as 0 when reading it back from the same address (0x97). After setting INTERP_ENABLE to 0 in addres 0x97 to disable interpolation, the bit shows as 1 when reading it back.

### SOFT_SYNC

Address 0x99[5]

Setting SOFT_SYNC bit to 1 enables the TGC engine to run periodically following a given TGC curve, without the need for a high pulse signal in the SYNC pin (see more details in the *Soft Synchronization* section).

### UNIFORM_GAIN_MODE

Address 0x99[4]

Setting this bit to 0 (default) directs the TGC engine to follow an arbitrary gain-versus-time curve. If this bit is set to 1, the gain is ramped up with a slope set by the UNIFORM_GAIN_SLOPE register. (See more details in the *Uniform Gain Increment Mode* section.)

### UNIFORM_GAIN_SLOPE

Address 0x9B[7:0]

See the *Uniform Gain Increment Mode* section.

### STATIC_PGA

Address 0x99[3]

Setting this bit to 1 disables the TGC engine. COARSE_GAIN and FINE_GAIN control the gain value, which is independent of time.

### COARSE_GAIN

Address 0x9A[5:0]

This 6 bit register specifies the coarse gain from –5 to 31dB, in 1dB steps. Observe that only values from 0x00 to 0x24, both included, are valid. Setting a value bigger than 0x24 on the COARSE_GAIN register is the same as setting 0x24. COARSE_GAIN = [–5 + REG_VALUE ] dB

| REG_VALUE | GAIN |
|---|---|
| 0x0 | –5dB |
| 0x1 | –4dB |
| 0x24 | 31dB |

### FINE_GAIN

Address 0x99[2:0]

This 3 bit register specifies the fine gain in steps of 0.125dB resolution, from 0dB to 0.875dB. FINE_GAIN = [0.125 × REG_VALUE ] dB

| REG_VALUE | GAIN |
|---|---|
| 0x0 | 0dB |
| 0x1 | 0.125dB |
| 0x7 | 0.875dB |

## VGA/TGC OPERATION

The gain variation of the variable gain amplifier (VGA) versus time is called the TGC function and on the AFE5801 is controlled digitally. The gain is implemented by a switched network where the switches controlling the gain are synchronized with the ADC sampling instant to minimize glitches on the output data. The gain setting depends on the mode of operation selected by the user. There are 3 possible modes of operation: non-uniform gain, uniform gain, and static mode. The following sections describe each in detail.

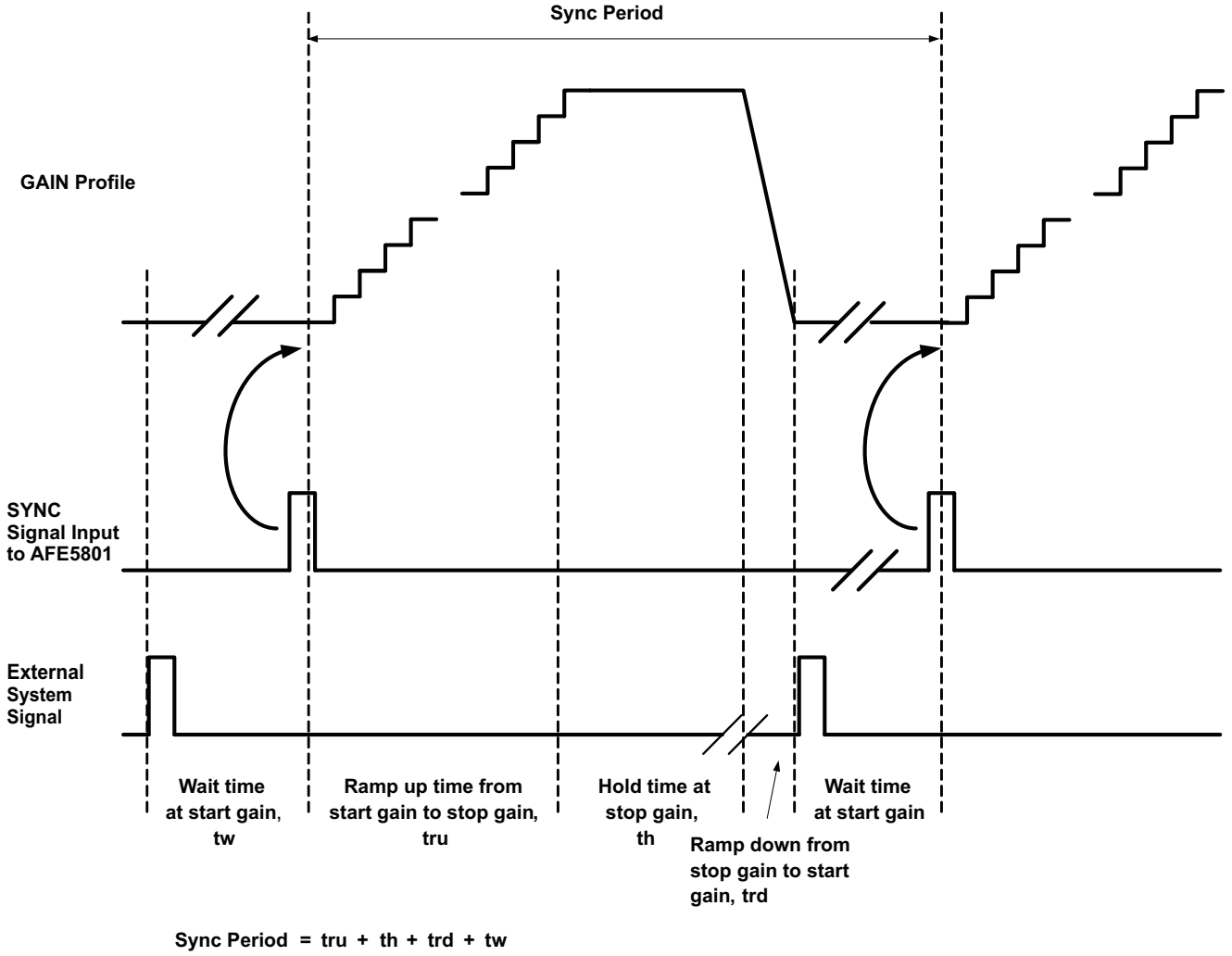



**Figure 38. SYNC Period**

### Non-Uniform Gain Increment Mode

In the non-uniform gain increment mode, the user sets an arbitrary shape for the gain versus time curve. For a given time/sampling instant, the digital gain setting is obtained from an internal memory of 148 positions/registers (named REG_VALUEs), each 9 bits wide, loaded by the user through the serial port (see Serial Interface section). Addresses 1 to 148 can be used to access these registers, while TGC_REGISTER_WREN = 1.

As explained above, the most significant bit of each register (REG_VALUE<8>) denotes either increment or decrement gain from current gain value. The other 8 bits (REG_VALUE<7:0>) denote the time (a multiple of 8 × Tclk, being Tclk the sampling clock) for the change of the gain from the CURRENT_GAIN to CURRENT_GAIN ±1dB (depending on the REG_VALUE<8>). The fastest ramp (shortest time) for this 1dB gain change is set by REG_VALUE<7:0> equal to 0x00 and it is 8 × Tclk. The slowest ramp (longest time) for this 1dB gain change is set by REG_VALUE<7:0> equal to 0xFF and it is 255 × 8 × Tclk.

INTERP_ENABLE sets the way the gain is increased/decreased. By default the gain ramp is implemented in steps of 1dB (INTERP_ENABLE equal to 0). If INTERP_ENABLE is equal to 1, the actual 1dB gain step is implemented in 8 steps of 0.125dB.

The 148 REG_VALUE registers can be used to store either a single curve or multiple TGC curves. The START_INDEX register points to the REG_VALUE register where the TGC curve starts and the STOP_INDEX register points to the REG_VALUE register where the TGC curve stops. Using the START_INDEX and STOP_INDEX registers the desired TGC curves can be chosen.

As shown in Figure 38, a pulse high signal on the SYNC pin will set the starting gain value of the TGC curve to the START_GAIN register value, and it will initiate the progression through the different REG_VALUEs, starting at START_INDEX. Observe that there is no option to delay the start of gain stepping after the SYNC pulse is received. Then, the progression continues until either the STOP_INDEX is reached or maximum/minimum gain is exceeded. After that, the last valid value of gain is held for an extra given number of clocks set by the register HOLD_GAIN_TIME.

After the elapsing of clocks mentioned by the HOLD_GAIN_TIME register, the TGC starts to step down (or up) to the START_GAIN in steps of 1dB every Tclk (channel sampling clock) in preparation for the next TGC profile. The TGC will start updating/following the REG_VALUEs again after a new high pulse on the SYNC pin is given.

The SYNC signal is latched by the rising edge of the channel sampling clock. In other words, the gain increments at the rising edge of the channel sampling clock. Setup time with rising edge is 7ns, and hold time 4ns.

### *Soft Synchronization*

The TGC can run periodically following a given TGC curve but without the need for a high pulse signal in the SYNC pin. This is done by setting SOFT_SYNC bit to 1. Once this bit is set, the sequence of events is the same as with the hardwired SYNC pulse. The TGC curve updates from START_INDEX to STOP_INDEX. After reaching STOP_INDEX or the maximum/minimum gain, the STOP_GAIN value is held for HOLD_VALUE_TIME and then the gain ramps up or down to START_GAIN. After this the TGC update starts again automatically and repeats all these steps periodically till the SOFT_SYNC bit becomes zero.

The SYNC process through register write occurs at the serial clock edge where the register is written. If serial clock and sample clock (channel sampling clock) are synchronous then the described relation in the hardwired SYNC section will hold and the SYNC bit is latched by the rising edge of the channel sampling clock, respecting a setup time with rising edge of 7ns and hold time of 4ns. If sample clock and serial clock are not synchronous then this relationship does not apply and a clock uncertainty of ±1 sample will apply in respect to the nearest sample clock rising edge.

Example 1: In the following example of non-uniform gain mode, all the 148 registers are loaded. Nevertheless, the start address for the TGC is set in START_INDEX to 2 and the stop address (STOP_INDEX) to 7. The START_GAIN is set to 6 and HOLD_GAIN_TIME is 4.

With a high pulse on the SYNC pin the gain starts from 1dB (START_GAIN = 0x06). 1dB to 2dB ramp is done in 120Tclks, using eight 0.125dB steps (as INTERP_ENABLE is set to 1), each 15Tclks long. The ramp from 2dB to 3dB is done in 64Tclks, also in 0.125dB steps. The ramp from 3dB to 4dB is done in 40 Tclks. Decrement from 4dB to 3dB in 64Tclks. Gain increment from 3dB to 4dB in 56 Tclks and from 4dB to 4.875dB in 80 Tclks.

Observe that in the case where INTERP_ENABLE = 1, STOP_GAIN = START_GAIN + (STOP_INDEX – START_INDEX) – ( 2 × Number of decrements) + 0.875dB. In the case where INTERP_ENABLE = 0, STOP_GAIN = START_GAIN + (STOP_INDEX – START_INDEX) – ( 2 × Number of Decrements). This is due to the fact that the interpolation engine keeps the gain increasing or decreasing when INTERP_ENABLE = 1, while the gain is frozen when INTERP_ENABLE = 0.

| TGC REG INDEX | REG_VALUE[8:0] | Number of Tclks | Direction of Gain Change |
|---|---|---|---|
| 1 | 0x004 | 4 × 8 = 32 | Increment |
| 2 | 0x00F | 15 × 8 = 120 | Increment |
| 3 | 0x008 | 8 × 8 = 64 | Increment |
| 4 | 0x005 | 5 × 8 40 | Increment |
| 5 | 0x108 | 8 × 8 = 64 | Decrement |
| 6 | 0x007 | 7 × 8 = 56 | Increment |
| 7 | 0x00A | 10 × 8 = 80 | Increment |
| ... | ... | ... | ... |
| 147 | 0x00F | 15 × 8 = 120 | Increment |
| 148 | 0x00F | 15 × 8 = 120 | Increment |

| NAME | VALUE |
|---|---|
| START_INDEX | 0x02 |
| STOP_INDEX | 0x07 |
| START_GAIN | 0x06 |
| HOLD_GAIN_TIME | 0x04 |
| INTERP_ENABLE | 1 |
| UNIFORM_GAIN_MODE | 0 |

### Uniform Gain Increment Mode

By setting UNIFORM_GAIN_MODE to 1, the TGC engine can also be configured for a uniform increment gain ramp mode where the gain is ramped up from the START_GAIN value to the STOP_GAIN with a slope set by the UNIFORM_GAIN_SLOPE register. Note: STOP_GAIN is not a programmable register, but just an internally computed value from START_GAIN, UNIFORM_GAIN_SLOPE, START_INDEX and STOP_INDEX.

If INTERP_ENABLE = 1, UNIFORM_GAIN_SLOPE sets the number of Tclk (channel sampling clock) at a given gain before incrementing or decrementing 0.125dB. If INTERP_ENABLE = 0, this register sets the number of 8 × Tclk (eight sampling periods) at a given gain before incrementing or decrementing 1dB. Observe that in both cases the time it takes to step by 1dB is the same. In INTERP_ENABLE = 0 the gain is stationary at the same setting for the given time, whereas in the other case the gain increments in fine gain steps of 0.125dB to cover that 1dB step

When INTERP_ENABLE is zero, the STOP_GAIN is computed as START_GAIN + (STOP_INDEX-START_INDEX). Nevertheless, when INTERP_ENABLE = 1, the STOP_GAIN is equal to START_GAIN + (STOP_INDEX - START_INDEX) + 0.875dB. This is basically due to the fact that the interpolation engine keeps the gain increasing on the second case, while, as explained above, is frozen on the first case. Observe that START_INDEX and STOP_INDEX are not used in this case as pointers to the REG_VALUEs table. Instead, only the difference between the two is important to compute STOP_GAIN. As such, START_INDEX can be set to zero and STOP_INDEX will store STOP_GAIN – START_GAIN. Observe that only positive slope ramps are possible.

Example 1: setting START_GAIN = 0x2 (–3dB), START_INDEX = 0x00, STOP_INDEX = 0x06, INTERP_ENABLE = 0 and UNIFORM_GAIN_SLOPE = 0x8, will set the gain at –3dB for 8 × 8 × Tclk, then to –2dB for another 64 Tclk, and so on, through –1, 0, 1, 2 and 3. After spending 64 × Tclk in 3dB, the gain will stay at that gain setting for HOLD_GAIN_TIME and start stepping down back to START_GAIN, with 1dB per Tclk.

Example 2: for the same settings, START_GAIN = 0x2 (–3dB), START_INDEX = 0x00, STOP_INDEX = 0x06, and UNIFORM_GAIN_SLOPE = 0x8, if we set INTERP_ENABLE = 1, the gain will start at –3dB for 8Tclk, then –2.875dB for another 8Tclk, then –2.750dB and so on, till 3dB. At this point, while in example 1, with INTERP_ENABLE = 0 the gain would be frozen for another 64 Tclk, in this example, the gain will continue to increase with 0.125dB steps every 8Tclk till 3.875dB is reached. There will stay for another 8Tclk before starting to wait for HOLD_GAIN_TIME and start stepping down.

Example 3: for START_GAIN = 0x2 (–3dB) , START_INDEX = 0x00, STOP_INDEX = 0x00, INTERP_ENABLE = 1 and UNIFORM_GAIN_SLOPE = 0x1, the gain will step through –3dB, –2.875, –2.75, –2.625, –2.5, –2.375, –2.25 and –2.125, staying at each of these 8 values 1 clock cycle (8 total). Then it will wait for HOLD_GAIN_TIME in –2.125dB and then it will start stepping down back to –3dB.

Example 4: same settings as example 3, but with INTERP_ENABLE = 0, would simply set the VGA gain to –3dB for 8 clock cycles and then the logic would wait for HOLD_GAIN_TIME.

### Static PGA Mode

The 3rd mode of operation is actually a mode where the TGC engine is disabled by writing 1 into the STATIC_PGA bit. This enables the use of a fixed gain mode where the gain is obtained by the sum of a coarse and a fine gain. Coarse gain can be set from –5 to 31dB, in 1dB steps, by the register COARSE_GAIN (6 bit word from 0x00 to 0x24). Setting a value bigger than 0x24 on the COARSE_GAIN register is the same as setting 0x24. The fine gain can be set in steps of 0.125dB resolution, from 0dB to 0.875dB by the FINE_GAIN register (3 bit word with range from 0x00 to 0x07). Observe that the maximum gain, when both registers are set to their maximum gains, is actually 31.875dB.

## ANTI-ALIAS FILTER (AAF)

The AFE5801 integrates a selectable third-order low-pass filter for each of the eight channels. The cutoff frequency can be set for all the channels simultaneously through the serial interface (see FILTER_BW register, in the General Purpose Register table) between 3 possible settings: 7.5, 10 and 14MHz. Figure 18 shows the frequency response for each of these settings. The filter characteristics are set by passive components which are subject to variations over process and temperature. A typical variation of ±5% on the frequency characteristics is expected.

## CLAMPING CIRCUIT AND OVERLOAD RECOVERY

The AFE5801 is designed in particular for ultrasound applications where the front-end device is required to recover very quickly from an overload condition. Such overload can either be the result of a transmit pulse feed-through or a strong echo, which can cause overload of the VGA and ADC.

Enabled by default, the AFE5801 includes a clamping circuit to further optimize the overload recovery behavior of the complete channel (see Figure 34). The circuit can be disabled by writing a 1 in the bit 14 of the address 70 (decimal) of the General Purpose Register Map. The clamp is set to limit the signal at 3dB above the full scale of the ADC (2Vpp).

## CLOCK INPUTS

The eight channels on the device operate from a single clock input. To ensure that the aperture delay and jitter are the same for all channels, the AFE5801 uses a clock tree network to generate individual sampling clocks to each channel. The clock lines for all channels are matched from the source point to the sampling circuit of each of the eight internal ADCs. The variation on this delay is described in the Aperture Delay parameter of the Output Interface Timing. Its variation over time is described in the Aperture Jitter number of the same table.

The AFE5801 clock input can be driven differentially (sine wave, LVPECL or LVDS) or single-ended (LVCMOS). The clock input of the device has an internal buffer/clock amplifier (see Figure 39) which is enabled or disabled automatically depending on the type of clock provided (autodetect feature). When enabled, the device will consume 6mW more power from the AVDD18 supply rail, but it will also accept differential or single ended inputs of smaller swing.

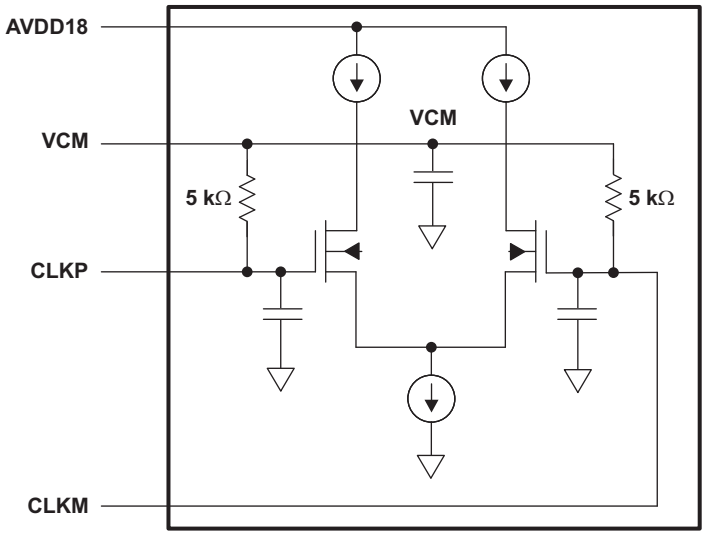



**Figure 39. Internal Clock Buffer for Differential Clock Mode**

If the preferred clocking scheme for the device is single-ended, CLKINM pin should be connected to ground, i.e., shorted directly to AVSS (see Figure 41). In this case, the autodetect feature will shut down the internal clock buffer and the device will go into single-ended clock input automatically. The user should connect the single-ended clock source directly (no decoupling) to CLKINP pin, which would be the only device clock input. In that case, it is recommended the use of low jitter square signals (LVCMOS levels, 1.8V amplitude) to drive the ADC (see SLYT075 for further details on the theory).

For single ended sinusoidal clocks or for differential clocks (differential sinewave, LVPECL, LVDS…), the clock amplifier should be enabled. For that, the connection scheme of Figure 40 should be used. The common-mode voltage of the clock source should match one of the clock inputs of the AFE5801 (VCM) which is set internally using 5kΩ resistors, as shown in Figure 39. The easiest way to ensure this is to AC couple the inputs as shown in Figure 40. The same scheme applies to the case where the clock is single ended but its amplitude is small or its edges are not sharp (for instance, with a sinusoidal single-ended clock). In this case, the input clock signal can be connected with a capacitor to CLKINP (as in Figure 40) and the CLKINM should be connected to ground also through a capacitor, i.e., AC coupled to AVSS.

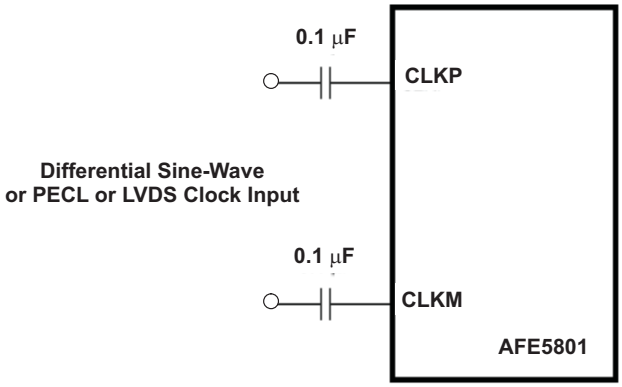



**Figure 40. Differential Clock Driving Circuit**

If a transformer is used with the secondary floating (for instance, to pass from single-ended to differential) , it can then obviously be connected directly to the clock inputs, without the need of the 100nF series capacitors.

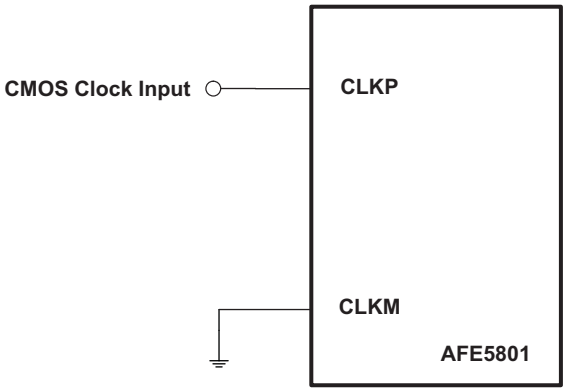



**Figure 41. Single-Ended Clock Driving Circuit**

Finally, on the differential clock configurations, Figure 42 shows the use of the CDCM7005 to generate the AFE5801 clock signals.

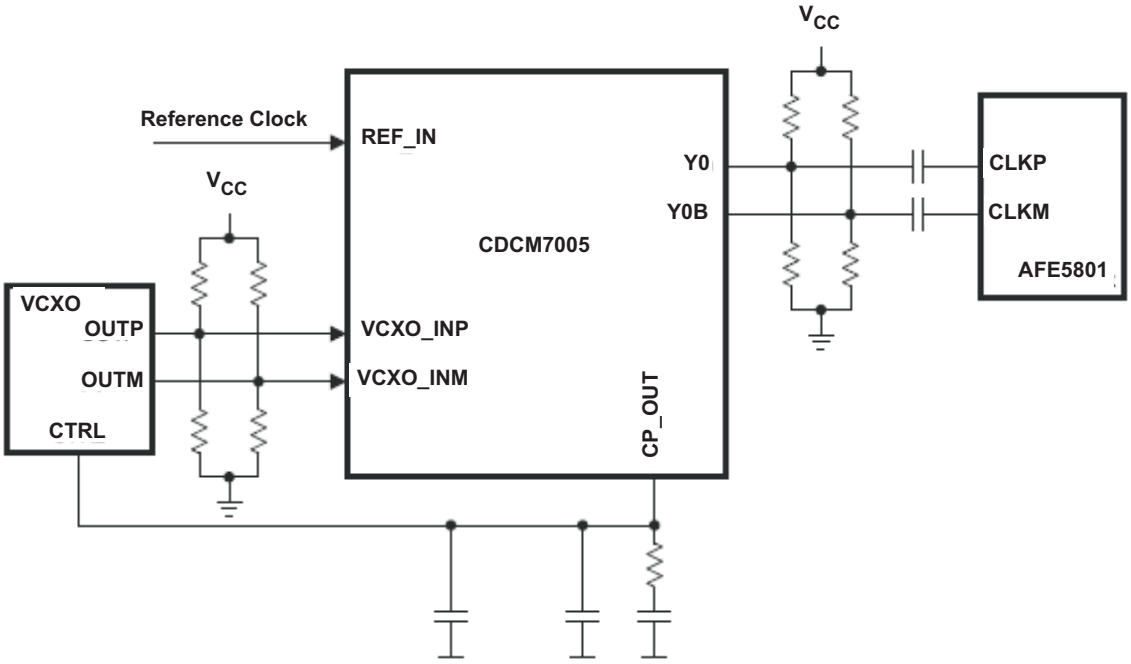



**Figure 42. PECL Clock Drive Using CDCM7005**

## DIGITAL OUTPUTS

The conversion results from all eight ADCs are serialized and output using one LVDS data pair per ADC, at 12 times the device input clock rate. Besides that, two more LVDS pairs are used to facilitate the interface to the circuit reading the ADC output. For one side, a reference frame LVDS signal running at the input clock rate indicates the beginning and end of the sample word. On top of that, the device outputs a reference clock running at 6 times the input clock rate, with rise and fall times aligned with the individual bits. See the Output Interface Timing section for a description of the timing diagram as well as details on the timing margins.

Figure 43 represents the device LVDS output circuit. Observe that for an LVDS output high (OUTP = 1.375V, OUTM = 1.025V) the high switches would be closed and the low switches would be open. For LVDS output low (OUTP = 1.025V, OUTM = 1.375V) the low switches would be closed and the high left open. As the high and low switches have a nominal $R_{ON}$ of 50Ω ±10%, notice that the output impedance will be nominally 100Ω in any of those two configurations (high or low switches closed).

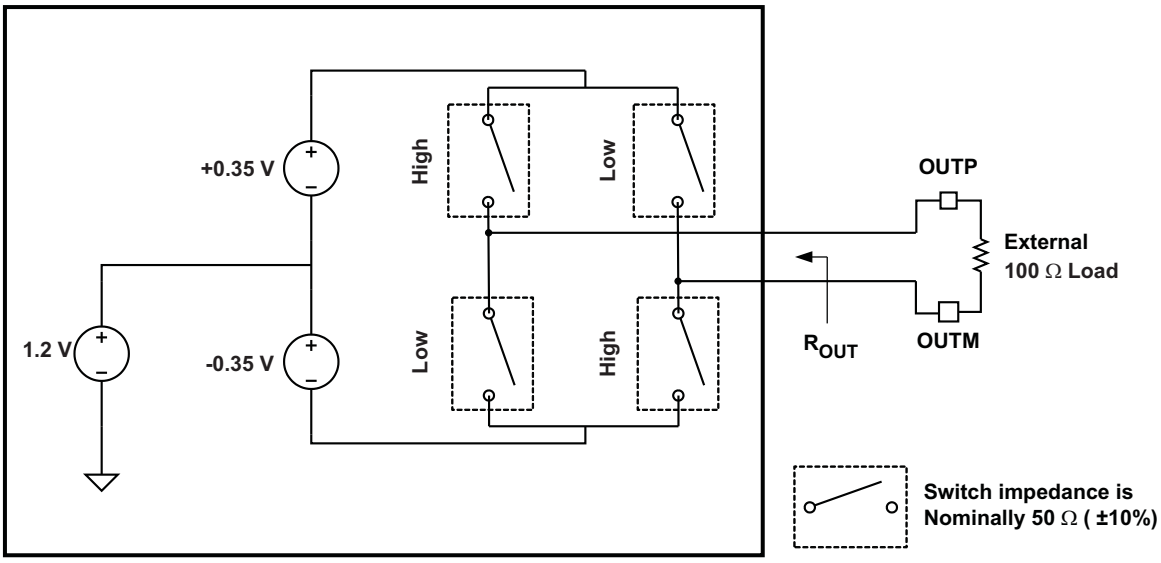



**Figure 43. LVDS Output Circuit**

## EXTERNAL/INTERNAL REFERENCE

See EXTERNAL_REFERENCE register description in the General Purpose Register Description Section.

## POWER SUPPLIES

The use of low noise power supplies with adequate decoupling is recommended, being the linear supplies the first choice vs switched ones, which tend to generate more noise components that can be coupled to the AFE5801.

There is no need of any type of power-up sequencing, although a positive pulse must be applied to the Reset pin once the power supplies are considered stable (see Serial Interface Section)

There are several types of powerdown modes. On the standby mode all circuits but the reference generator are powered-down. This enables for a fast recovery from power down to full operation. On the full power down mode, all the blocks are powered down (except some digital circuits). The power savings are bigger but the power-up will also be slower (see specification tables for more details). The device includes also the possibility of powering down pairs of channels (corresponding to the same ADC) through the use of PDN_Channel<7:0> and powering down the LVDS outputs by using PDN_LVDS.

Finally, notice that the metallic heat sink under the package is also connected to analog ground.

## LAYOUT INFORMATION

The evaluation board represents a good guideline of how to layout the board to obtain the maximum performance out of the AFE5801. General design rules as the use of multilayer boards, single ground plane for both, analog and digital ADC ground connections, and local decoupling ceramic chip capacitors should be applied. The input traces should be isolated from any external source of interference or noise, including the digital outputs as well as the clock traces. Clock should also be isolated from other signals although the low frequencies of the input signal relaxes the jitter requirements.

In order to maintain proper LVDS timing, all LVDS traces should follow a controlled impedance design (for example, 100Ω differential). In addition, all LVDS trace lengths should be equal and symmetrical. It is recommended to keep trace length variations less than 150mil (0.150in or 3.81mm).

It is necessary to solder the exposed pad at the bottom of the package to a ground plane for best thermal performance. For detailed information, see application notes QFN Layout Guidelines (SLOA122A) and QFN/SON PCB Attachment (SLUA271A).

## DEFINITION OF SPECIFICATIONS

**Analog Bandwidth –** The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

**Aperture Delay –**The delay in time between the rising or the falling edge of the input sampling clock (depending on the channel) and the actual time at which the sampling occurs. This delay will be different across channels. The maximum variation is specified as aperture delay variation (channel-channel).

**Aperture Uncertainty (Jitter) –** The sample-to-sample variation in aperture delay.

**Clock Pulse Width/Duty Cycle –** The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

**Maximum Conversion Rate –** The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

**Minimum Conversion Rate –** The minimum sampling rate at which the ADC functions.

**Differential Nonlinearity (DNL) –** An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

**Integral Nonlinearity (INL) –** The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

**Gain Error –** The difference between the actual gain of a channel & its ideal (theoretical) gain, i.e., the error in the absolute gain of the channel.

**Gain Matching –** The gain difference between two channels with same theoretical gain setting. For perfect matching, the difference should be zero. On the context of this device, the gain matching is obtained in two different ways:

1. The values on the specification table represent the expected gain matching between any two channels on the system. The gain is measured on every channel of every device, for a given gain setting, at any temperature. The difference between the maximum recorded gain and the minimum recorded gain represents the gain matching at that given gain setting. The same is done for every gain setting and the maximum difference for any gain setting is presented on the table.
2. The gain matching histogram represents the channel to channel matching inside the same device, i.e., the maximum expected gain difference between any two channels of the same device, or in other words, the peak-to-peak variation of absolute gains across all channels in the device. At a given gain setting for all the channels of a given device (at one temperature assumed common to the whole device), the difference between the channel with maximum gain and the channel with minimum gain represents one count. The same thing is done for all the devices and for 3 temperatures (–40C, 25C and 85C). Every measurement of a device at one given temperature represents one count.

**Offset Error –** The offset error is the difference, given in mV, between the ADC's actual average idle-channel output code and the ideal average idle-channel output code.

**Temperature Drift –** The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from $T_{MIN}$ to $T_{MAX}$. It is calculated by dividing the maximum deviation of the parameter across the $T_{MIN}$ to $T_{MAX}$ range by the difference $T_{MAX} – T_{MIN}$.

**Signal-to-Noise Ratio –** SNR is the ratio of the power of the fundamental (PS) to the noise floor power (PN), excluding the power at DC and the first nine harmonics.

$$SNR = 10Log10\frac{P_S}{P_N} \quad (1)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the full-scale converter range.

**Signal-to-Noise and Distortion (SINAD) –** SINAD is the ratio of the power of the fundamental ($P_S$) to the power of all the other spectral components including noise ($P_N$) and distortion ($P_D$), but excluding dc.

$$SINAD = 10 \log 10 \frac{P_S}{P_N + P_D} \quad (2)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the full-scale converter range.

**Effective Number of Bits (ENOB) –** The ENOB is a measure the performance of a converter as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (3)$$

**Spurious-Free Dynamic Range (SFDR) –** SFDR is the ratio of the power of the fundamental (PS) to the highest FFT bin, harmonic or not, excluding DC. SFDR is typically given in units of dBc (dB to carrier).

**Second Harmonic Distortion (HD2) –** HD2 is the ratio of the power of the fundamental (PS) to the second harmonic, typically given in units of dBc (dB to carrier).

**Third Harmonic Distortion (HD3) –**HD3 is the ratio of the power of the fundamental (PS) to the third harmonic, typically given in units of dBc (dB to carrier).

**Total Harmonic Distortion (THD) –** THD is the ratio of the power of the fundamental ($P_S$) to the power of the first nine harmonics (PD).

$$THD = 10 \log 10 \frac{P_S}{P_D} \quad (4)$$

THD is typically given in units of dBc (dB to carrier).

**AC Power Supply Rejection Ratio (AC PSRR) –** A measure of the device immunity to variations in its supply voltage. In this datasheet, if ΔVSUP represents the change in supply voltage and ΔVOUT is the resultant change of the ADC output code (referred to the input), then:

$$PSRR = 20 \log \left( \frac{\Delta Vout}{\Delta Vsup} \right) \quad (5)$$

# REVISION HISTORY

**Changes from Revision C (January 2010) to Revision D** **Page**

- Deleted INVERT_CHANNEL and MSB_FIRST rows from register map table ..... 21
- Deleted INVERT_CHANNEL register description ..... 23
- Deleted MSB_FIRSTL register description ..... 23

**Changes from Revision B (April 2009) to Revision C** **Page**

- Added pullup/pulldown resistors to descriptions of PDN, RESET, SCLK, SDATA, $\overline{SEN}$, and SYNC terminals ..... 3
- Added a note to the TERMINAL FUNCTIONS table, referenced from pin 28 within the table ..... 3
- Listed names of digital control pins and changed maximum voltage rating for them ..... 4
- Added a minimum value for LVDS ac-coupled clock input in RECOMMENDED OPERATING CONDITIONS ..... 5
- Added rows for $V_{IH}$ and $V_{IL}$ to CLOCK INPUT section of RECOMMENDED OPERATING CONDITIONS table ..... 5
- Added note to ELECTRICAL CHARACTERISTICS table regarding the effects of enabling clamping ..... 5
- Added note to ELECTRICAL CHARACTERISTICS table regarding the effects of enabling clamping ..... 6
- Added note to ELECTRICAL CHARACTERISTICS table for $I_{DVDD18}$ row in POWER section ..... 6
- Listed names of digital-input and digital-output pins in *Digital Characteristics* table ..... 7
- Added section for SDOUT to *Digital Characteristics* table ..... 7
- Added a reference to *Recommended Operating Conditions* table to the note following the *Digital Characteristics* table ..... 7
- Added note for FCLK timing to *Output Interface Timing* table ..... 8
- Modified next-to-last paragraph in *Theory of Operation* section ..... 17
- Added a new paragraph to the end of the *Input Configuration* section ..... 18
- Added two new paragraphs to the end of the *Register Initialization* section ..... 18
- Added a sentence to the last paragraph of the *Reset Timing* section ..... 19
- Changed "Serial Interface Register Write" from a section heading to a figure caption ..... 20
- Added a parenthetical expression to a sentence in the *General-Purpose Register Map* section ..... 20
- Deleted text from ADDRESS 3[8] DESCRIPTION ..... 21
- Changed DESCRIPTION for ADDRESS 7[8:7] in register map. ..... 21
- Added two sentences to EXTERNAL_REFERENCE register description ..... 22
- Changed address of LOW_FREQUENCY_NOISE_SUPPRESSION to 1[11] ..... 23
- Added reference to INTERP_ENABLE section ..... 25
- Added a NOTE explaining readback from address 0x97 ..... 28
- Arranged TGC control register-description sections in alphabetical order by register name ..... 29
- Changed "16 channels" to "eight channels" in the *ANTI-ALIAS FILTER (AAF)* section ..... 33
- Changed "16 channels" to "eight channels" in the *CLOCK INPUTS* section ..... 33
- Changed "clock channels" to "clock lines" in the *Clock Inputs* section ..... 33
- Deleted two sentences from first paragraph of *CLOCK INPUTS* section ..... 33

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| AFE5801IRGCR | ACTIVE | VQFN | RGC | 64 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | AFE5801 | Samples |
| AFE5801IRGCT | ACTIVE | VQFN | RGC | 64 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | AFE5801 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

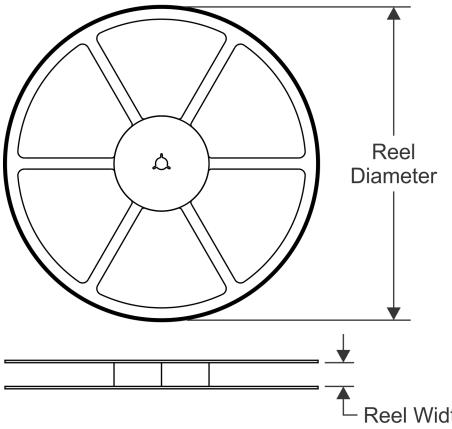
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

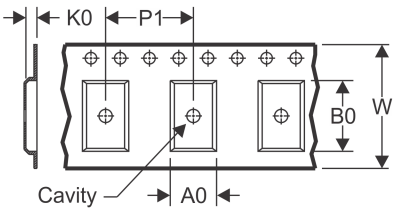
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

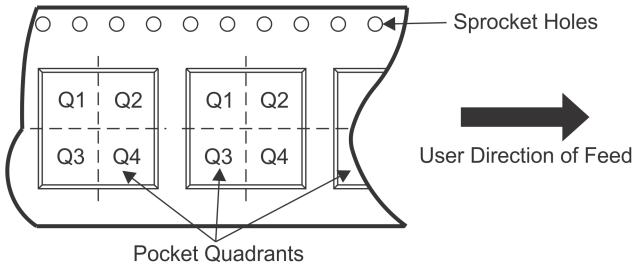



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

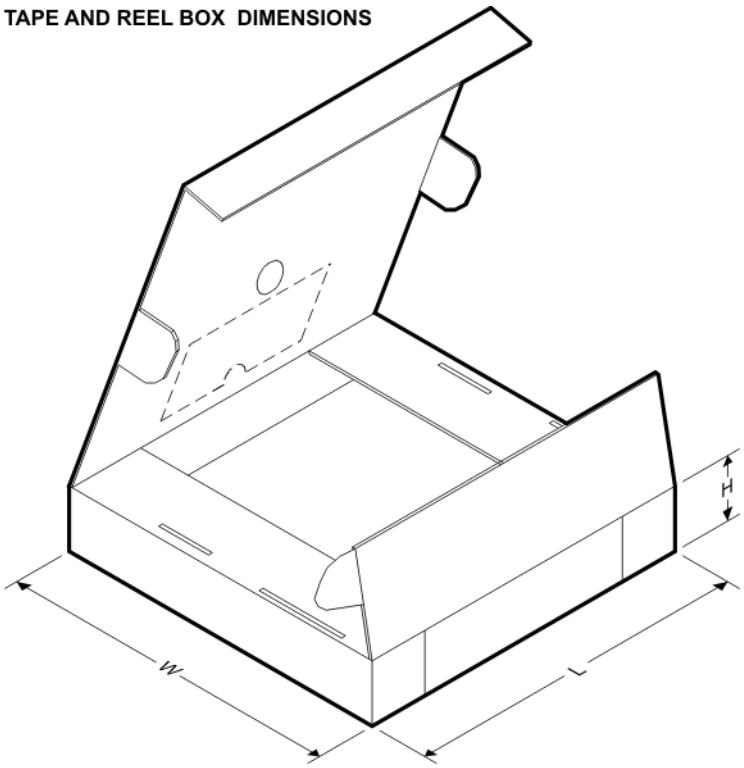
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AFE5801IRGCR | VQFN | RGC | 64 | 2000 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| AFE5801IRGCT | VQFN | RGC | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| AFE5801IRGCR | VQFN | RGC | 64 | 2000 | 350.0 | 350.0 | 43.0 |
| AFE5801IRGCT | VQFN | RGC | 64 | 250 | 213.0 | 191.0 | 55.0 |

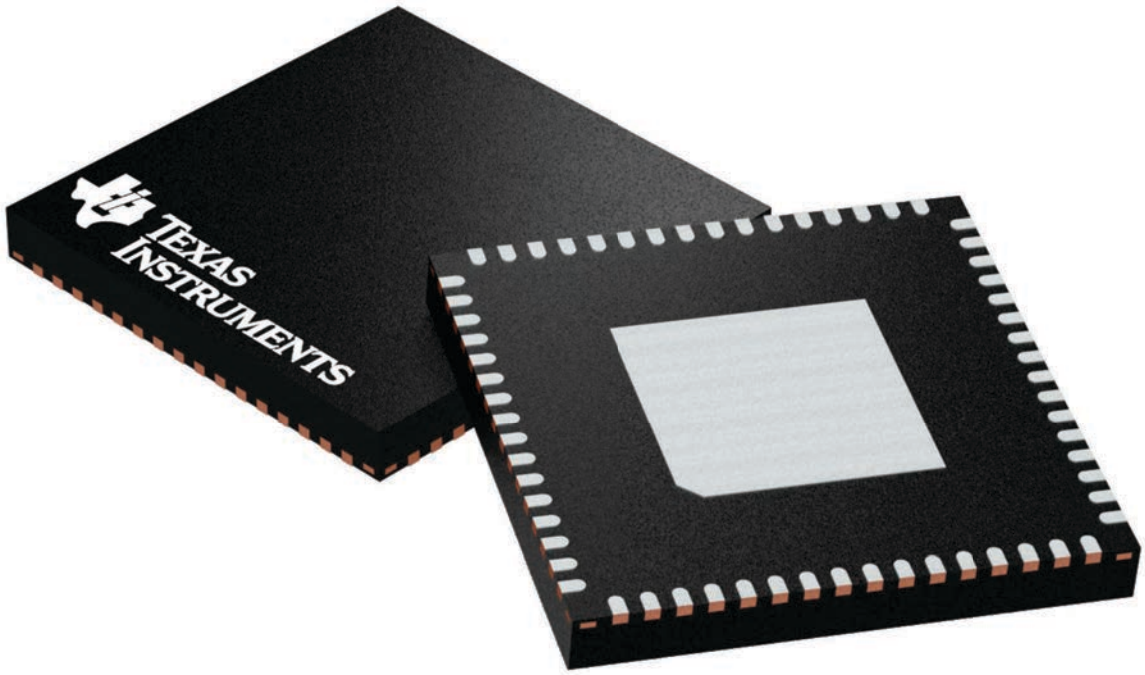
# GENERIC PACKAGE VIEW

## RGC 64

## VQFN - 1 mm max height

**9 x 9, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

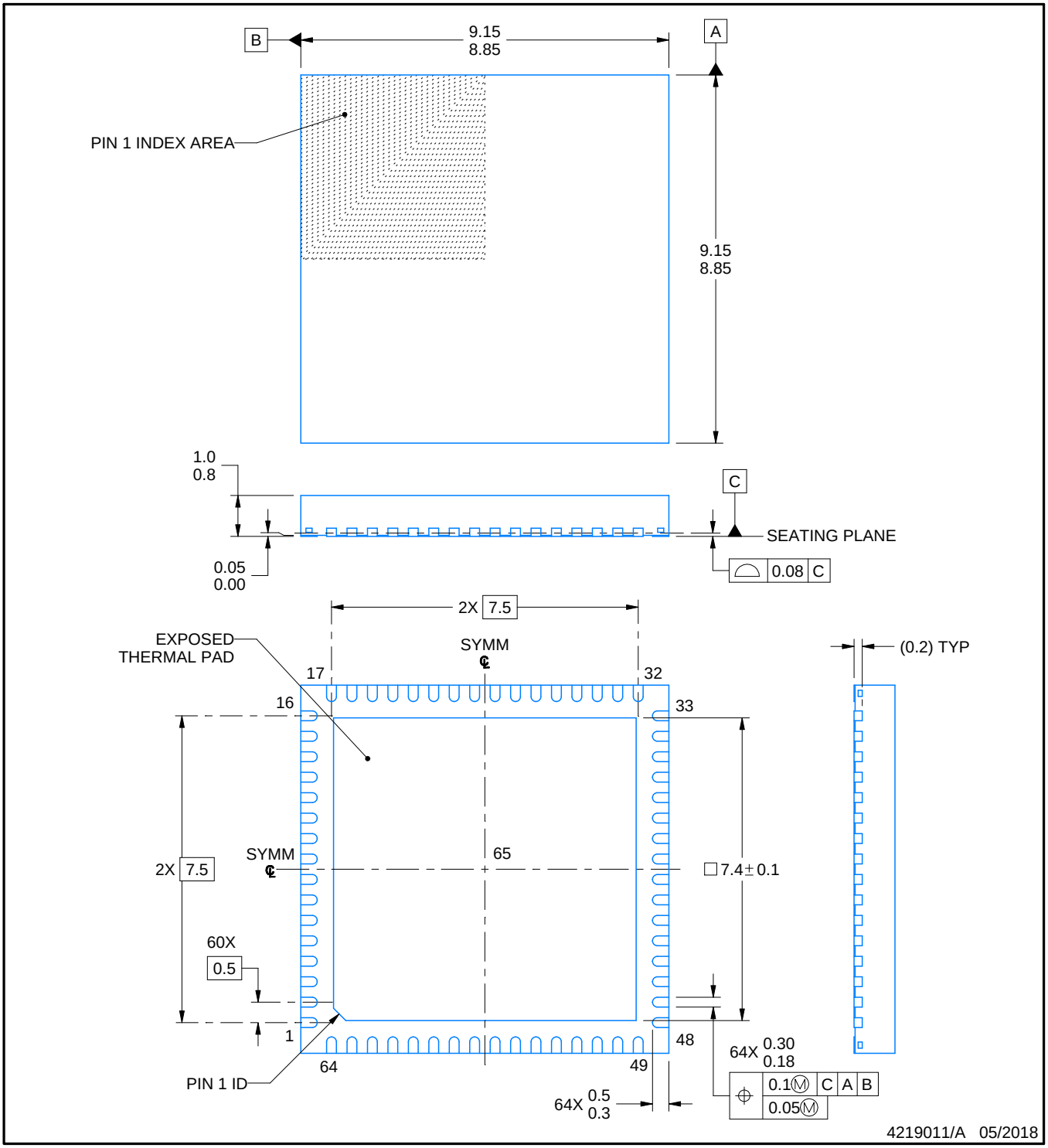
4224597/A

# RGC0064H

# PACKAGE OUTLINE

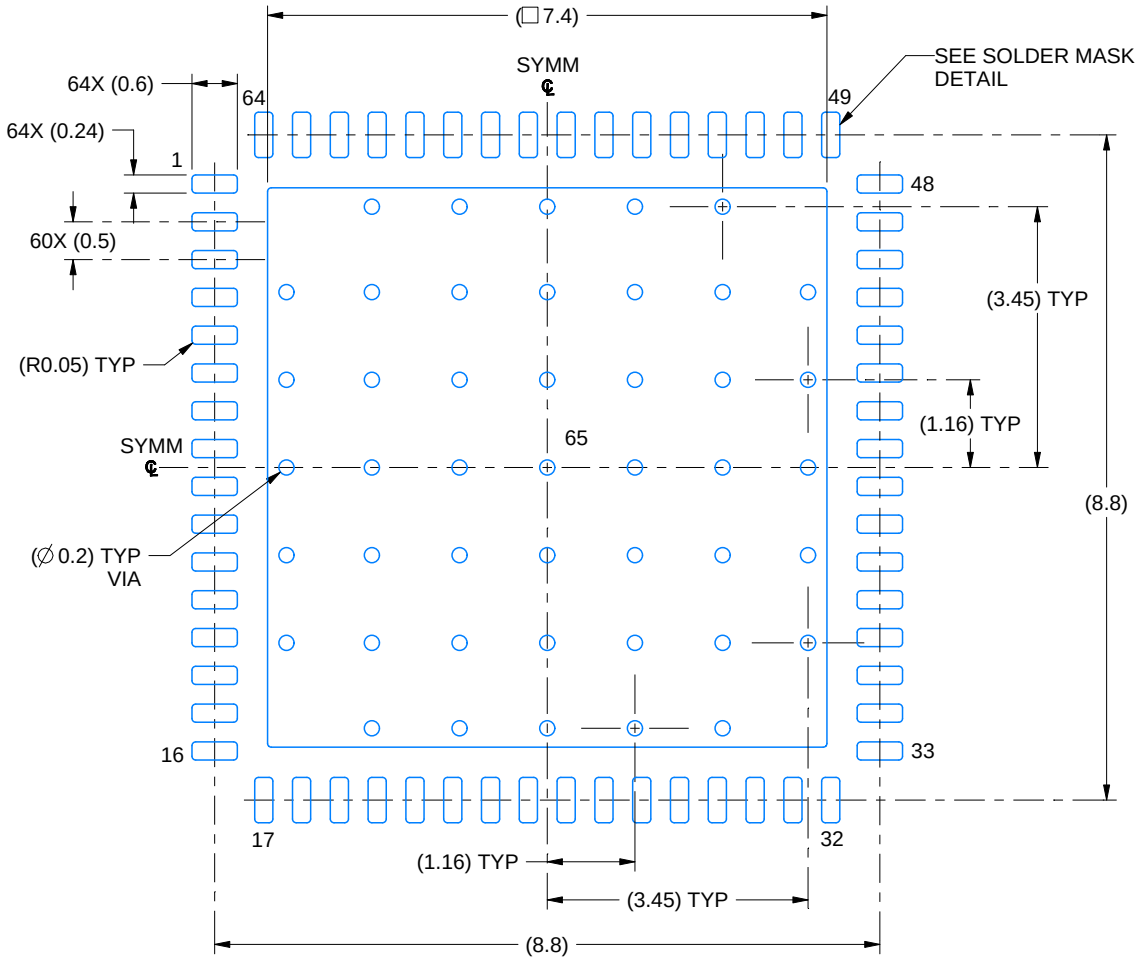
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

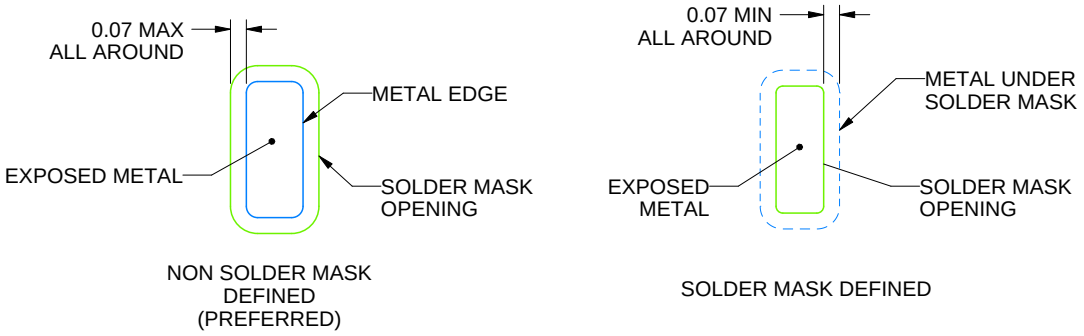



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




SOLDER MASK DETAILS

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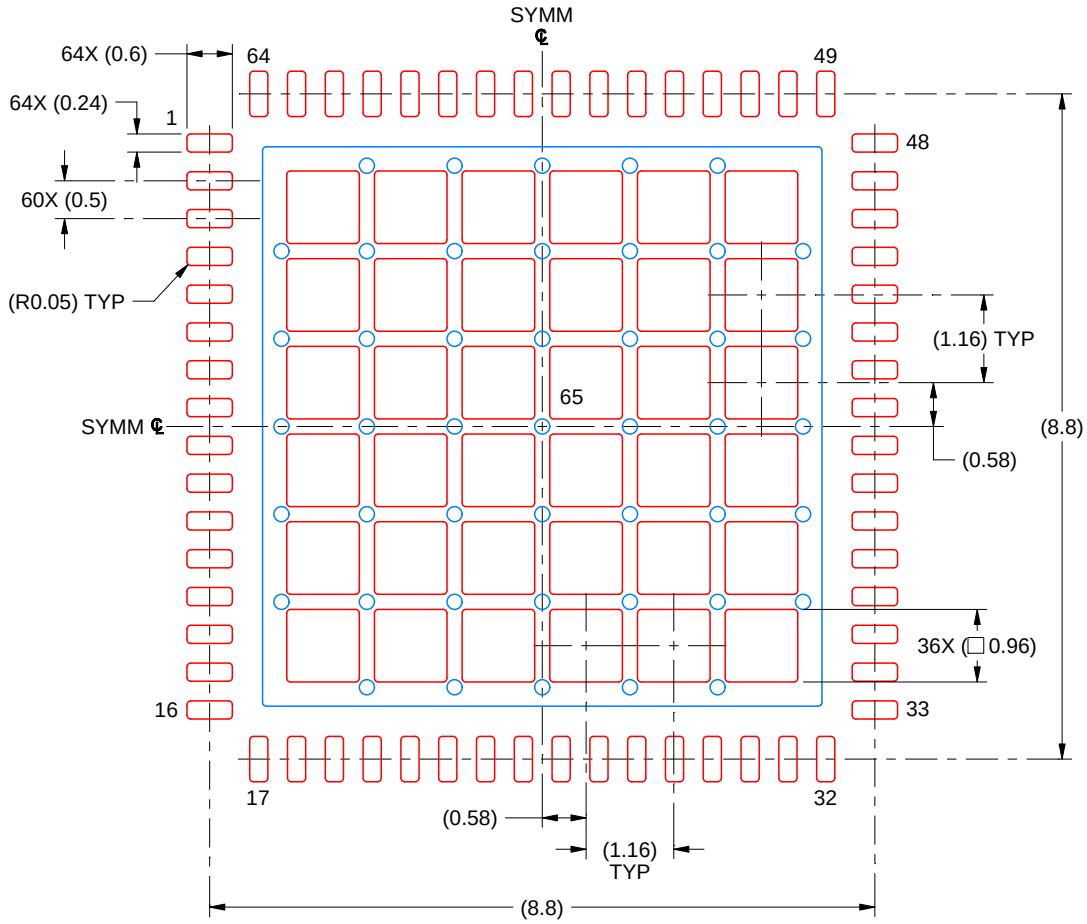
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
61% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265