HOLT INTEGRATED CIRCUITS INC.

HI-3000H, HI-3001H

1Mbps Avionics CAN Transceiver with High Operating Temperature

March 2020

GENERAL DESCRIPTION

The HI-3000H is a 1 Mbps Controller Area Network (CAN) transceiver optimized for use in high temperature avionics applications. The device is capable of operating at extended temperature ranges of -55°C to 175°C for plastic packages and -55°C to 200°C for the ceramic CERDIP-8 package. It interfaces between a CAN protocol controller and the physical wires of the bus in a CAN network. Differential output amplitude and current drive capability are specifically enhanced to meet the needs of long cable runs typical of avionics applications.

The HI-3000H supports two modes of operation: Normal Mode and Standby Mode. The Standby Mode is a very low-current mode which continues to monitor bus activity and allows an external controller to manage wake-up.

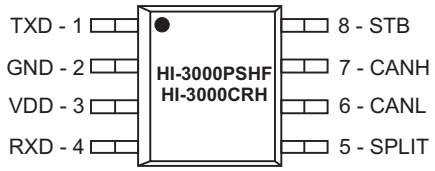
Superior common-mode receiver performance makes the device especially suitable for applications where ground reference voltages may vary from point to point over long distances along the CAN bus. In addition, the HI-3000H provides a SPLIT pin to give an output reference voltage of VDD/2 which can be used for stabilizing the recessive bus level when the split termination technique is used to terminate the bus.

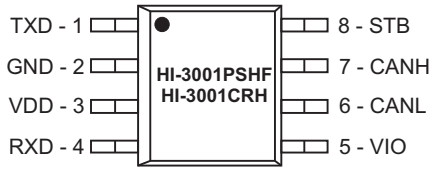
A TXD dominant time-out feature protects the bus from being driven into a permanent dominant state (so-called “babbling idiot”) if pin TXD becomes permanently low due to application failure.

The device also has short circuit protection to +/-58V on CANH, CANL and SPLIT pins and ESD protection to +/- 6kV on all pins.

The HI-3001H is identical to the HI-3000H except the SPLIT pin is substituted with a VIO supply voltage pin. This allows the HI-3001H to interface directly with controllers with 3.3V supply voltages.

PIN CONFIGURATIONS (Top Views)





8-Pin Plastic SOIC package (Narrow Body)
& 8-Pin Ceramic CERDIP

FEATURES

- Extended Temperature Ranges -55°C to 175°C (plastic SOIC-8 package) and -55°C to 200°C (ceramic CERDIP-8 package)
- Fully compliant with ARINC 825 and ISO 11898-5 standards.
- Signaling rates up to 1Mbit/s.
- Internal VDD/2 voltage source available to stabilize the recessive bus level if split termination is used (HI-3000H SPLIT pin).
- VIO input on HI-3001H allows for direct interfacing with 3.3V controllers.
- Detection of permanent dominant on TXD pin (babbling idiot protection).
- High impedance allows connection of up to 120 nodes.
- Input levels compatible with 3.3V or 5V controllers.
- CANH, CANL and SPLIT pins short-circuit proof to +/-58V.
- Will not disturb the bus if unpowered.

PIN DESCRIPTIONS

SIGNAL	FUNCTION	DESCRIPTION
TXD	INPUT	100kOhm internal pull-up. Transmit Data Input.
GND	POWER	Chip 0V supply
VDD	POWER	Positive supply, 5V +/-5%. Bypass with 0.1uF ceramic capacitor.
RXD	OUTPUT	Receive Data Output.
CANL	BUS I/O	CAN Bus Line Low.
CANH	BUS I/O	CAN Bus Line High.
STB	INPUT	100kOhm internal pull-up. Standby Mode selection input. Drive STB low or connect to GND for Normal operation. Drive STB high to select low-current Standby Mode.
SPLIT (HI-3000H)	INPUT	Supplies a VDD/2 output to provide recessive bus level stabilization when a split termination is used to terminate the bus.
VIO (HI-3001H)	INPUT	Connect to a 3.3V supply to allow compatibility of all digital I/O (RXD, TXD, STB) with a 3.3V controller input.

BLOCK DIAGRAM

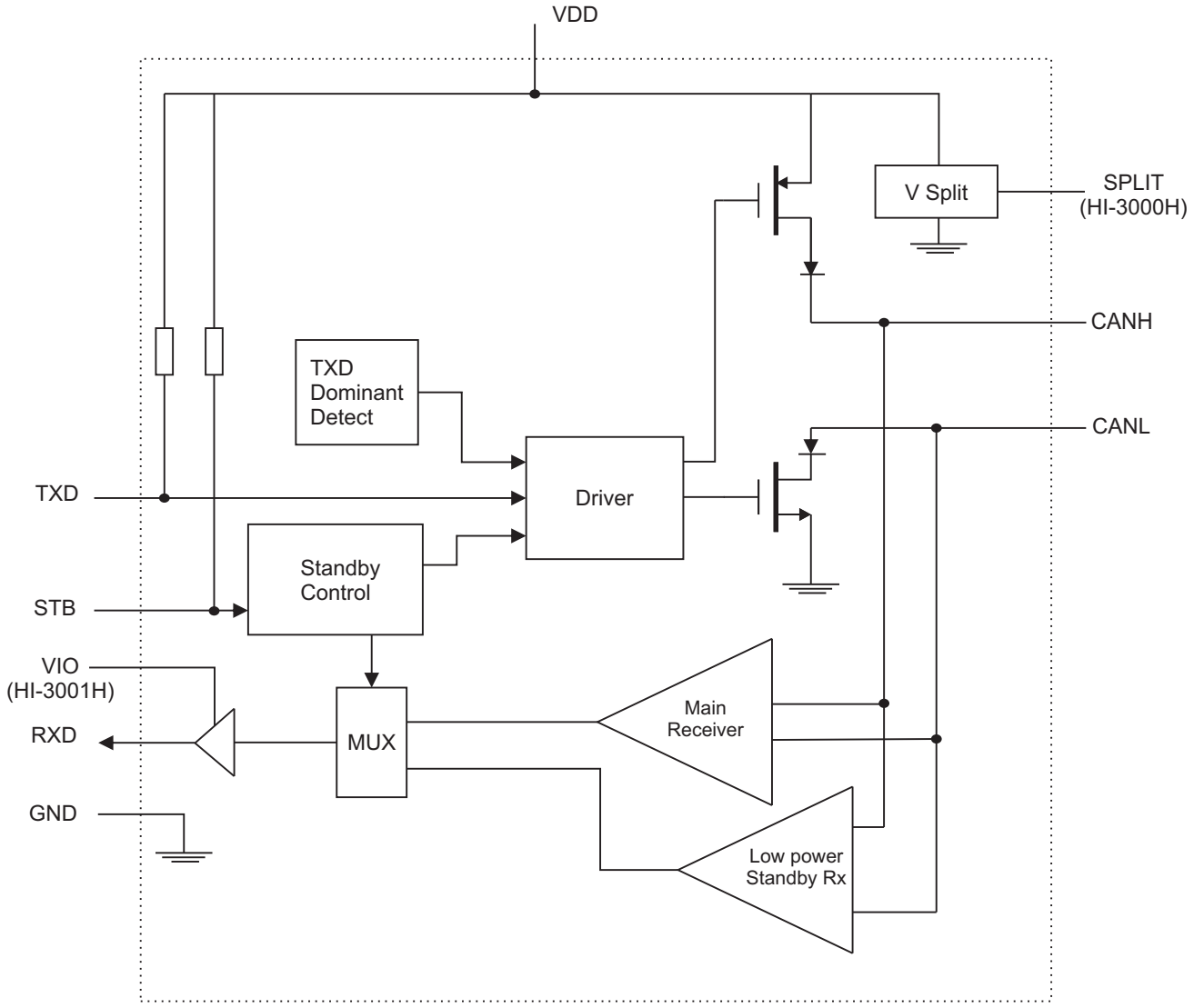


Figure 1. HI-3000H Functional Block Diagram

FUNCTIONAL DESCRIPTION

OPERATING MODES

The HI-3000H provides two modes of operation which are selectable via the STB pin. Table 1 summarizes the modes.

Table 1 - Operating Modes

MODE	STB pin
Normal	LOW
Standby	HIGH

Normal Mode

Normal mode is selected by setting the STB pin to a LOW logic level (GND). In this mode, the transceiver transmits and receives data in the usual way from the CANH and CANL bus lines. The differential receiver converts the analog bus data to digital data which is output on the RXD pin (Note: the RXD output on HI-3001H is compatible with 3.3V controllers if the VIO pin is connected to a 3.3V supply).

Standby Mode

Standby Mode is selected by setting the STB pin to a HIGH logic level. In this mode, the transmitter is switched off and a low power differential receiver monitors the bus lines for activity. A dominant signal of more than 3μs will be reflected on the RXD pin as a logic LOW, where it may be detected by the host as a wake-up request. The device will not leave standby mode until the host forces the STB pin to a logic low.

SPLIT Circuit

The SPLIT pin provides a stable VDD/2 DC voltage. This pin can be used to stabilize the recessive common mode voltage by connecting the SPLIT pin to the center tap of the split termination (see figure 7). In the case of a recessive bus voltage dropping below the ideal value of VDD/2 (e.g. due to an unpowered node with high leakage from the bus lines to ground), the split circuit will force the recessive voltage to VDD/2.

INTERNAL PROTECTION FEATURES

Short-circuit protection

Short-circuit protection is provided on the CANH, CANL and SPLIT pins. These pins are protected from ESD to over 6KV (HBM) and from shorts between -58V and +58V continuous, as specified in ISO 11898-5. The short circuit current is limited to less than 200mA typical.

TXD permanent dominant time-out

A timer circuit prevents the bus lines being driven into a permanent dominant state, which would result in a situation blocking all bus traffic. This could happen in the case of the TXD pin becoming permanently low due to a hardware or application failure. The timer is triggered by a negative edge on the TXD pin (start of dominant state). If the TXD pin is not set high (recessive state) after a typical time of 2ms, the transmitter outputs will be disabled, driving the bus lines into the recessive state. The timer is reset by a positive edge on the TXD pin. Note that the minimum TXD dominant time-out time, tdom = 300µs, defines the minimum possible bit rate of 40kbit/s (the CAN protocol specifies a maximum of 11 successive dominant bits − 5 successive dominant bits immediately followed by an error frame).

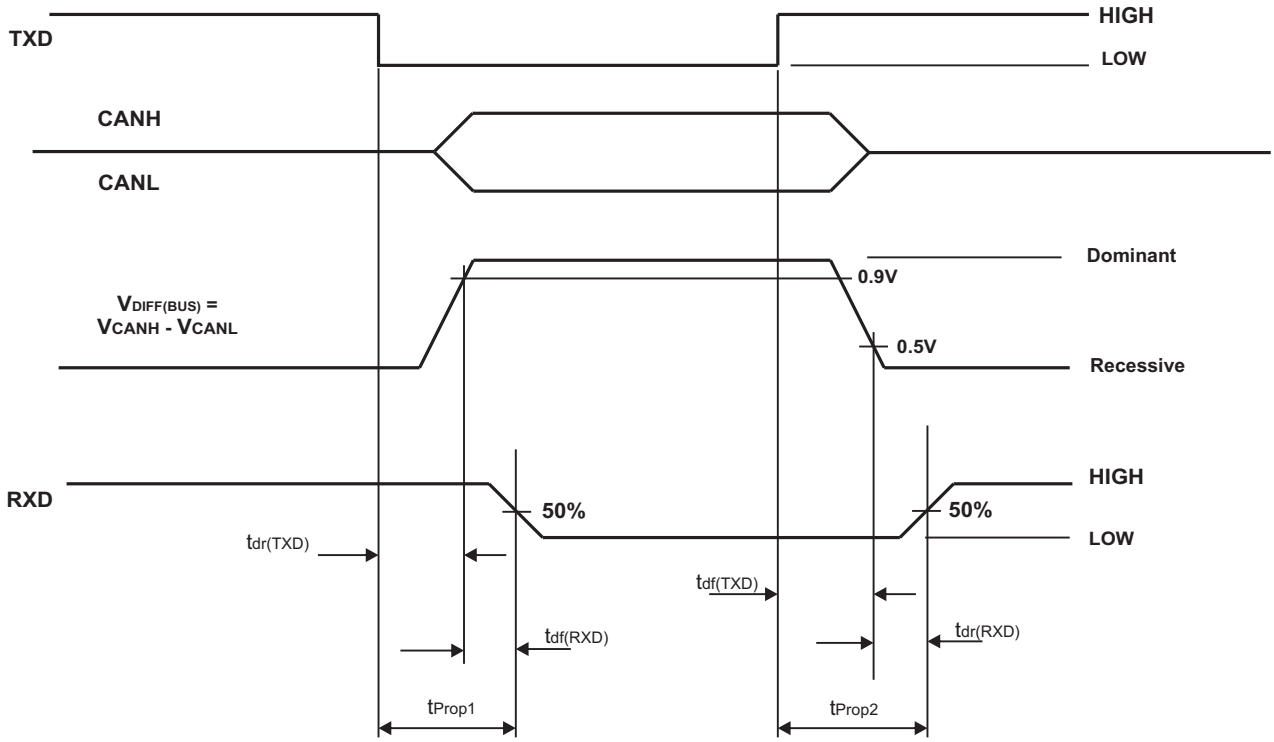
Fail-safe features

Pin TXD has a pull up in order to force a recessive level if pin TXD is left open.

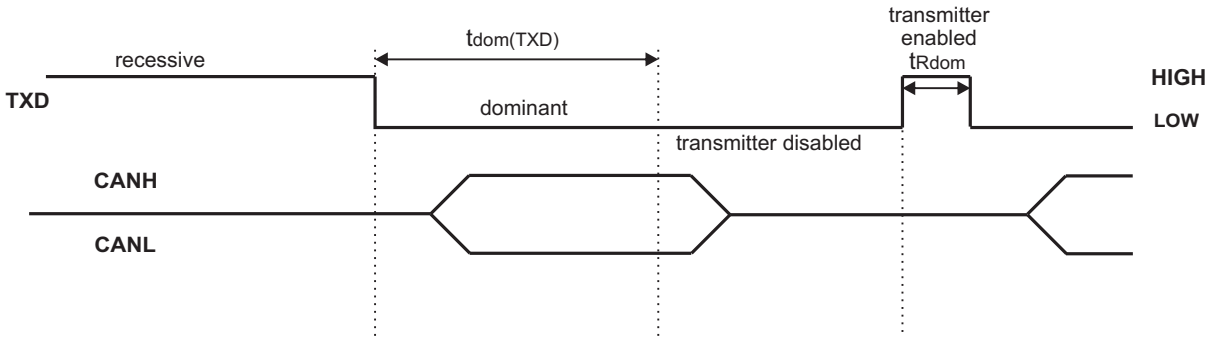
Pins TXD and STB will become floating if power is lost. This will prevent reverse currents via these pins.

TIMING DIAGRAMS

Timing Delays



TXD dominant time-out feature



ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND = 0V)

Supply Voltage, VDD, VIO : .....7V Current at Input pins .....-100mA to +100mA DC Voltages at TXD, RXD and STB .....-0.5V to V_{DD} +0.5V DC Voltages at CANH, CANL and SPLIT: .....-58V to +58V Internal Power Dissipation: .....900mW Electrostatic Discharge (ESD)[1], All pins .....+/- 6kV	Operating Temperature Range: (Plastic).....-55°C to +175°C (Ceramic).....-55°C to +200°C Storage Temperature Range: -65°C to +150°C Soldering Temperature: (Ceramic).....60 sec. at +300°C (Plastic - leads).....10 sec. at +280°C (Plastic - body).....+260°C Max.

NOTES:
1. Human Body Model (HBM).

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V±5%, Operating temperature range (unless otherwise noted). Positive currents flow into the IC.

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
SUPPLY CURRENT						
V_{DD} Supply Current	I_{DD}	Recessive: $V_{TXD} = V_{DD}$		6	10	mA
		Dominant: V_{TXD} = 0 V		50	70	mA
		Standby Mode: $V_{TXD} = V_{DD}$		15	50	µA
VIO Supply Current	I_{IO}				100	µA
DIGITAL INPUTS (Pins TXD, STB)						
HIGH-level input voltage (see Note 1)	V_{IH}		80%V_{DD}		V_{DD} + 0.5	V
LOW-level input voltage (TXD pin)	V_{IL}		− 0.5		20%V_{DD}	V
HIGH-level input current	I_{IH}	$V_{TXD} = V_{DD}$ or VIO	− 5	0	+ 5	µA
LOW-level input current	I_{IL}	V_{TXD} = 0 V		− 50	− 150	µA
DIGITAL OUTPUTS						
HIGH-level output voltage (RXD Pin) (see Note 1)	V_{OH}	I_{OH} = 1mA	90%V_{DD}			V
LOW-level output voltage (RXD Pin)	V_{OL}	I_{OL} = 1mA	0	0.1	10%V_{DD}	V
Output voltage (SPLIT Pin)	V_{SPLIT}	− 100 µA < I_{SPLIT} < 100 µA	0.45V_{DD}	0.5V_{DD}	0.55V_{DD}	V
Standby leakage current (SPLIT Pin)	I_{STB}		-5		+5	µA
DRIVER						
CANH dominant output voltage	$V_{O(CANH)}$	V_{TXD} = 0 V	3	3.6	4.25	V
CANL dominant output voltage	$V_{O(CANL)}$	V_{TXD} = 0 V (See Fig. 2)	0.5	1.4	1.75	V
Recessive output voltage	$V_{CANH(r)}$, $V_{CANL(r)}$	$V_{TXD} = V_{DD}$, R_L = 0 (See Fig. 2)	2	0.5V_{DD}	3	V
Bus output voltage in standby	V_{STB}	$V_{TXD} = V_{DD}$, R_L = 0 (See Fig. 2)	-0.1		0.1	V
Dominant differential output voltage	$V_{DIFF(d)(o)}$	V_{TXD} = 0 V, 45 Ω < R_L < 65 Ω	1.5	1.8	3	V
Recessive differential output voltage	$V_{DIFF(r)(o)}$	$V_{TXD} = V_{DD}$, no load (See Fig. 2)	− 50	0	50	mV
Matching of dominant output voltage, $V_{DD} - V_{O(CANH)} - V_{O(CANL)}$	V_{OM}	(See Fig. 4)	− 100	-40	150	mV
Steady state common mode output voltage	$V_{OC(ss)}$	V_{STB} = 0V, R_L = 60 Ω (See Fig. 5)	2	0.5V_{DD}	3	V

NOTE:
1. When VIO is connected (HI-3001H), limits are referenced wrt VIO rather than V_{DD}.

DC ELECTRICAL CHARACTERISTICS (cont.)

V_{DD} = 5V±5%, Operating temperature range. Positive currents flow into the IC.

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Short-circuit steady-state output current	$I_{OS(ss)}$	V_{CANH} = +58V, V_{CANL} open	-20		20	mA
		V_{CANH} = -58V, V_{CANL} openV	-200		100	mA
		V_{CANL} = +58V, V_{CANH} open	100		200	mA
		V_{CANL} = -58V, V_{CANH} open (See Fig. 6)	-20		20	mA
RECEIVER						
Differential receiver threshold voltage	$V_{Th(Rx)(diff)}$	− 12 V < V_{CANH}, V_{CANL} < + 12 V	500	700	900	mV
Differential hysteresis voltage	$V_{Hys(Rx)(diff)}$	− 12 V < V_{CANH}, V_{CANL} < + 12 V	50	120	200	mV
Differential hysteresis voltage in Standby mode	$V_{Hys(Stb)(diff)}$	− 12 V < V_{CANH}, V_{CANL} < + 12 V	500		1150	mV
Input leakage current, unpowered node	I_{CANH}, I_{CANL}	V_{DD} = V_{IO} 0 V, V_{CANH} = V_{CANL} = 5V	− 200		+ 200	µA
Differential input resistance	$R_{IN(DIFF)}$	V_{TXD} = V_{DD}, − 12 V < V_{CANH}, V_{CANL} < + 12 V	25	50	100	kΩ
Common mode input resistance	$R_{IN(CM)}$	V_{TXD} = V_{DD}, − 12 V < V_{CANH}, V_{CANL} < + 12 V	15	30	45	kΩ
Deviation between common mode input resistance between CANH and CANL	$R_{IN(CM)(m)}$	V_{CANH} = V_{CANL}	− 3		+ 3	%

AC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V±5%, Operating temperature range. Positive currents flow into the IC.

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Bit time	t_{Bit}		1		25	µs
Bit rate	f_{Bit}		40		1000	kHz
Common mode input capacitance[3]	$C_{IN(CM)}$	V_{TXD} = V_{DD}, 1Mbit/s data rate		20		pF
Differential input capacitance[3]	$C_{DIFF(CM)}$	V_{TXD} = V_{DD}, 1Mbit/s data rate		10		pF
Delay TXD to bus active	$t_{dr(TXD)}$	See Timing Diagrans		40	90	ns
Delay TXD to bus inactive	$t_{df(TXD)}$			40	90	ns
Delay bus active to RXD	$t_{df(RXD)}$			30	70	ns
Delay bus inactive to RXD	$t_{dr(RXD)}$			70	150	ns
Propagation delay TXD to RXD (recessive to dominant)	t_{Prop1}			70	160	ns
Propagation delay TXD to RXD (dominant to recessive)	t_{Prop2}			110	240	ns
TXD permanent dominant time-out	t_{dom}	V_{TXD} = 0 V	0.3	2	6	ms
TXD permanent dominant timer reset time	t_{Rdom}	Rising edge on TXD while in permanent dominant state			1	µs
Dominant time required on bus for wake up from standby	t_{wake}		0.5	3	5	µs

NOTES:
1. All currents into the device pins are positive; all currents out of the device pins are negative.
2. All typicals are given for V_{DD} = 5V, T_A = 25°C.
3. Guaranteed by design but not tested.

Application and Test Information

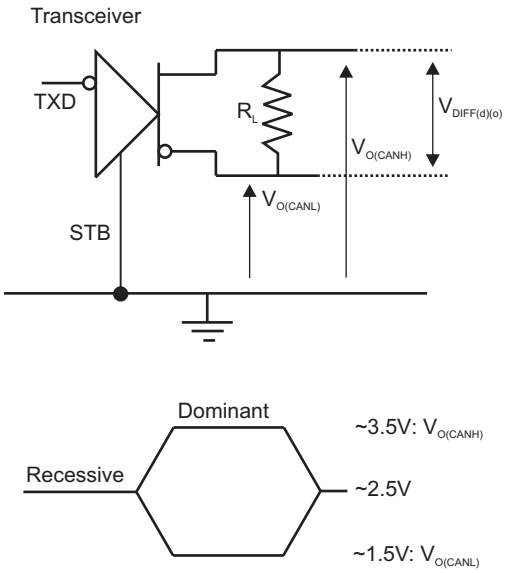


Figure 2. CAN Bus Driver Circuit

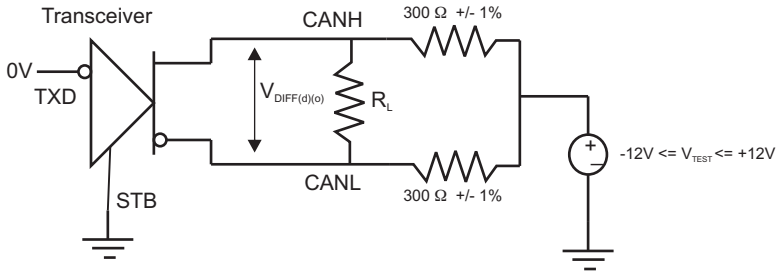


Figure 3. CAN Bus Driver (Dominant) Test Circuit

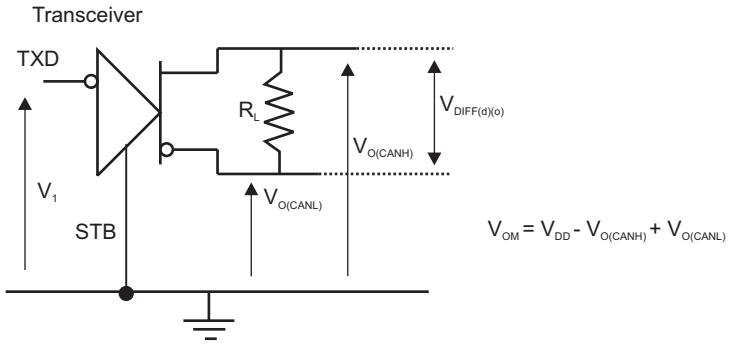


Figure 4. Driver Output Symmetry Test.

Application and Test Information

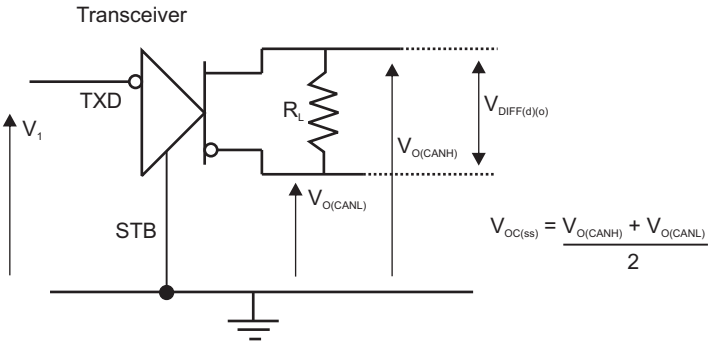


Figure 5. Common Mode Output Voltage Test.

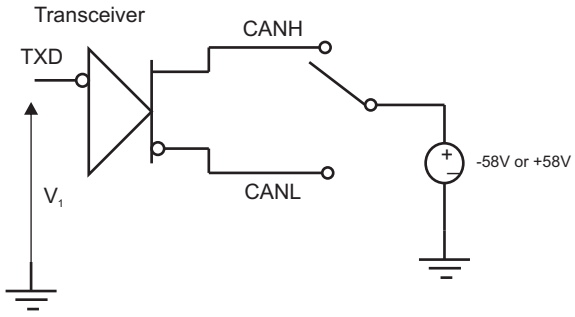


Figure 6. CAN Bus Driver Short-Circuit Test. (Note: V1 is a pulse from 0V to V_{DD} with duty cycle of 99% such that permanent dominant time-out is avoided).

Application and Test Information

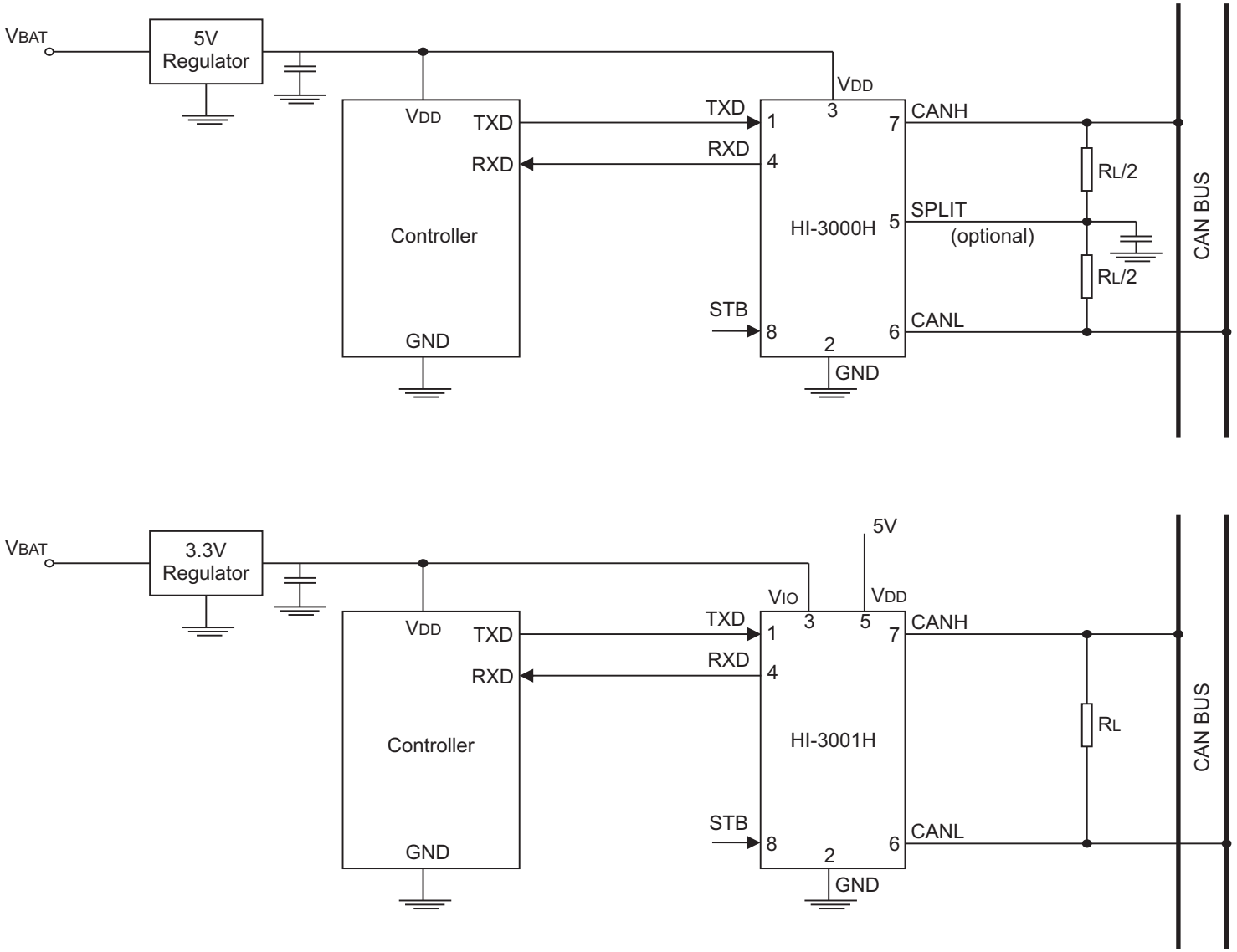


Figure 7. Typical Application Connections

ORDERING INFORMATION

HI - 300x PS H x

PART NUMBER	LEAD FINISH
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	PACKAGE DESCRIPTION
PS	8 PIN PLASTIC NARROW BODY SOIC (8HN): -55°C to +175°C.

PART NUMBER	DESCRIPTION
3000	SPLIT pin option
3001	VIO pin option

HI - 300x CR H

PART NUMBER	PACKAGE DESCRIPTION
CR	8 PIN CERDIP (8D) **not available Pb-free**: -55°C to +200°C.

PART NUMBER	DESCRIPTION
3000	SPLIT pin option
3001	VIO pin option

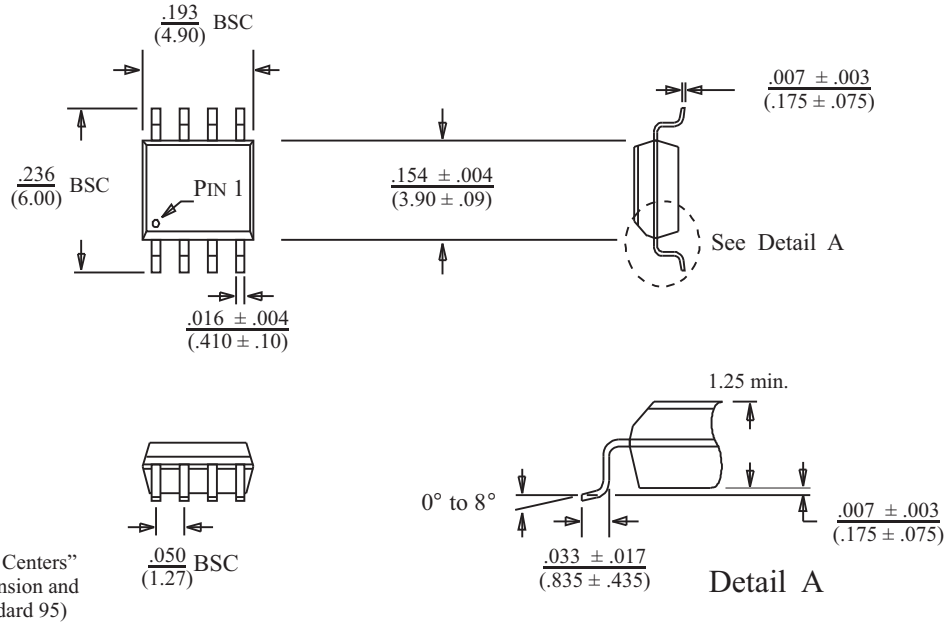
REVISION HISTORY

P/N	Rev	Date	Description of Change
DS3000H	New	12/05/12	Initial Release
	G	03/04/20	Change “Compatible with ARINC 825 and ISO 11898-5 standards” to “Fully compliant with ARINC 825 and ISO 11898-5 standards” in Features.

8-PIN PLASTIC SMALL OUTLINE (SOIC) - NB
(Narrow Body)

inches (millimeters)

Package Type: 8HN

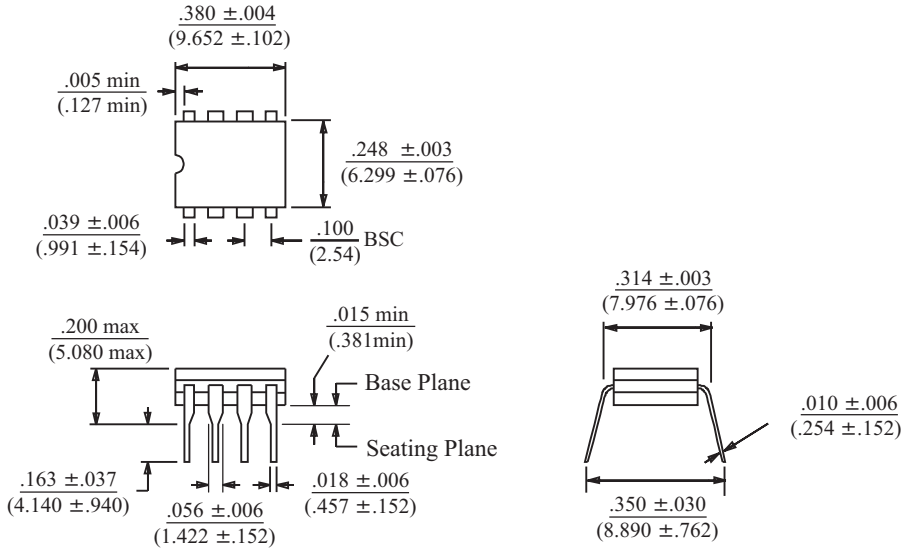


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

8-PIN CERDIP

inches (millimeters)

Package Type: 8D



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)