HMC1018LP4E

v01.1211

1.0 dB LSB GaAs MMIC 5-BIT DIGITAL ATTENUATOR, 0.1 - 30 GHz

Typical Applications

The HMC1018LP4E is ideal for:

- Fiber Optics & Broadband Telecom
- Microwave Radio & VSAT
- Military Radios, Radar & ECM
- Space Applications
- Sensors
- Test & Measurement Equipment

Features

1.0 dB LSB Steps to 31 dB

TTL/CMOS Compatible, Serial Control

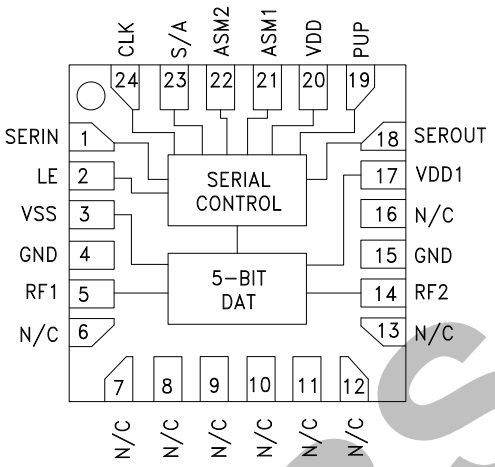
Unique Asynchronous Mode Control Allows Immediate Attenuation Level Setting

±1.0 dB Typical Bit Error

High Input IP3: +43 dBm

24 Lead 4x4mm SMT Package: 16mm2

Functional Diagram



General Description

The HMC1018LP4E is a broadband 5-bit GaAs IC digital attenuator in a low cost leadless surface mount package. Covering 0.1 to 30.0 GHz, the insertion loss is less than 5.5 dB typical. The attenuator bit values are 1.0 (LSB), 2, 4, 8, 16 for a total attenuation of 31 dB. Attenuation accuracy is excellent at ±0.4 dB typical step error with an IIP3 of +43 dBm. The control interface is CMOS/TTL compatible and accepts a three wire serial input. The HMC1018LP4E features a user selectable power up state and a serial-output port for cascading other Hittite serial controlled components.

Electrical Specifications, T_A = +25° C, With Vdd = Vdd1 = +5V, Vss = -5V

Parameter	Frequency (GHz)	Min.	Typ.	Max.	Units
Insertion Loss	0.1 - 18.0 GHz 18.0 - 26.5 GHz 26.5 - 30.0 GHz		4.5 5.5 7.0	6.0 7.0 8.0	dB dB dB
Attenuation Range	0.1 - 30.0 GHz		31		dB
Return Loss (RF1 & RF2, All Atten. States)	0.1 - 30.0 GHz		12		dB
Attenuation Accuracy: (Referenced to Insertion Loss) 1.0 - 15 dB States 16 - 31 dB States 16 - 31 dB States	 0.1 - 33.0 GHz 0.1 - 20.0 GHz 20.0 - 33.0 GHz	 ± (0.5 + 5%) of Atten. Setting Max ± (0.5 + 5%) of Atten. Setting Max ± (0.6 + 8%) of Atten. Setting Max			 dB dB dB
Input Power for 0.1 dB Compression	0.1 - 0.5 GHz 0.5 - 30.0 GHz		20 25		dBm dBm
Input Third Order Intercept Point (Two-Tone Input Power= 0 dBm Each Tone)	0.1 - 0.5 GHz 0.5 - 30.0 GHz		40 43		dBm dBm
Switching Characteristics tRISE, tFALL (10/90% RF) tON/tOFF (50% CTL to 10/90% RF)	0.1 - 30.0 GHz		 60 90		 ns ns
Idd1	0.1 - 30.0 GHz	2.5	4.5	6.5	mA
Iss	0.1 - 30.0 GHz	-7.0	-5.0	-3.0	mA

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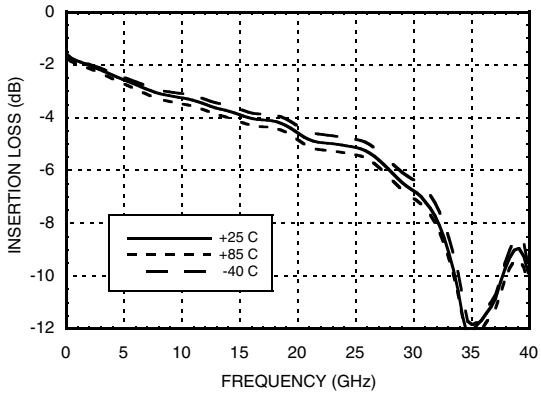
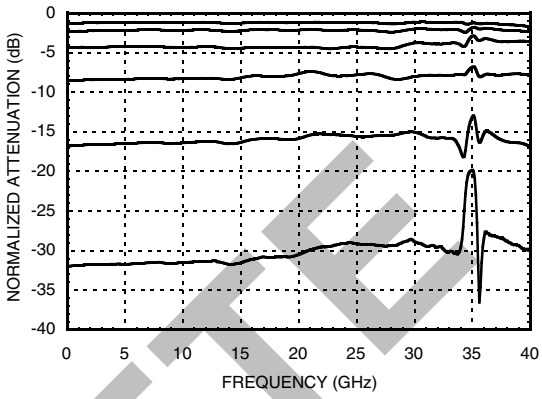
Insertion Loss vs. Temperature



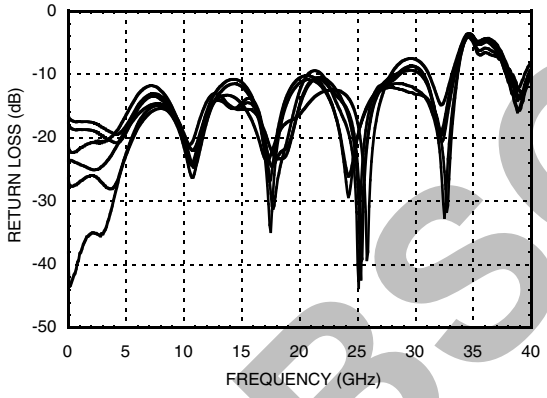
Normalized Attenuation

(Only Major States are Shown)



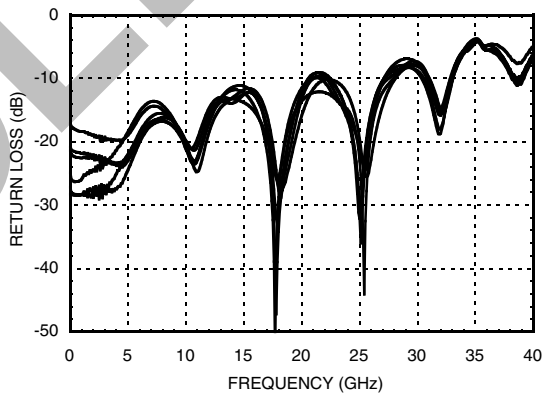
Input Return Loss

(Only Major States are Shown)

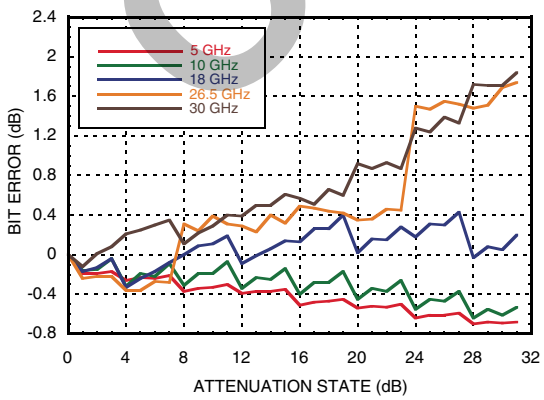


Output Return Loss

(Only Major States are Shown)

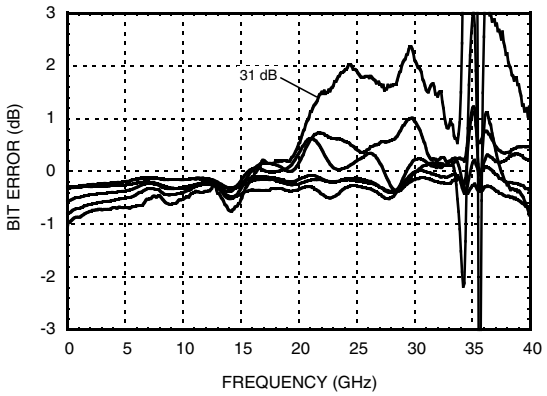


Bit Error vs. Attenuation State



Bit Error vs. Frequency

(Only Major States are Shown)



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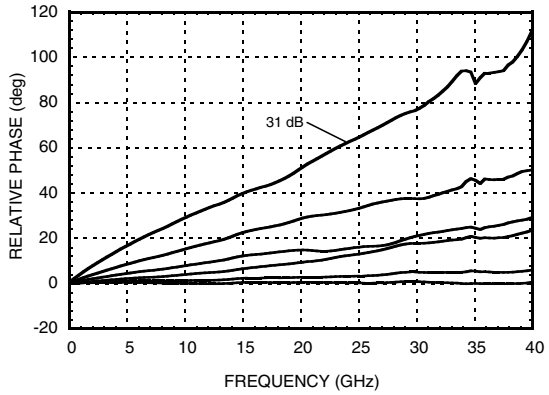
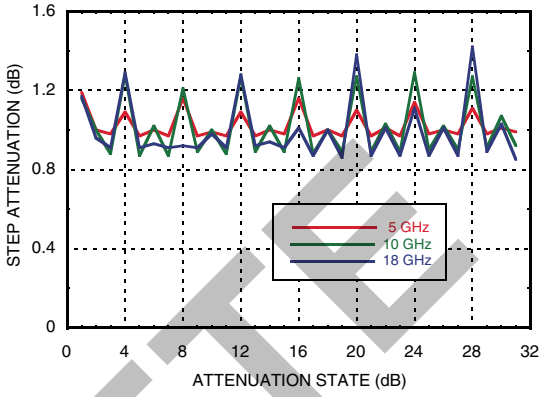
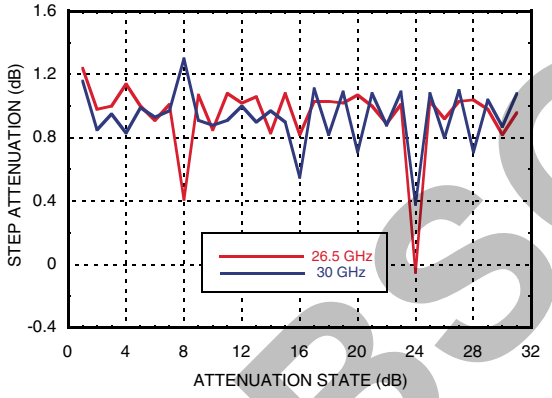
Relative Phase vs. Frequency
(Only Major States are Shown)



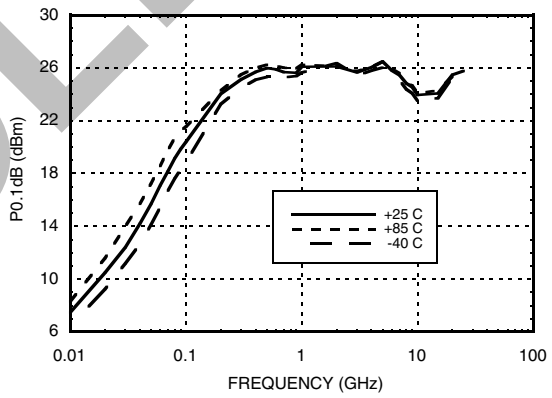
Step Attenuation vs. Attenuation State 0.1 - 18 GHz



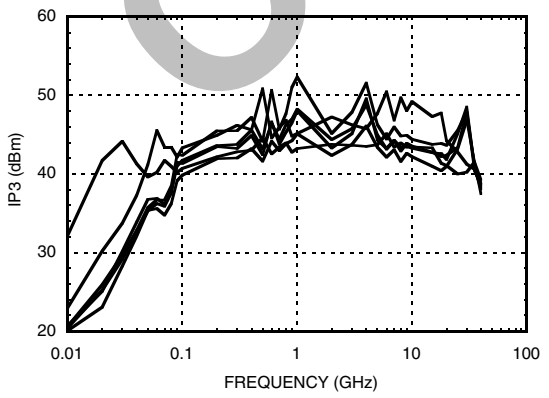
Step Attenuation vs. Attenuation State 18 - 30 GHz



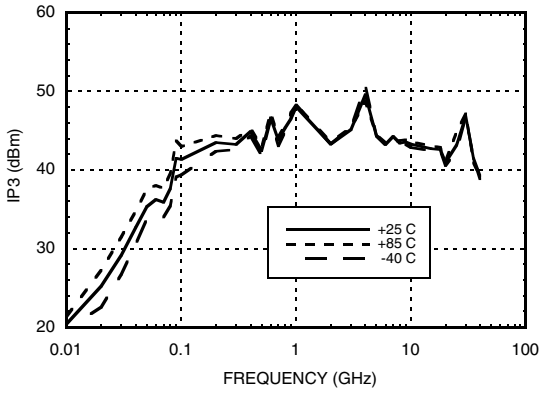
Input Power for 0.1 dB Compression



Input IP3 Over Major Attenuation States



Input IP3 vs. Temperature
(Minimum Attenuation State)



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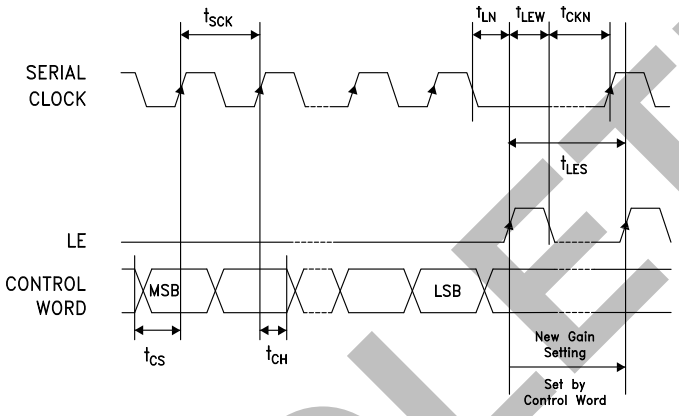
Serial Control Interface

The HMC1018LP4E contains a 3-wire SPI compatible digital interface (SERIN, CLK, LE). The serial control interface is activated when S/A is kept high. The 5-bit serial word must be loaded MSB first as a 6-bit word with the first bit ignored. The positive-edge sensitive CLK and LE requires clean transitions. If mechanical switches are used, sufficient debouncing should be provided. When LE is high, 5-bit data in the serial input register is transferred to the attenuator. When LE is high CLK is masked to prevent data transition during output loading.

For all modes of operations, the state will stay constant while LE is kept low.



Serial Mode Truth Table

Control Voltage Input					Attenuation State RF1 - RF2
P4 16 dB	P3 8 dB	P2 4 dB	P1 2 dB	P0 1 dB	
High	High	High	High	High	Reference I.L.
High	High	High	High	Low	1 dB
High	High	High	Low	High	2 dB
High	High	Low	High	High	4 dB
High	Low	High	High	High	8 dB
Low	High	High	High	High	16 dB
Low	Low	Low	Low	Low	31 dB

Any combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.

Parameter	Typ.
Min. serial period, t_{SCK}	100 ns
Control set-up time, t_{CS}	20 ns
Control hold-time, t_{CH}	20 ns
LE setup-time, t_{LN}	10 ns
Min. LE pulse width, t_{LEW}	10 ns
Min LE pulse spacing, t_{LES}	630 ns
Serial clock hold-time from LE, t_{CKN}	10 ns
Hold Time, $t_{PH.}$	0 ns
Latch Enable Minimum Width, t_{LEN}	10 ns
Setup Time, t_{PS}	2 ns

Asynchronous Mode

The HMC1018LP4E can be switched to an asynchronous mode to change the attenuation state rapidly to one of four predefined states. The logic state of ASM1-ASM2 determines one of the four attenuation states in the asynchronous mode per truth table. The asynchronous mode works either directly or latched. To activate the direct-asynchronous-mode, S/A needs to be at logic low and LE needs to be at logic high. In the direct-asynchronous-mode, any change in the logic state of ASM1-ASM2 directly affects the attenuation state. In the latched-asynchronous-mode, the attenuation state changes per the asynchronous mode truth table when S/A is at logic low and LE is pulsed per the timing diagram. The attenuation stays constant (latched) as long as LE stays low. In the asynchronous mode, the inputs SERIN and CLK do not affect the attenuation state.

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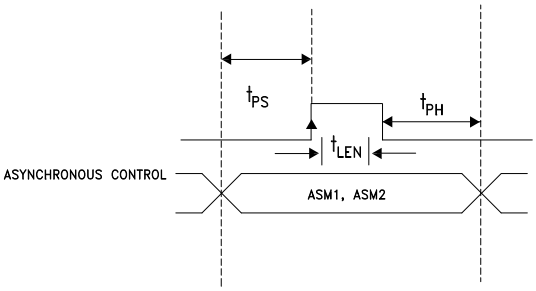
Timing Diagram (Latched Asynchronous Mode)



Asynchronous Mode Truth Table

ASM1	ASM2	Attenuation State RF1-RF2
High	High	Reference I.L.
High	Low	3 dB
Low	High	28 dB
Low	Low	31 dB

Power-Up States

If LE is set to logic LOW at power-up, the logic state of PUP determines the power-up state of the part per PUP truth table. If the LE is set to logic HIGH at power-up, the logic state of ASM1-ASM2 determines the power-up state of the part per truth table for the asynchronous mode. The attenuator latches in the desired power-up state approximately 200 ms after power-up.

PUP Truth Table

PUP	Attenuation State
High	Reference I.L.
Low	31 dB

Note: The logic state of ASM1-ASM2 determines the power-up state of the part per truth table for the asynchronous mode when LE is high at power-up.

Bias Voltages & Currents

Vdd	+5V @ 0.2 mA
Vdd1	+5V @ 4.5 mA
Vss	-5V @ 5 mA

Control Voltage

State	Bias Condition
Low	0 to 0.8V @ 1 µA
High	2 to 5V @ 1 µA

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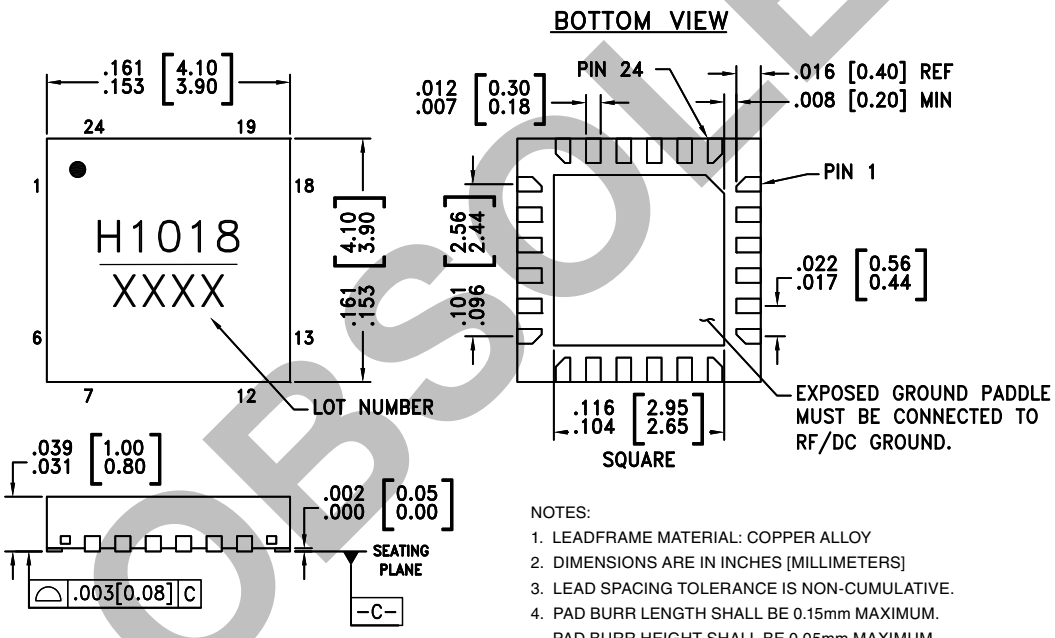
Absolute Maximum Ratings

RF Input Power (0.1 to 30.0 GHz)	+25 dBm
Control Voltage (CLK, SERIN, LE, PUP, ASM1, ASM2, S/A)	Vdd + 0.5V
Vdd, Vdd1	+7 Vdc
Vss	-7 Vdc
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 6.9 mW/°C above 85 °C)	0.451 W
Thermal Resistance	144 °C/W
Storage Temperature	-65 to + 150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC1018LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [1]	H1018 XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

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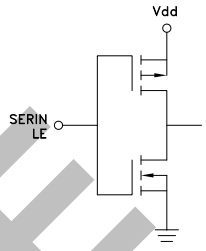
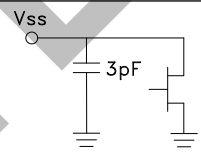
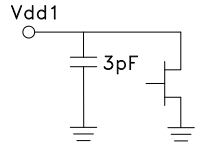
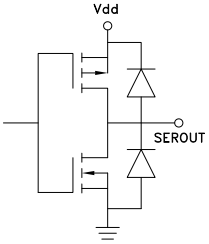
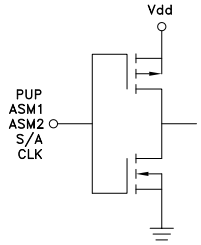
Pin Descriptions

Pad Number	Function	Description	Interface Schematic
1 2	SERIN LE	See truth table, control voltage table and timing diagram.	
3	Vss	Negative Bias -5V	
4, 15	GND	These pins and package bottom must be connected to RF/DC ground.	
6-13, 16	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
5, 14	RF1, RF2	These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required if RF line potential is not equal to 0V.	
17	Vdd1	Positive Bias +5V	
18	SEROUT	Serial input data delayed by 6 clock cycles.	
19 21 22 23 24	PUP ASM1 ASM2 S/A CLK	See truth table, control voltage table and timing diagram.	
20	Vdd	Serial Controller Bias +5V	

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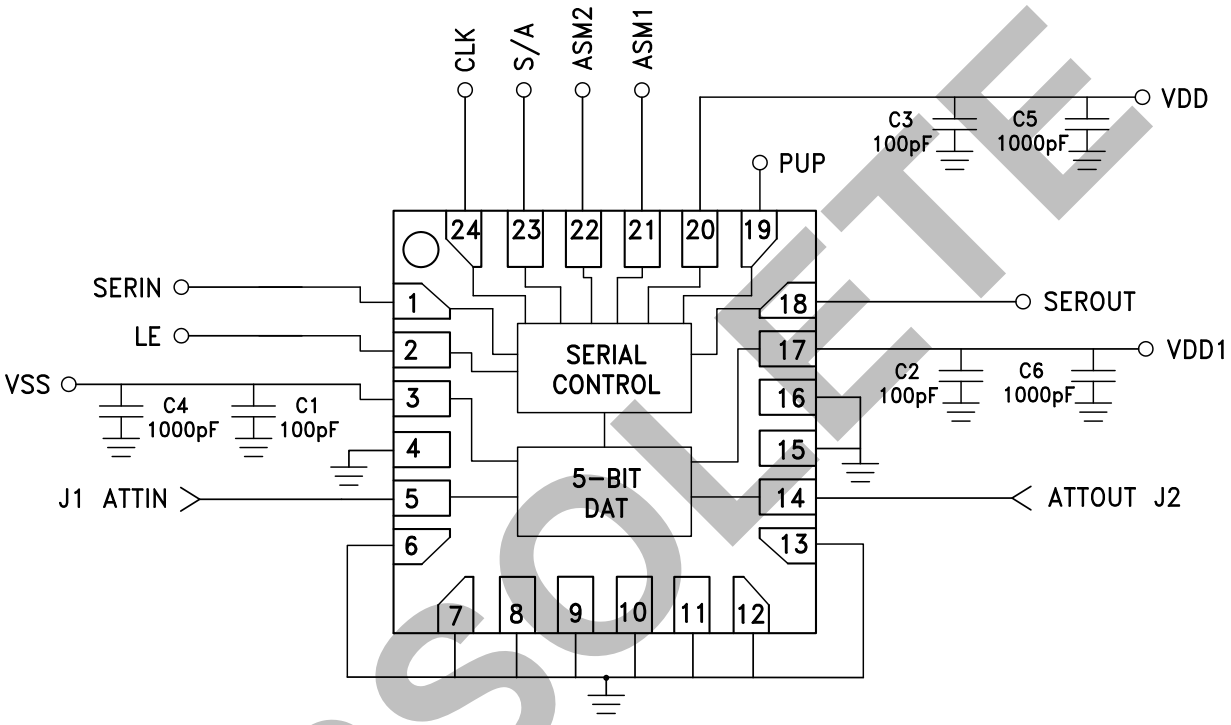
Application Circuit



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RoHS✓ EARTH FRIENDLY

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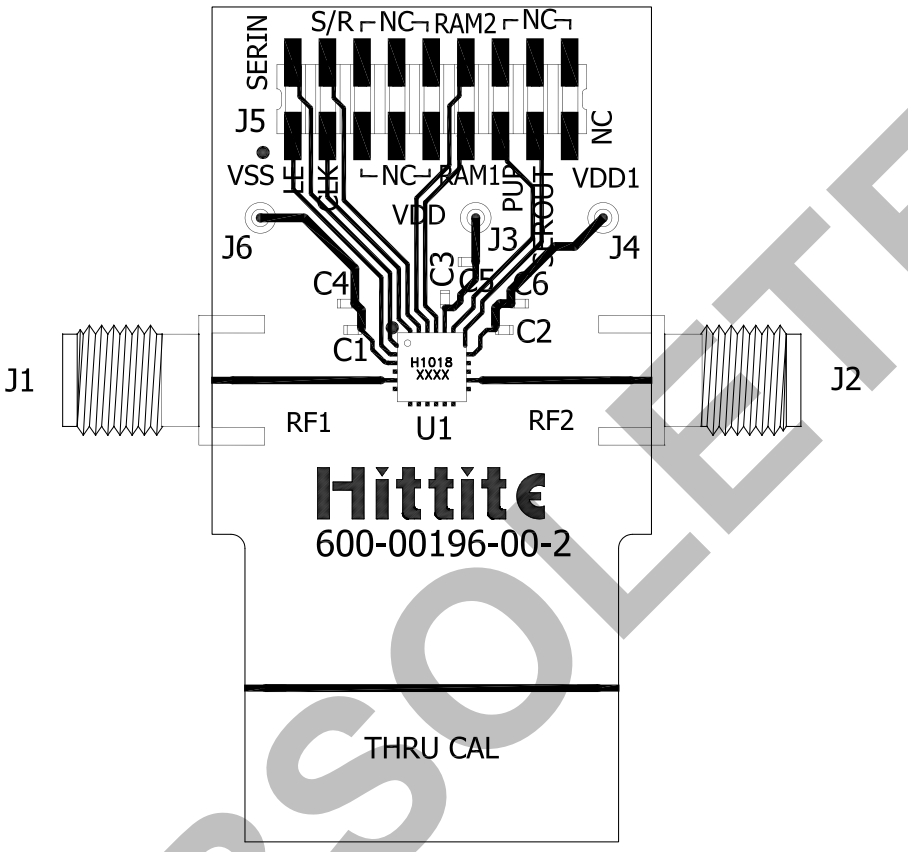
Evaluation PCB



List of Materials for Evaluation PCB EVAL01-HMC1018LP4E [1]

Item	Description
J1, J2	2.9 mm PC Mount RF Connector
J3, J4, J6	DC Connector
J5	2mm DC Header
C1-C3	100 pF Capacitor, 0402 Pkg.
C4-C6	1000 pF Capacitor, 0402 Pkg.
U1	HMC1018LP4E Digital Attenuator
PCB [2]	600-00196-00-2 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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