BURR - BROWN ®

DAC7613

For most current data sheet and other product information, visit www.burr-brown.com

12-Bit, Voltage Output DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW POWER: 1.8mW
- UNIPOLAR OR BIPOLAR OPERATION
- SETTLING TIME: 10µs to 0.012%
- 12-BIT LINEARITY AND MONOTONICITY: –40°C to +85°C
- DATA READBACK
- DOUBLE-BUFFERED DATA INPUTS
- 24-LEAD SSOP PACKAGE

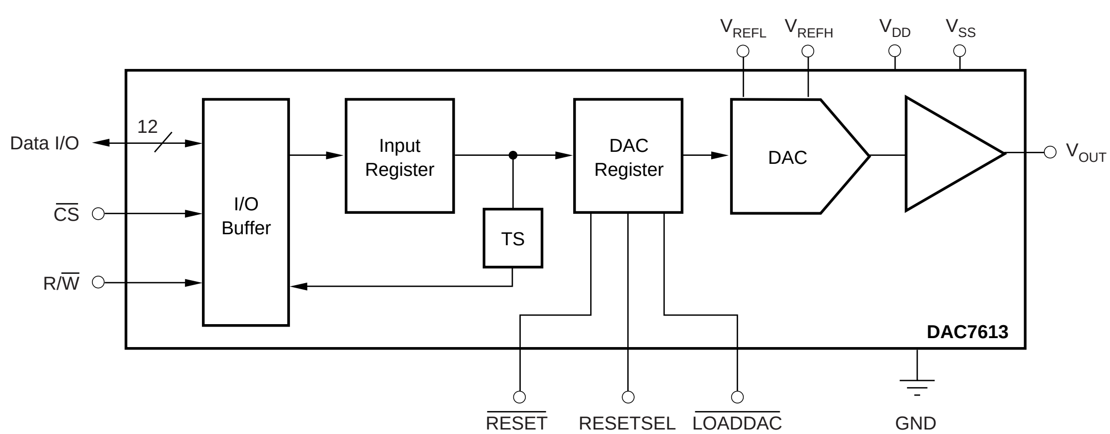
APPLICATIONS

- PROCESS CONTROL
- CLOSED-LOOP SERVO-CONTROL
- MOTOR CONTROL
- DATA ACQUISITION SYSTEMS

DESCRIPTION

The DAC7613 is a 12-bit, voltage output digital-to-analog converter with guaranteed 12-bit monotonic performance over the specified temperature range. The DAC7613 accepts a 12-bit parallel input data, has double-buffered DAC input logic and provides a readback mode of the internal input register. An asynchronous reset clears all registers to a mid-scale code of 800_H or to a zero-scale of 000_H. The DAC7613 can operate from a single +5V supply or from +5V and –5V supplies.

Low power and small size makes the DAC7613 ideal for data acquisition systems and closed-loop servo-control. The DAC7613 is available in a plastic SSOP-24 package, and offers guaranteed specifications over the –40°C to +85°C temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1500B
Printed in U.S.A. January, 2000
SBAS105

SPECIFICATION

At T_A = –40°C to +85°C, V_{DD} = +5V, V_{SS} = –5V, V_{REFH} = +2.5V, and V_{REFL} = –2.5V, unless otherwise noted.

		DAC7613E			DAC7613EB			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ACCURACY								
Linearity Error(1)	V_{SS} = 0V or –5V			±2			±1	LSB(2)
Differential Linearity Error	V_{SS} = 0V or –5V			±1			±1	LSB
Monotonicity	T_{MIN} to T_{MAX}	12			*			Bits
Zero-Scale Error	Code = 000_H			±4			*	LSB
Zero-Scale Drift			2	5		*	*	ppm/°C
Full-Scale Error	Code = FFF_H			±4			*	LS
Zero-Scale Error	Code = $00A_H$, V_{SS} = 0V			±8			*	LSB
Zero-Scale Drift	V_{SS} = 0V		5	10		*	*	ppm/°C
Full-Scale Error	Code = FFF_H, V_{SS} = 0V			±8			*	LSB
Power Supply Rejection			30			*		ppm/V
ANALOG OUTPUT								
Voltage Output(3)	V_{REFL} = 0V, V_{SS} = 0V	0		V_{REFH}	*		*	V
	V_{SS} = –5V	V_{REFL}		V_{REFH}	*		*	V
Output Current		–1.25		+1.25	*		*	mA
Load Capacitance	No Oscillation		100			*		pF
Short-Circuit Current			+5, –15			*		mA
Short-Circuit Duration			Indefinite			*		
REFERENCE INPUT								
V_{REFH} Input Range	V_{SS} = 0V or –5V	V_{REFL} + 1.25		+2.5	*		*	V
V_{REFL} Input Range	V_{SS} = 0V	0		V_{REFH} – 1.25	*		*	V
V_{REFL} Input Range	V_{SS} = –5V	–2.5		V_{REFH} – 1.25	*		*	V
DYNAMIC PERFORMANCE								
Settling Time(4)	To ±0.012%		5	10		*	*	µs
Output Noise Voltage	0Hz to 1MHz		40			*		nV/√Hz
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS		*			
Logic Levels								
V_{IH}	I_{IH} ≤ ±10µA	0.7 V_{DD}		V_{DD} + 0.3	*		*	V
V_{IL}	I_{IL} ≤ ±10µA	–0.3		0.3 V_{DD}	*		*	V
V_{OH}	I_{OH} = –0.8mA	3.6		V_{DD}	*		*	V
V_{OL}	I_{OL} = 1.6mA	0.0		0.4	*		*	V
Data Format			Straight Binary			*		
POWER SUPPLY REQUIREMENTS								
V_{DD}		4.75		5.25	*		*	V
V_{SS}	If V_{SS} ≠ 0V	–5.25		–4.75	*		*	V
I_{DD}			0.35	0.5		*	*	mA
I_{SS}		–0.65	–0.45		*	*		mA
Power Dissipation	V_{SS} = –5V		4	5.75		*	*	mW
	V_{SS} = 0V		1.8	2.5		*	*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

NOTES: (1) If V_{SS} = 0V, specification applies at code $00A_H$ and above. (2) LSB means Least Significant Bit, when V_{REFH} equals +2.5V and V_{REFL} equals –2.5V, then one LSB equals 1.22mV. (3) Ideal output voltage, does not take into account zero or full-scale error. (4) If V_{SS} = –5V, full-scale 5V step. If V_{SS} = 0V, full-scale positive 2.5V step and negative step from code FFF_H to $00A_H$.

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to V_{SS}	–0.3V to 11V
V_{DD} to GND	–0.3V to 5.5V
V_{REFL} to V_{SS}	–0.3V to (V_{DD} – V_{SS})
V_{DD} to V_{REFH}	–0.3V to (V_{DD} – V_{SS})
V_{REFH} to V_{REFL}	–0.3V to (V_{DD} – V_{SS})
Digital Input Voltage to GND	–0.3V to V_{DD} + 0.3V
Digital Output Voltage to GND	–0.3V to V_{DD} + 0.3V
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

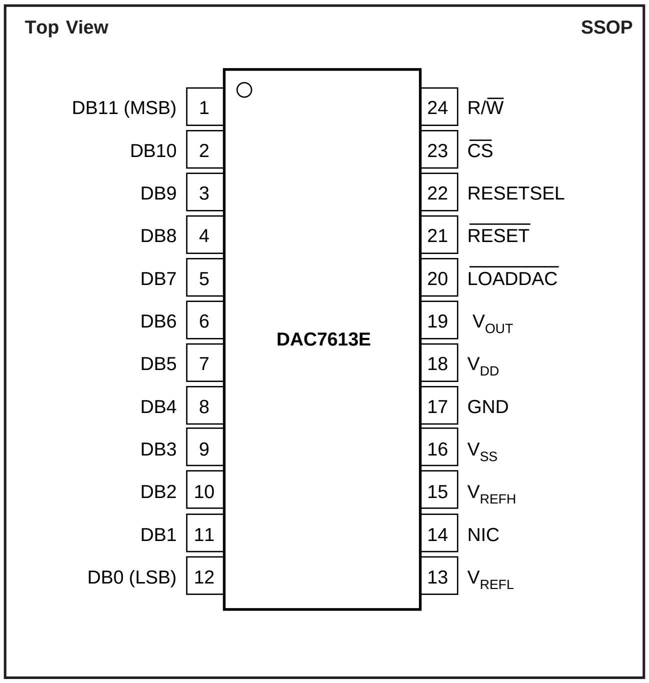
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	MAXIMUM LINEARITY ERROR (LSB)	MAXIMUM DIFFERENTIAL LINEARITY ERROR (LSB)	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFICATION TEMPERATURE RANGE	ORDERING NUMBER[1]	TRANSPORT MEDIA
DAC7613E	±2	±1	SSOP-24	338	–40°C to +85°C	DAC7613E	Rails
"	"	"	"	"	"	DAC7613E/1K	Tape and Reel
DAC7613EB	±1	±1	SSOP-24	338	–40°C to +85°C	DAC7613EB	Rails
"	"	"	"	"	"	DAC7613EB/1K	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of “DAC7613E/1K” will get a single 1000-piece Tape and Reel.

PIN CONFIGURATION



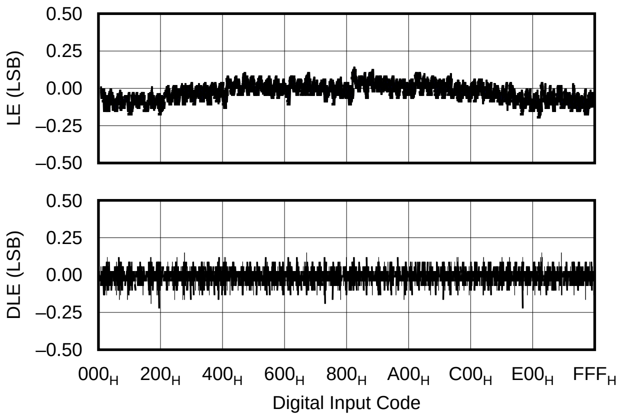
PIN DESCRIPTIONS

PIN	LABEL	DESCRIPTION
1	DB11	Data Bit 11, MSB
2	DB10	Data Bit 10
3	DB9	Data Bit 9
4	DB8	Data Bit 8
5	DB7	Data Bit 7
6	DB6	Data Bit 6
7	DB5	Data Bit 5
8	DB4	Data Bit 4
9	DB3	Data Bit 3
10	DB2	Data Bit 2
11	DB1	Data Bit 1
12	DB0	Data Bit 0, LSB
13	V_{REFL}	Reference Input Voltage Low. Sets minimum output voltage for the DAC.
14	NIC	Not Internally Connected
15	V_{REFH}	Reference Input Voltage High. Sets maximum output voltage for the DAC.
16	V_{SS}	Negative Analog Supply Voltage, 0V or –5V nominal.
17	GND	Ground
18	V_{DD}	Positive Power Supply
19	V_{OUT}	DAC Voltage Output
20	$\overline{LOADDAC}$	The selected DAC register becomes transparent when $\overline{LOADDAC}$ is LOW. It is in the latched state when $\overline{LOADDAC}$ is HIGH.
21	$\overline{RESET}$	Asynchronous Reset Input. Sets the DAC register to either zero-scale (000_H) or mid-scale (800_H) when LOW. RESETSEL determines which code is active.
22	RESETSEL	When LOW, a LOW on $\overline{RESET}$ will cause the DAC register to be set to code 000_H. When RESETSEL is HIGH, a LOW on $\overline{RESET}$ will set the registers to code 800_H.
23	$\overline{CS}$	Chip Select. Active LOW.
24	R/$\overline{W}$	Enabled by $\overline{CS}$. Controls data read and write from the input register.

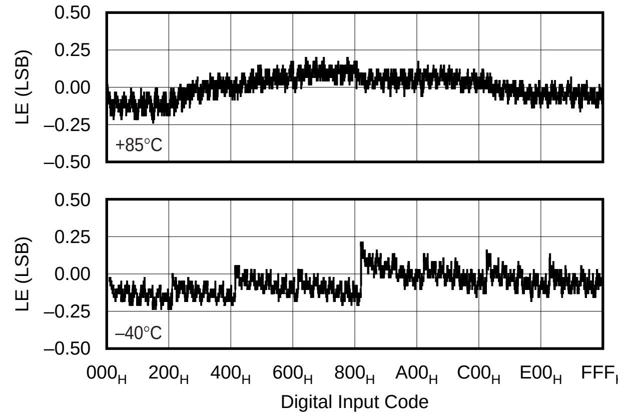
TYPICAL PERFORMANCE CURVES: V_{SS} = 0V

At T_A = +25°C, V_{DD} = +5V, V_{REFH} = +2.5V, and V_{REFL} = 0V, representative unit, unless otherwise specified.

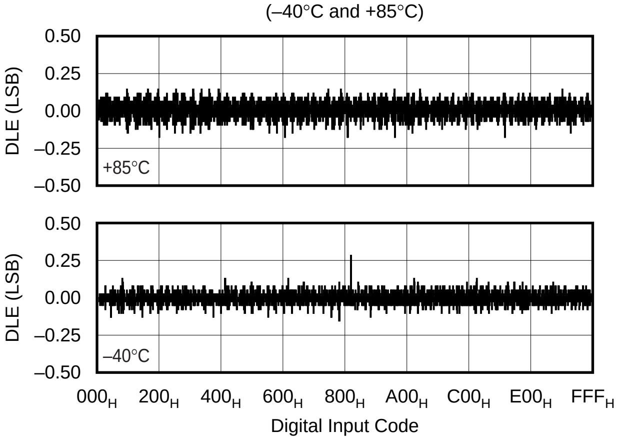
LINEARITY ERROR and
DIFFERENTIAL LINEARITY ERROR vs CODE



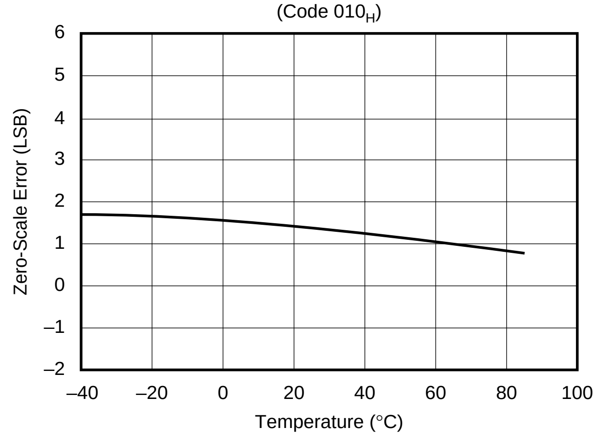
LINEARITY ERROR vs CODE
(–40°C and +85°C)



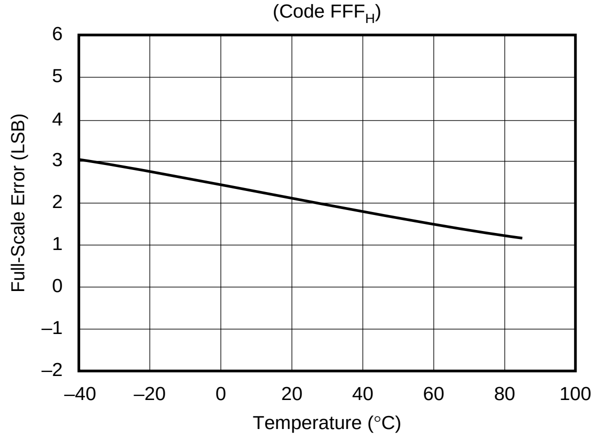
DIFFERENTIAL LINEARITY ERROR vs CODE
(–40°C and +85°C)



ZERO-SCALE ERROR vs TEMPERATURE
(Code 010_H)



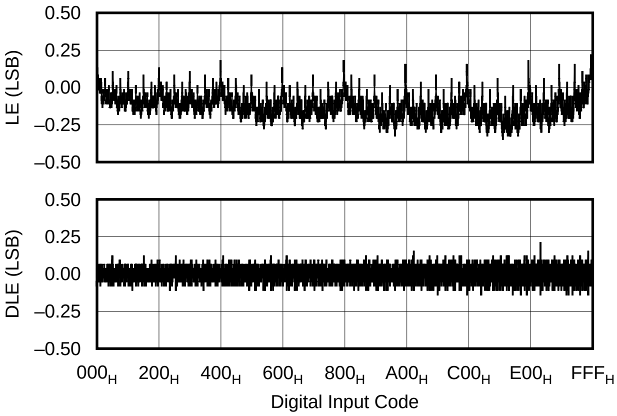
FULL-SCALE ERROR vs TEMPERATURE
(Code FFF_H)



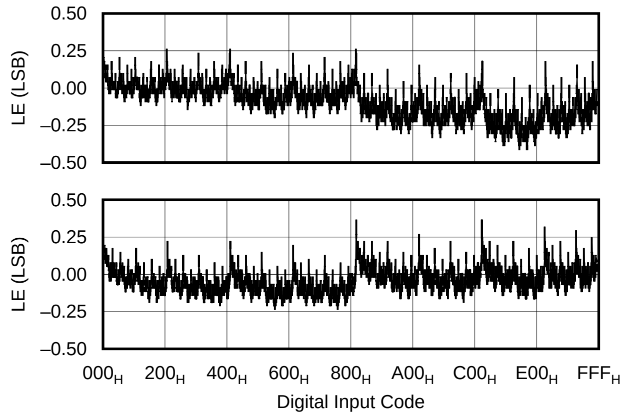
TYPICAL PERFORMANCE CURVES: V_{SS} = – 5V

At T_A = +25°C, V_{DD} = +5V, V_{REFH} = +2.5V, and V_{REFL} = 0V, representative unit, unless otherwise specified.

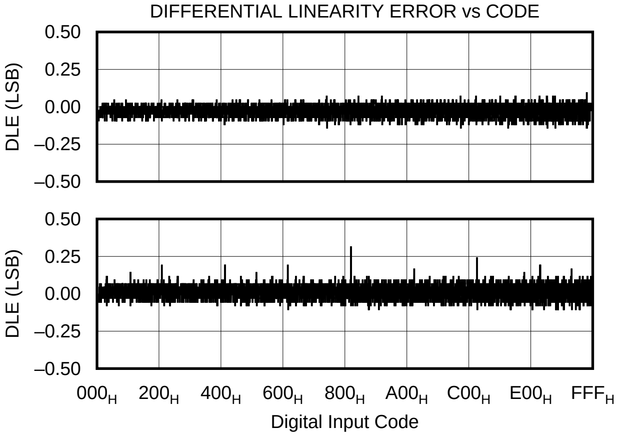
LINEARITY ERROR and
DIFFERENTIAL LINEARITY ERROR vs CODE



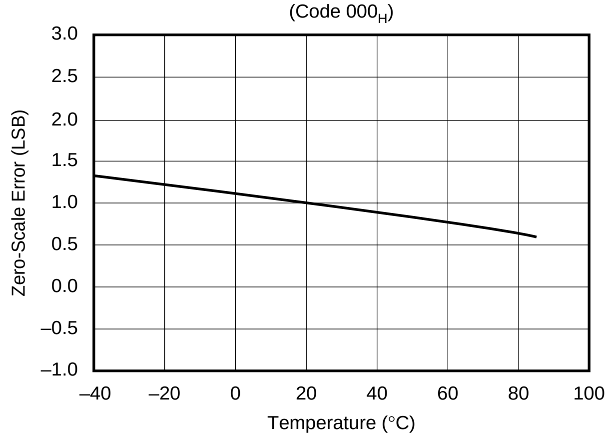
LINEARITY ERROR vs CODE



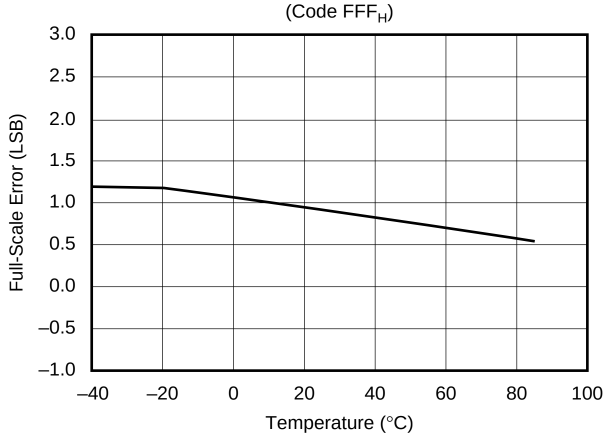
DIFFERENTIAL LINEARITY ERROR vs CODE



ZERO-SCALE ERROR vs TEMPERATURE
(Code 000_H)



FULL-SCALE ERROR vs TEMPERATURE
(Code FFF_H)



THEORY OF OPERATION

The DAC7613 is a 12-bit, voltage output Digital-to-Analog Converter (DAC). The architecture is a classic R-2R ladder configuration followed by an operational amplifier that serves as a buffer. The minimum voltage output ("zero-scale") and maximum voltage output ("full-scale") are set by the external voltage references (V_{REFL} and V_{REFH}, respectively). The digital input is a 12-bit parallel word and the DAC input register offers a readback capability. The converter can be powered from a single +5V supply or a dual ±5V supply. The device offers a reset function which immediately sets the DAC output voltage and DAC register to mid-scale (code 800_H) or to zero-scale (code 000_H), depending on the status of the reset selection. See Figures 1 and 2 for the basic operation of the DAC7613.

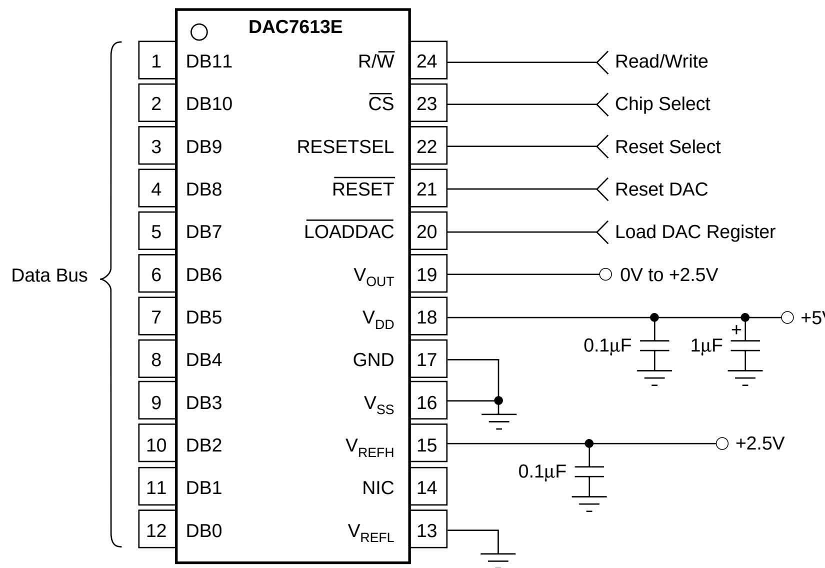


FIGURE 1. Basic Single-Supply Operation of the DAC7613.

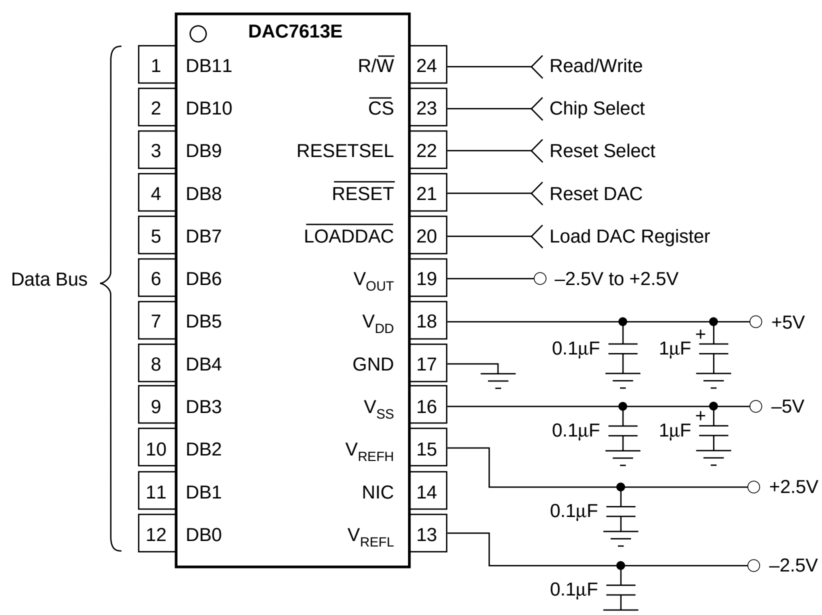


FIGURE 2. Basic Dual-Supply Operation of the DAC7613.

ANALOG OUTPUTS

When V_{SS} = –5V (dual supply operation), the output amplifier can swing to within 2.25V of the supply rails, guaranteed over the –40°C to +85°C temperature range. With V_{SS} = 0V (single-supply operation), the output can swing to ground. Note that the settling time of the output op amp will be longer with voltages very near ground. Additionally, care must be taken when measuring the zero-scale error when V_{SS} = 0V. Since the output voltage cannot swing below ground, the output voltage may not change for the first few digital input codes (000_H, 001_H, 002_H, etc.) if the output amplifier has a negative offset.

The behavior of the output amplifier can be critical in some applications. Under short-circuit conditions (DAC output shorted to ground), the output amplifier can sink a great deal more current than it can source. See the Specifications table for more details concerning short-circuit current.

REFERENCE INPUTS

The reference inputs, V_{REFL} and V_{REFH}, can be any voltage between V_{SS} + 2.25V and V_{DD} – 2.25V provided that V_{REFH} is at least 1.25V greater than V_{REFL}. The minimum output of each DAC is equal to V_{REFL} plus a small offset voltage (essentially, the offset of the output op amp). The maximum output is equal to V_{REFH} plus a similar offset voltage. Note that V_{SS} (the negative power supply) must either be connected to ground or must be in the range of –4.75V to –5.25V. The voltage on V_{SS} sets several bias points within the converter. If V_{SS} is not in one of these two configurations, the bias values may be in error and proper operation of the device is not guaranteed.

The current into the V_{REFH} input depends on the DAC output voltages and can vary from a few microamps to approximately 0.1 milliamp. The V_{REFH} source will not be required to sink current, only source it. Bypassing the reference voltage or voltages with at least a 0.1µF capacitor placed as close to the DAC7613 package is strongly recommended.

DIGITAL INTERFACE

Table I shows the basic control logic for the DAC7613. Note that the internal register is level triggered and not edge triggered. When the appropriate signal is LOW, the register becomes transparent. When this signal is returned HIGH, the digital word currently in the register is latched. The first register (the input register) is triggered via the R/$\overline{W}$, and $\overline{CS}$ inputs. The second register (the DAC register) is transparent when $\overline{LOADDAC}$ input is pulled LOW.

The double-buffered architecture is mainly designed so that the DAC input register can be written at any time and then the DAC voltage updated by pulling $\overline{LOADDAC}$ LOW.

R/$\overline{W}$	$\overline{CS}$	RST	$\overline{LOADDAC}$	INPUT REGISTER	DAC REGISTER	MODE
L	L	H	L	Write	Write	Write
L	L	H	H	Write	Hold	Write Input
H	L	H	H	Read	Hold	Read Input
X	H	H	L	Hold	Update	Update
X	H	H	H	Hold	Hold	Hold
X	H	L	X	Hold	Reset	Reset

X = Don't Care.

TABLE I. DAC7613 Control Logic Truth Table.

DIGITAL TIMING

Figure 3 and Table II provide detailed timing for the digital interface of the DAC7613.

DIGITAL INPUT CODING

The DAC7613 input data is in Straight Binary format. The output voltage is given by the following equation:

$$V_{OUT} = V_{REFL} + \frac{(V_{REFH} - V_{REFL}) \cdot N}{4096} \quad (1)$$

where N is the digital input code. This equation does not include the effects of offset (zero-scale) or gain (full-scale) errors.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{RCS}	$\overline{CS}$ LOW for Read	200			ns
t_{RDS}	R/$\overline{W}$ HIGH to $\overline{CS}$ LOW	10			ns
t_{RDH}	R/$\overline{W}$ HIGH after $\overline{CS}$ HIGH	0			ns
t_{DZ}	$\overline{CS}$ HIGH to Data Bus in High Impedance		100		ns
t_{CSD}	$\overline{CS}$ LOW to Data Bus Valid		100	160	ns
t_{WCS}	$\overline{CS}$ LOW for Write	50			ns
t_{WS}	R/$\overline{W}$ LOW to $\overline{CS}$ LOW	0			ns
t_{WH}	R/$\overline{W}$ LOW after $\overline{CS}$ HIGH	5			ns
t_{DS}	Data Valid to $\overline{CS}$ LOW	0			ns
t_{DH}	Data Valid after $\overline{CS}$ HIGH	5			ns
t_{LWD}	$\overline{LOADDAC}$ LOW	50			ns
t_{RESET}	RESET LOW	50			ns

TABLE II. Timing Specifications (T_A = –40°C to +85°C).

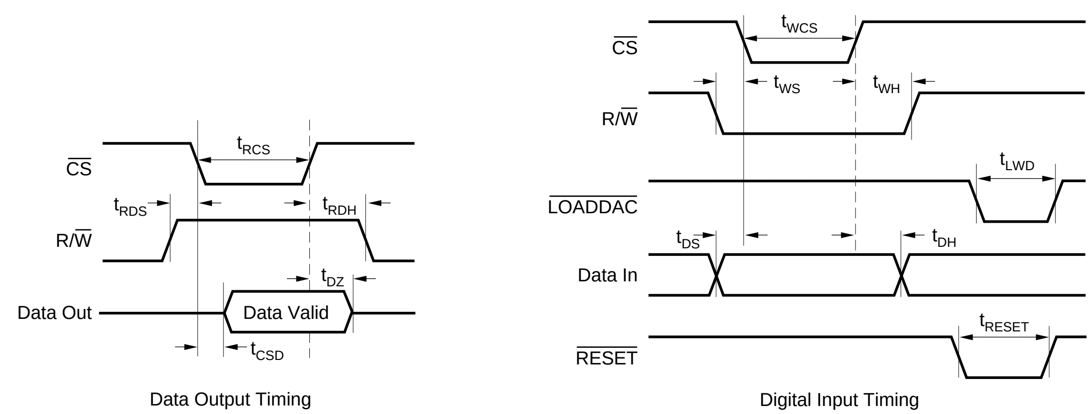


FIGURE 3. Digital Input and Output Timing.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7613E	ACTIVE	SSOP	DB	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7613E	Samples
DAC7613E/1K	ACTIVE	SSOP	DB	24	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7613E	Samples
DAC7613EB	ACTIVE	SSOP	DB	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7613E B	Samples
DAC7613EB/1K	ACTIVE	SSOP	DB	24	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7613E B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

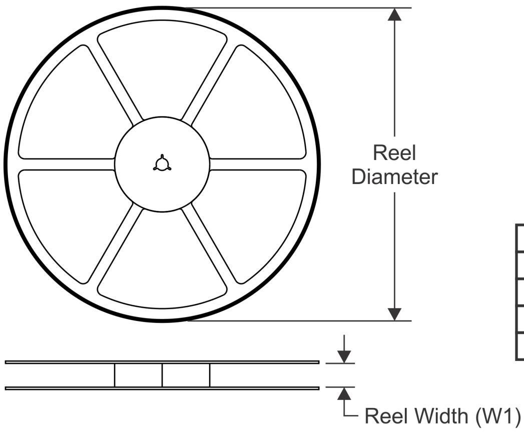
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

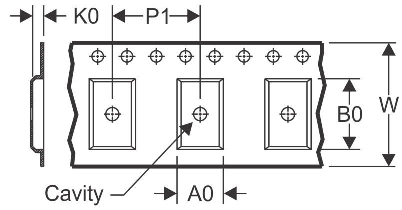
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

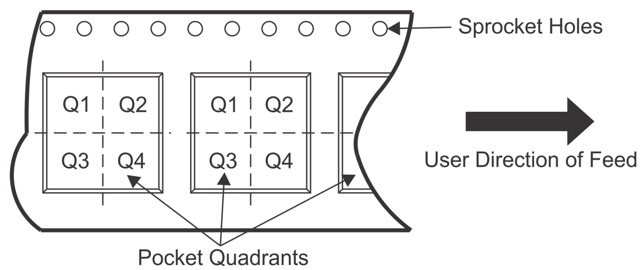


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

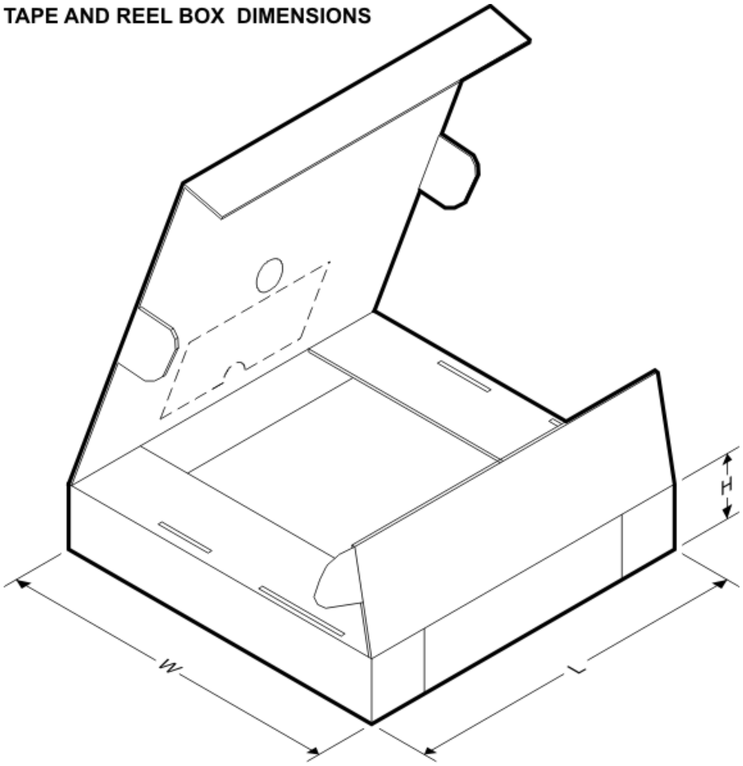
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7613E/1K	SSOP	DB	24	1000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
DAC7613EB/1K	SSOP	DB	24	1000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7613E/1K	SSOP	DB	24	1000	346.0	346.0	33.0
DAC7613EB/1K	SSOP	DB	24	1000	346.0	346.0	33.0

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265