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# F DN327N

## N-Channel 1.8 V<sub>GS</sub> Specified PowerTrench® MOSFET

### General Description

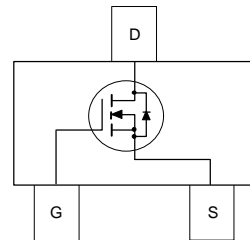
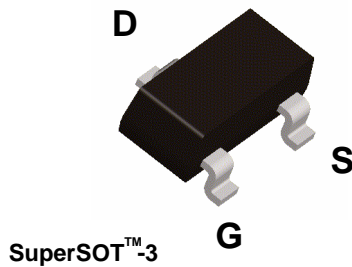
This 20V N-Channel MOSFET uses Fairchild's high voltage PowerTrench process. It has been optimized for power management applications.

### Applications

- Load switch
- Battery protection
- Power management

### Features

- 2 A, 20 V.  $R_{DS(ON)} = 70 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$   
 $R_{DS(ON)} = 80 \text{ m}\Omega @ V_{GS} = 2.5 \text{ V}$   
 $R_{DS(ON)} = 120 \text{ m}\Omega @ V_{GS} = 1.8 \text{ V}$
- Low gate charge (4.5 nC typical)
- Fast switching speed
- High performance trench technology for extremely low  $R_{DS(ON)}$



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage	20	V
V <sub>GSS</sub>	Gate-Source Voltage	± 8	V
I <sub>D</sub>	Drain Current – Continuous (Note 1a)	2	A
	– Pulsed	8	
P <sub>D</sub>	Power Dissipation for Single Operation (Note 1a) (Note 1b)	0.5	W
		0.46	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	–55 to +150	°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	75	°C/W

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
327	F DN327N	7"	8mm	3000 units

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		12		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSSF}$	Gate–Body Leakage, Forward	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate–Body Leakage, Reverse	$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

**On Characteristics (Note 2)**

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.4	0.7	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5\text{ V}, I_D = 2.0\text{ A}$ $V_{GS} = 2.5\text{ V}, I_D = 1.9\text{ A}$ $V_{GS} = 1.8\text{ V}, I_D = 1.6\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 2\text{ A}, T_J = 125^\circ\text{C}$		40 49 65 55	70 80 120 103	m $\Omega$
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	8			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 2\text{ A}$		11		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}$		423		pF
$C_{oss}$	Output Capacitance	$f = 1.0\text{ MHz}$		87		pF
$C_{rss}$	Reverse Transfer Capacitance			48		pF

**Switching Characteristics (Note 2)**

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 10\text{ V}, I_D = 1\text{ A},$		6	12	ns
$t_r$	Turn–On Rise Time	$V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$		6.5	13	ns
$t_{d(off)}$	Turn–Off Delay Time			14	29	ns
$t_f$	Turn–Off Fall Time			2	4	ns
$Q_g$	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 2\text{ A},$		4.5	6.3	nC
$Q_{gs}$	Gate–Source Charge	$V_{GS} = 4.5\text{ V}$		0.89		nC
$Q_{gd}$	Gate–Drain Charge			0.95		nC

**Drain–Source Diode Characteristics and Maximum Ratings**

$I_S$	Maximum Continuous Drain–Source Diode Forward Current				0.42	A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.42\text{ A}$ (Note 2)		0.6	1.2	V

**Notes:**

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $250^\circ\text{C/W}$  when mounted on a  $0.02\text{ in}^2$  pad of 2 oz. copper.



b)  $270^\circ\text{C/W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$

## Typical Characteristics

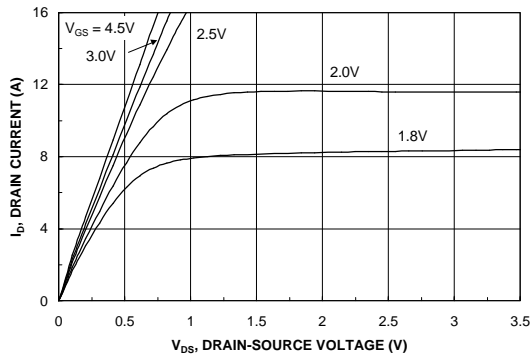


Figure 1. On-Region Characteristics.

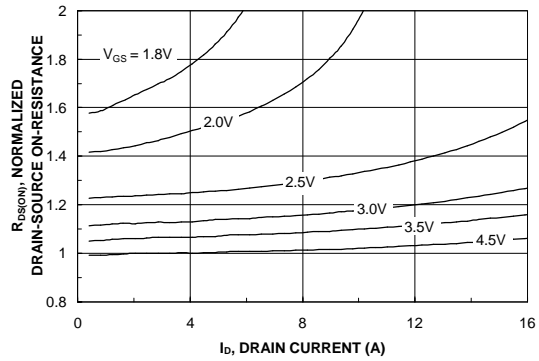


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

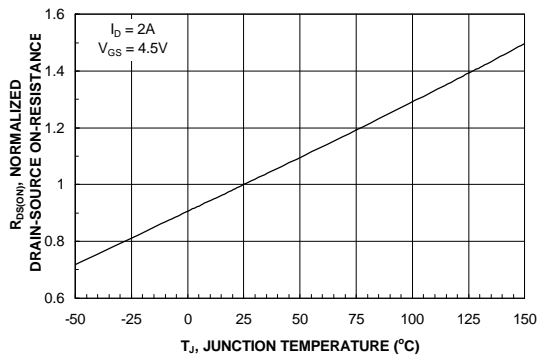


Figure 3. On-Resistance Variation with Temperature.

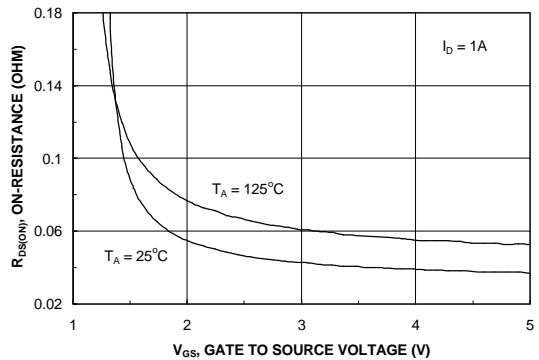


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

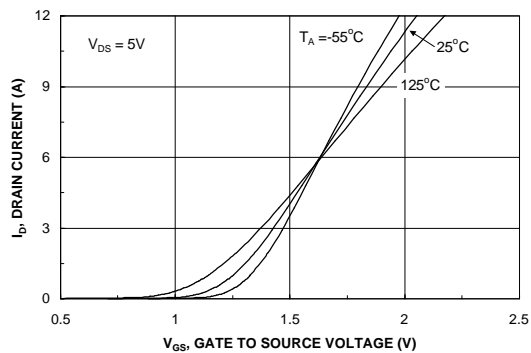


Figure 5. Transfer Characteristics.

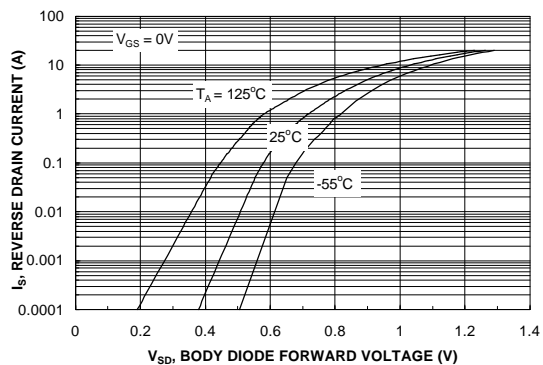
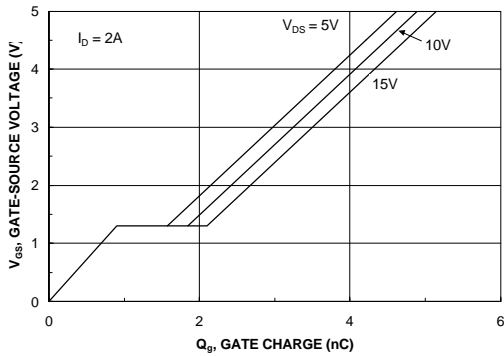
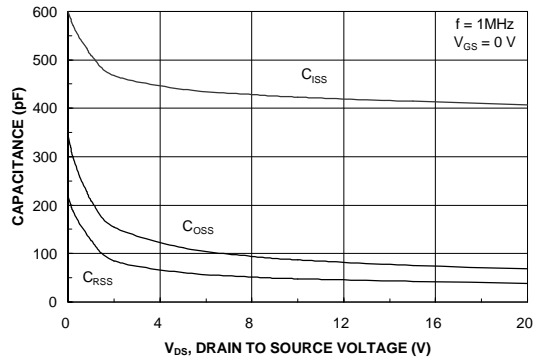


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

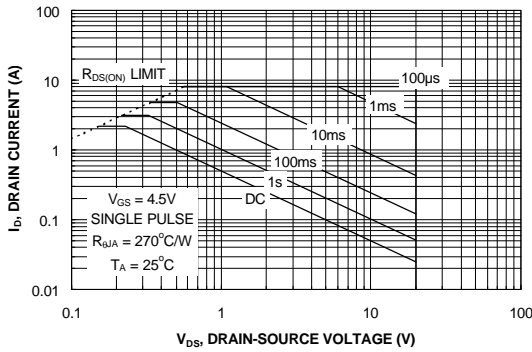
## Typical Characteristics



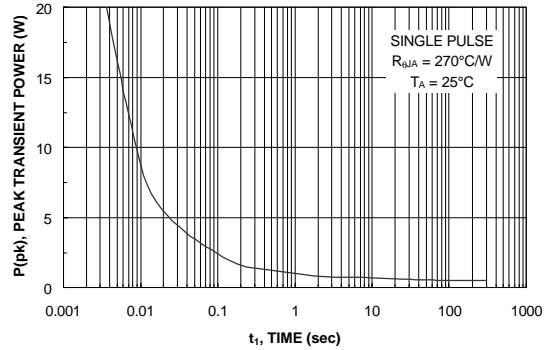
**Figure 7. Gate Charge Characteristics.**



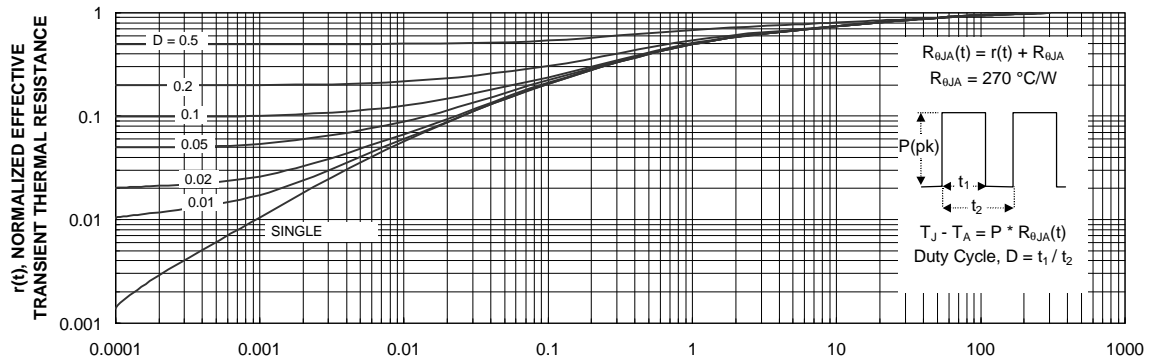
**Figure 8. Capacitance Characteristics.**



**Figure 9. Maximum Safe Operating Area.**



**Figure 10. Single Pulse Maximum Power Dissipation.**



**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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