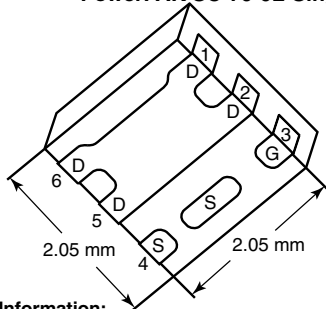


## P-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω) (Max.)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)
- 30	0.0185 at V <sub>GS</sub> = - 10 V	- 24	21 nC
	0.0235 at V <sub>GS</sub> = - 4.5 V	- 21	
	0.0260 at V <sub>GS</sub> = - 3.7 V	- 20	
	0.0377 at V <sub>GS</sub> = - 2.5 V	- 10	

**PowerPAK SC-70-6L-Single**

**Ordering Information:**

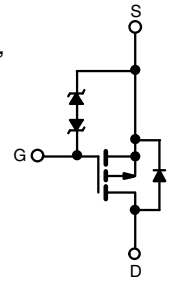
SiA453EDJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

**FEATURES**

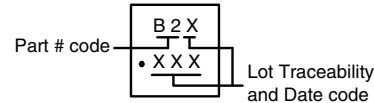
- TrenchFET® Power MOSFET
- Thermally Enhanced PowerPAK® SC-70 Package
  - Small Footprint Area
  - Low On-Resistance
- 100 % R<sub>g</sub> and UIS Tested
- Typical ESD Protection: 4000 V (HBM)
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
 COMPLIANT  
 HALOGEN  
**FREE**
**APPLICATIONS**

- Portable Devices such as Smart Phones, Tablet PCs and Mobile Computing
  - Load Switch
  - Power Management
  - Input Protection Switch (over voltage, reverse voltage)



P-Channel MOSFET

**Marking Code**


ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	- 30	V
Gate-Source Voltage	V <sub>GS</sub>	± 12	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	- 24
		T <sub>C</sub> = 70 °C	- 19
		T <sub>A</sub> = 25 °C	- 10 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	- 8 <sup>b, c</sup>
Pulsed Drain Current (t = 100 μs)	I <sub>DM</sub>	- 80	A
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	
		T <sub>A</sub> = 25 °C	- 2.9 <sup>b, c</sup>
Single Avalanche Current	I <sub>AS</sub>	- 10	mJ
Single Avalanche Energy	E <sub>AS</sub>	5	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	19
		T <sub>C</sub> = 70 °C	12
		T <sub>A</sub> = 25 °C	3.5 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	2.2 <sup>b, c</sup>
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 50 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, f</sup>	R <sub>thJA</sub>	28	36	°C/W
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	5.3	6.5	

**Notes**

- T<sub>C</sub> = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 80 °C/W.

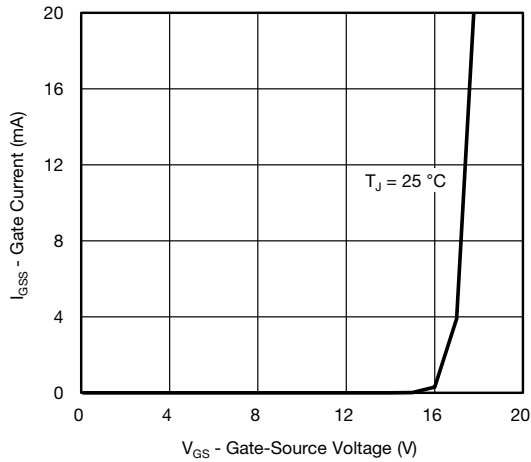
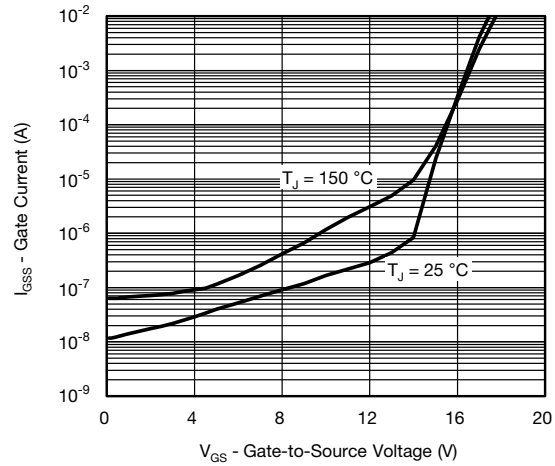
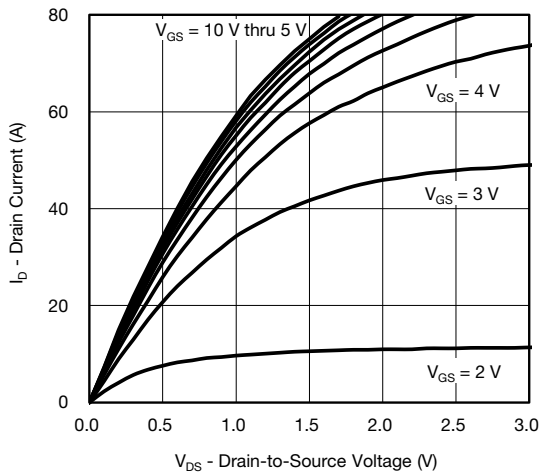
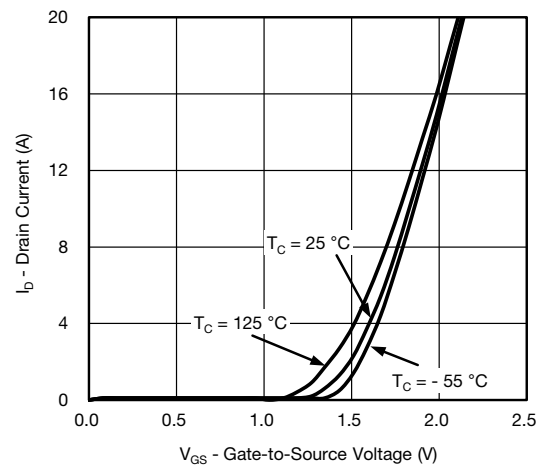
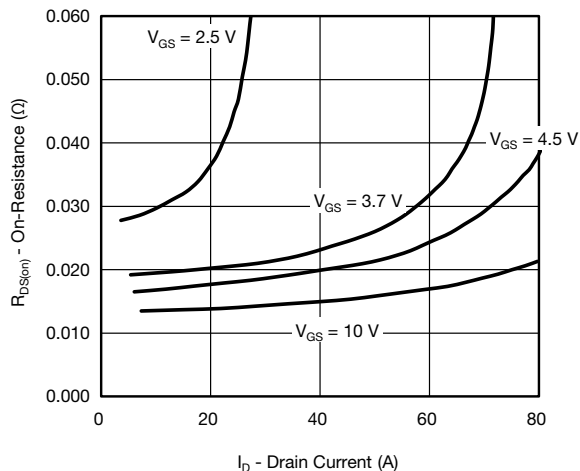
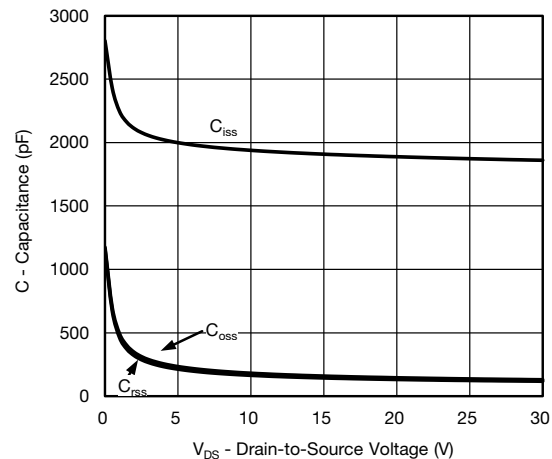


<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-30			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-21		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			3.1		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.6		-1.4	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			$\pm 4$	$\mu\text{A}$
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 4.5\text{ V}$			$\pm 0.5$	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$			-1	
		$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			-10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -10\text{ V}$	-10			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -5\text{ A}$		0.0150	0.0185	$\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -5\text{ A}$		0.0185	0.0235	
		$V_{GS} = -3.7\text{ V}, I_D = -5\text{ A}$		0.0205	0.0260	
		$V_{GS} = -2.5\text{ V}, I_D = -2\text{ A}$		0.0290	0.0377	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{GS} = -15\text{ V}, I_D = -5\text{ A}$		22		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1900		pF
Output Capacitance	$C_{oss}$			160		
Reverse Transfer Capacitance	$C_{rss}$			145		
Total Gate Charge	$Q_g$	$V_{DS} = -15\text{ V}, V_{GS} = -10\text{ V}, I_D = -11\text{ A}$		44	66	nC
				21	32	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = -15\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -11\text{ A}$		3.9		
Gate-Drain Charge	$Q_{gd}$			5.9		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	1.8	9	18	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\text{ V}, R_L = 1.7\text{ }\Omega$ $I_D \cong -9\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		25	50	ns
Rise Time	$t_r$			45	90	
Turn-Off Delay Time	$t_{d(off)}$			65	130	
Fall Time	$t_f$			28	55	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\text{ V}, R_L = 1.7\text{ }\Omega$ $I_D \cong -9\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		10	20	
Rise Time	$t_r$			5	10	
Turn-Off Delay Time	$t_{d(off)}$			90	180	
Fall Time	$t_f$			25	50	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			-16	A
Pulse Diode Forward Current ( $t = 100\text{ }\mu\text{s}$ )	$I_{SM}$				-80	
Body Diode Voltage	$V_{SD}$	$I_S = -9\text{ A}, V_{GS} = 0\text{ V}$		-0.85	-1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = -9\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		22	45	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			20	40	nC
Reverse Recovery Fall Time	$t_a$			16		ns
Reverse Recovery Rise Time	$t_b$			6		

**Notes**

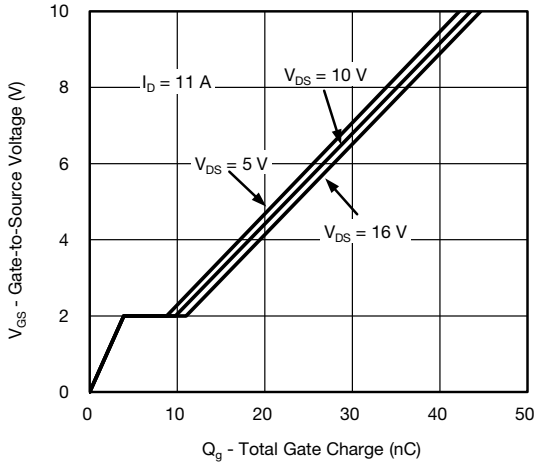
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

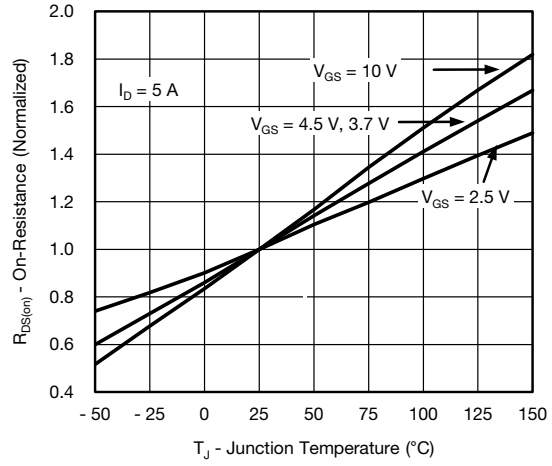
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Gate Current vs. Gate-Source Voltage**

**Gate Current vs. Gate-to-Source Voltage**

**Output Characteristics**

**Transfer Characteristics**

**On-Resistance vs. Drain Current and Gate Voltage**

**Capacitance**



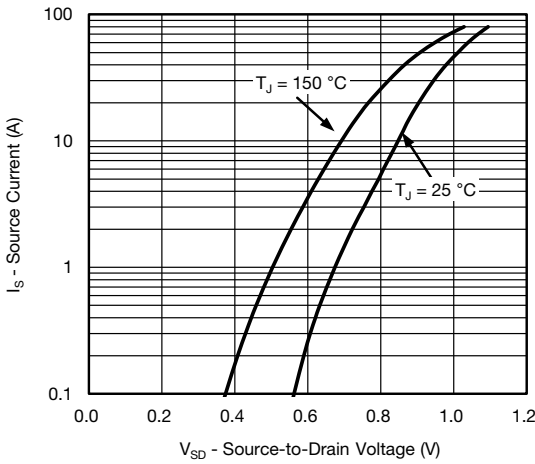
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



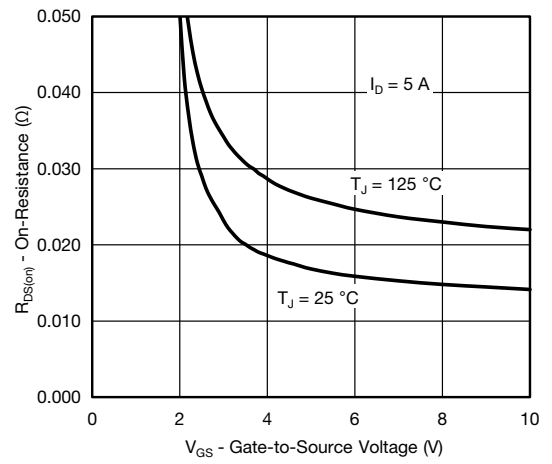
**Gate Charge**



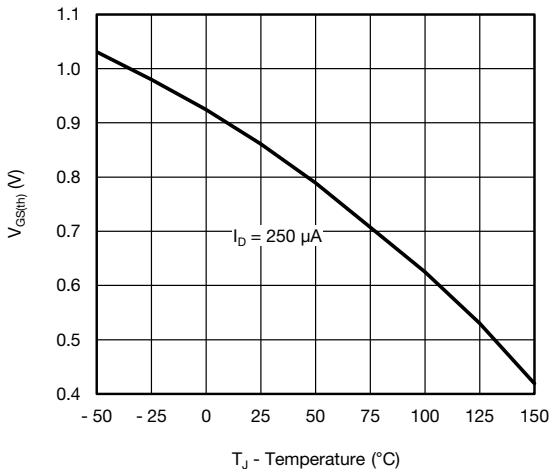
**On-Resistance vs. Junction Temperature**



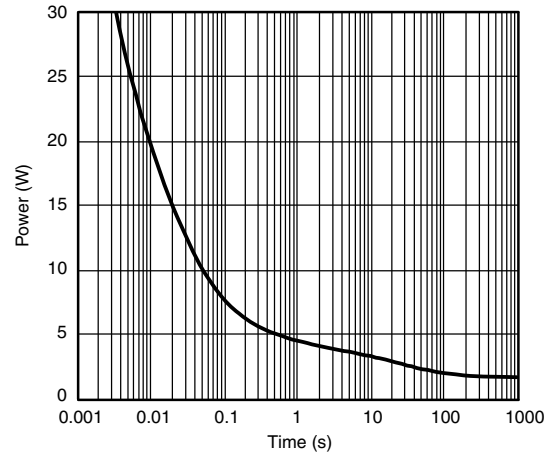
**Source-Drain Diode Forward Voltage**



**On-Resistance vs. Gate-to-Source Voltage**



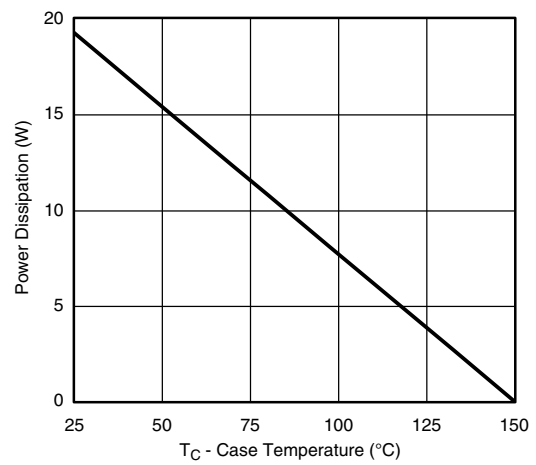
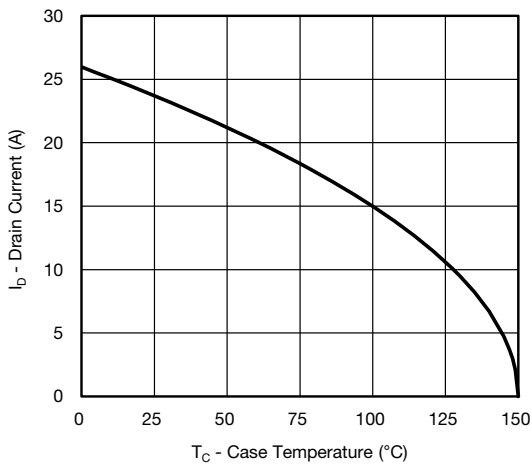
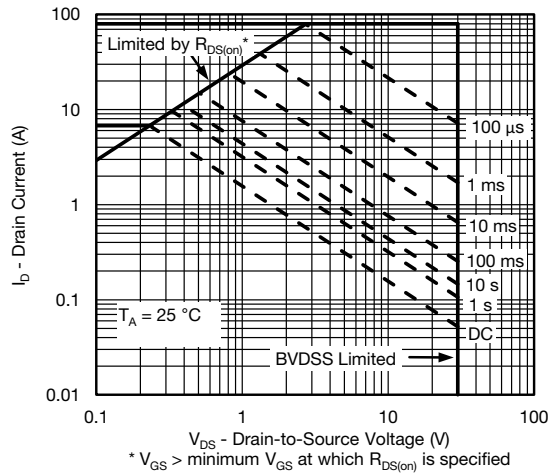
**Threshold Voltage**



**Single Pulse Power, Junction-to-Ambient**



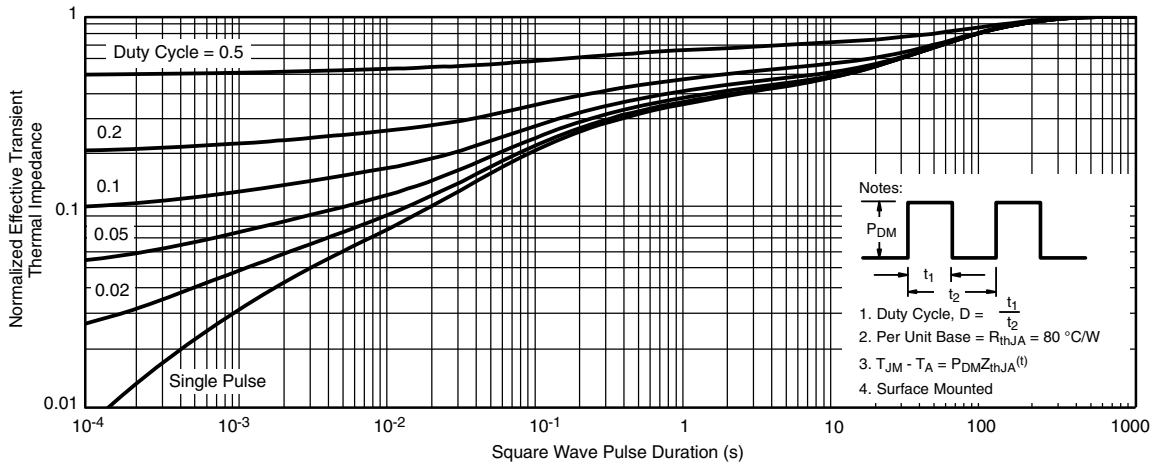
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



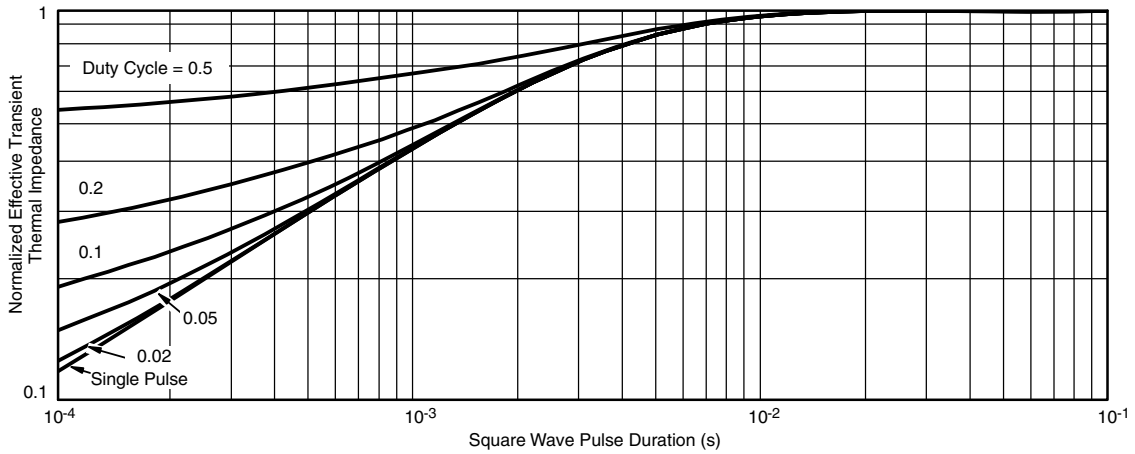
\* The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

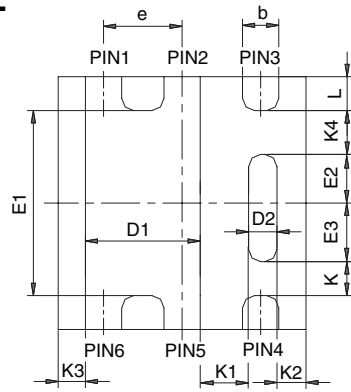


**Normalized Thermal Transient Impedance, Junction-to-Case**

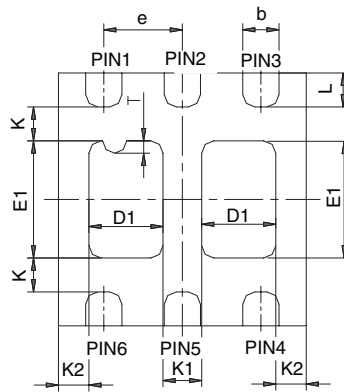
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?62864](http://www.vishay.com/ppg?62864).



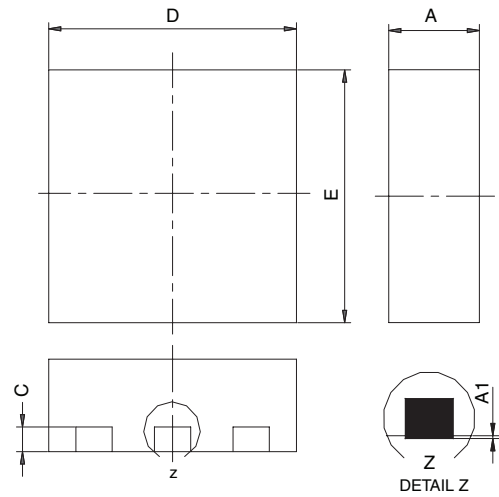
PowerPAK® SC70-6L



BACKSIDE VIEW OF SINGLE



BACKSIDE VIEW OF DUAL

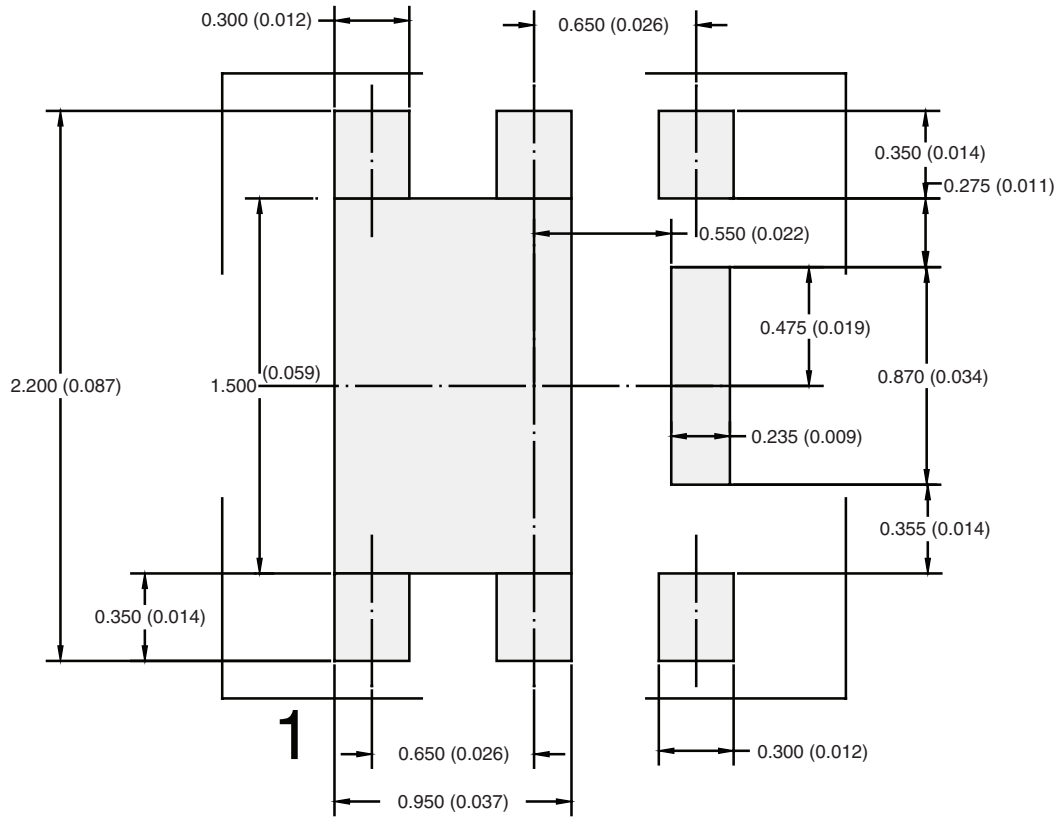


- Notes:  
 1. All dimensions are in millimeters  
 2. Package outline exclusive of mold flash and metal burr  
 3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

ECN: C-07431 – Rev. C, 06-Aug-07  
 DWG: 5934

## RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

[Return to Index](#)





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