Ordering number : ENA2145

LV56351HA

Bi-CMOS IC

1ch DC/DC boost converter

ON Semiconductor®

http://onsemi.com

Overview

LV56351HA integrates 1ch DC/DC boost converter and 1ch LDO. It is suitable as the power supply for BS/CS antennas of LCD/PDP TV and BD recorders that require automatic recovery without IC destruction and malfunction when the output is short-circuited.

Functions

[DC/DC boost converter]
- Soft-start time: 2.8ms
- Frequency 425kHz operation
- Pulse by pulse over current limiter
- Short circuit protector (SCP)

[LDO]
- Over current limiter (Fold back)

[All]
- Under voltage lockout
- Thermal shutdown protector
- Power good

Specifications

Maximum Ratings at Ta = 25°C

Parameter		Symbol	Conditions	Ratings	Unit
V_{CC} maximum supply voltage		V_{CC} max		-0.3 to 25	V
LDOIN maximum input voltage		V_{LDOIN} max		-0.3 to 30	V
SW maximum voltage		V_{SW} max		-0.3 to 30	V
Allowable power dissipation		Pd max	*1	1.45	W
Operating temperature		Topr		-30 to +85	°C
Operating junction temperature		Tjopr		-30 to +125	°C
Storage temperature		Tstg		-40 to +150	°C
Allowable pin voltage	V_{CC}, EN			25	V
	SW, LDOIN, LDOOUT			30	V
	IN1, IN2, FB, SCP, PGOOD, DDCTL			6	V

*1 Mounted on a specified board : 32mm × 38mm × 1.6mm, glass epoxy, double side board.

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
V_{CC} supply voltage	V_{CC}		8 to 23	V
LDOIN input voltage	V_{LDOIN}		8 to 28	V
SW voltage	V_{SW}		-0.3 to 28	V
EN voltage	V_{EN}		0 to 23	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 12V, V_{EN}=2V, LDOIN=16V, LDOOUT=15V

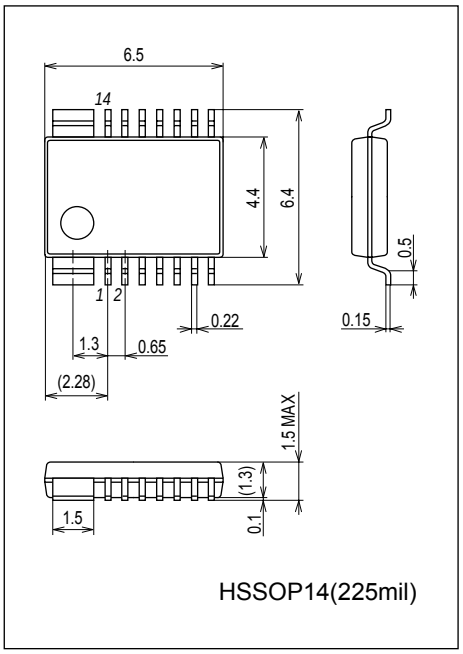
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
All						
Supply current1	I_{CC}	Switching is turned off		1.8	3.5	mA
Supply current2	I_{OFF}	EN = 0V			10	μA
Reference voltage	V_{REF}		1.2348	1.26	1.2852	V
Enable voltage	V_{EN}		2.0			V
Disable voltage	V_{DIS}				0.4	V
EN input current	I_{EN}	V_{EN} = 2.0V			10	μA
PGOOD threshold	VPG	IN1 ≥ VREF×85% and IN2 ≥ VREF×85%		VREF×0.85		V
PGOOD sink current	IPG	V_{PGOOD} = 0.5V		1.0		mA
PGOOD leak current	IPGLK	V_{PGOOD} = 2V			10	μA
UVLO on voltage	V_{UVLO}			7.0		V
Thermal shutdown temperature	T_{TSD}	*2	130			°C
TSD hysteresis	T_{HYS}	*2		30		°C
DC/DC boost converter						
FB output voltage "Low"	FB_{Low}	IN1 = 2.0V, I_{FB} = -20μA (Sink)			0.2	V
FB output voltage "High"	FB_{High}	IN1 = 0.2V, I_{FB} = 20μA (Source)	1.8			V
Soft-start time	T_{SS}			2.8		ms
Oscillator frequency	F_{OSC}			425		kHz
Max on duty	D_{MAX}		78	85	92	%
SW on resistance	R_{ON}			0.7		Ω
SW peak current	I_{PK}		1.5	1.8		A
SCP source current	I_{SCP}			4.8		μA
SCP threshold	V_{SCP}			VREF		V
DDCTL on voltage	$V_{DDCTLON}$	DC/DC Off	2.0			V
DDCTL off voltage	$V_{DDCTLOFF}$	DC/DC On			0.4	V
DDCTL input current	I_{DDCTL}	V_{DDCTL} = 2V			20	μA
LDO						
Maximum output current	I_{OMAX}		350	520	670	mA
Line regulation	R_{LN}	16V < LDOIN < 21V			20	mV
Load regulation	R_{LD}	10mA < I_O < 300mA			20	mV
Dropout voltage	V_{DROP}	I_O = 300mA		0.25	0.4	V
Short current	I_{SHORT}	LDOOUT = GND			100	mA

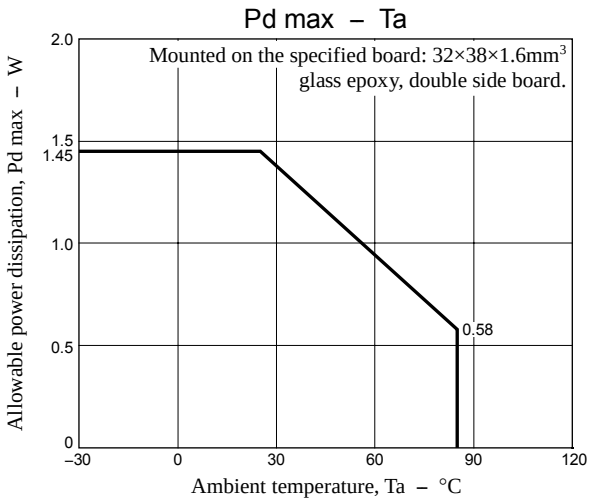
*2: Design guarantee value.

Package Dimensions

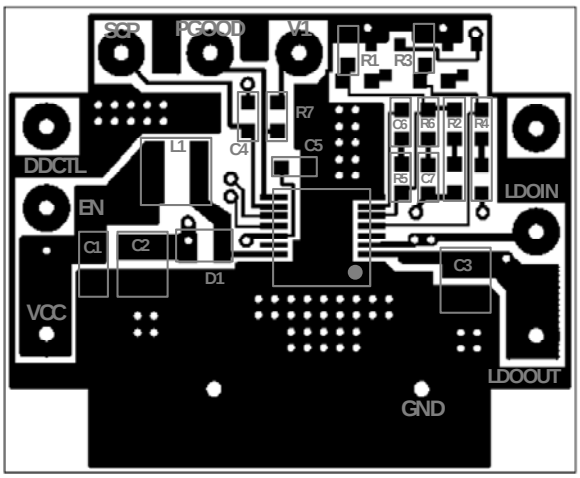
unit : mm (typ)

3313A

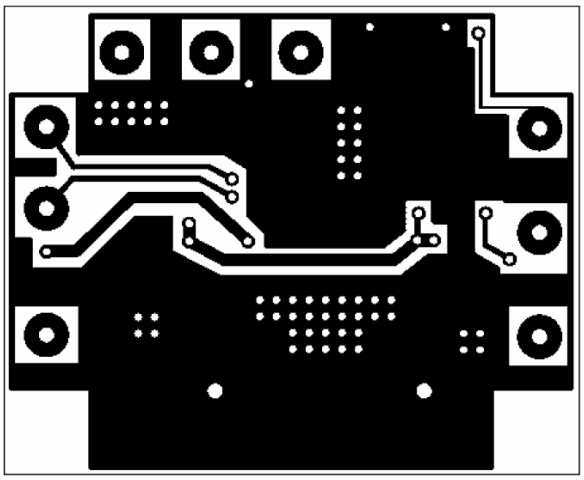




Specified board (32mm × 38mm × 1.6mm, glass epoxy, double side board)

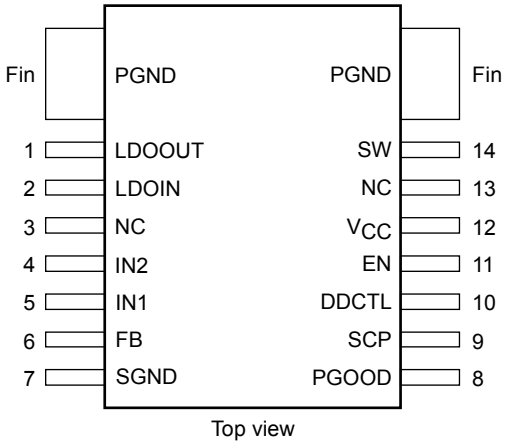


〈〈front〉〉



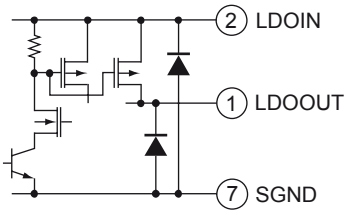
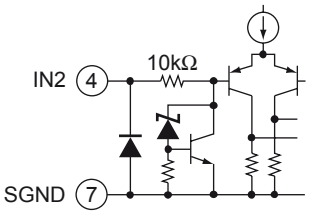
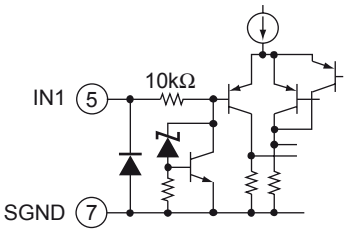
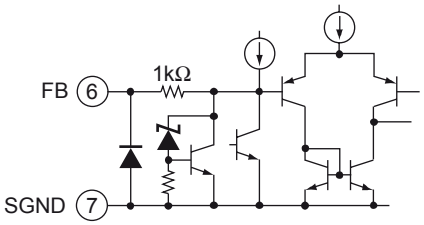
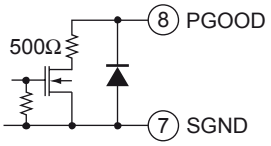
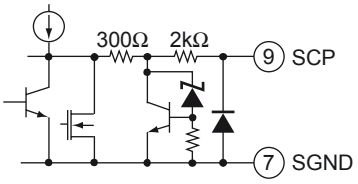
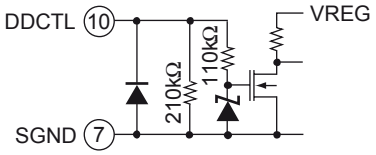
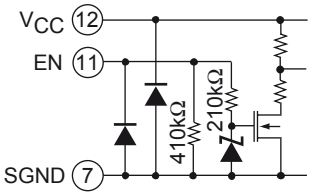
〈〈back〉〉

Pin assignment



Top view

Pin function

Pin No.	Pin name	Function	Equivalent circuit
1 2 7	LDOOUT LDOIN SGND	LDO output LDO input Signal ground (*3)	
4	IN2	LDO feedback input	
5	IN1	DC/DC error amplifier input	
6	FB	DC/DC error amplifier output	
8	PGOOD	Power good output	
9	SCP	DC/DC SCP capacitor connect pin for timer setting	
10	DDCTL	DC/DC on and off control	
11 12	EN V_{CC}	Enable Power supply	

*3: When you use this IC, Please short-circuit all the pins of SGND and PGND on the IC mounting side.

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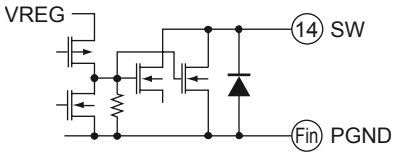
Pin No.	Pin name	Function	Equivalent circuit
14	SW	DC/DC open drain output	
Fin	PGND	Power ground (*3)	

*3: When you use this IC, Please short-circuit all the pins of SGND and PGND on the IC mounting side.

Function overview

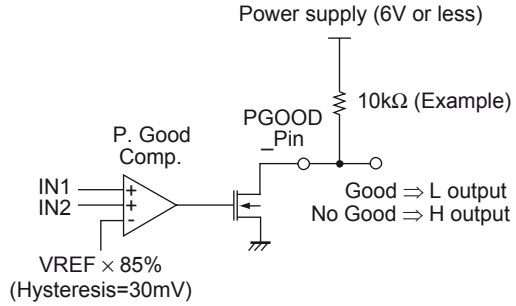
(1) UVLO (Under Voltage Lockout)

UVLO stops outputs of both DC/DC and LDO to prevent malfunction when V_{CC} decreases. UVLO operates when V_{CC} falls below the UVLO voltage. This function is a non-latch-type, and recovers these outputs automatically when V_{CC} exceeds the UVLO voltage.

(2) Power good

Power good notifies that the output voltages of DC/DC and LDO are within the range of the setting voltage. The two output voltages are monitored through the voltage of IN1 and IN2. The output is judged to be “power good” when both outputs are 85% or higher compared to the setting voltages. If either IN1 or IN2 voltage falls below VREF×85%, PGOOD output becomes L → H (No Good). When IN1 and IN2 voltages become (VREF×85%) + 30mV or higher, PGOOD output becomes H → L (Good). During soft start, the output is H (No Good).

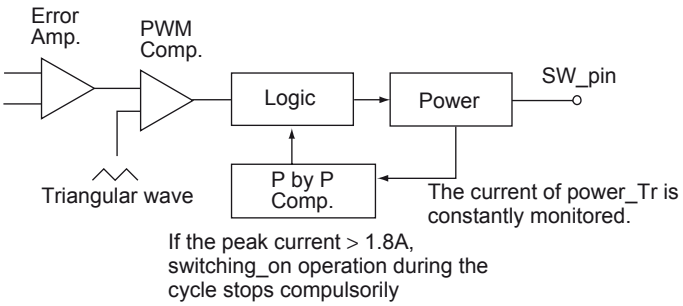
⟨⟨Power good circuit diagram⟩⟩



(3) Pulse-by-Pulse over current protection (P by P)

The P by P stops switch-on operation of a certain cycle by force when the current of power MOSFET reaches the maximum output peak current.

⟨⟨P by P circuit diagram⟩⟩



(4) Short Circuit Protector (SCP)

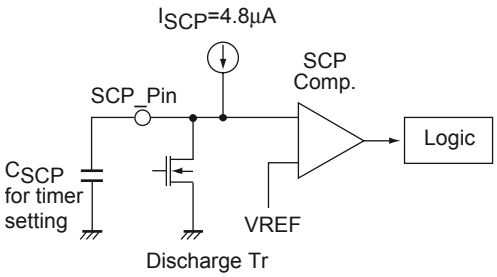
When output voltage of DC/DC decreases due to short-circuit; for example, SCP latches off the outputs of DC/DC and LDO by timer.

When output voltage of DC/DC decreases and FB turns to H, which is the error amplifier output, charge at 4.8μA constant current starts to SCP capacitor for timer setting. When SCP voltage exceeds the threshold voltage (=VREF), latch-off occurs. If the output voltage recovers until the time the SCP voltage reaches to the threshold voltage, SCP capacitor is discharged and timer is reset. To restart the output after latch-off, you need to input EN signal again. If you do not use the SCP function, make sure to short SCP and GND.

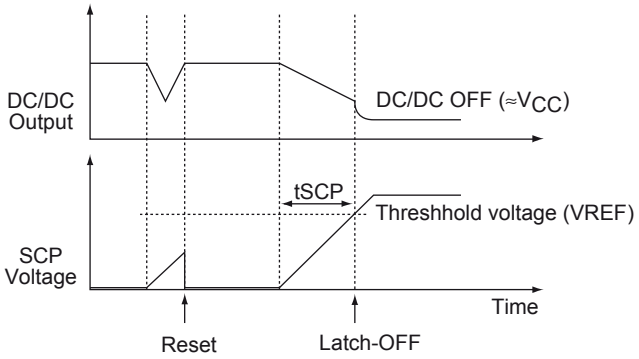
To define timer, you need to calculate a value of SCP capacitor using the following formula because timer (tSCP) depends on capacitance.

$$C_{SCP} = (I_{SCP} \times tSCP)/VREF$$

〈〈SCP circuit diagram〉〉



〈〈Waveform of SCP_Pin〉〉



(5) DC/DC on and off control

This function controls on and off of DC/DC during the operation of IC.

〈〈Turning on DC/DC〉〉

Where DDCTL = Low or open, DC/DC and LDO operate at the same time.

〈〈Turning off DC/DC〉〉

Where DDCTL = High, DC/DC is compulsorily stopped and only LDO operates.

When DDCTL is switched from H to L (or open), LDO stops temporarily and DC/DC starts with soft start and then LDO restart. If you switch DDCTL during IC operation, make sure that the output waveforms of DC/DC and LDO are normal.

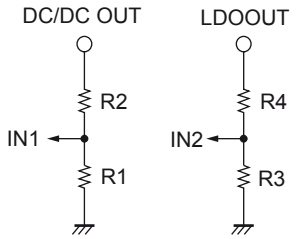
Output voltage setting

Output voltages are given by the following formulas.

DCDCOUT = (1+R2/R1) × VREF [V]

LDOOUT = (1+R4/R3) × VREF [V]

〈〈Resistance for output setting〉〉

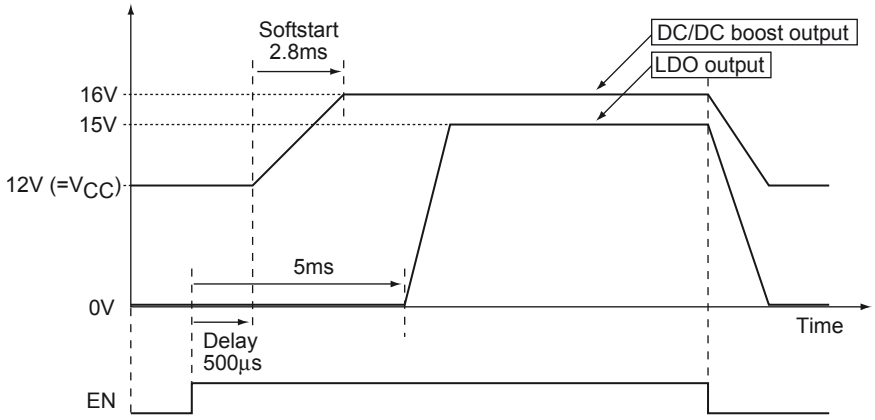


Start and stop

Start: Make sure to input EN signal (L ⇒ H) after supplying V_{CC} = 12V.

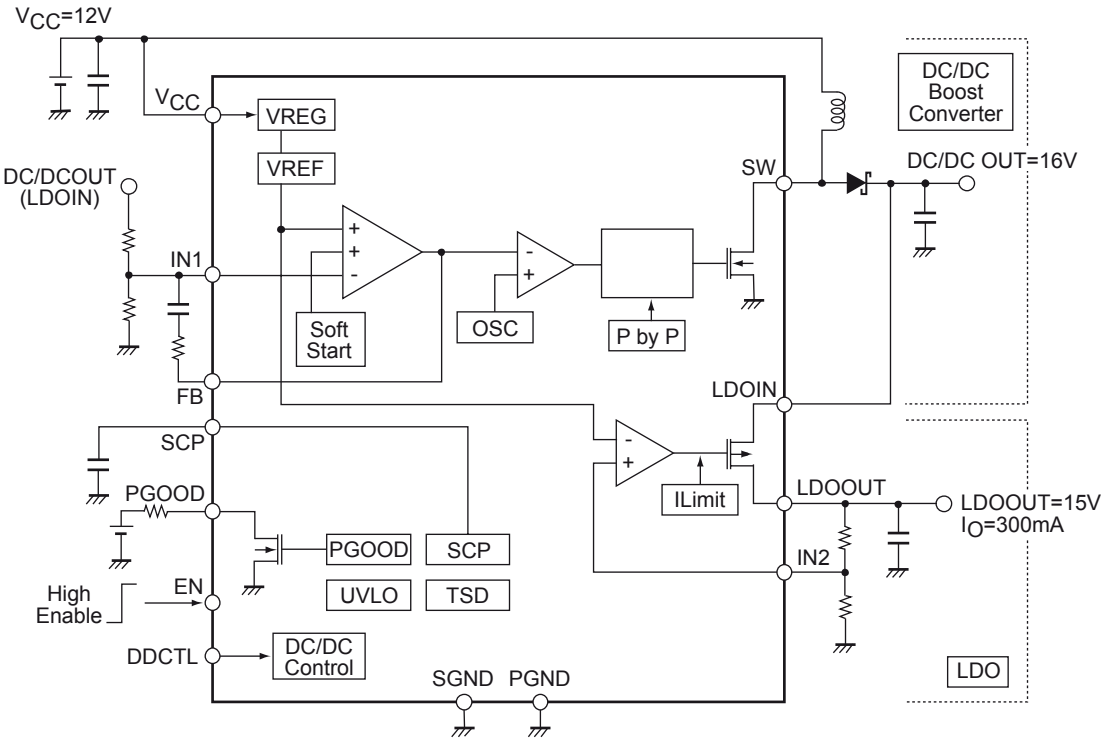
Stop: Reverse-operation of start.

〈〈Output waveform during start and stop〉〉



Block diagram and Application circuit 1 (for BS antenna)

Condition: V_{CC} = 12V, DCDCOUT = 16V, LDOOUT = 15V



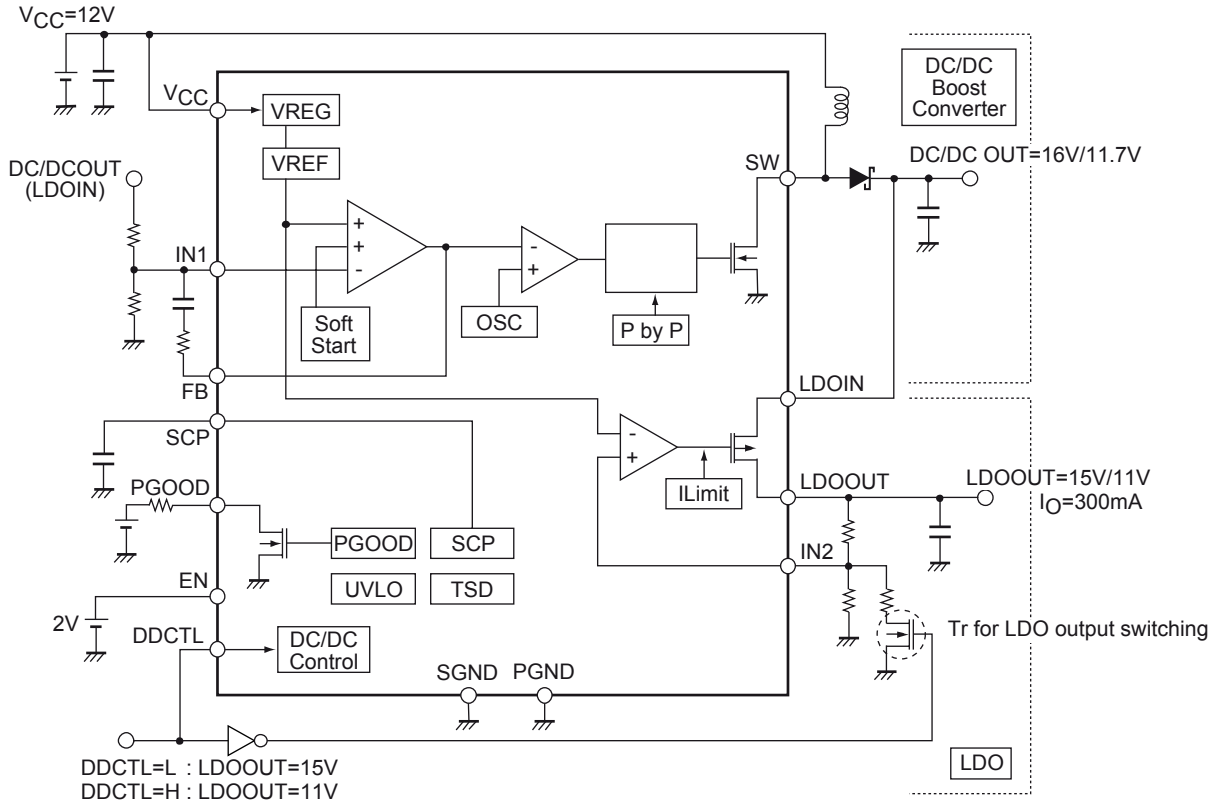
〈〈Note〉〉

When LDOOUT is in the over current state or the short-circuit state, IC and external parts are protected by over current limiter of LDO. And when DC/DCOUT is short-circuited, IC stops by timer latch-off type SCP function.

Application circuit 2 (for BS/CS antenna)

BS condition: V_{CC} = 12V, DCDCOUT = 16V, LDOOUT = 15V

CS condition: V_{CC} = 12V, DCDC = OFF, LDOOUT = 11V

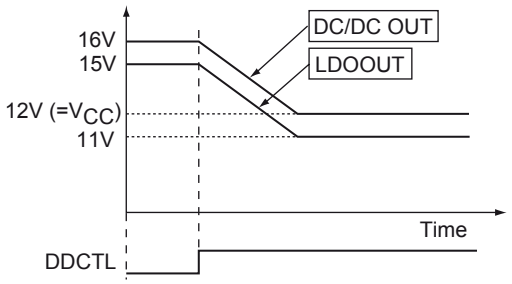


〈〈Addition〉〉

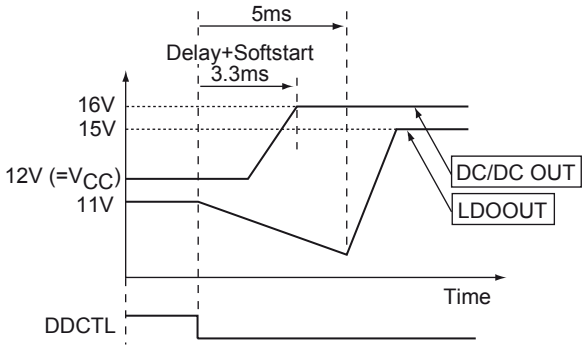
The above application circuit enables switching between 15V for BS and 11V for CS.
Where DDCTL=L, DC/DC booster is turned on and set as follows: DC/DCOUT=16V, LDOOUT=15V
Where DDCTL=H, DC/DC booster is turned off and set as follows: DC/DCOUT=11.7V, LDOOUT=11V
(because the resistance value of output setting of LDO is switched)

〈〈Output waveform at switching〉〉

LDOOUT = 15V ⇒ 11V



LDOOUT = 11V ⇒ 15V



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