MTCH810

Haptics Controller

Description

The MTCH810 provides an easy way to add Haptic feedback to any button/sliders capacitive touch interface. The device integrates a single-channel Haptic driver output with an industry standard I^{2}C™ slave interface to create a simple Haptic feedback peripheral.

Features

- Internal Library of Effects:
  - 14 Haptic effect commands
  - Firmware revision query command
  - Abort Playback command
- I^{2}C Control Interface:
  - 7-bit Addressing mode (address = 0x10)
  - Supports 100 kHz and 400 kHz transfer rate
- Wide Operating Voltage: 2.3V-5.5V
- Minimal Number of External Components
- Low-Power Consumption when Idle
- Operating Temperature: -40˚C to +85˚C

Package Type

The device is only offered in an 8-pin 3x3 DFN package (see Figure 1).
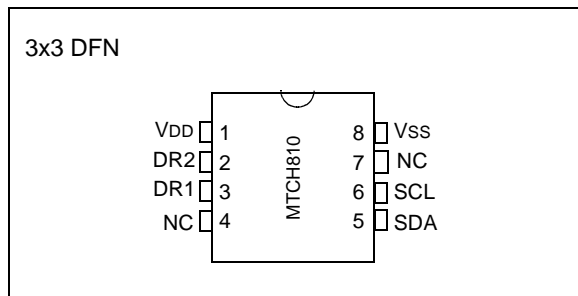
FIGURE 1:   8-PIN DFN DIAGRAM FOR MTCH810

TABLE 1:   8-PIN DFN PINOUT DESCRIPTION

Name	8-Pin DFN	Description
VDD	1	Power supply input
DR2	2	Drive output 2
DR1	3	Drive output 1
NC	4	No connection
SDA	5	I^{2}C™ Data
SCL	6	I^{2}C™ Clock
NC	7	No connection
VSS	8	Ground

Pin Description

DR1

This is the non-inverting PWM Haptics drive output. It should be connected to the non-inverting input of a Haptic driver circuit designed for Eccentric Rotating Mass Actuators (ERMs).

DR2

It should be connected to the inverting input of a Haptic driver circuit designed for ERM Actuators.

SDA

This pin is the serial data connection of the I^{2}C interface. It should be connected to the I^{2}C master SDA signal with a pull-up resistor to VDD.

SCL

This pin is the serial clock connection of the I^{2}C interface. It should be connected to the I^{2}C master SCL signal with a pull-up resistor to VDD.

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1.0   DEVICE OVERVIEW

The Microchip mTouch™ technology MTCH810 Haptics feedback controller provides an easy way to add tactile feedback to any application. The device implements all the digital functions for a Haptics feedback system. The Haptic effects are designed to provide feedback for a "Button and Slider" type capacitive touch interface. When combined with an analog power driver and an Eccentric Rotating Mass (ERM) style actuator, the resulting circuit comprises a complete tactile feedback Haptic system.

The device is controlled through an I^2C slave interface. In response to a two-byte command, the MTCH810 (in combination with the driver and ERM) generates one of 13 different Haptic vibration effects. The effects are 180-220 Hz vibrations with different amplitude envelopes and durations. The effects create a variety of different 'feels' to provide feedback for different capacitive touch commands, status and error conditions. Several effects are similar with different power levels in order to allow the users to compensate for the variations in the coupling of the vibrations to the user's finger tip.

Two additional commands allow the termination of an effect early and the ability to read the effects table revision.

1.1   Communications

• I^2C, Slave mode

1.2   Drive Outputs

• DR1 is a dedicated PWM output
• DR2 is a dedicated inverted PWM output

1.3   PWM Resolution

• 10 bits

1.4   Pin Description

1.4.1   DR1

This is the enable/non-inverting digital PWM Haptics drive output. It should be connected to the non-inverting input of a Haptic power driver circuit design for ERM actuators. The PWM output should only be active when an effect is in progress.

1.4.2   DR2

This is the inverting digital PWM Haptics driver output. It should be connected to the inverting input of a Haptic power driver circuit designed for ERM actuators. The PWM output should only be active when an effect is in progress.

1.4.3 I^2C – SERIAL DATA PIN (SDA)

The SDA pin is the serial data pin of the I^2C interface. The SDA pin is used to write or read the registers and Configuration bits. The SDA pin is an open-drain N-channel driver. Therefore, it needs an external pull-up resistor from the VDD line to the SDA pin. Except for the Start and Stop conditions, the data on the SDA pin must be stable during the high period of the clock. The high or low state of the SDA pin can only change when the clock signal on the SCL pin is low. Refer to **Section 2.1.2 "I^{2}C Operation"** for more details on the I^2C serial interface communication.

1.4.4 I^2C – SERIAL CLOCK PIN (SCL)

The SCL pin is the serial clock pin of the I^2C interface. The I^2C interface only acts as a slave and the SCL pin accepts only external serial clocks. The input data from the master device is shifted into the SDA pin on the rising edges of the SCL clock, and the output from the device occurs at the falling edges of the SCL clock. The SCL pin is an open-drain N-channel driver. Therefore, it needs an external pull-up resistor from the VDD line to the SCL pin. Refer to Section **Section 2.1.2 "I^{2}C Operation"** for more details on I^2C serial interface communication. For more details, see Figure 1-1 and Table 1-1.

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1.4.4.1 Clock Stretching

A feature of the SCL pin is clock stretching. This allows the I^2C slave to hold communications at the end of each byte from the master. Its purpose is to allow the slave sufficient time to process the data before the next byte is sent. It accomplishes the clock hold by turning on the open-drain output, holding the clock line low. This prevents the master from starting the transmission of the next byte in the packet. For proper operation, the I^2C master must be capable of recognizing a clock stretch condition, and suspending transmission until the MTCH810 releases the SCL pin.

> **Note:** The MTCH810 includes a time-out function on the clock stretching function that will reset the I^2C interface in the event that the I^2C interface hangs in a clock stretch condition.

1.5 Haptic Commands

The commands are transmitted via the I^2C serial interface as a Start condition, address plus write bit, two successive bytes and a Stop condition. For the effect table revision number, the Write command is followed by an I^2C read of two bytes. Table 2-2 and Table 2-3 list all the commands supported by the MTCH810.

1.6 Hardware

To build a complete Haptic system, the two digital PWM outputs must be filtered to produce a DC drive signal, and amplified to produce a minimum of 300 mA of drive at 3V. This output is then used to drive an ERM actuator. Figure 1-1 below shows a typical controller, driver and actuator combination for a Haptic system.

The MTCH810 is the controller in the system, accepting I^2C commands and generating the appropriate PWM signals to create the Haptic effect. The outputs from the MTCH810 are then filtered and amplified by the DRV8601. The amplifier stage is essentially an audio frequency amplifier configured for differential inputs and outputs. The output of the amplifier then drives the ERM.

The RC network in the feedback path provides a pole in the transfer function at 160 Hz to roll off the high frequency gain and attenuate the ripple at the PWM frequency. The connection between the DR1 output and the enable of the amplifier allows the controller to generate an output for the ERM with a drive/coast format, rather than a drive/brake control. Using a differential output eliminates the need for a large capacitor on the output to AC couple the drive signal to the ERM.

> **Note:** Any audio frequency drive circuits will work in the application, provided it can supply 300 mA at 3V and turn on in less than 1 mS. Amplifiers with built-in "click and pop" elimination have soft-start enables which have a turn on time of >10 mS and are not suitable for a Haptic driver.

Table 1-1 lists the qualified ERM actuators and their manufacturers.

TABLE 1-1: APPROVED ACTUATORS AND SPECIFICATIONS

Actuator	Dimensions (mm)	Rated Voltage	Haptic Transient Overdrive Voltage	Impedance
Nidec NRS-3388i	4.6 ± 0.2D 15.6 ± 0.9L	1.3V ± 0.2V	3.3V	10.6Ω ± 20%
Johnson Electric 1999-1MB0037EP	6.0H x 8.0W 21.5L	4.5V	5.0V	10Ω - typical

FIGURE 1-1: TYPICAL SCHEMATIC
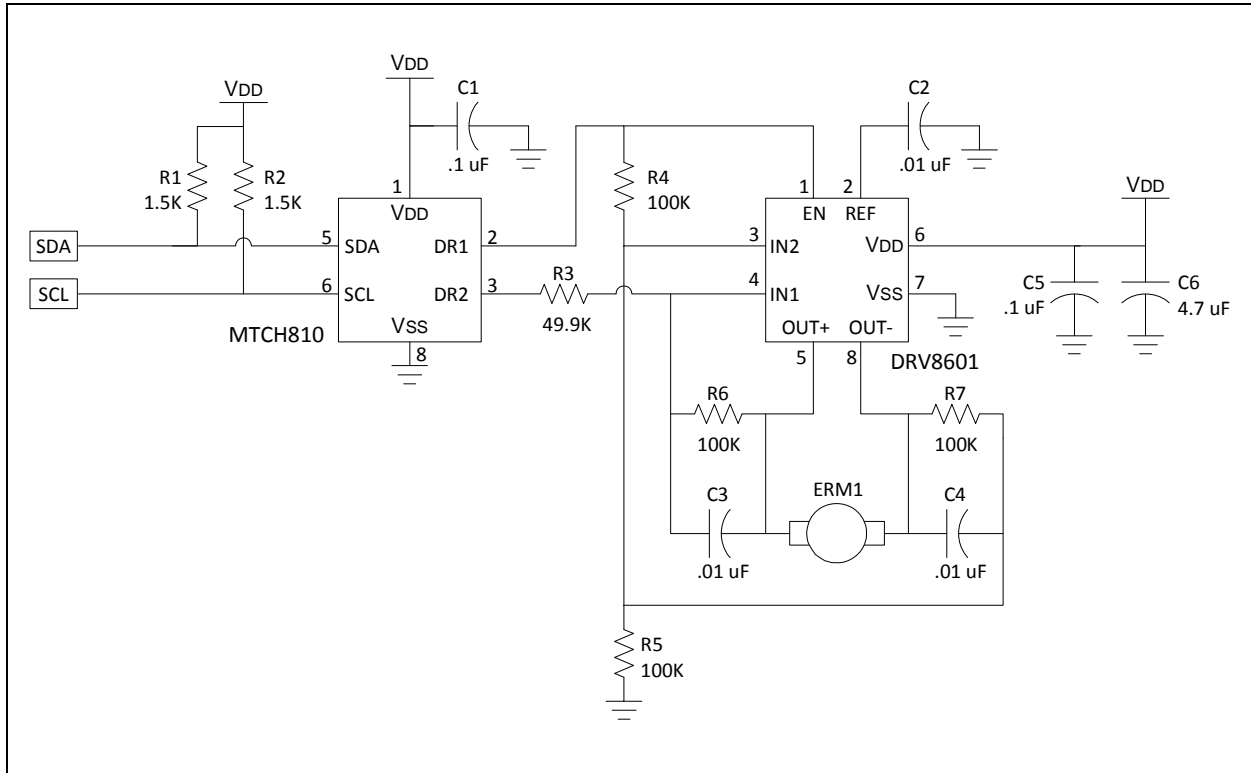
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2.0   I^{2}C™ SERIAL INTERFACE

This device supports the I^{2}C serial protocol. The I^{2}C module operates in Slave mode, so it does not generate the serial clock.

2.1   Overview

This I^{2}C interface is a two-wire interface. Figure 2-1 shows a typical I^{2}C Interface connection.

The I^{2}C interface specifies different communication bit rates. These are referred to as Standard, Fast or High Speed modes. The MTCH810 device supports these three modes. The bit rates of these modes are:

- Standard mode: Bit Rates up to 100 kbit/s
- Fast mode: Bit Rates up to 400 kbit/s

A device that sends data onto the bus is defined as a transmitter, and a device receiving data is defined as a receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access and generates the Start and Stop conditions. The MTCH810 device works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated. Communication is initiated by the master (microcontroller) which sends the Start bit, followed by the slave address byte. The first byte transmitted is always the slave address byte, which contains the device code, the address bits and the R/$\overline{\text{W}}$ bit.

FIGURE 2-1:   TYPICAL I^{2}C™ INTERFACE
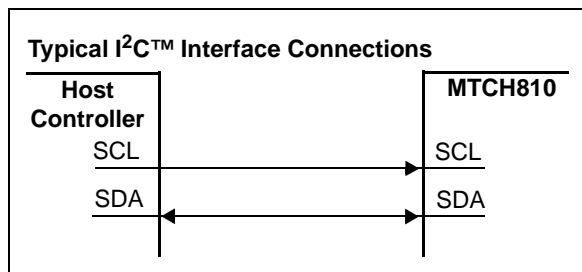
The I^{2}C serial protocol only defines the field types, field lengths, timings, etc. of a frame. The frame content defines the behavior of the device. For details on the frame content (commands/data) refer to **Section 2.3 "I2C Commands"**.

Refer to the *NXP User Manual* (UM10204_3) for more details on the I^{2}C specifications.

2.1.1   SIGNAL DESCRIPTIONS

The I^{2}C interface uses up to two pins (signals). These are:

- SDA (Serial Data) (see **Section 1.4.3 "I2C – Serial Data Pin (SDA)"**)
- SCL (Serial Clock) (see **Section 1.4.4 "I2C – Serial Clock Pin (SCL)"**)

2.1.2   I^{2}C OPERATION

The MTCH810 device I^{2}C module is compatible with the NXP I^{2}C specification. The following lists some of the module's features:

- 7-bit Slave Addressing
- Supports Three Clock Rate modes:
   - Standard mode, clock rates up to 100 kHz
   - Fast mode, clock rates up to 400 kHz
- Support Multi-Master Applications

The I^{2}C 10-bit addressing mode is not supported.

The NXP I^{2}C specification only defines the field types, field lengths, timings, etc. of a frame. The frame content defines the behavior of the device. The frame content for this device is defined in **Section 2.3 "I2C Commands"**.

### 2.1.3   I^{2}C BIT STATES AND SEQUENCE

Figure 2-8 shows an I^{2}C 8-bit transfer sequence, while Figure 2-7 shows the bit definitions. The serial clock is generated by the master. The following definitions are used for the bit states:

- Start bit (S)
- Data bit
- Acknowledge (A) bit (driven low)/ No Acknowledge ($\overline{\text{A}}$) bit (not driven low)
- Repeated Start bit (Sr)
- Stop bit (P)

2.1.4   START BIT

The Start bit (see Figure 2-2) indicates the beginning of a data transfer sequence. The Start bit is defined as the SDA signal falling when the SCL signal is high.
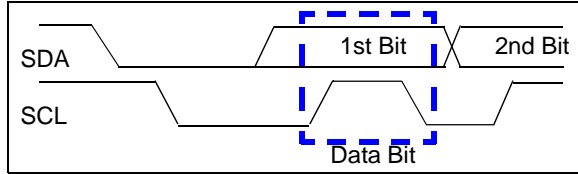
FIGURE 2-2:   START BIT

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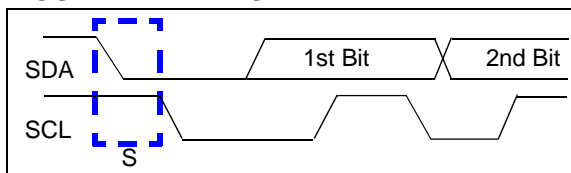
2.1.5 DATA BIT

The SDA signal may change state while the SCL signal is low. While the SCL signal is high, the SDA signal MUST be stable (see Figure 2-3).

FIGURE 2-3: **DATA BIT**

2.1.6 ACKNOWLEDGE (A) BIT

The A bit (see Figure 2-4) is typically a response from the receiving device to the transmitting device. Depending on the context of the transfer sequence, the A bit may indicate different things. Typically, the slave device will supply an A response after the Start bit and eight data bits have been received. An A bit has the SDA signal low.

FIGURE 2-4: **ACKNOWLEDGE WAVEFORM**
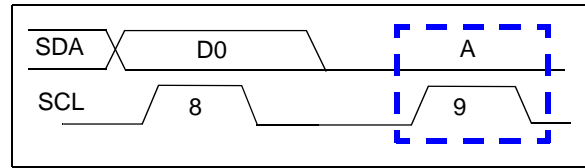
2.1.7 NOT A ($\overline{A}$) RESPONSE

The $\overline{A}$ bit has the SDA signal high. Table 2-1 shows the conditions where the slave device will issue a Not A ($\overline{A}$).

TABLE 2-1: **MTCH810 A / $\overline{A}$ RESPONSES**

| Event	Acknowledge Bit Response	Comment
General Call	$\overline{A}$	
Slave Address valid	A	
Slave Address not valid	$\overline{A}$	
Bus Collision	N/A	Treated as "Don't Care" if the collision occurs on the Start bit. Otherwise, I2C™ resets.

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2.1.8 REPEATED START BIT

The Repeated Start bit (see Figure 2-5) indicates that the current master device wishes to continue communicating with the current slave device without releasing the I^{2}C bus. The Repeated Start condition is the same as the Start condition, except that the Repeated Start bit follows a Start bit (with the Data bits + A bit) and not a Stop bit.

The Start bit is the beginning of a data transfer sequence and is defined as the SDA signal falling when the SCL signal is high.

> **Note 1:** A bus collision during the Repeated Start condition occurs if:
> - SDA is sampled low when SCL goes from low-to-high.
> - SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data '1'.

FIGURE 2-5: **REPEAT START CONDITION WAVEFORM**
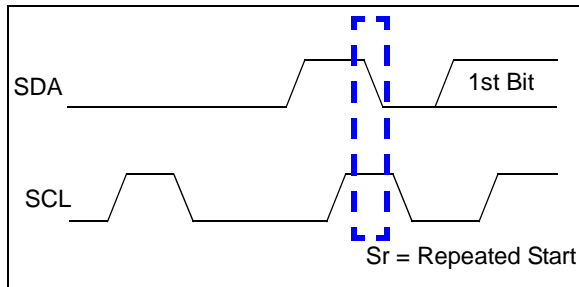
2.1.9 STOP BIT

The Stop bit (see Figure 2-6) indicates the end of the I^{2}C data transfer sequence. The Stop bit is defined as the SDA signal rising when the SCL signal is high.

A Stop bit resets the I^{2}C interface of the MTCH810 device.

FIGURE 2-6: **STOP CONDITION RECEIVE OR TRANSMIT MODE**
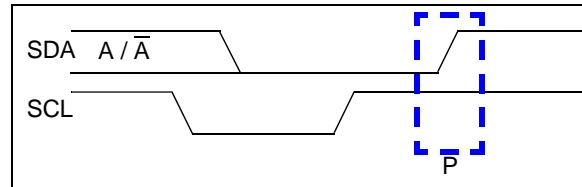
2.1.9.1 Aborting a Transmission

If any part of the I^{2}C transmission does not meet the command format, it is aborted. This can be intentionally accomplished with a Start or Stop condition. This is done so that noisy transmissions (usually an extra Start or Stop condition) are aborted before they corrupt the device.
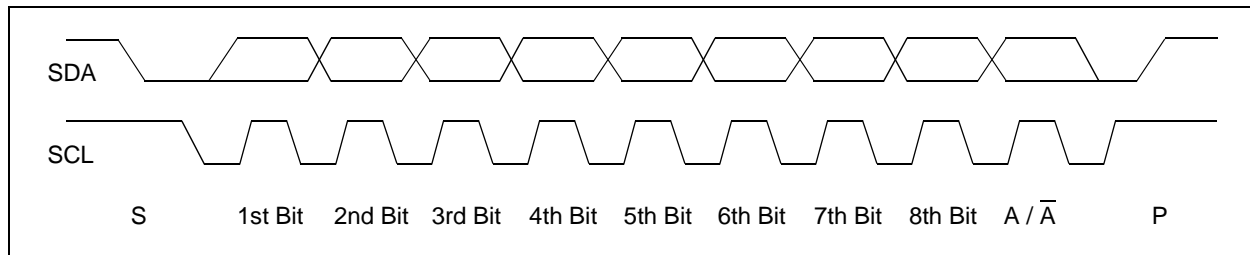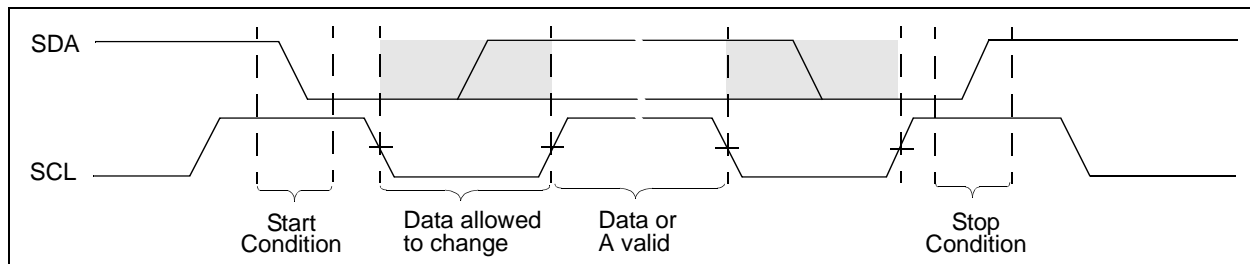
FIGURE 2-7: **TYPICAL 8-BIT I^{2}C™ WAVEFORM FORMAT**

**FIGURE 2-8:** **I^{2}C™ DATA STATES AND BIT SEQUENCE**

2.1.9.2 Device Addressing

The address byte is the first byte received following the Start condition from the master device. The full seven bits of the I²C slave address is "0010000".

Figure 2-9 shows the I²C slave address byte format, which contains the seven address bits and a Read/Write (R/$\overline{W}$) bit.

FIGURE 2-9: **SLAVE ADDRESS BITS IN THE I²C™ CONTROL BYTE**

Note 1: Address Bits (A6:A0) can be reprogrammed by the customer.
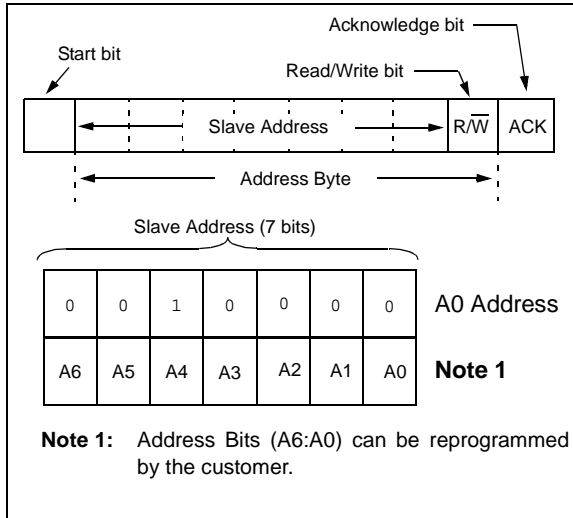
2.2 Device Commands

This section documents the commands that the device supports.

The commands can be grouped into the following categories:

• Effect Commands
• Revision and Control Commands

TABLE 2-2: **EFFECT COMMANDS**

Index	I²C™ Message	Haptic Effect Description
0	0x00 0x00	Strong click
1	0x01 0xFF	Med. strong click 60%
2	0x02 0xFE	Low strong click 30%
3	0x03 0xFD	Sharp click
4	0x04 0xFC	Sharp click 60%
5	0x05 0xFB	Sharp click 30%
6	0x06 0xFA	Soft bump
7	0x07 0xF9	Med. soft bump 60%
8	0x08 0xF8	Soft bump 30%
9	0x09 0xF7	Double click
10	0x0A 0xF6	Double click 60%
11	0x0B 0xF5	Triple click
12	0x0C 0xF4	Soft buzz
13	0x0D 0xF3	Strong buzz

TABLE 2-3: **REVISION AND CONTROL COMMANDS**

Index	I²C™ Message	Haptic Effect Description
14	0x0E 0xF2	Read effect library version number
15	0x0F 0xF1	Abort effect playback

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2.3 I²C COMMANDS

The I²C protocol does not specify how commands are formatted, so this section specifies the MTCH810 device I²C command formats and operation.

The commands can be grouped into the following categories:

- Effect Commands
- Revision and Control Commands

The supported commands are shown in Table 2-2 and Table 2-3.

2.3.1 EFFECT COMMANDS

Effect commands are used to initiate a specific Haptic effect. The command consists of two bytes which are the XOR of one another. The effect begins with the completion of the I²C Stop condition.

2.3.2 REVISION AND CONTROL COMMANDS

Revision and Control commands are used to either retrieve the current revision of the effects table within the controller, or to terminate early a Haptic effect. Just like the Effect commands, the command codes are two's compliments of one another. The Terminate-early command is executed at the completion of the I²C Stop condition. When the Revision command is sent, the controller then formats the revision data and waits for an I²C read from the master.

2.3.3 ABORTING A COMMAND TRANSMISSION

A Restart or Stop condition in an expected data bit position will abort the current command sequence and data will not be written to the MTCH810. Write commands are automatically aborted if the binary XOR checksum is not valid.

2.3.4 WRITE COMMAND (NORMAL AND HIGH VOLTAGE)

The format of the command is shown in Figure 2-10. The MTCH810 generates the A / $\overline{A}$ bits.

A Write command will only start a write cycle after a properly formatted Write command has been received and the Stop condition has occurred.

FIGURE 2-10: WRITE RANDOM ADDRESS COMMAND
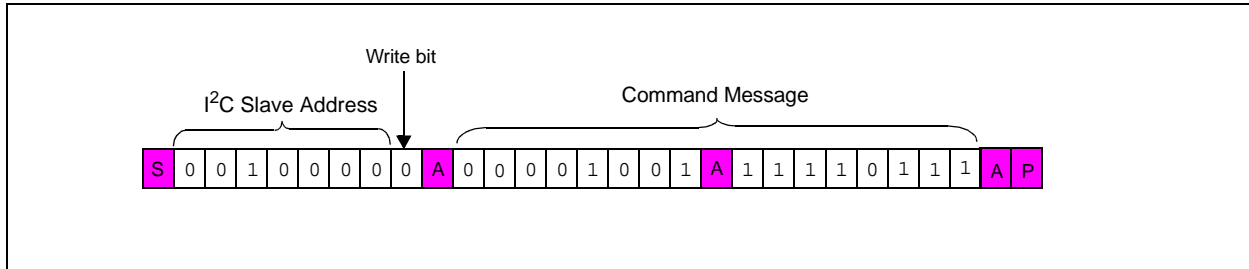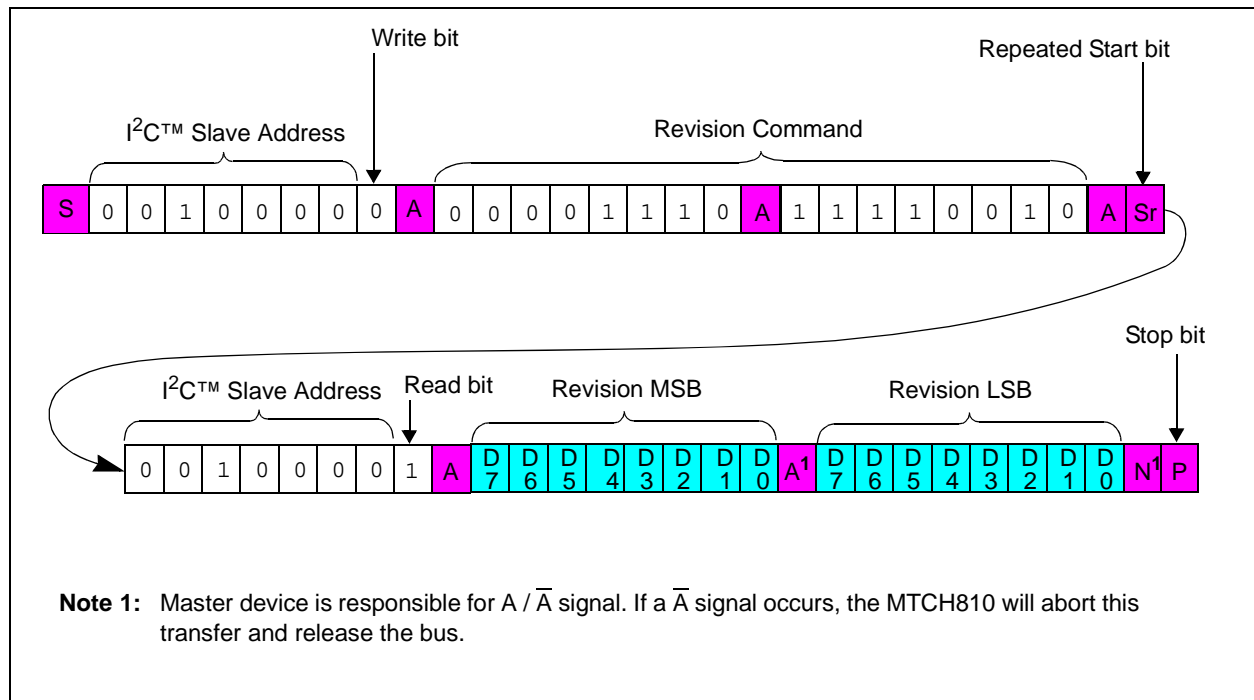
2.3.5 REVISION COMMAND

The format of the Revision command (see Figure 2-11) includes the Start condition, I²C control byte (with R/$\overline{W}$ bit set to 0), A bit, the first command byte, A bit, followed by the two's compliment of the command byte, a Repeated Start bit, I²C control byte (with R/$\overline{W}$ bit set to 1) and the MTCH810 device transmitting the requested data bytes one at a time, until the master sends a Stop condition.

The I²C control byte requires the R/$\overline{W}$ bit to be equal to a logic one (R/$\overline{W}$ = 1) in order to generate a read sequence. The data read will start with the Most Significant Byte (MSB) of the revision date and automatically increment to the next byte after each byte request. The sequence is ended with the master generating a Stop or Restart condition. Figure 2-11 shows the waveforms for a single read.

2.3.5.1 Ignoring an I²C Transmission and "Falling Off" the Bus

The MTCH810 device expects to receive complete, valid I²C commands and will assume that any command not defined as a valid command is due to a bus corruption and will enter a passive high condition on the SDA signal. All signals will be ignored until the next valid Start condition and control byte are received.

FIGURE 2-11: READ REVISION COMMAND

Note 1: Master device is responsible for A / $\overline{A}$ signal. If a $\overline{A}$ signal occurs, the MTCH810 will abort this transfer and release the bus.

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3.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings[†]

Ambient temperature under bias .... -40°C to +125°C

Storage temperature .... -65°C to +150°C

Voltage on V_{DD} with respect to V_{SS} .... -0.3V to +4.0V

Voltage on all other pins with respect to V_{SS} .... -0.3V to (V_{DD} + 0.3V)

Total power dissipation[1] ....800 mW

Maximum current out of V_{SS} pin, -40°C ≤ T_A ≤ +85°C for industrial .... 85 mA

Maximum current into V_{DD} pin, -40°C ≤ T_A ≤ +85°C for industrial .... 80 mA

Clamp current, I_K (V_{PIN} < 0 or V_{PIN} > V_{DD}) .... ± 20 mA

Maximum output current sunk by any DR pin ....25 mA

Maximum output current sourced by any DR pin ....25 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$.

> **† NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
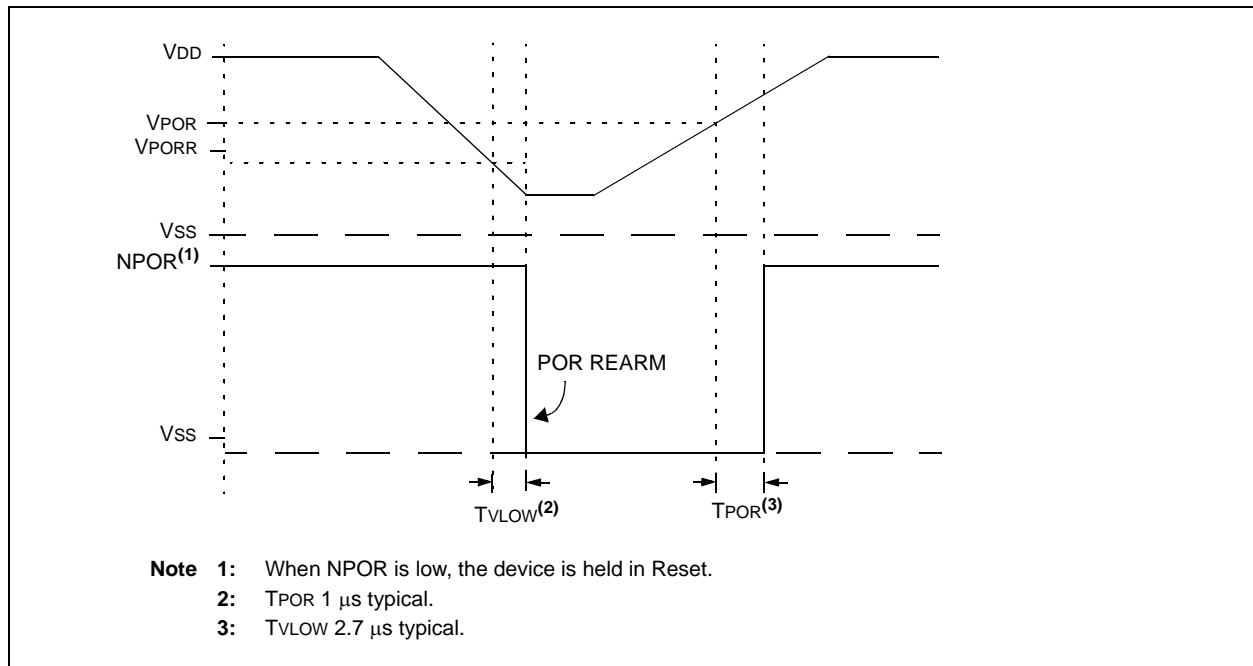
3.1 DC Characteristics: MTCH810

MTCH810			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
Param. No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
D001	VDD	**Supply Voltage**	1.8	—	3.6	V	
D002 D003	VPOR*	**Power-on Reset Release Voltage**	—	1.6	—	V	
	VPORR*	**Power-on Reset Rearm Voltage**	—	0.8	—	V	Device in Sleep mode
D004*	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	

*   These parameters are characterized but not tested.

†   Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

FIGURE 3-1:   POR AND POR REARM WITH SLOW RISING VDD

Note 1: When NPOR is low, the device is held in Reset.
   2: TPOR 1 µs typical.
   3: TVLOW 2.7 µs typical.

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3.2 DC Characteristics: MTCH810-I/E

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature-40°C $\leq$ TA $\leq$ +85°C for industrial				
Param. No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
	VIL	**Input Low Voltage**					
		DR PORT:					
D030A		with TTL buffer	—	—	0.15 VDD	V	1.8V $\leq$ VDD $\leq$ 3.6V
D031		with I²C™ levels	—	—	0.3 VDD	V	
	VIH	**Input High Voltage**					
		DR Ports:					
D040A		with TTL buffer	0.25 VDD + 0.8	—	—	V	1.8V $\leq$ VDD $\leq$ 3.6V
D041		with I²C™ levels	0.7 VDD	—	—	V	
	IIL	**Input Leakage Current[1]**					
D060		DR Ports	—	± 5	± 125	nA	VSS $\leq$ VPIN $\leq$ VDD, Pin at high-impedance at 85°C
			—	± 5	± 1000	nA	125°C
	VOL	**Output Low Voltage[3]**					
D080		DR Ports	—	—	0.6	V	IOL = 6 mA, VDD = 3.3V IOL = 1.8 mA, VDD = 1.8V
	VOH	**Output High Voltage[3]**					
D090		DR Ports	VDD - 0.7	—	—	V	IOH = 3 mA, VDD = 3.3V IOH = 1 mA, VDD = 1.8V
		Capacitive Loading Specs on Output Pins					
D101A*	CIO	All DR pins	—	—	50	pF	

*   These parameters are characterized but not tested.

†   Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Negative current is defined as current sourced by the pin.

    2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

    3: Including OSC2 in CLKOUT mode.

FIGURE 3-2: **LOAD CONDITIONS**

Load Condition

Pin

CL

Vss

Legend: CL = 50 pF for all pins
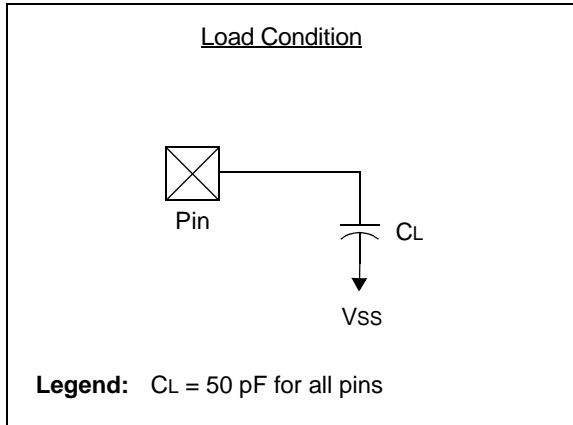
TABLE 3-1: **DR TIMING PARAMETERS**

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
OS18*	TioR	DR output rise time	— —	90 55	140 80	ns	VDD = 1.8V VDD = 3.0-3.6V
OS19*	TioF	DR output fall time	— —	60 44	80 60	ns	VDD = 1.8V VDD = 3.0-3.6V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated.

MTCH810

FIGURE 3-3: **BROWN-OUT RESET TIMING AND CHARACTERISTICS**
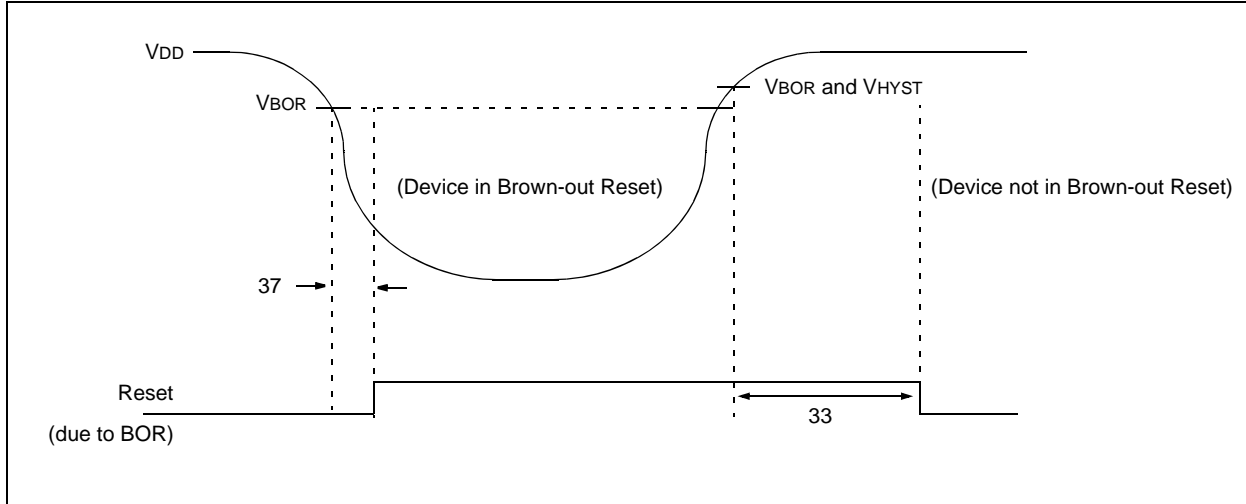
TABLE 3-2: **RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET PARAMETERS**

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
31	TWDTLP	Watchdog Timer Time-out Period	205	256	305	ms	VDD = 1.8V-3.6V, 1:1 Prescaler used
33*	TPWRT	Power-up Timer Period	40	65	140	ms	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 3-4: **I²C™ BUS START/STOP BITS TIMING**

Note: Refer to Figure 3-2 for load conditions.
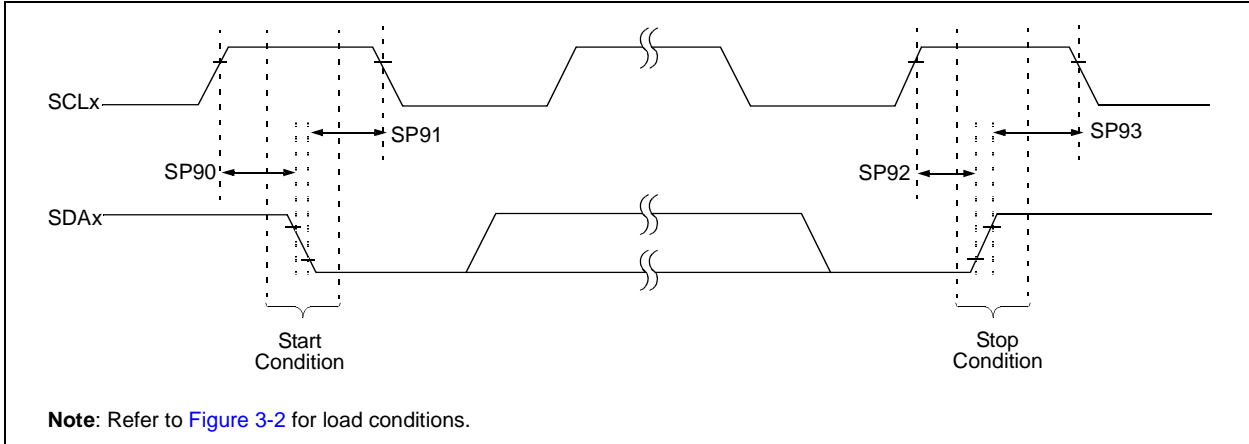
FIGURE 3-5: **I²C™ BUS DATA TIMING**

Note: Refer to Figure 3-2 for load conditions.
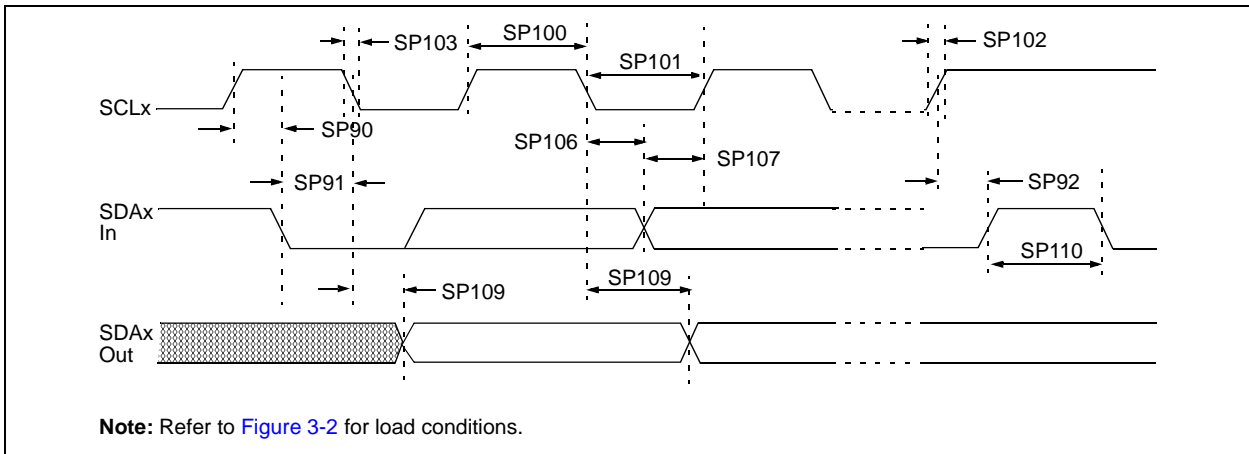
TABLE 3-3: I²C™ BUS DATA REQUIREMENTS

Param. No.	Symbol	Characteristic		Min.	Max.	Units	Conditions
SP100*	T$_{HIGH}$	Clock high time	400 kHz mode	0.6	—	μs	
SP101*	T$_{LOW}$	Clock low time	400 kHz mode	1.3	—	μs	
SP102*	T$_R$	SDAx and SCLx rise time	400 kHz mode	20 + 0.1C$_B$	300	ns	C$_B$ is specified to be from 10-400 pF
SP103*	T$_F$	SDAx and SCLx fall time	400 kHz mode	20 + 0.1C$_B$	250	ns	C$_B$ is specified to be from 10-400 pF
SP106*	T$_{HD:DAT}$	Data input hold time	400 kHz mode	0	0.9	μs	
SP107*	T$_{SU:DAT}$	Data input setup time	400 kHz mode	100	—	ns	
SP109*	T$_{AA}$	Output valid from clock	400 kHz mode	—	—	ns	
SP110*	T$_{BUF}$	Bus free time	400 kHz mode	1.3	—	μs	Time the bus must be free before a new transmission can start
SP111*	C$_B$	Bus capacitive loading		—	400	pF	
SP112*	T$_{TIMEOUT}$	Maximum message time	400 kHz mode	29.5	36.0	ms	

* These parameters are characterized but not tested.

4.0   PACKAGING INFORMATION

4.1   Package Marking Information

8-Lead DFN (3x3x0.9 mm)   Example

```
XXXX        C810
YYWW        1243
 NNN         017
```

PIN 1   PIN 1
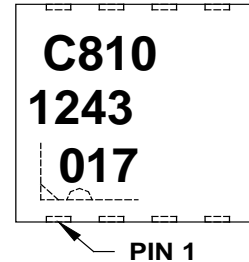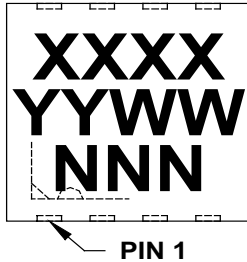
TABLE 4-1:   8-LEAD 3x3x0.9 DFN (MF) TOP MARKING

Part Number	Marking
MTCH810-I/MF	C810

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:		In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

4.2   Package Details

The following sections give the technical details of the packages.

8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

TOP VIEW

SEATING PLANE

BOTTOM VIEW
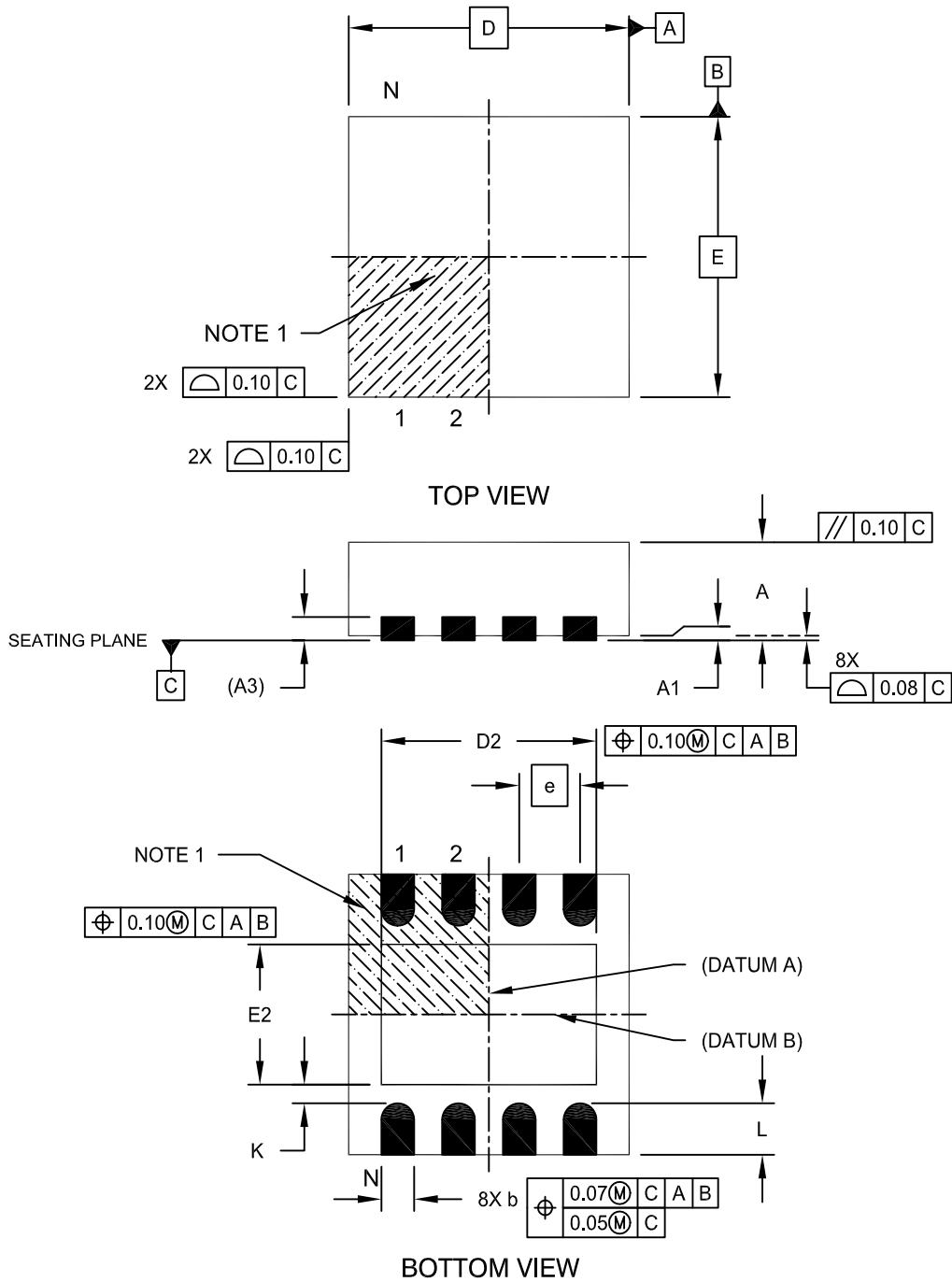
Microchip Technology Drawing No. C04-062C Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

NOTE 2
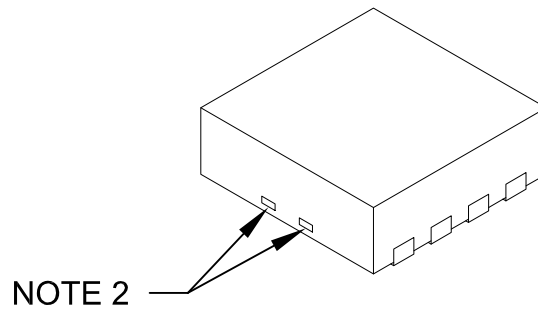
	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Width	E2	1.34	-	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.60	-	2.40
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.20	0.30	0.55
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-062C Sheet 2 of 2

MTCH810

8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
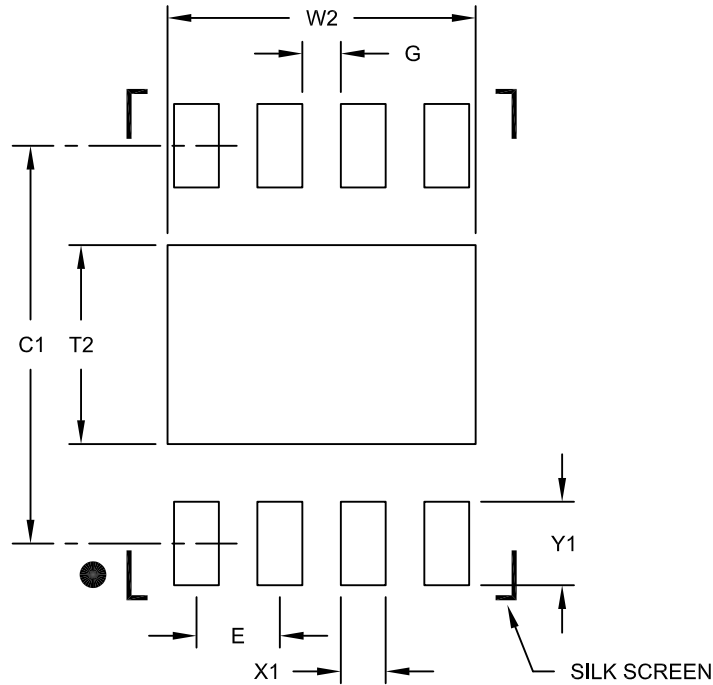
RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			2.40
Optional Center Pad Length	T2			1.55
Contact Pad Spacing	C1		3.10	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.65
Distance Between Pads	G	0.30		

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2062B

APPENDIX A: DATA SHEET REVISION HISTORY

Revision A (12/2012)

Initial release.

Revision B (02/2015)

Updated the Packaging Information chapter.

MTCH810

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To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X]$^{(1)}$	-	X	/XX	XXX
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Device: MTCH810

Tape and Reel Option:
Blank = Standard packaging (tube or tray)
T = Tape and Reel$^{(1)}$

Temperature Range:
I = -40°C to +85°C (Industrial)

Package:$^{(2)}$
MF = DFN

Pattern:
QTP, SQTP, Code or Special Requirements (blank otherwise)

Examples:

a) MTCH810 - I/MF
Industrial temperature,
DFN package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: For other small form-factor package availability and marking information, please visit www.microchip.com/packaging or contact your local sales office.

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