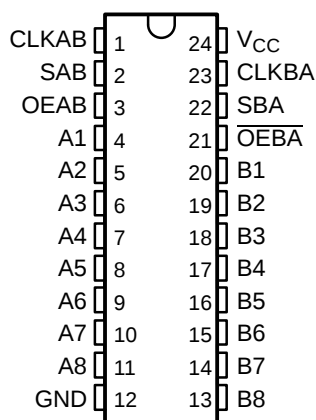


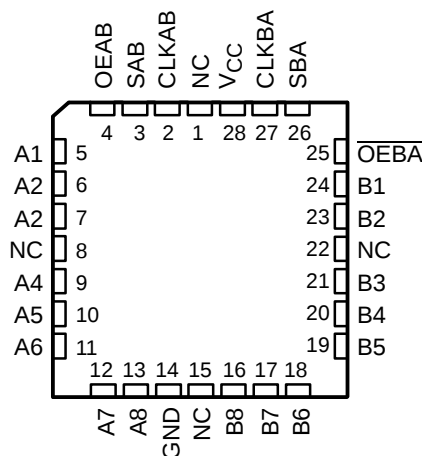
FEATURES

- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 7.4 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- I_{off} Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

SN54LVC652A . . . JT OR W PACKAGE
SN74LVC652A . . . DB, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LVC652A . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

DESCRIPTION/ORDERING INFORMATION

The SN54LVC652A octal bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC652A octal bus transceiver and register is designed for 1.65-V to 3.6-V V_{CC} operation.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube of 25	SN74LVC652ADW	LVC652A
		Reel of 2000	SN74LVC652ADWR	
	SOP – NS	Reel of 2000	SN74LVC652ANSR	LVC652A
	SSOP – DB	Reel of 2000	SN74LVC652ADBR	LC652A
	TSSOP – PW	Tube of 60	SN74LVC652APW	LC652A
		Reel of 2000	SN74LVC652APWR	
		Reel of 250	SN74LVC652APWT	
–55°C to 125°C	CDIP – JT	Tube of 15	SNJ54LVC652AJT	SNJ54LVC652AJT
	CFP – W	Tube of 85	SNJ54LVC652AW	SNJ54LVC652AW
	LCCC – FK	Tube of 42	SNJ54LVC652AFK	SNJ54LVC652AFK

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN54LVC652A, SN74LVC652A

OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

SCAS303L—JANUARY 1993—REVISED SEPTEMBER 2005

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. [Figure 1](#) illustrates the four fundamental bus-management functions that are performed with the 'LVC652A devices.

Data on the A or B data bus, or both, is stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs, regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

FUNCTION TABLE

INPUTS						DATA I/O ⁽¹⁾		OPERATION OR FUNCTION
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified ⁽²⁾	Store A, hold B
H	H	↑	↑	X ⁽²⁾	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified ⁽²⁾	Input	Hold A, store B
L	L	↑	↑	X	X ⁽²⁾	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

(1) The data-output functions can be enabled or disabled by a variety of level combinations at OEAB or $\overline{\text{OEBA}}$. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

(2) Select control = L; clocks can occur simultaneously. Select control = H; clocks must be staggered to load both registers.

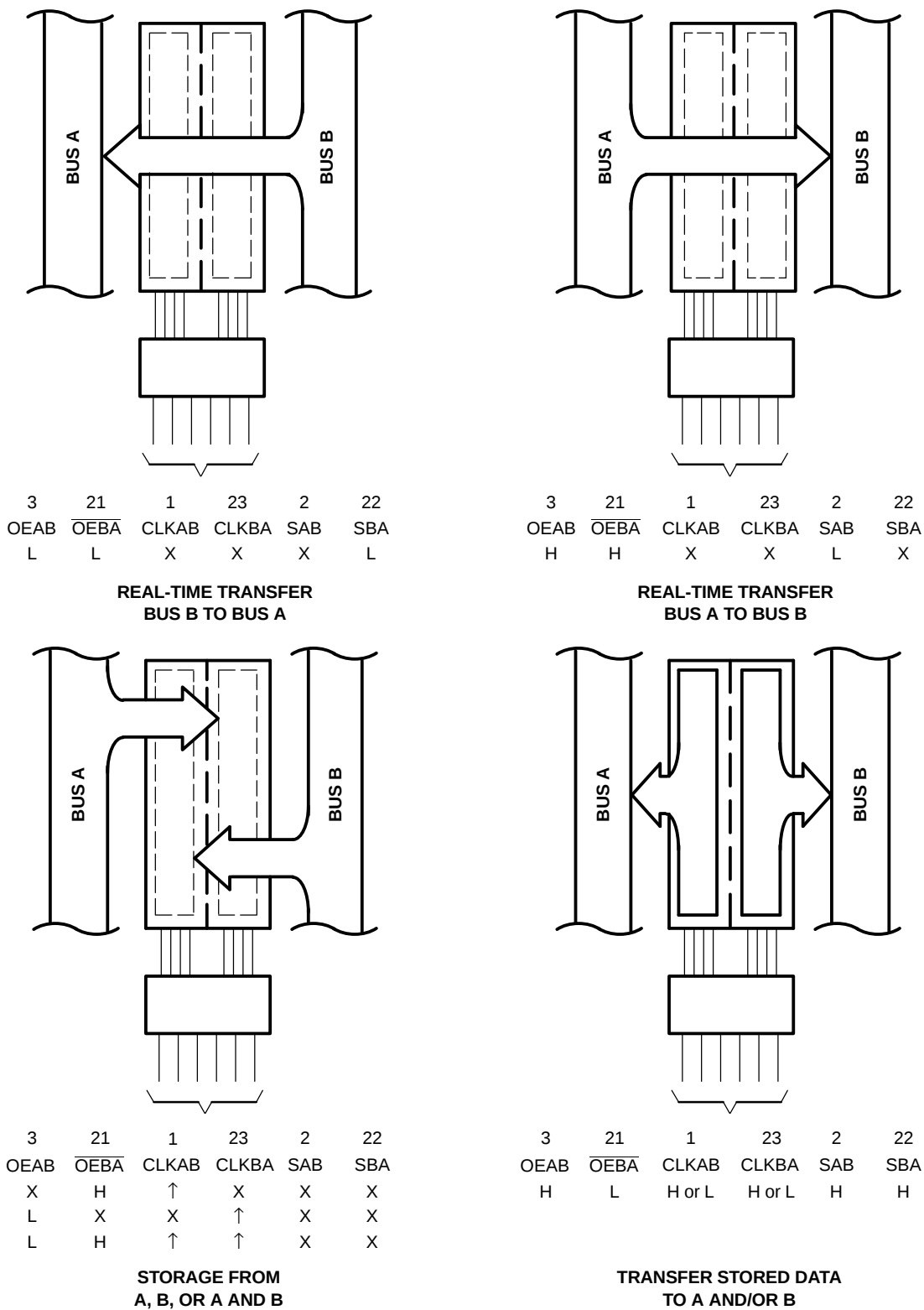


Figure 1. Bus-Management Functions

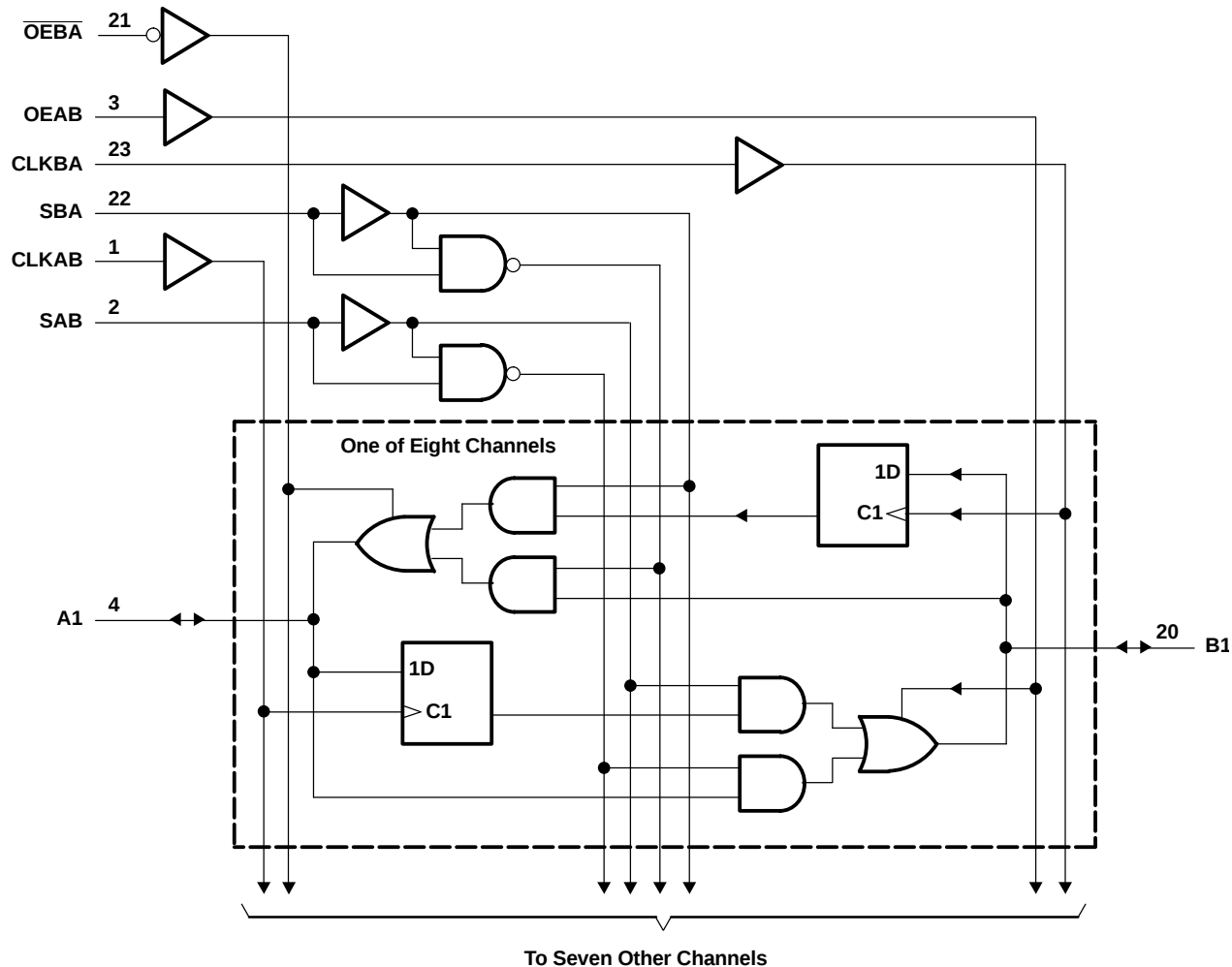
SN54LVC652A, SN74LVC652A

OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

SCAS303L—JANUARY 1993—REVISED SEPTEMBER 2005

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DB, DW, JT, NS, PW, and W packages.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	6.5	V
V_I	Input voltage range	–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾	–0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		–50 mA
I_{OK}	Output clamp current	$V_O < 0$		–50 mA
I_O	Continuous output current		±50	mA
	Continuous current through V_{CC} or GND		±100	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DB package		63
		DW package		46
		NS package		65
		PW package		88
T_{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

			SN54LVC652A		SN74LVC652A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V_{IH}	High-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$			$0.65 \times V_{CC}$		V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$			1.7		
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2		2		
V_{IL}	Low-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$			$0.35 \times V_{CC}$		V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$			0.7		
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		0.8		0.8	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3-state	0	5.5	0	5.5	
I_{OH}	High-level output current	$V_{CC} = 1.65\text{ V}$				–4	mA
		$V_{CC} = 2.3\text{ V}$				–8	
		$V_{CC} = 2.7\text{ V}$		–12		–12	
		$V_{CC} = 3\text{ V}$		–24		24	
I_{OL}	Low-level output current	$V_{CC} = 1.65\text{ V}$				4	mA
		$V_{CC} = 2.3\text{ V}$				8	
		$V_{CC} = 2.7\text{ V}$		12		12	
		$V_{CC} = 3\text{ V}$		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			5		5	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LVC652A, SN74LVC652A

OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	SN54LVC652A		SN74LVC652A		UNIT
				MIN	TYP ⁽¹⁾ MAX	MIN	TYP ⁽¹⁾ MAX	
V _{OH}	I _{OH} = −100 μA	1.65 V to 3.6 V			V _{CC} − 0.2		V	
		2.7 V to 3.6 V	V _{CC} − 0.2					
	I _{OH} = −4 mA	1.65 V		1.2				
	I _{OH} = −8 mA	2.3 V		1.7				
	I _{OH} = −12 mA	2.7 V	2.2	2.2				
		3 V	2.4	2.4				
	I _{OH} = −24 mA	3 V	2.2	2.2				
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	V		
		2.7 V to 3.6 V	0.2					
	I _{OL} = 4 mA	1.65 V		0.45				
	I _{OL} = 8 mA	2.3 V		0.7				
	I _{OL} = 12 mA	2.7 V	0.4	0.4				
	I _{OL} = 24 mA	3 V	0.55	0.55				
I _I	Control inputs	V _I = 0 to 5.5 V	3.6 V		±5	±5	μA	
I _{off}		V _I or V _O = 5.5 V	0			±10	μA	
I _{OZ} ⁽²⁾		V _O = 0 to 5.5 V	3.6 V		±15	±10	μA	
I _{CC}	V _I = V _{CC} or GND	I _O = 0	3.6 V		10	10	μA	
	3.6 V ≤ V _I ≤ 5.5 V ⁽³⁾				10	10		
ΔI _{CC}		One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	500	μA	
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V		4.5	4.5	pF	
C _{i0}	A or B port	V _O = V _{CC} or GND	3.3 V		7.5	7.5	pF	

(1) All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

(2) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(3) This applies in the disabled state only.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

		SN54LVC652A				UNIT
		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	80		100		MHz
t _w	Pulse duration	3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	1.6		1.5		ns
t _h	Hold time, data after CLK↑	0.5		1.5		ns

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

		SN74LVC652A								UNIT
		$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	(1)		(1)		80		100		MHz
t _w	Pulse duration	(1)		(1)		3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	(1)		(1)		1.9		1.9		ns
t _h	Hold time, data after CLK↑	(1)		(1)		1.5		1.7		ns

(1) This information was not available at the time of publication.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC652A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
f _{max}			80		100		MHz
t _{pd}	A or B	B or A	7.8		1	7.4	ns
	CLK	A or B	8.4		1	8	
	SAB or SBA	B or A	9.6		1	8.7	
t _{en}	$\overline{\text{OEBA}}$	A	8.9		1	7.4	ns
t _{dis}	$\overline{\text{OEBA}}$	A	8.1		1	7.5	ns
t _{en}	OEAB	B	8.6		1	7.1	ns
t _{dis}	OEAB	B	7.7		1	7.4	ns

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC652A								UNIT
			$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			(1)		(1)		80		100		MHz
t_{pd}	A or B	B or A	(1)	(1)	(1)	(1)	7.8		1.5	7.4	ns
	CLK	A or B	(1)	(1)	(1)	(1)	8.4		1.5	8	
	SAB or SBA	B or A	(1)	(1)	(1)	(1)	9.6		1.5	8.7	
t_{en}	$\overline{\text{OEBA}}$	A	(1)	(1)	(1)	(1)	8.9		1.5	7.4	ns
t_{dis}	$\overline{\text{OEBA}}$	A	(1)	(1)	(1)	(1)	8.1		1.5	7.5	ns
t_{en}	OEAB	B	(1)	(1)	(1)	(1)	8.6		1.5	7.1	ns
t_{dis}	OEAB	B	(1)	(1)	(1)	(1)	7.7		1.5	7.4	ns

(1) This information was not available at the time of publication.

SN54LVC652A, SN74LVC652A

OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

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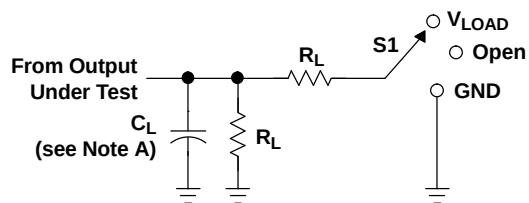
Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	TYP	TYP	
C_{pd} Power dissipation capacitance per transceiver	Outputs enabled	$f = 10\text{ MHz}$	(1)	(1)	84	μF
	Outputs disabled		(1)	(1)	9.5	

(1) This information was not available at the time of publication.

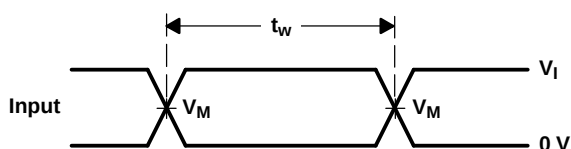
PARAMETER MEASUREMENT INFORMATION



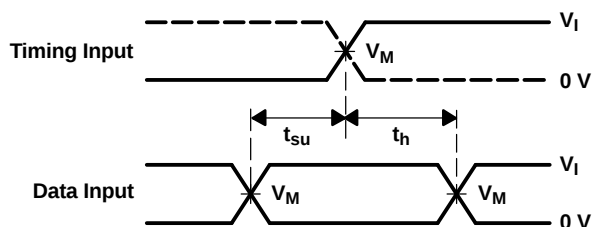
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

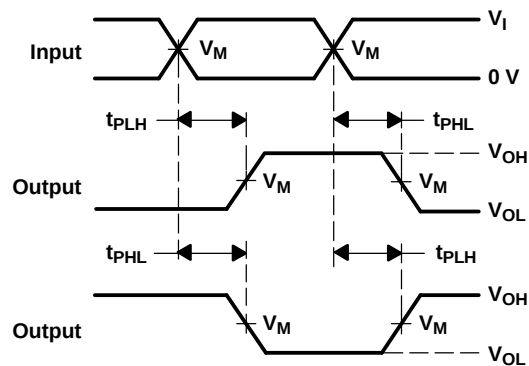
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



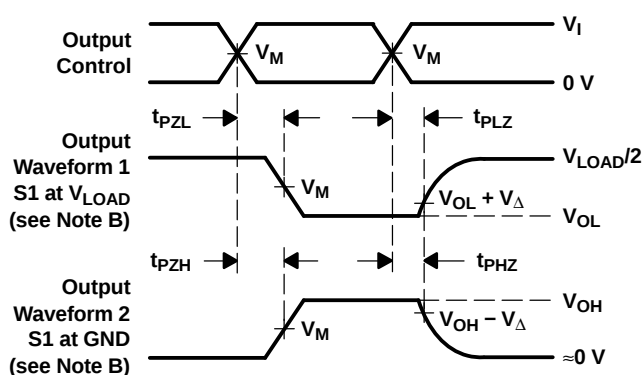
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC652ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC652A	Samples
SN74LVC652ADWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC652A	Samples
SN74LVC652ADWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC652A	Samples
SN74LVC652APW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC652A	Samples
SN74LVC652APWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC652A	Samples
SN74LVC652APWT	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC652A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

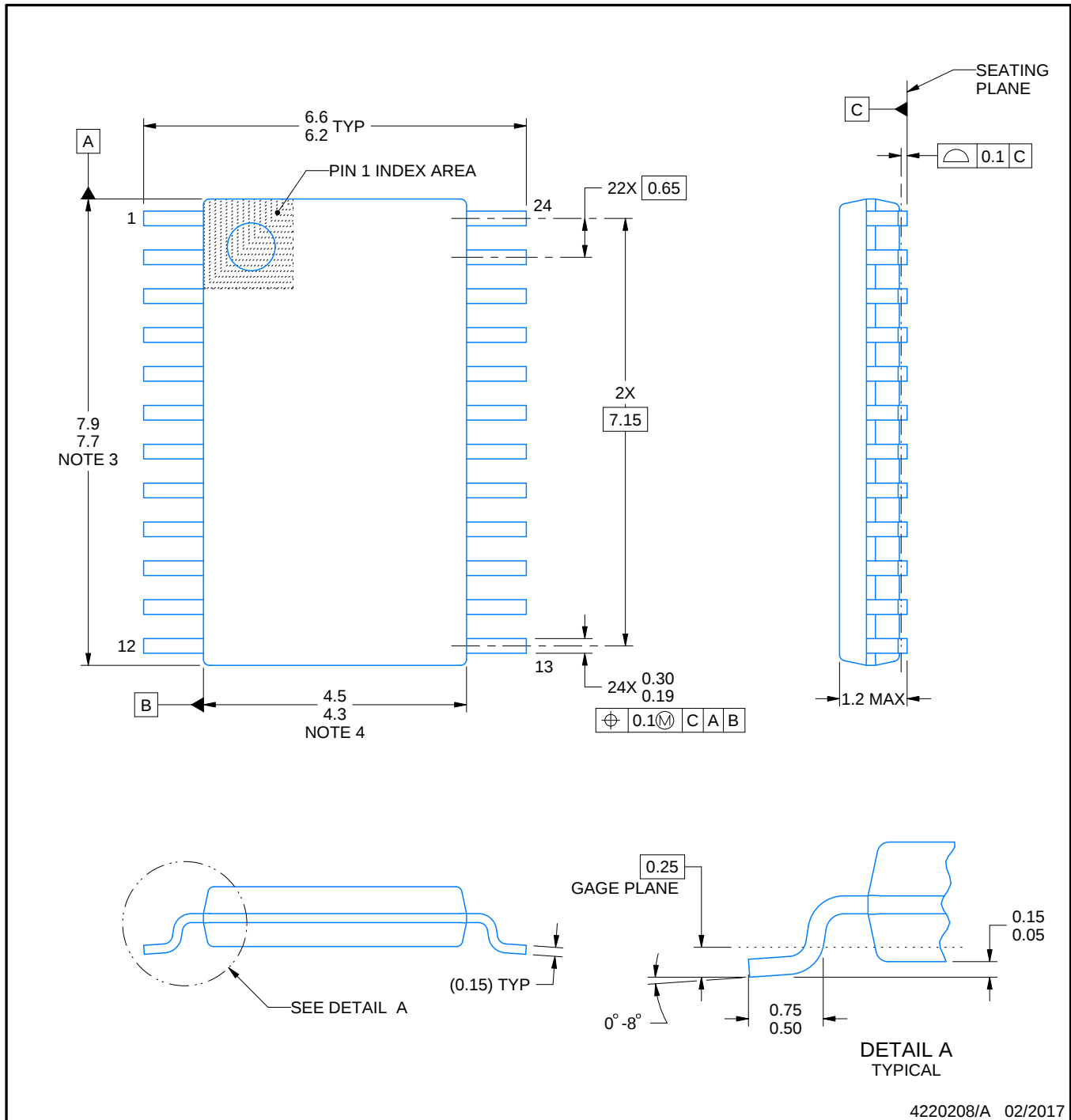
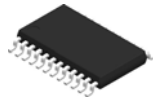
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC652ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVC652APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74LVC652APWT	TSSOP	PW	24	250	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC652ADWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74LVC652APWR	TSSOP	PW	24	2000	367.0	367.0	38.0
SN74LVC652APWT	TSSOP	PW	24	250	367.0	367.0	38.0



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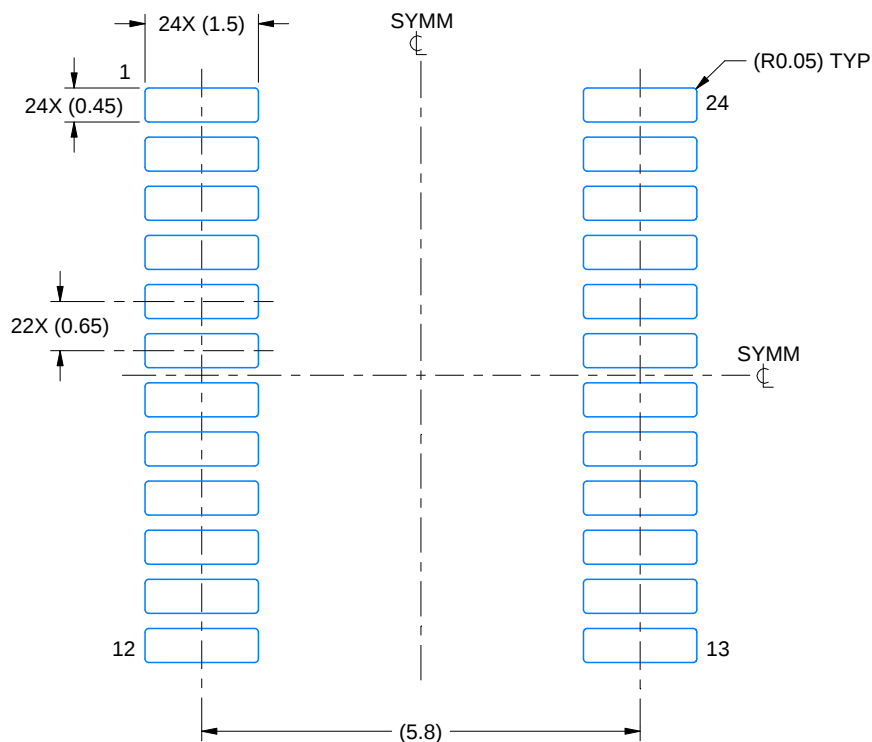
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

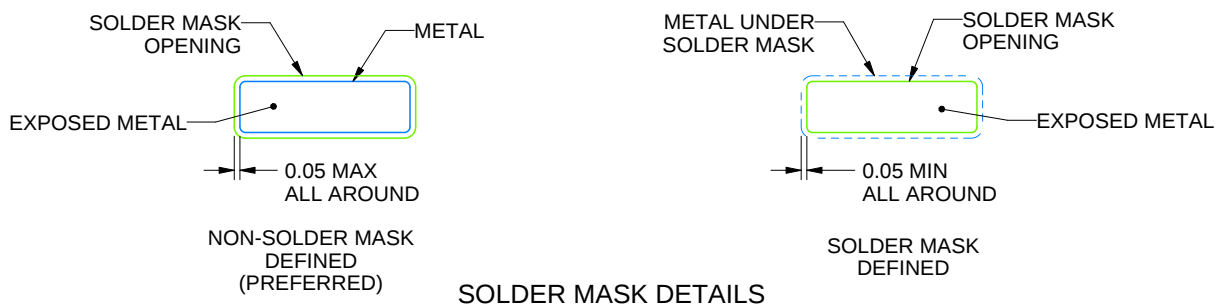
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



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NOTES: (continued)

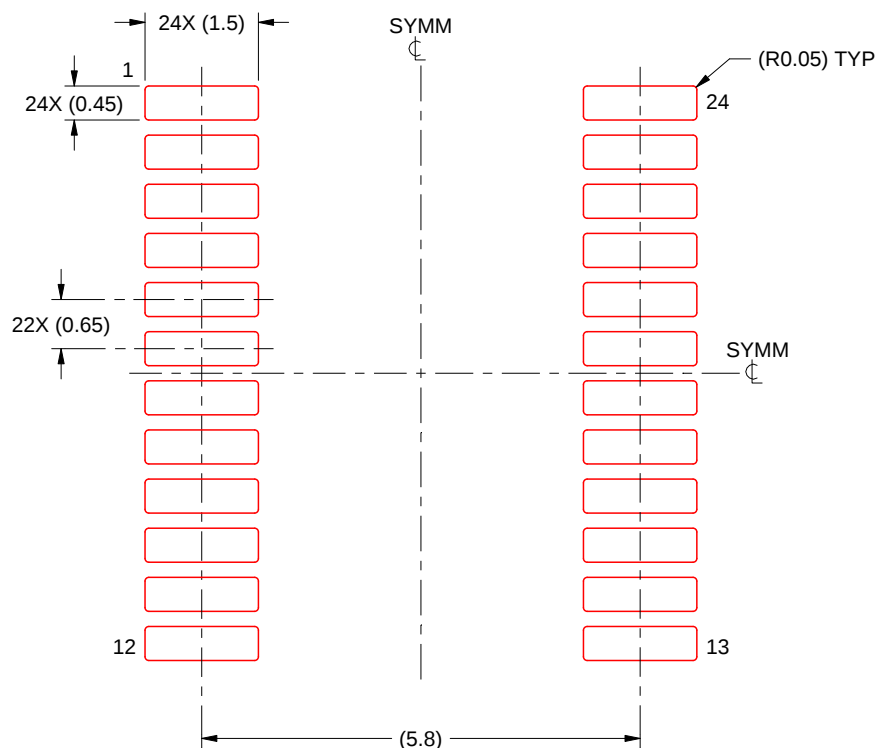
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

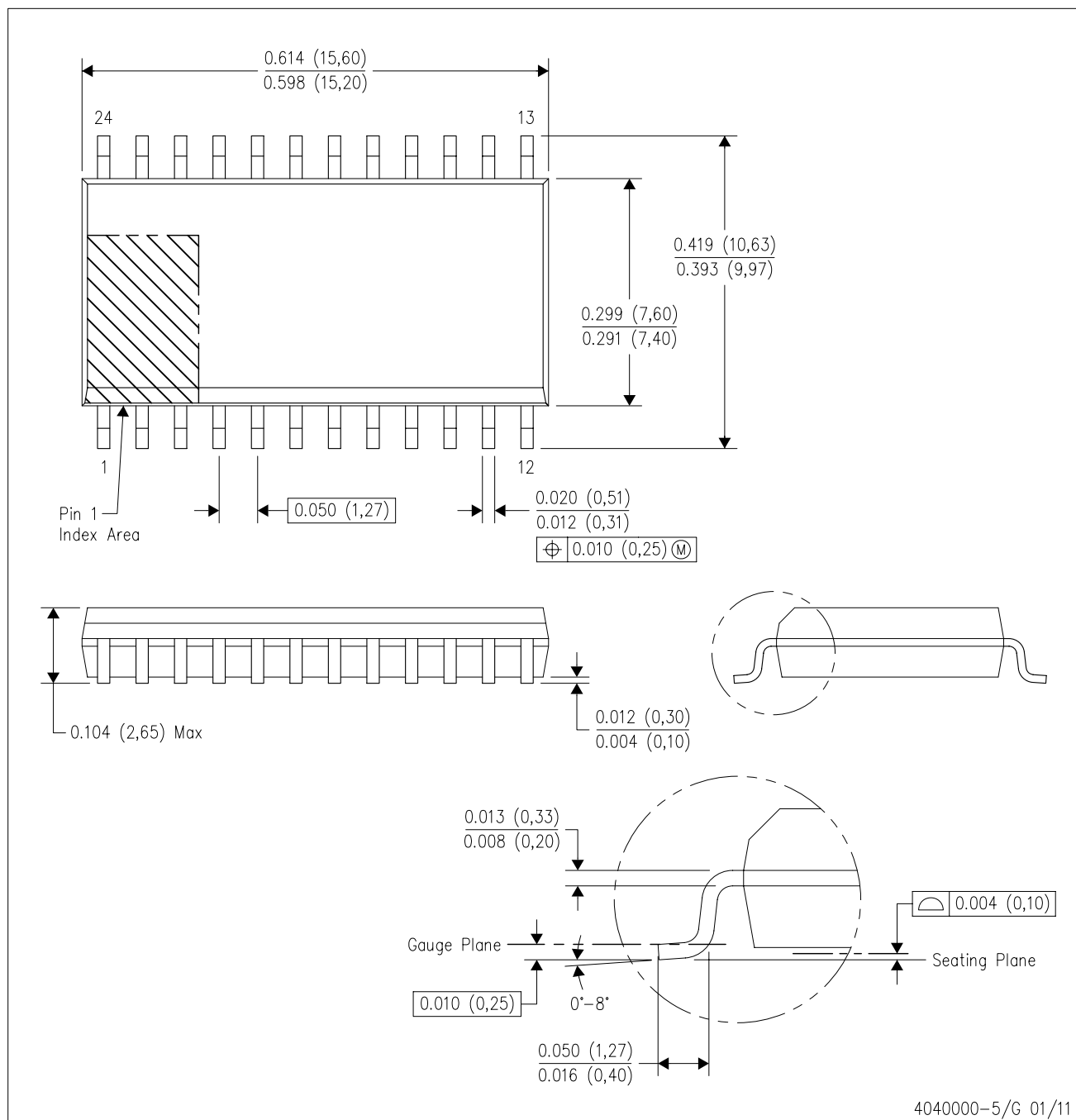
4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R-PDSO-G24)

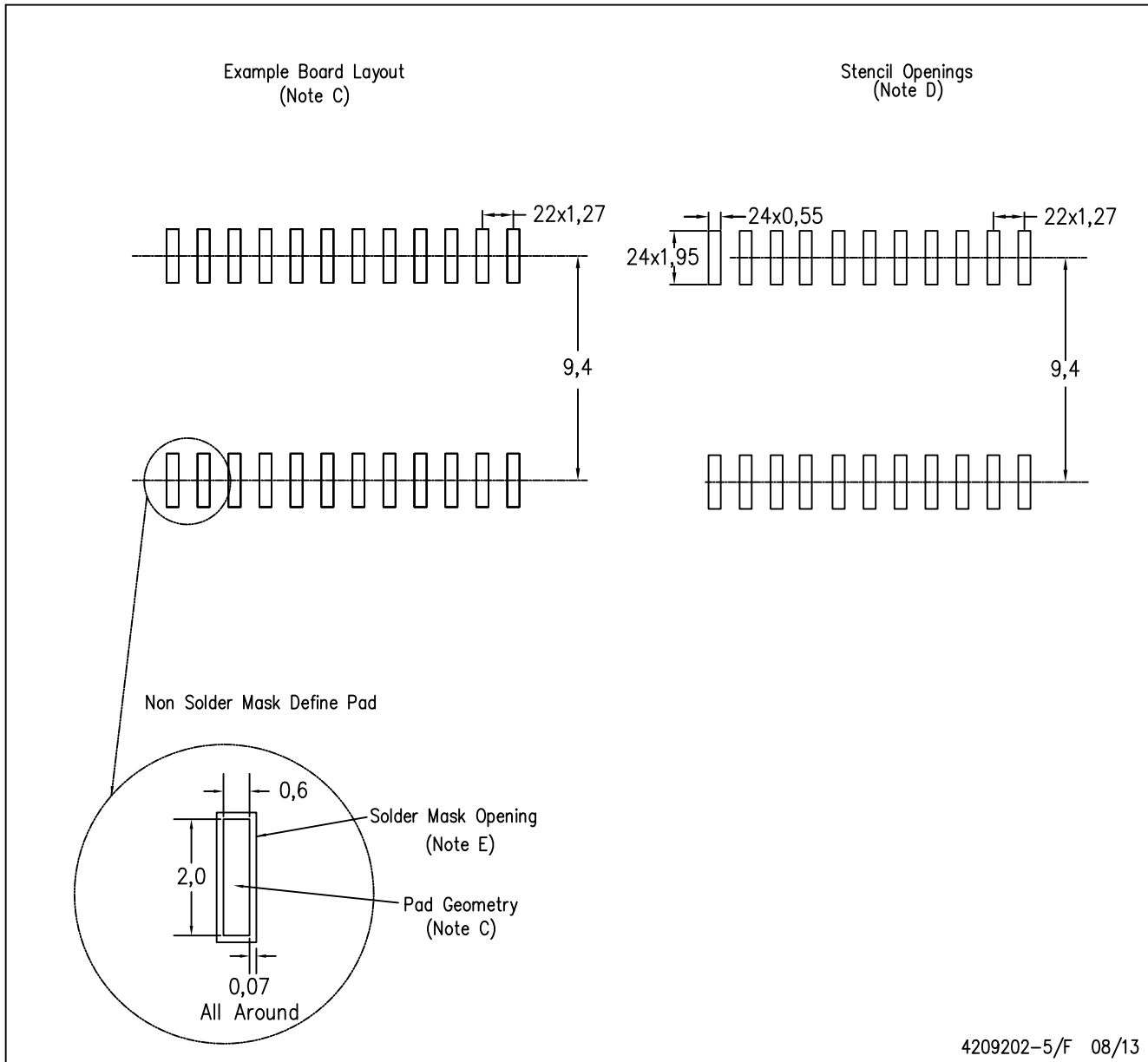
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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