

MSP430FR572x Mixed-Signal Microcontrollers

1 Device Overview

1.1 Features

- Embedded Microcontroller
 - 16-Bit RISC Architecture up to 8-MHz Clock
 - Wide Supply Voltage Range (2 V to 3.6 V)
 - –40°C to 85°C Operation
- Optimized Ultra-Low-Power Modes
 - Active Mode: 81.4 μ A/MHz (Typical)
 - Standby (LPM3 With VLO): 6.3 μ A (Typical)
 - Real-Time Clock (RTC) (LPM3.5 With Crystal): 1.5 μ A (Typical)
 - Shutdown (LPM4.5): 0.32 μ A (Typical)
- Ultra-Low-Power Ferroelectric RAM (FRAM)
 - Up to 16KB of Nonvolatile Memory
 - Ultra-Low-Power Writes
 - Fast Write at 125 ns per Word (16KB in 1 ms)
 - Built-In Error Correction Coding (ECC) and Memory Protection Unit (MPU)
 - Universal Memory = Program + Data + Storage
 - 10^{15} Write Cycle Endurance
 - Radiation Resistant and Nonmagnetic
- Intelligent Digital Peripherals
 - 32-Bit Hardware Multiplier (MPY)
 - Three-Channel Internal DMA
 - Real-Time Clock (RTC) With Calendar and Alarm Functions
 - Five 16-Bit Timers With up to Three Capture/Compare Registers
 - 16-Bit Cyclic Redundancy Checker (CRC)
- High-Performance Analog
 - 16-Channel Analog Comparator With Voltage Reference and Programmable Hysteresis
 - 12-Channel 10-Bit Analog-to-Digital Converter (ADC) With Internal Reference and Sample-and-Hold
 - 200 ksp/s at 100- μ A Consumption
- Enhanced Serial Communication
 - eUSCI_A0 and eUSCI_A1 Support:
 - UART With Automatic Baud-Rate Detection
 - IrDA Encode and Decode
 - SPI
 - eUSCI_B0 Supports:
 - I²C With Multiple-Slave Addressing
 - SPI
 - Hardware UART Bootloader (BSL)
- Power Management System
 - Fully Integrated LDO
 - Supply Voltage Supervisor for Core and Supply Voltages With Reset Capability
 - Always-On Zero-Power Brownout Detection
 - Serial Onboard Programming With No External Voltage Needed
- Flexible Clock System
 - Fixed-Frequency DCO With Six Selectable Factory-Trimmed Frequencies (Device Dependent)
 - Low-Power Low-Frequency Internal Clock Source (VLO)
 - 32-kHz Crystals (LFXT)
 - High-Frequency Crystals (HFXT)
- Development Tools and Software
 - Free Professional Development Environment ([Code Composer Studio™ IDE](#))
 - Low-Cost Full-Featured Kit ([MSP-EXP430FR5739](#))
 - Full Development Kit ([MSP-FET430U40A](#))
 - Target Board ([MSP-TS430RHA40A](#))
- Family Members
 - See [Family Members](#) for Available Device Variants and Packages
 - For Complete Module Descriptions, See the [MSP430FR57xx Family User's Guide](#)

1.2 Applications

- Home Automation
- Security
- Sensor Management
- Data Acquisition

CAUTION These products use FRAM nonvolatile memory technology. FRAM retention is sensitive to extreme temperatures, such as those experienced during reflow or hand soldering. See [Absolute Maximum Ratings](#) for more information.

CAUTION System-level ESD protection must be applied in compliance with the device-level ESD specification to prevent electrical overstress or disturb of data or code memory. See [MSP430™ System-Level ESD Considerations](#) for more information.



1.3 Description

The TI MSP430FR572x family of ultra-low-power microcontrollers consists of multiple devices that feature embedded FRAM nonvolatile memory, ultra-low-power 16-bit MSP430™ CPU, and different peripherals targeted for various applications. The architecture, FRAM, and peripherals, combined with seven low-power modes, are optimized to achieve extended battery life in portable and wireless sensing applications. FRAM is a new nonvolatile memory that combines the speed, flexibility, and endurance of SRAM with the stability and reliability of flash, all at lower total power consumption. Peripherals include a 10-bit ADC, a 16-channel comparator with voltage reference generation and hysteresis capabilities, three enhanced serial channels capable of I²C, SPI, or UART protocols, an internal DMA, a hardware multiplier, an RTC, five 16-bit timers, and digital I/Os.

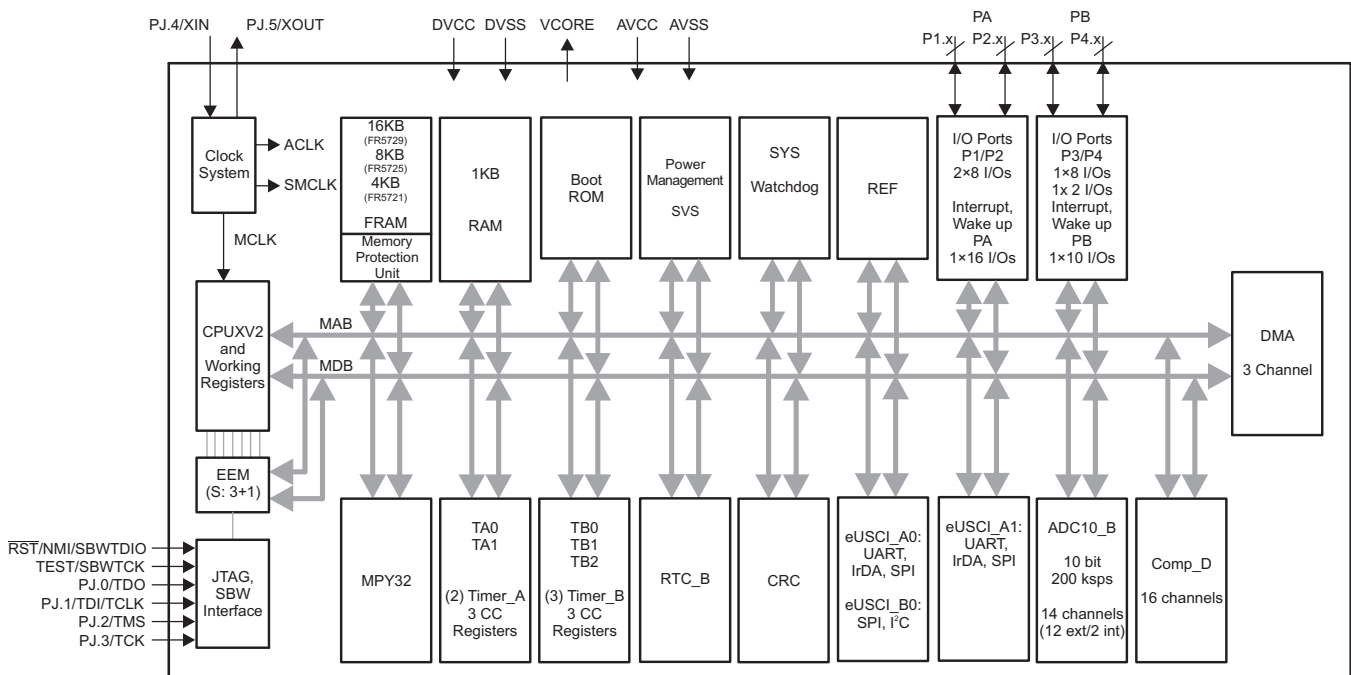
Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE ⁽²⁾ |
|-----------------|------------|--------------------------|
| MSP430FR5729RHA | VQFN (40) | 6 mm × 6 mm |
| MSP430FR5729DA | TSSOP (38) | 12.5 mm × 6.2 mm |
| MSP430FR5728RGE | VQFN (24) | 4 mm × 4 mm |
| MSP430FR5728PW | TSSOP (28) | 9.7 mm × 4.4 mm |

- (1) For the most current part, package, and ordering information, see the *Package Option Addendum* in Section 8, or see the TI website at www.ti.com.
- (2) The dimensions shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in Section 8.

1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram for the MSP430FR5721, MSP430FR5725, and MSP430FR5729 devices in the RHA package. For the functional block diagrams for all device variants and package options, see Section 6.1.



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Figure 1-1. Functional Block Diagram – RHA Package – MSP430FR5721, MSP430FR5725, MSP430FR5729

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from October 1, 2016 to December 5, 2017

Page

- Added the note that begins "In LPM3, the VLO frequency varies..." following [Section 5.15](#), *Internal Very-Low-Power Low-Frequency Oscillator (VLO)*..... [24](#)

3 Device Comparison

Table 3-1 summarizes the available family members.

Table 3-1. Family Members⁽¹⁾⁽²⁾

| DEVICE | FRAM (KB) | SRAM (KB) | SYSTEM CLOCK (MHz) | ADC10_B | Comp_D | Timer_A ⁽³⁾ | Timer_B ⁽⁴⁾ | eUSCI | | I/O | PACKAGE |
|--------------|-----------|-----------|--------------------|-------------------|--------|------------------------|------------------------|----------------------------|----------------------------------|-----|---------|
| | | | | | | | | Channel A: UART, IrDA, SPI | Channel B: SPI, I ² C | | |
| MSP430FR5729 | 16 | 1 | 8 | 12 ext, 2 int ch. | 16 ch. | 3, 3 | 3, 3, 3 | 2 | 1 | 32 | RHA |
| | | | | | | | | | | 30 | DA |
| MSP430FR5728 | 16 | 1 | 8 | 6 ext, 2 int ch. | 10 ch. | 3, 3 | 3 | 1 | 1 | 17 | RGE |
| | | | | 8 ext, 2 int ch. | 12 ch. | | | | | 21 | PW |
| MSP430FR5727 | 16 | 1 | 8 | – | 16 ch. | 3, 3 | 3, 3, 3 | 2 | 1 | 32 | RHA |
| | | | | | | | | | | 30 | DA |
| MSP430FR5726 | 16 | 1 | 8 | – | 10 ch. | 3, 3 | 3 | 1 | 1 | 17 | RGE |
| | | | | | 12 ch. | | | | | 21 | PW |
| MSP430FR5725 | 8 | 1 | 8 | 12 ext, 2 int ch. | 16 ch. | 3, 3 | 3, 3, 3 | 2 | 1 | 32 | RHA |
| | | | | | | | | | | 30 | DA |
| MSP430FR5724 | 8 | 1 | 8 | 6 ext, 2 int ch. | 10 ch. | 3, 3 | 3 | 1 | 1 | 17 | RGE |
| | | | | 8 ext, 2 int ch. | 12 ch. | | | | | 21 | PW |
| MSP430FR5723 | 8 | 1 | 8 | – | 16 ch. | 3, 3 | 3, 3, 3 | 2 | 1 | 32 | RHA |
| | | | | | | | | | | 30 | DA |
| MSP430FR5722 | 8 | 1 | 8 | – | 10 ch. | 3, 3 | 3 | 1 | 1 | 17 | RGE |
| | | | | | 12 ch. | | | | | 21 | PW |
| MSP430FR5721 | 4 | 1 | 8 | 12 ext, 2 int ch. | 16 ch. | 3, 3 | 3, 3, 3 | 2 | 1 | 32 | RHA |
| | | | | | | | | | | 30 | DA |
| MSP430FR5720 | 4 | 1 | 8 | 6 ext, 2 int ch. | 10 ch. | 3, 3 | 3 | 1 | 1 | 17 | RGE |
| | | | | 8 ext, 2 int ch. | 12 ch. | | | | | 21 | PW |

- (1) For the most current package and ordering information, see the Package Option Addendum in Section 8, or see the TI website at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.
- (3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.
- (4) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

Products for MSP 16-Bit and 32-Bit MCUs Low-power mixed-signal processors with smart analog and digital peripherals for a wide range of industrial and consumer applications.

Products for Ultra-Low-Power MCUs MSP Ultra-Low-Power microcontrollers (MCUs) from Texas Instruments (TI) offer the lowest power consumption and the perfect mix of integrated peripherals for a wide range of low power and portable applications.

Products for MSP430FRxx FRAM MCUs 16-bit microcontrollers for ultra-low-power sensing and system management in building automation, smart grid, and industrial designs.

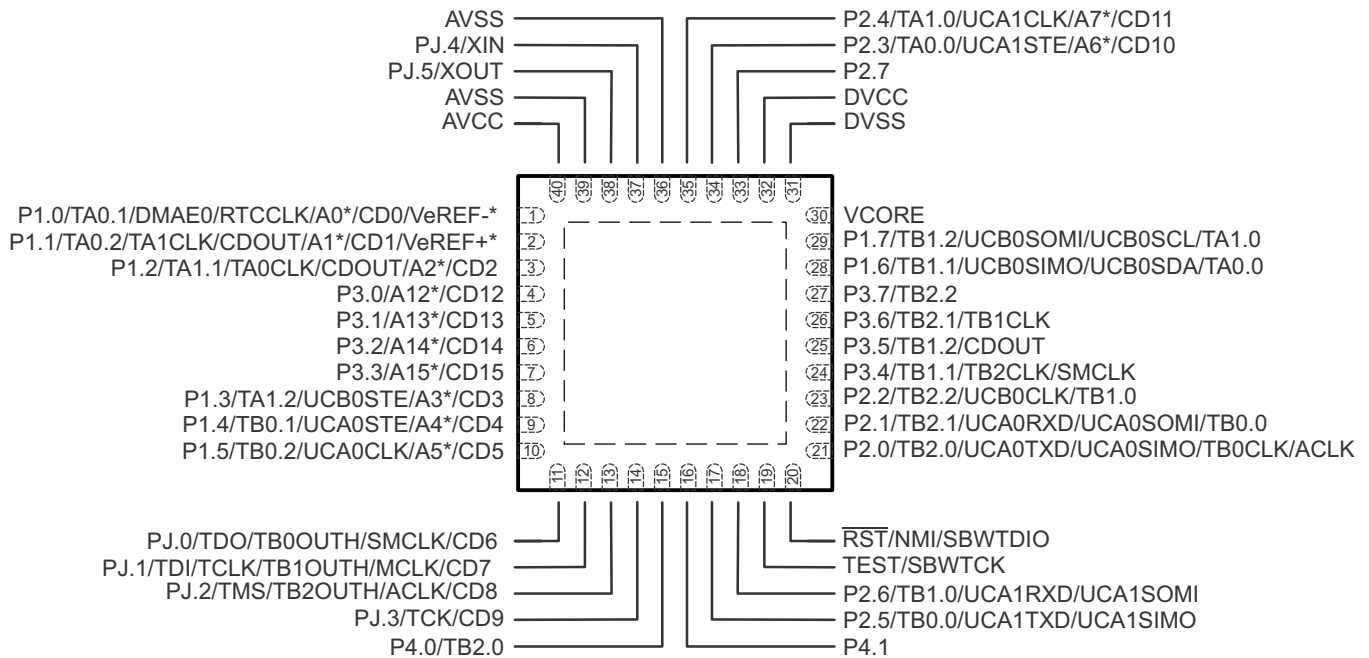
Companion Products for MSP430FR5729 Review products that are frequently purchased or used in conjunction with this product.

Reference Designs for MSP430FR5729 TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

4 Terminal Configuration and Functions

4.1 Pin Diagram – RHA Package – MSP430FR5721, MSP430FR5723, MSP430FR5725, MSP430FR5727, MSP430FR5729

Figure 4-1 shows the pin diagram for the MSP430FR5721, MSP430FR5723, MSP430FR5725, MSP430FR5727, and MSP430FR5729 devices in the 40-pin RHA package.



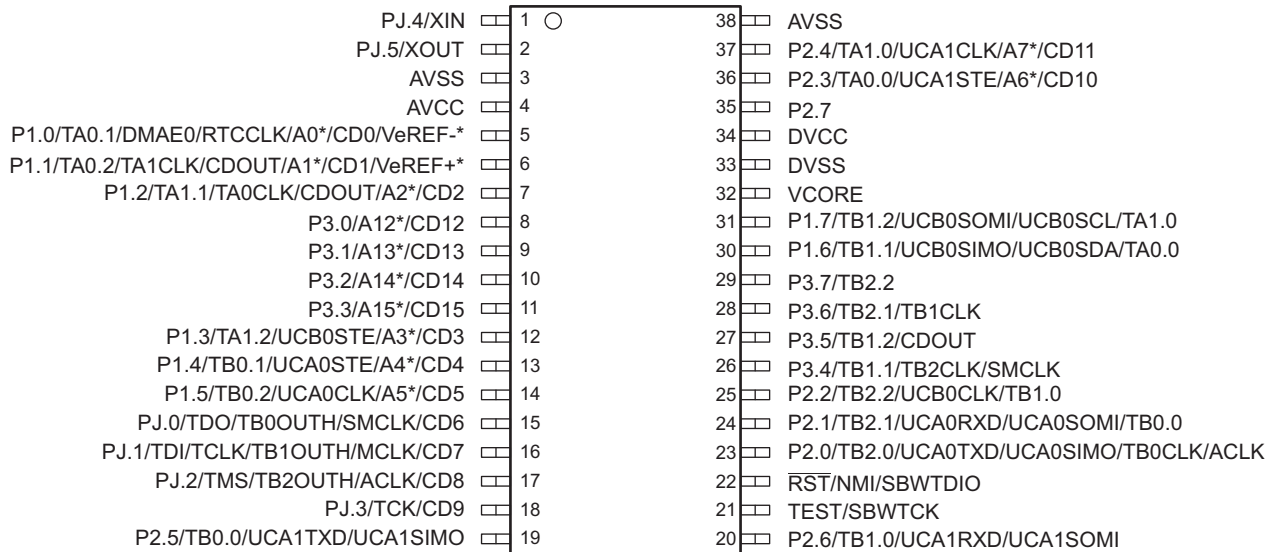
* Not available on MSP430FR5727, MSP430FR5723

Note: Exposed thermal pad connection to V_{SS} recommended.

Figure 4-1. 40-Pin RHA Package (Top View)

4.2 Pin Diagram – DA Package – MSP430FR5721, MSP430FR5723, MSP430FR5725, MSP430FR5727, MSP430FR5729

Figure 4-2 shows the pin diagram for the MSP430FR5721, MSP430FR5723, MSP430FR5725, MSP430FR5727, and MSP430FR5729 devices in the 38-pin DA package.

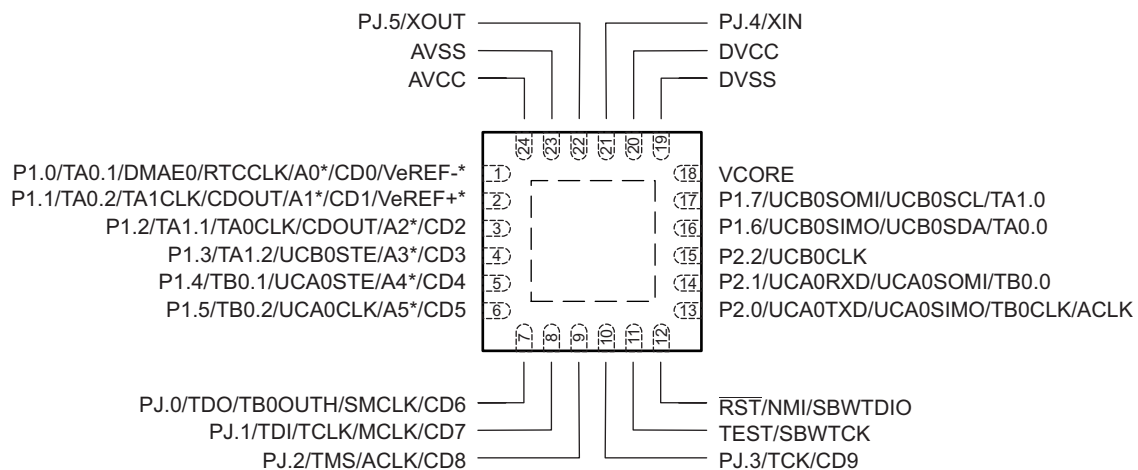


* Not available on MSP430FR5727, MSP430FR5723

Figure 4-2. 38-Pin DA Package (Top View)

4.3 Pin Diagram – RGE Package – MSP430FR5720, MSP430FR5722, MSP430FR5724, MSP430FR5726, MSP430FR5728

Figure 4-3 shows the pin diagram for the MSP430FR5720, MSP430FR5722, MSP430FR5724, MSP430FR5726, and MSP430FR5728 devices in the 24-pin RGE package.



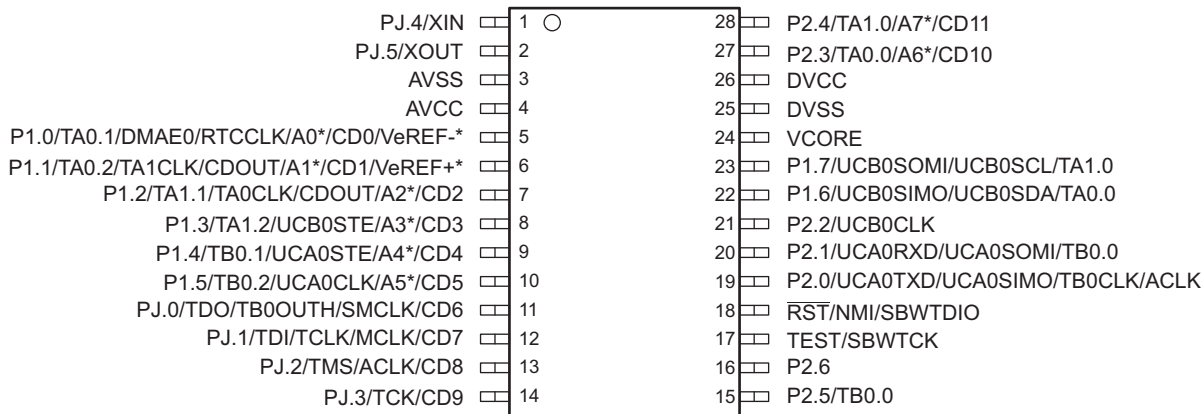
* Not available on MSP430FR5726, MSP430FR5722

Note: Exposed thermal pad connection to V_{SS} recommended.

Figure 4-3. 24-Pin RGE Package (Top View)

**4.4 Pin Diagram – PW Package –
MSP430FR5720, MSP430FR5722, MSP430FR5724, MSP430FR5726, MSP430FR5728**

Figure 4-4 shows the pin diagram for the MSP430FR5720, MSP430FR5722, MSP430FR5724, MSP430FR5726, and MSP430FR5728 devices in the 28-pin PW package.



* Not available on MSP430FR5726, MSP430FR5722

Figure 4-4. 28-Pin PW Package (Top View)

4.5 Signal Descriptions

Table 4-1 describes the signals for all device variants and packages.

Table 4-1. Signal Descriptions

| TERMINAL | | | | | I/O (1) | DESCRIPTION |
|--|-----|-----|----|-----|------------|--|
| NAME | NO. | | | | | |
| | RHA | RGE | DA | PW | | |
| P1.0/TA0.1/DMAE0/ RTCCCLK/A0/CD0/VeREF- | 1 | 1 | 5 | 5 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 TA0 CCR1 capture: CCI1A input, compare: Out1 External DMA trigger RTC clock calibration output Analog input A0 – ADC (not available on devices without ADC) Comparator_D input CD0 External applied reference voltage (not available on devices without ADC) |
| P1.1/TA0.2/TA1CLK/ CDOUT/A1/CD1/VeREF+ | 2 | 2 | 6 | 6 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 TA0 CCR2 capture: CCI2A input, compare: Out2 TA1 input clock Comparator_D output Analog input A1 – ADC (not available on devices without ADC) Comparator_D input CD1 Input for an external reference voltage to the ADC (not available on devices without ADC) |
| P1.2/TA1.1/TA0CLK/ CDOUT/A2/CD2 | 3 | 3 | 7 | 7 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 TA1 CCR1 capture: CCI1A input, compare: Out1 TA0 input clock Comparator_D output Analog input A2 – ADC (not available on devices without ADC) Comparator_D input CD2 |
| P3.0/A12/CD12 | 4 | N/A | 8 | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE) Analog input A12 – ADC (not available on devices without ADC or package options PW, RGE) Comparator_D input CD12 (not available on package options PW, RGE) |
| P3.1/A13/CD13 | 5 | N/A | 9 | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE) Analog input A13 – ADC (not available on devices without ADC or package options PW, RGE) Comparator_D input CD13 (not available on package options PW, RGE) |
| P3.2/A14/CD14 | 6 | N/A | 10 | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE) Analog input A14 – ADC (not available on devices without ADC or package options PW, RGE) Comparator_D input CD14 (not available on package options PW, RGE) |
| P3.3/A15/CD15 | 7 | N/A | 11 | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE) Analog input A15 – ADC (not available on devices without ADC or package options PW, RGE) Comparator_D input CD15 (not available on package options PW, RGE) |

(1) I = input, O = output, N/A = not available

Table 4-1. Signal Descriptions (continued)

| TERMINAL | | | | | I/O (1) | DESCRIPTION |
|--|-----|-----|-----|-----|------------|--|
| NAME | NO. | | | | | |
| | RHA | RGE | DA | PW | | |
| P1.3/TA1.2/UCB0STE/ A3/CD3 | 8 | 4 | 12 | 8 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 TA1 CCR2 capture: CCI2A input, compare: Out2 Slave transmit enable – eUSCI_B0 SPI mode Analog input A3 – ADC (not available on devices without ADC) Comparator_D input CD3 |
| P1.4/TB0.1/UCA0STE/ A4/CD4 | 9 | 5 | 13 | 9 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 TB0 CCR1 capture: CCI1A input, compare: Out1 Slave transmit enable – eUSCI_A0 SPI mode Analog input A4 – ADC (not available on devices without ADC) Comparator_D input CD4 |
| P1.5/TB0.2/UCA0CLK/ A5/CD5 | 10 | 6 | 14 | 10 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 TB0 CCR2 capture: CCI2A input, compare: Out2 Clock signal input – eUSCI_A0 SPI slave mode, Clock signal output – eUSCI_A0 SPI master mode Analog input A5 – ADC (not available on devices without ADC) Comparator_D input CD5 |
| PJ.0/TDO/TB0OUTH/ SMCLK/CD6 (2) | 11 | 7 | 15 | 11 | I/O | General-purpose digital I/O Test data output port Switch all PWM outputs high impedance input – TB0 SMCLK output Comparator_D input CD6 |
| PJ.1/TDI/TCLK/TB1OUTH/ MCLK/CD7 (2) | 12 | 8 | 16 | 12 | I/O | General-purpose digital I/O Test data input or test clock input Switch all PWM outputs high impedance input – TB1 (not available on devices without TB1) MCLK output Comparator_D input CD7 |
| PJ.2/TMS/TB2OUTH/ ACLK/CD8 (2) | 13 | 9 | 17 | 13 | I/O | General-purpose digital I/O Test mode select Switch all PWM outputs high impedance input – TB2 (not available on devices without TB2) ACLK output Comparator_D input CD8 |
| PJ.3/TCK/CD9 (2) | 14 | 10 | 18 | 14 | I/O | General-purpose digital I/O Test clock Comparator_D input CD9 |
| P4.0/TB2.0 | 15 | N/A | N/A | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE) TB2 CCR0 capture: CCI0B input, compare: Out0 (not available on devices without TB2 or package options DA, PW, RGE) |
| P4.1 | 16 | N/A | N/A | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options DA, PW, RGE) |
| P2.5/TB0.0/UCA1TXD/ UCA1SIMO | 17 | N/A | 19 | 15 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 TB0 CCR0 capture: CCI0A input, compare: Out0 Transmit data – eUSCI_A1 UART mode, Slave in, master out – eUSCI_A1 SPI mode (not available on devices without UCSI_A1) |

(2) See Section 6.7 for use with JTAG function.

Table 4-1. Signal Descriptions (continued)

| TERMINAL | | | | | I/O (1) | DESCRIPTION |
|---|-----|-----|----|-----|------------|---|
| NAME | NO. | | | | | |
| | RHA | RGE | DA | PW | | |
| P2.6/TB1.0/UCA1RXD/ UCA1SOMI | 18 | N/A | 20 | 16 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 TB1 CCR0 capture: CCI0A input, compare: Out0 (not available on devices without TB1) Receive data – eUSCI_A1 UART mode, Slave out, master in – eUSCI_A1 SPI mode (not available on devices without UCSI_A1) |
| TEST/SBWTCK ⁽²⁾ ⁽³⁾ | 19 | 11 | 21 | 17 | I | Test mode pin – enable JTAG pins Spy-Bi-Wire input clock |
| $\overline{\text{RST}}$ /NMI/SBWDIO ⁽²⁾ ⁽³⁾ | 20 | 12 | 22 | 18 | I/O | Reset input active low Non-maskable interrupt input Spy-Bi-Wire data input/output |
| P2.0/TB2.0/UCA0TXD/ UCA0SIMO/TB0CLK/ACLK ⁽³⁾ | 21 | 13 | 23 | 19 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 TB2 CCR0 capture: CCI0A input, compare: Out0 (not available on devices without TB2) Transmit data – eUSCI_A0 UART mode Slave in, master out – eUSCI_A0 SPI mode TB0 clock input ACLK output |
| P2.1/TB2.1/UCA0RXD/ UCA0SOMI/TB0.0 ⁽³⁾ | 22 | 14 | 24 | 20 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 TB2 CCR1 capture: CCI1A input, compare: Out1 (not available on devices without TB2) Receive data – eUSCI_A0 UART mode Slave out, master in – eUSCI_A0 SPI mode TB0 CCR0 capture: CCI0A input, compare: Out0 |
| P2.2/TB2.2/UCB0CLK/ TB1.0 | 23 | 15 | 25 | 21 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 TB2 CCR2 capture: CCI2A input, compare: Out2 (not available on devices without TB2) Clock signal input – eUSCI_B0 SPI slave mode, Clock signal output – eUSCI_B0 SPI master mode TB1 CCR0 capture: CCI0A input, compare: Out0 (not available on devices without TB1) |
| P3.4/TB1.1/TB2CLK/ SMCLK | 24 | N/A | 26 | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE) TB1 CCR1 capture: CCI1B input, compare: Out1 (not available on devices without TB1) TB2 clock input (not available on devices without TB2 or package options PW, RGE) SMCLK output (not available on package options PW, RGE) |
| P3.5/TB1.2/CDOOUT | 25 | N/A | 27 | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE) TB1 CCR2 capture: CCI2B input, compare: Out2 (not available on devices without TB1) Comparator_D output (not available on package options PW, RGE) |
| P3.6/TB2.1/TB1CLK | 26 | N/A | 28 | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE) TB2 CCR1 capture: CCI1B input, compare: Out1 (not available on devices without TB2) TB1 clock input (not available on devices without TB1 or package options PW, RGE) |

(3) See Section 6.6 and Section 6.7 for use with BSL and JTAG functions.

Table 4-1. Signal Descriptions (continued)

| TERMINAL | | | | | I/O (1) | DESCRIPTION |
|---------------------------------------|-----|-----|-----|-----|------------|---|
| NAME | NO. | | | | | |
| | RHA | RGE | DA | PW | | |
| P3.7/TB2.2 | 27 | N/A | 29 | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE) TB2 CCR2 capture: CCI2B input, compare: Out2 (not available on devices without TB2 or package options PW, RGE) |
| P1.6/TB1.1/UCB0SIMO/ UCB0SDA/TA0.0 | 28 | 16 | 30 | 22 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 TB1 CCR1 capture: CCI1A input, compare: Out1 (not available on devices without TB1) Slave in, master out – eUSCI_B0 SPI mode I ² C data – eUSCI_B0 I ² C mode TA0 CCR0 capture: CCI0A input, compare: Out0 |
| P1.7/TB1.2/UCB0SOMI/ UCB0SCL/TA1.0 | 29 | 17 | 31 | 23 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 TB1 CCR2 capture: CCI2A input, compare: Out2 (not available on devices without TB1) Slave out, master in – eUSCI_B0 SPI mode I ² C clock – eUSCI_B0 I ² C mode TA1 CCR0 capture: CCI0A input, compare: Out0 |
| VCORE (4) | 30 | 18 | 32 | 24 | | Regulated core power supply (internal use only, no external current loading) |
| DVSS | 31 | 19 | 33 | 25 | | Digital ground supply |
| DVCC | 32 | 20 | 34 | 26 | | Digital power supply |
| P2.7 | 33 | N/A | 35 | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE) |
| P2.3/TA0.0/UCA1STE/ A6/CD10 | 34 | N/A | 36 | 27 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options RGE) TA0 CCR0 capture: CCI0B input, compare: Out0 (not available on package options RGE) Slave transmit enable – eUSCI_A1 SPI mode (not available on devices without eUSCI_A1) Analog input A6 – ADC (not available on devices without ADC) Comparator_D input CD10 (not available on package options RGE) |
| P2.4/TA1.0/UCA1CLK/ A7/CD11 | 35 | N/A | 37 | 28 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options RGE) TA1 CCR0 capture: CCI0B input, compare: Out0 (not available on package options RGE) Clock signal input – eUSCI_A1 SPI slave mode, Clock signal output – eUSCI_A1 SPI master mode (not available on devices without eUSCI_A1) Analog input A7 – ADC (not available on devices without ADC) Comparator_D input CD11 (not available on package options RGE) |
| AVSS | 36 | N/A | 38 | N/A | | Analog ground supply |
| PJ.4/XIN | 37 | 21 | 1 | 1 | I/O | General-purpose digital I/O Input terminal for crystal oscillator XT1 |
| PJ.5/XOUT | 38 | 22 | 2 | 2 | I/O | General-purpose digital I/O Output terminal of crystal oscillator XT1 |
| AVSS | 39 | 23 | 3 | 3 | | Analog ground supply |
| AVCC | 40 | 24 | 4 | 4 | | Analog power supply |
| QFN Pad | Pad | Pad | N/A | N/A | | QFN package pad. Connection to VSS recommended. |

(4) V_{CORE} is for internal use only. No external current loading is possible. V_{CORE} should only be connected to the recommended capacitor value, C_{VCORE}.

5 Specifications

5.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|--|------|-----------------------|------|
| Voltage applied at V _{CC} to V _{SS} | -0.3 | 4.1 | V |
| Voltage applied to any pin (excluding V _{CORE}) ⁽²⁾ | -0.3 | V _{CC} + 0.3 | V |
| Diode current at any device pin | | ±2 | mA |
| Maximum junction temperature, T _J | | 95 | °C |
| Storage temperature T _{stg} ^{(3) (4) (5)} | -55 | 125 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to V_{SS}. V_{CORE} is for internal device use only. No external DC loading or voltage should be applied.
- (3) Data retention on FRAM cannot be ensured when exceeding the specified maximum storage temperature, T_{stg}.
- (4) For soldering during board manufacturing, it is required to follow the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.
- (5) Programming of devices with user application code should only be performed after reflow or hand soldering. Factory programmed information, such as calibration values, are designed to withstand the temperatures reached in the current JEDEC J-STD-020 specification.

5.2 ESD Ratings

| | VALUE | UNIT |
|--|--|-------|
| V _(ESD) Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±1000 |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±250 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

| | MIN | NOM | MAX | UNIT | |
|---|---|-----|-----|------|-----|
| V _{CC} Supply voltage during program execution and FRAM programming (AVCC = DVCC) ⁽¹⁾ | 2.0 | | 3.6 | V | |
| V _{SS} Supply voltage (AVSS = DVSS) | | 0 | | V | |
| T _A Operating free-air temperature | -40 | | 85 | °C | |
| T _J Operating junction temperature | -40 | | 85 | °C | |
| C _{VCORE} Required capacitor at V _{CORE} ⁽²⁾ | | 470 | | nF | |
| C _{VCC} /C _{VCORE} Capacitor ratio of V _{CC} to V _{CORE} | | 10 | | | |
| f _{SYSTEM} Processor frequency (maximum MCLK frequency) ⁽³⁾ | No FRAM wait states ⁽⁴⁾ , 2 V ≤ V _{CC} ≤ 3.6 V | | 0 | 8.0 | MHz |

- (1) TI recommends powering AVCC and DVCC from the same source. A maximum difference of 0.3 V between AVCC and DVCC can be tolerated during power up and operation.
- (2) A capacitor tolerance of ±20% or better is required.
- (3) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.
- (4) When using manual wait state control, see the *MSP430FR57xx Family User's Guide* for recommended settings for common system frequencies.

5.4 Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)⁽¹⁾ ⁽²⁾ ⁽³⁾

| PARAMETER | EXECUTION MEMORY | V _{CC} | Frequency (f _{MCLK} = f _{SMCLK}) | | | | | | UNIT |
|--|------------------------------|-----------------|---|------|-------|------|-------|------|------|
| | | | 1 MHz | | 4 MHz | | 8 MHz | | |
| | | | TYP | MAX | TYP | MAX | TYP | MAX | |
| I _{AM, FRAM_UNI} ⁽⁴⁾ | FRAM | 3 V | 0.27 | | 0.58 | | 1.0 | | mA |
| I _{AM,0%} ⁽⁵⁾ | FRAM 0% cache hit ratio | 3 V | 0.42 | 0.73 | 1.2 | 1.6 | 2.2 | 2.8 | mA |
| I _{AM,50%} ^{(5) (6)} | FRAM 50% cache hit ratio | 3 V | 0.31 | | 0.73 | | 1.3 | | mA |
| I _{AM,66%} ^{(5) (6)} | FRAM 66% cache hit ratio | 3 V | 0.27 | | 0.58 | | 1.0 | | mA |
| I _{AM,75%} ^{(5) (6)} | FRAM 75% cache hit ratio | 3 V | 0.25 | | 0.5 | | 0.82 | | mA |
| I _{AM,100%} ^{(5) (6)} | FRAM 100% cache hit ratio | 3 V | 0.2 | 0.43 | 0.3 | 0.55 | 0.42 | 0.8 | mA |
| I _{AM, RAM} ^{(6) (7)} | RAM | 3 V | 0.2 | 0.4 | 0.35 | 0.55 | 0.55 | 0.75 | mA |

- (1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance are chosen to closely match the required 9 pF.
- (3) Characterized with program executing typical data processing.
- (4) Program and data reside entirely in FRAM. No wait states enabled. DCORSEL = 0, DCOFSELx = 3 (f_{DCO} = 8 MHz). MCLK = SMCLK.
- (5) Program resides in FRAM. Data resides in SRAM. Average current dissipation varies with cache hit-to-miss ratio as specified. Cache hit ratio represents number cache accesses divided by the total number of FRAM accesses. For example, a 25% ratio implies one of every four accesses is from cache, the remaining are FRAM accesses.
For 1, 4, and 8 MHz, DCORSEL = 0, DCOFSELx = 3 (f_{DCO} = 8 MHz). MCLK = SMCLK. No wait states enabled.
- (6) See Figure 5-1 for typical curves. Each characteristic equation shown in the graph is computed using the least squares method for best linear fit using the typical data shown in .
f_{ACLK} = 32786 Hz, f_{MCLK} = f_{SMCLK} at specified frequency. No peripherals active.
XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0.
- (7) All execution is from RAM.
For 1, 4, and 8 MHz, DCORSEL = 0, DCOFSELx = 3 (f_{DCO} = 8 MHz). MCLK = SMCLK.

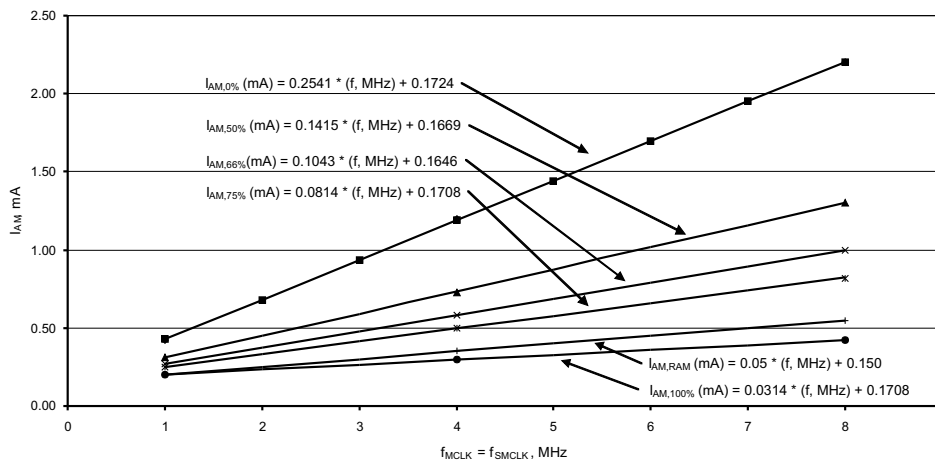


Figure 5-1. Typical Active Mode Supply Currents, No Wait States

5.5 Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) ⁽¹⁾ ⁽²⁾

| PARAMETER | V_{CC} | -40°C | | 25°C | | 60°C | | 85°C | | UNIT |
|---|-------------|-------|-----|------|------|------|-----|------|------|---------|
| | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM0,1MHz}$ Low-power mode 0 ⁽³⁾ ⁽⁴⁾ | 2 V, 3 V | 166 | | 175 | | 190 | | 225 | | μA |
| $I_{LPM0,8MHz}$ Low-power mode 0 ⁽⁵⁾ ⁽⁴⁾ | 2 V, 3 V | 170 | | 177 | 244 | 195 | | 225 | 360 | μA |
| $I_{LPM0,24MHz}$ Low-power mode 0 ⁽⁶⁾ ⁽⁴⁾ | 2 V, 3 V | 274 | | 285 | 340 | 315 | | 340 | 455 | μA |
| I_{LPM2} Low-power mode 2 ⁽⁷⁾ ⁽⁸⁾ | 2 V, 3 V | 56 | | 61 | 80 | 75 | | 110 | 210 | μA |
| $I_{LPM3,XT1LF}$ Low-power mode 3, crystal mode ⁽⁹⁾ ⁽⁸⁾ | 2 V, 3 V | 3.4 | | 6.4 | 15 | 18 | | 48 | 150 | μA |
| $I_{LPM3,VLO}$ Low-power mode 3, VLO mode ⁽¹⁰⁾ ⁽⁸⁾ | 2 V, 3 V | 3.3 | | 6.3 | 15 | 18 | | 48 | 150 | μA |
| I_{LPM4} Low-power mode 4 ⁽¹¹⁾ ⁽⁸⁾ | 2 V, 3 V | 2.9 | | 5.9 | 15 | 18 | | 48 | 150 | μA |
| $I_{LPM3.5}$ Low-power mode 3.5 ⁽¹²⁾ | 2 V, 3 V | 1.3 | | 1.5 | 2.2 | 1.9 | | 2.8 | 5.0 | μA |
| $I_{LPM4.5}$ Low-power mode 4.5 ⁽¹³⁾ | 2 V, 3 V | 0.3 | | 0.32 | 0.66 | 0.38 | | 0.57 | 2.55 | μA |

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance are chosen to closely match the required 9 pF.

(3) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVE_x = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = 1 MHz. DCORSEL = 0, DCOFSEL_x = 3 (f_{DCO} = 8 MHz)

(4) Current for brownout, high-side supervisor (SVS_H), and low-side supervisor (SVS_L) included.

(5) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVE_x = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = 8 MHz. DCORSEL = 0, DCOFSEL_x = 3 (f_{DCO} = 8 MHz)

(6) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVE_x = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = 24 MHz. DCORSEL = 1, DCOFSEL_x = 3 (f_{DCO} = 24 MHz)

(7) Current for watchdog timer (clocked by ACLK) and RTC (clocked by XT1 LF mode) included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVE_x = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 0 MHz, DCORSEL = 0, DCOFSEL_x = 3, DCO bias generator enabled.

(8) Current for brownout and high-side supervisor (SVS_H) included. Low-side supervisor (SVS_L) disabled.

(9) Current for watchdog timer (clocked by ACLK) and RTC (clocked by XT1 LF mode) included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVE_x = 0).

CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz

(10) Current for watchdog timer (clocked by ACLK) included. ACLK = VLO.

CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), f_{ACLK} = f_{VLO} , f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz

(11) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4), f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz

(12) Internal regulator disabled. No data retention. RTC active clocked by XT1 LF mode.

CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM3.5), f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz

(13) Internal regulator disabled. No data retention.

CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5), f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz

5.6 Thermal Resistance Characteristics

| PARAMETER | | PACKAGE | VALUE ⁽¹⁾ | UNIT |
|-----------------------|--|---------------|----------------------|------|
| θ_{JA} | Junction-to-ambient thermal resistance, still air ⁽²⁾ | TSSOP-24 (PW) | 78.8 | °C/W |
| $\theta_{JC(TOP)}$ | Junction-to-case (top) thermal resistance ⁽³⁾ | | 19.4 | °C/W |
| θ_{JB} | Junction-to-board thermal resistance ⁽⁴⁾ | | 36.7 | °C/W |
| Ψ_{JB} | Junction-to-board thermal characterization parameter | | 36.2 | °C/W |
| Ψ_{JT} | Junction-to-top thermal characterization parameter | | 0.5 | °C/W |
| $\theta_{JC(BOTTOM)}$ | Junction-to-case (bottom) thermal resistance ⁽⁵⁾ | | N/A | °C/W |
| θ_{JA} | Junction-to-ambient thermal resistance, still air ⁽²⁾ | QFN-24 (RGE) | 42.1 | °C/W |
| $\theta_{JC(TOP)}$ | Junction-to-case (top) thermal resistance ⁽³⁾ | | 38.8 | °C/W |
| θ_{JB} | Junction-to-board thermal resistance ⁽⁴⁾ | | 18.1 | °C/W |
| Ψ_{JB} | Junction-to-board thermal characterization parameter | | 18.0 | °C/W |
| Ψ_{JT} | Junction-to-top thermal characterization parameter | | 0.6 | °C/W |
| $\theta_{JC(BOTTOM)}$ | Junction-to-case (bottom) thermal resistance ⁽⁵⁾ | | 2.8 | °C/W |
| θ_{JA} | Junction-to-ambient thermal resistance, still air ⁽²⁾ | SOIC-38 (DA) | 74.5 | °C/W |
| $\theta_{JC(TOP)}$ | Junction-to-case (top) thermal resistance ⁽³⁾ | | 22.0 | °C/W |
| θ_{JB} | Junction-to-board thermal resistance ⁽⁴⁾ | | 40.7 | °C/W |
| Ψ_{JB} | Junction-to-board thermal characterization parameter | | 40.3 | °C/W |
| Ψ_{JT} | Junction-to-top thermal characterization parameter | | 0.9 | °C/W |
| $\theta_{JC(BOTTOM)}$ | Junction-to-case (bottom) thermal resistance ⁽⁵⁾ | | N/A | °C/W |
| θ_{JA} | Junction-to-ambient thermal resistance, still air ⁽²⁾ | QFN-40 (RHA) | 37.8 | °C/W |
| $\theta_{JC(TOP)}$ | Junction-to-case (top) thermal resistance ⁽³⁾ | | 27.4 | °C/W |
| θ_{JB} | Junction-to-board thermal resistance ⁽⁴⁾ | | 12.6 | °C/W |
| Ψ_{JB} | Junction-to-board thermal characterization parameter | | 12.6 | °C/W |
| Ψ_{JT} | Junction-to-top thermal characterization parameter | | 0.4 | °C/W |
| $\theta_{JC(BOTTOM)}$ | Junction-to-case (bottom) thermal resistance ⁽⁵⁾ | | 3.6 | °C/W |

(1) N/A = Not applicable

(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

(5) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

5.7 Schmitt-Trigger Inputs – General-Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5, $\overline{\text{RST/NMI}}$)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------|---|--|-----------------|------|-----|------|------|
| V _{IT+} | Positive-going input threshold voltage | | 2 V | 0.80 | | 1.40 | V |
| | | | 3 V | 1.50 | | 2.10 | |
| V _{IT-} | Negative-going input threshold voltage | | 2 V | 0.45 | | 1.10 | V |
| | | | 3 V | 0.75 | | 1.65 | |
| V _{hys} | Input voltage hysteresis (V _{IT+} – V _{IT-}) | | 2 V | 0.25 | | 0.8 | V |
| | | | 3 V | 0.30 | | 1.0 | |
| R _{Pull} | Pullup or pulldown resistor | For pullup: V _{IN} = V _{SS} For pulldown: V _{IN} = V _{CC} | | 20 | 35 | 50 | kΩ |
| C _I | Input capacitance | V _{IN} = V _{SS} or V _{CC} | | | 5 | | pF |

5.8 Inputs – Ports P1 and P2 ⁽¹⁾ (P1.0 to P1.7, P2.0 to P2.7)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|--------------------|---|-----------------|-----|-----|------|
| t _(int) | External interrupt timing ⁽²⁾ External trigger pulse duration to set interrupt flag | 2 V, 3 V | 20 | | ns |

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.

(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t_(int) is met. It may be set by trigger signals shorter than t_(int).

5.9 Leakage Current – General-Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5, $\overline{\text{RST/NMI}}$)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|------------------------|---|-----------------|-----|-----|------|
| I _{lkg(Px.x)} | High-impedance leakage current ⁽¹⁾ ⁽²⁾ | 2 V, 3 V | -50 | 50 | nA |

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

5.10 Outputs – General-Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------|---------------------------|---|-----------------|------------------------|------------------------|------|
| V _{OH} | High-level output voltage | I _(OHmax) = -1 mA ⁽¹⁾ | 2 V | V _{CC} - 0.25 | V _{CC} | V |
| | | I _(OHmax) = -3 mA ⁽²⁾ | | V _{CC} - 0.60 | V _{CC} | |
| | | I _(OHmax) = -2 mA ⁽¹⁾ | 3 V | V _{CC} - 0.25 | V _{CC} | |
| | | I _(OHmax) = -6 mA ⁽²⁾ | | V _{CC} - 0.60 | V _{CC} | |
| V _{OL} | Low-level output voltage | I _(OLmax) = 1 mA ⁽¹⁾ | 2 V | V _{SS} | V _{SS} + 0.25 | V |
| | | I _(OLmax) = 3 mA ⁽²⁾ | | V _{SS} | V _{SS} + 0.60 | |
| | | I _(OLmax) = 2 mA ⁽¹⁾ | 3 V | V _{SS} | V _{SS} + 0.25 | |
| | | I _(OLmax) = 6 mA ⁽²⁾ | | V _{SS} | V _{SS} + 0.60 | |

- (1) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
- (2) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

5.11 Output Frequency – General-Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5)

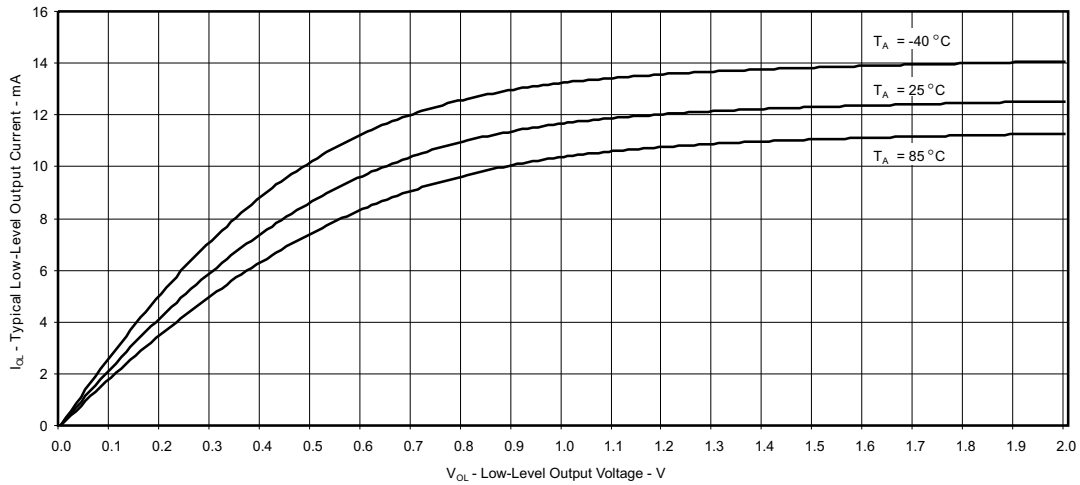
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------------|-----------------------------------|--|-----------------|-----|-----|------|
| f _{Px.y} | Port output frequency (with load) | P _{x.y} ⁽¹⁾ ⁽²⁾ | 2 V | | 16 | MHz |
| | | | 3 V | | 24 | |
| f _{Port_CLK} | Clock output frequency | ACLK, SMCLK, or MCLK at configured output port, C _L = 20 pF, no DC loading ⁽²⁾ | 2 V | | 16 | MHz |
| | | | 3 V | | 24 | |

- (1) A resistive divider with 2 × 1.6 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. C_L = 20 pF is connected from the output to V_{SS}.
- (2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

5.12 Typical Characteristics – Outputs

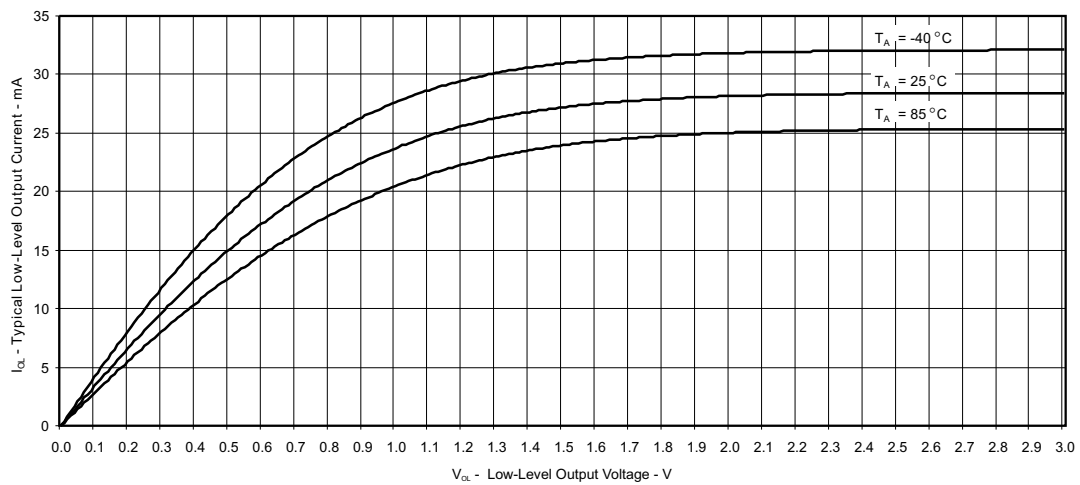
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)



V_{CC} = 2.0 V

Measured at Px.y

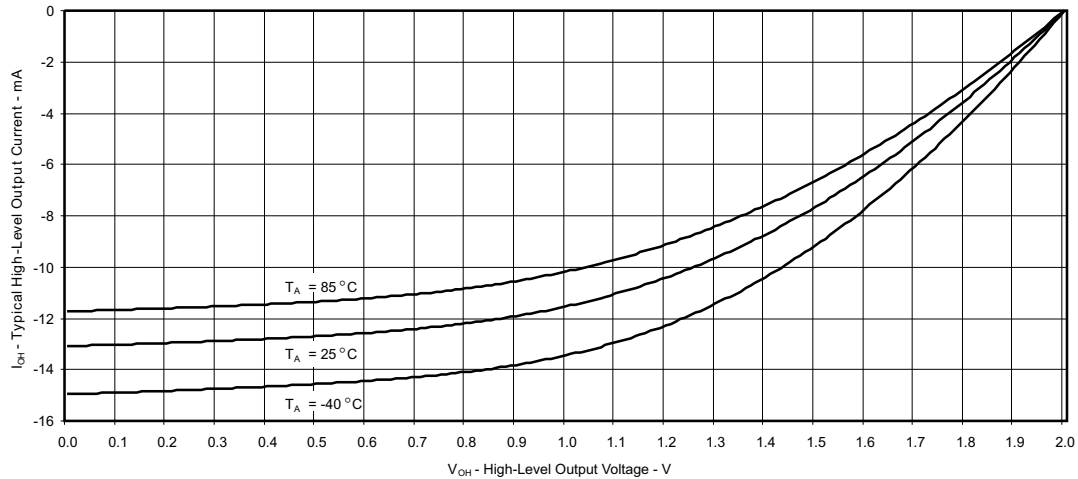
Figure 5-2. Typical Low-Level Output Current vs Low-Level Output Voltage



V_{CC} = 3.0 V

Measured at Px.y

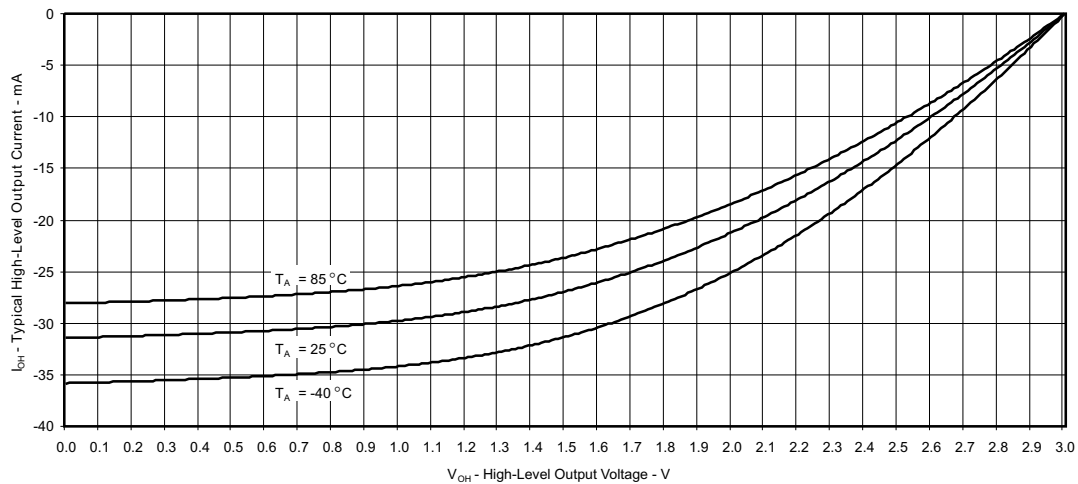
Figure 5-3. Typical Low-Level Output Current vs Low-Level Output Voltage



$V_{CC} = 2.0$ V

Measured at Px.y

Figure 5-4. Typical High-Level Output Current vs High-Level Output Voltage



$V_{CC} = 3.0$ V

Measured at Px.y

Figure 5-5. Typical High-Level Output Current vs High-Level Output Voltage

5.13 Crystal Oscillator, XT1, Low-Frequency (LF) Mode ⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|--|--|-----------------|-----|--------|-------|------------|
| $\Delta I_{VCC,LF}$ | Additional current consumption XT1 LF mode from lowest drive setting | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {1}, $C_{L,eff} = 9$ pF, $T_A = 25^\circ\text{C}$, | 3 V | | 60 | | nA |
| | | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {2}, $T_A = 25^\circ\text{C}$, $C_{L,eff} = 9$ pF | 3 V | | 90 | | |
| | | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {3}, $T_A = 25^\circ\text{C}$, $C_{L,eff} = 12$ pF | 3 V | | 140 | | |
| $f_{XT1,LF0}$ | XT1 oscillator crystal frequency, LF mode | XTS = 0, XT1BYPASS = 0 | | | 32768 | | Hz |
| $f_{XT1,LF,SW}$ | XT1 oscillator logic-level square-wave input frequency, LF mode | XTS = 0, XT1BYPASS = 1 ⁽²⁾ ⁽³⁾ | | 10 | 32.768 | 50 | kHz |
| OA_{LF} | Oscillation allowance for LF crystals ⁽⁴⁾ | XTS = 0, XT1BYPASS = 0, XT1DRIVE = {0}, $f_{XT1,LF} = 32768$ Hz, $C_{L,eff} = 6$ pF | | | 210 | | k Ω |
| | | XTS = 0, XT1BYPASS = 0, XT1DRIVE = {3}, $f_{XT1,LF} = 32768$ Hz, $C_{L,eff} = 12$ pF | | | 300 | | |
| | Duty cycle, LF mode | XTS = 0, Measured at ACLK, $f_{XT1,LF} = 32768$ Hz | | 30% | | 70% | |
| $f_{Fault,LF}$ | Oscillator fault frequency, LF mode ⁽⁵⁾ | XTS = 0 ⁽⁶⁾ | | 10 | | 10000 | Hz |
| $t_{START,LF}$ | Start-up time, LF mode ⁽⁷⁾ | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {0}, $T_A = 25^\circ\text{C}$, $C_{L,eff} = 6$ pF | 3 V | | 1000 | | ms |
| | | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {3}, $T_A = 25^\circ\text{C}$, $C_{L,eff} = 12$ pF | | | 1000 | | |
| $C_{L,eff}$ | Integrated effective load capacitance, LF mode ⁽⁸⁾ ⁽⁹⁾ | XTS = 0 | | | 1 | | pF |

- (1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
 - Keep the trace between the device and the crystal as short as possible.
 - Design a good ground plane around the oscillator pins.
 - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 - Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
 - If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.
- (3) Maximum frequency of operation of the entire device cannot be exceeded.
- (4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
 - For XT1DRIVE = {0}, $C_{L,eff} \leq 6$ pF.
 - For XT1DRIVE = {1}, $6 \text{ pF} \leq C_{L,eff} \leq 9$ pF.
 - For XT1DRIVE = {2}, $6 \text{ pF} \leq C_{L,eff} \leq 10$ pF.
 - For XT1DRIVE = {3}, $6 \text{ pF} \leq C_{L,eff} \leq 12$ pF.
- (5) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
- (6) Measured with logic-level input frequency but also applies to operation with crystals.
- (7) Includes start-up counter of 4096 clock cycles.
- (8) Requires external capacitors at both terminals.
- (9) Values are specified by crystal manufacturers. Include parasitic bond and package capacitance (approximately 2 pF per pin). Recommended values supported are 6 pF, 9 pF, and 12 pF. Maximum shunt capacitance of 1.6 pF.

5.14 Crystal Oscillator, XT1, High-Frequency (HF) Mode ⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------|---|--|-----------------|-----|-----|-----|------|
| I _{VCC,HF} | XT1 oscillator crystal current HF mode | f _{OSC} = 4 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE = {0}, T _A = 25°C, C _{L,eff} = 16 pF | 3 V | | 175 | | μA |
| | | f _{OSC} = 8 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE = {1}, T _A = 25°C, C _{L,eff} = 16 pF | | | 300 | | |
| | | f _{OSC} = 16 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE = {2}, T _A = 25°C, C _{L,eff} = 16 pF | | | 350 | | |
| | | f _{OSC} = 24 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE = {3}, T _A = 25°C, C _{L,eff} = 16 pF | | | 550 | | |
| f _{XT1,HF0} | XT1 oscillator crystal frequency, HF mode 0 | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {0} ⁽²⁾ | | 4 | | 6 | MHz |
| f _{XT1,HF1} | XT1 oscillator crystal frequency, HF mode 1 | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {1} ⁽²⁾ | | 6 | | 10 | MHz |
| f _{XT1,HF2} | XT1 oscillator crystal frequency, HF mode 2 | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {2} ⁽²⁾ | | 10 | | 16 | MHz |
| f _{XT1,HF3} | XT1 oscillator crystal frequency, HF mode 3 | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {3} ⁽²⁾ | | 16 | | 24 | MHz |
| f _{XT1,HF,SW} | XT1 oscillator logic-level square-wave input frequency, HF mode | XTS = 1, XT1BYPASS = 1 ^{(3) (2)} | | 1 | | 24 | MHz |
| O _{AHF} | Oscillation allowance for HF crystals ⁽⁴⁾ | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {0}, f _{XT1,HF} = 4 MHz, C _{L,eff} = 16 pF | | | 450 | | Ω |
| | | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {1}, f _{XT1,HF} = 8 MHz, C _{L,eff} = 16 pF | | | 320 | | |
| | | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {2}, f _{XT1,HF} = 16 MHz, C _{L,eff} = 16 pF | | | 200 | | |
| | | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {3}, f _{XT1,HF} = 24 MHz, C _{L,eff} = 16 pF | | | 200 | | |
| t _{START,HF} | Start-up time, HF mode ⁽⁵⁾ | f _{OSC} = 4 MHz, XTS = 1, XT1BYPASS = 0, XT1DRIVE = {0}, T _A = 25°C, C _{L,eff} = 16 pF | 3 V | | 8 | | ms |
| | | f _{OSC} = 24 MHz, XTS = 1, XT1BYPASS = 0, XT1DRIVE = {3}, T _A = 25°C, C _{L,eff} = 16 pF | | | | 2 | |

- (1) To improve EMI on the XT1 oscillator the following guidelines should be observed.
- Keep the traces between the device and the crystal as short as possible.
 - Design a good ground plane around the oscillator pins.
 - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 - Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
 - If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) Maximum frequency of operation of the entire device cannot be exceeded.
- (3) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.
- (4) Oscillation allowance is based on a safety factor of 5 for recommended crystals.
- (5) Includes start-up counter of 4096 clock cycles.

Crystal Oscillator, XT1, High-Frequency (HF) Mode ⁽¹⁾ (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|---|---|-----------------|-----|-----|-----|------|
| C _{L,eff} | Integrated effective load capacitance ⁽⁶⁾ ⁽⁷⁾ | XTS = 1 | | | 1 | | pF |
| | Duty cycle, HF mode | XTS = 1, Measured at ACLK, f _{X_{T1},HF2} = 24 MHz | | 40% | 50% | 60% | |
| f _{Fault,HF} | Oscillator fault frequency, HF mode ⁽⁸⁾ | XTS = 1 ⁽⁹⁾ | | 145 | | 900 | kHz |

- (6) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (7) Requires external capacitors at both terminals. Values are specified by crystal manufacturers. Recommended values supported are 14 pF, 16 pF, and 18 pF. Maximum shunt capacitance of 7 pF.
- (8) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.
- (9) Measured with logic-level input frequency but also applies to operation with crystals.

5.15 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------------------|------------------------------------|---------------------------------|-----------------|-----|-----|-----|------|
| f _{VLO} | VLO frequency | Measured at ACLK | 2 V to 3.6 V | 5 | 8.3 | 13 | kHz |
| df _{VLO} /dT | VLO frequency temperature drift | Measured at ACLK ⁽¹⁾ | 2 V to 3.6 V | | 0.5 | | %/°C |
| df _{VLO} /dV _{CC} | VLO frequency supply voltage drift | Measured at ACLK ⁽²⁾ | 2 V to 3.6 V | | 4 | | %/V |
| f _{VLO,DC} | Duty cycle | Measured at ACLK | 2 V to 3.6 V | 40% | 50% | 60% | |

- (1) Calculated using the box method: (MAX(−40°C to 85°C) – MIN(−40°C to 85°C)) / MIN(−40°C to 85°C) / (85°C – (−40°C))
- (2) Calculated using the box method: (MAX(2.0 V to 3.6 V) – MIN(2.0 V to 3.6 V)) / MIN(2.0 V to 3.6 V) / (3.6 V – 2 V)

NOTE

In LPM3, the VLO frequency varies by up to ±6% (typical), due to bias current sampling. This frequency variation is not a violation VLO specifications (see [Section 5.15](#)).

5.16 DCO Frequencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CC} T_A | MIN | TYP | MAX | UNIT |
|---------------|-----------------------------|---|-------------------------------|-----|------|-------|------|
| $f_{DCO,LO}$ | DCO frequency low, trimmed | Measured at ACLK, DCORSEL = 0 | 2 V to 3.6 V –40°C to 85°C | | 5.37 | ±3.5% | MHz |
| | | | 2 V to 3.6 V 0°C to 50°C | | 5.37 | ±2.0% | |
| $f_{DCO,MID}$ | DCO frequency mid, trimmed | Measured at ACLK, DCORSEL = 0 | 2 V to 3.6 V –40°C to 85°C | | 6.67 | ±3.5% | MHz |
| | | | 2 V to 3.6 V 0°C to 50°C | | 6.67 | ±2.0% | |
| $f_{DCO,HI}$ | DCO frequency high, trimmed | Measured at ACLK, DCORSEL = 0 | 2 V to 3.6 V –40°C to 85°C | | 8 | ±3.5% | MHz |
| | | | 2 V to 3.6 V 0°C to 50°C | | 8 | ±2.0% | |
| $f_{DCO,DC}$ | Duty cycle | Measured at ACLK, divide by 1, No external divide, all DCO settings | 2 V to 3.6 V –40°C to 85°C | 40% | 50% | 60% | |

5.17 MODOSC

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|-----------------|---------------------|-------------------------------|--------------|-----|-----|-----|------|
| I_{MODOSC} | Current consumption | Enabled | 2 V to 3.6 V | | 44 | 80 | µA |
| f_{MODOSC} | MODOSC frequency | | 2 V to 3.6 V | 4.5 | 5.0 | 5.5 | MHz |
| $f_{MODOSC,DC}$ | Duty cycle | Measured at ACLK, divide by 1 | 2 V to 3.6 V | 40% | 50% | 60% | |

5.18 PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|--------------------------------|--------------------------------|-----|-----|-----|------|
| V _{CORE(AM)} | Core voltage, active mode | 2 V ≤ DV _{CC} ≤ 3.6 V | | 1.5 | | V |
| V _{CORE(LPM)} | Core voltage, low-current mode | 2 V ≤ DV _{CC} ≤ 3.6 V | | 1.5 | | V |

5.19 PMM, SVS, BOR

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|---|---------------------------------|------|------|------|------|
| I _{SVSH,AM} | SVS _H current consumption, active mode | V _{CC} = 3.6 V | | 5 | | μA |
| I _{SVSH,LPM} | SVS _H current consumption, low power modes | V _{CC} = 3.6 V | | 0.8 | 1.5 | μA |
| V _{SVSH-} | SVS _H on voltage level, falling supply voltage | | 1.83 | 1.88 | 1.93 | V |
| V _{SVSH+} | SVS _H off voltage level, rising supply voltage | | 1.88 | 1.93 | 1.98 | V |
| t _{PD,SVSH, AM} | SVS _H propagation delay, active mode | dV _{CC} /dt = 10 mV/μs | | 10 | | μs |
| t _{PD,SVSH, LPM} | SVS _H propagation delay, low power modes | dV _{CC} /dt = 1 mV/μs | | 30 | | μs |
| I _{SVSL} | SVS _L current consumption | | | 0.3 | 0.5 | μA |
| V _{SVSL-} | SVS _L on voltage level | | | 1.42 | | V |
| V _{SVSL+} | SVS _L off voltage level | | | 1.47 | | V |

5.20 Wake-up Times From Low-Power Modes

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} T _A | MIN | TYP | MAX | UNIT |
|-----------------------------|---|---------------------------------|-----------------------------------|-----|------|------|------|
| t _{WAKE-UP LPM0} | Wake-up time from LPM0 to active mode ⁽¹⁾ | | 2 V, 3 V -40°C to 85°C | | 0.58 | 1 | μs |
| t _{WAKE-UP LPM12} | Wake-up time from LPM1, LPM2 to active mode ⁽¹⁾ | | 2 V, 3 V -40°C to 85°C | | 12 | 25 | μs |
| t _{WAKE-UP LPM34} | Wake-up time from LPM3 or LPM4 to active mode ⁽¹⁾ | | 2 V, 3 V -40°C to 85°C | | 78 | 120 | μs |
| t _{WAKE-UP LPMx.5} | Wake-up time from LPM3.5 or LPM4.5 to active mode ⁽¹⁾ | | 2 V, 3 V 0°C to 85°C | | 310 | 575 | μs |
| | | | 2 V, 3 V -40°C to 85°C | | 310 | 1100 | |
| t _{WAKE-UP RESET} | Wake-up time from $\overline{\text{RST}}$ to active mode ⁽²⁾ | V _{CC} stable | 2 V, 3 V -40°C to 85°C | | 230 | 280 | μs |
| t _{WAKE-UP BOR} | Wake-up time from BOR or power-up to active mode | dV _{CC} /dt = 2400 V/s | 2 V, 3 V -40°C to 85°C | | 1.6 | | ms |
| t _{RESET} | Pulse duration required at $\overline{\text{RST}}$ /NMI terminal to accept a reset event ⁽³⁾ | | 2 V, 3 V -40°C to 85°C | | 4 | | ns |

- (1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.
- (2) The wake-up time is measured from the rising edge of the $\overline{\text{RST}}$ signal until the first instruction of the user program is executed.
- (3) Meeting or exceeding this time makes sure a reset event occurs. Pulses shorter than this minimum time may or may not cause a reset event to occur.

5.21 Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|-------------------------------|---|-----------------|-----|-----|-----|------|
| f _{TA} | Timer_A input clock frequency | Internal: SMCLK, ACLK External: TACLK Duty cycle = 50% ±10% | 2 V, 3 V | | | 8 | MHz |
| t _{TA,cap} | Timer_A capture timing | All capture inputs, Minimum pulse duration required for capture | 2 V, 3 V | 20 | | | ns |

5.22 Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|-------------------------------|---|-----------------|-----|-----|-----|------|
| f _{TB} | Timer_B input clock frequency | Internal: SMCLK, ACLK External: TBCLK Duty cycle = 50% ±10% | 2 V, 3 V | | | 8 | MHz |
| t _{TB,cap} | Timer_B capture timing | All capture inputs, Minimum pulse duration required for capture | 2 V, 3 V | 20 | | | ns |

5.23 eUSCI (UART Mode) Clock Frequency

| PARAMETER | | CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|---|--|-----------------|-----|---------------------|-----|------|
| f _{eUSCI} | eUSCI input clock frequency | Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ±10% | | | f _{SYSTEM} | | MHz |
| f _{BITCLK} | BITCLK clock frequency (equals baud rate in MBaud) | | | | | 5 | MHz |

5.24 eUSCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------|---|-----------------|-----------------|-----|-----|-----|------|
| t _t | UART receive deglitch time ⁽¹⁾ | UCGLITx = 0 | 2 V, 3 V | 5 | 15 | 20 | ns |
| | | UCGLITx = 1 | | 20 | 45 | 60 | |
| | | UCGLITx = 2 | | 35 | 80 | 120 | |
| | | UCGLITx = 3 | | 50 | 110 | 180 | |

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

5.25 eUSCI (SPI Master Mode) Clock Frequency

| PARAMETER | | CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--------------------|-----------------------------|--|-----------------|-----|-----|---------------------|------|
| f _{eUSCI} | eUSCI input clock frequency | Internal: SMCLK, ACLK Duty cycle = 50% ±10% | | | | f _{SYSTEM} | MHz |

5.26 eUSCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) ⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|--|--|-----------------|-----|-----|-----|------------------|
| t _{STE,LEAD} | STE lead time, STE active to clock | UCSTEM = 0, UCMODE _x = 01 or 10 | 2 V, 3 V | 1 | | | UCxCLK cycles |
| | | UCSTEM = 1, UCMODE _x = 01 or 10 | 2 V, 3 V | 1 | | | |
| t _{STE,LAG} | STE lag time, Last clock to STE inactive | UCSTEM = 0, UCMODE _x = 01 or 10 | 2 V, 3 V | 1 | | | UCxCLK cycles |
| | | UCSTEM = 1, UCMODE _x = 01 or 10 | 2 V, 3 V | 1 | | | |
| t _{STE,ACC} | STE access time, STE active to SIMO data out | UCSTEM = 0, UCMODE _x = 01 or 10 | 2 V, 3 V | | | 55 | ns |
| | | UCSTEM = 1, UCMODE _x = 01 or 10 | 2 V, 3 V | | | 35 | |
| t _{STE,DIS} | STE disable time, STE inactive to SIMO high impedance | UCSTEM = 0, UCMODE _x = 01 or 10 | 2 V, 3 V | | | 40 | ns |
| | | UCSTEM = 1, UCMODE _x = 01 or 10 | 2 V, 3 V | | | 30 | |
| t _{SU,MI} | SOMI input data setup time | | 2 V | 35 | | | ns |
| | | | 3 V | 35 | | | |
| t _{HD,MI} | SOMI input data hold time | | 2 V | 0 | | | ns |
| | | | 3 V | 0 | | | |
| t _{VALID,MO} | SIMO output data valid time ⁽²⁾ | UCLK edge to SIMO valid, C _L = 20 pF | 2 V | | | 30 | ns |
| | | | 3 V | | | 30 | |
| t _{HD,MO} | SIMO output data hold time ⁽³⁾ | C _L = 20 pF | 2 V | 0 | | | ns |
| | | | 3 V | 0 | | | |

- (1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO}(eUSCI) + t_{SU,SI}(Slave), t_{SU,MI}(eUSCI) + t_{VALID,SO}(Slave))$.
For the slave parameters $t_{SU,SI}(Slave)$ and $t_{VALID,SO}(Slave)$ see the SPI parameters of the attached slave.
- (2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-6](#) and [Figure 5-7](#).
- (3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in [Figure 5-6](#) and [Figure 5-7](#).

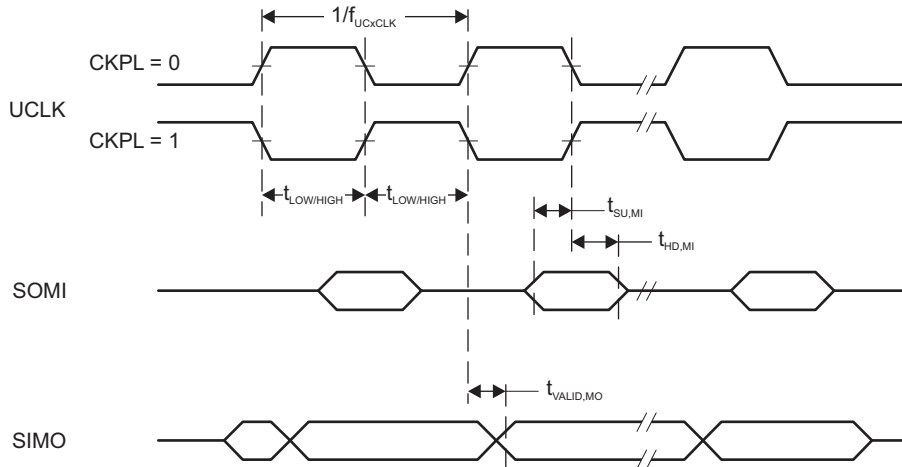


Figure 5-6. SPI Master Mode, CKPH = 0

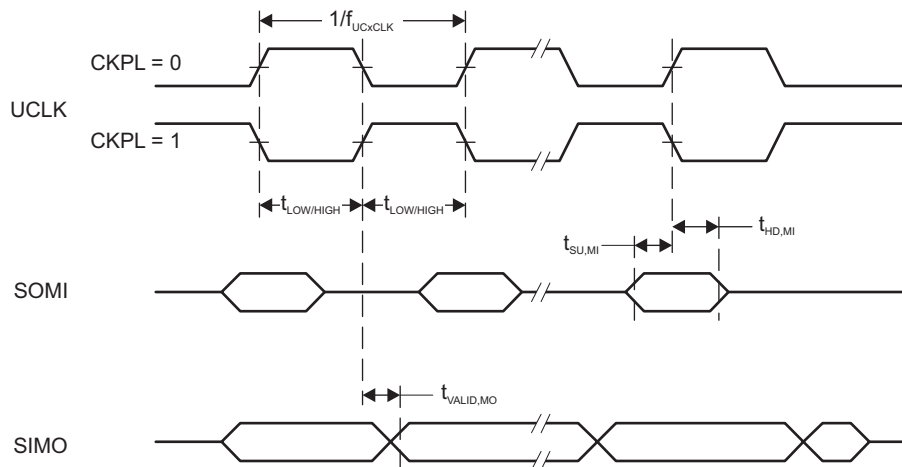


Figure 5-7. SPI Master Mode, CKPH = 1

5.27 eUSCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) ⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|---|--|-----------------|-----|-----|-----|------|
| t _{STE,LEAD} | STE lead time, STE active to clock | | 2 V | 7 | | | ns |
| | | | 3 V | 7 | | | |
| t _{STE,LAG} | STE lag time, Last clock to STE inactive | | 2 V | 0 | | | ns |
| | | | 3 V | 0 | | | |
| t _{STE,ACC} | STE access time, STE active to SOMI data out | | 2 V | | | 65 | ns |
| | | | 3 V | | | 40 | |
| t _{STE,DIS} | STE disable time, STE inactive to SOMI high impedance | | 2 V | | | 40 | ns |
| | | | 3 V | | | 35 | |
| t _{SU,SI} | SIMO input data setup time | | 2 V | 2 | | | ns |
| | | | 3 V | 2 | | | |
| t _{HD,SI} | SIMO input data hold time | | 2 V | 5 | | | ns |
| | | | 3 V | 5 | | | |
| t _{VALID,SO} | SOMI output data valid time ⁽²⁾ | UCLK edge to SOMI valid, C _L = 20 pF | 2 V | | | 30 | ns |
| | | | 3 V | | | 30 | |
| t _{HD,SO} | SOMI output data hold time ⁽³⁾ | C _L = 20 pF | 2 V | 4 | | | ns |
| | | | 3 V | 4 | | | |

- (1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$.
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ see the SPI parameters of the attached slave.
- (2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-8](#) and [Figure 5-9](#).
- (3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-8](#) and [Figure 5-9](#).

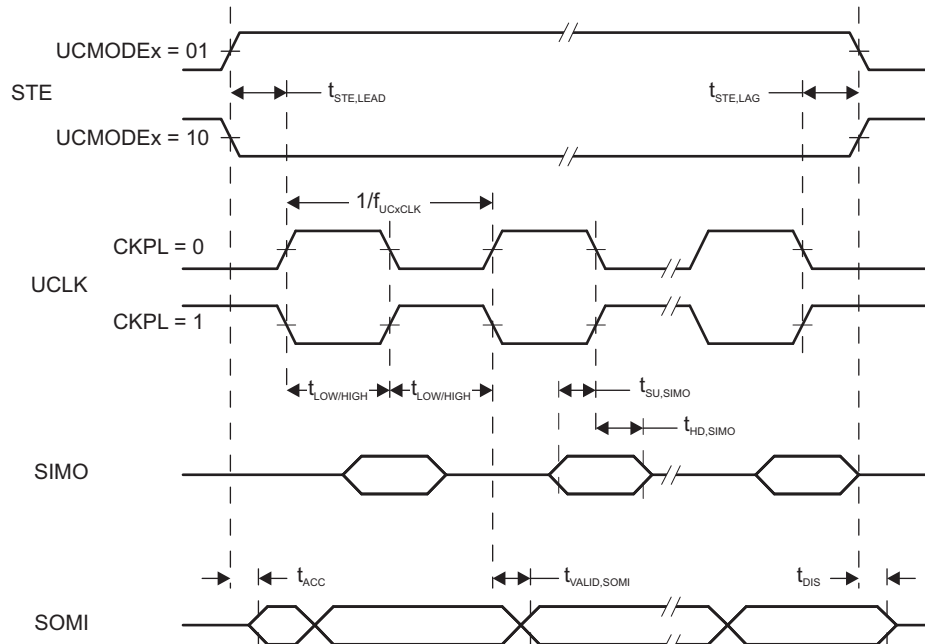


Figure 5-8. SPI Slave Mode, CKPH = 0

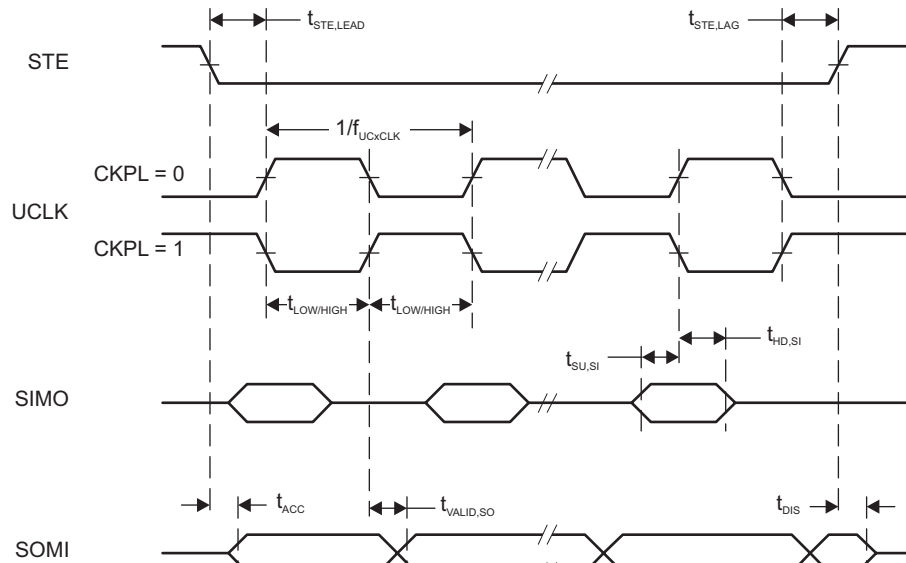


Figure 5-9. SPI Slave Mode, CKPH = 1

5.28 eUSCI (I²C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5-10](#))

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------------|---|--|------|-----|---------------------|------|
| f _{eUSCI} | eUSCI input clock frequency Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ±10% | | | | f _{SYSTEM} | MHz |
| f _{SCL} | SCL clock frequency | 2 V, 3 V | 0 | | 400 | kHz |
| t _{HD,STA} | Hold time (repeated) START | f _{SCL} = 100 kHz 2 V, 3 V | 4.0 | | | μs |
| t _{SU,STA} | Setup time for a repeated START | f _{SCL} = 100 kHz 2 V, 3 V | 4.7 | | | μs |
| t _{HD,DAT} | Data hold time | 2 V, 3 V | 0 | | | ns |
| t _{SU,DAT} | Data setup time | 2 V, 3 V | 250 | | | ns |
| t _{SU,STO} | Setup time for STOP | f _{SCL} = 100 kHz 2 V, 3 V | 4.0 | | | μs |
| t _{SP} | Pulse duration of spikes suppressed by input filter | UCGLITx = 0 2 V, 3 V | 50 | | 600 | ns |
| | | UCGLITx = 1 | 25 | | 300 | |
| | | UCGLITx = 2 | 12.5 | | 150 | |
| | | UCGLITx = 3 | 6.25 | | 75 | |
| t _{TIMEOUT} | Clock low time-out | UCCLTOx = 1 2 V, 3 V | | 27 | | ms |
| | | UCCLTOx = 2 | | 30 | | |
| | | UCCLTOx = 3 | | 33 | | |

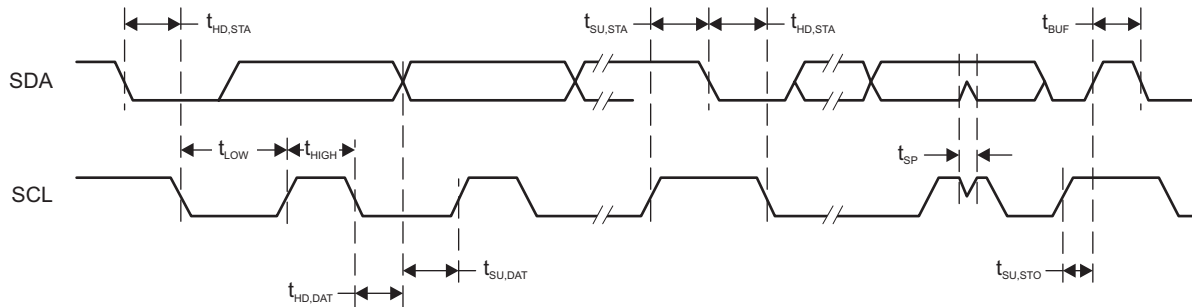


Figure 5-10. I²C Mode Timing

5.29 10-Bit ADC, Power Supply and Input Range Conditions

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------------|---|---|-----------------|-----|-----|------------------|------|
| AV _{CC} | Analog supply voltage | AV _{CC} and DV _{CC} are connected together, AV _{SS} and DV _{SS} are connected together, V _(AVSS) = V _(DVSS) = 0 V | | 2.0 | | 3.6 | V |
| V _(Ax) | Analog input voltage range | All ADC10 pins | | 0 | | AV _{CC} | V |
| I _{ADC10_A} | Operating supply current into AV _{CC} terminal, reference current not included | f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0 | 2 V | | 90 | 140 | μA |
| | | | 3 V | | 100 | 160 | |
| C _I | Input capacitance | Only one terminal Ax can be selected at one time from the pad to the ADC10_A capacitor array including wiring and pad | 2.2 V | | 6 | 8 | pF |
| R _I | Input MUX ON resistance | AV _{CC} ≥ 2 V, 0 V ≤ V _{Ax} ≤ AV _{CC} | | | | 36 | kΩ |

5.30 10-Bit ADC, Timing Parameters

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|------------------------------------|--|-----------------|------|-----|------|------|
| f _{ADC10CLK} | | For specified performance of ADC10 linearity parameters | 2 V to 3.6 V | 0.45 | 5 | 5.5 | MHz |
| f _{ADC10OSC} | Internal ADC10 oscillator (MODOSC) | ADC10DIV = 0, f _{ADC10CLK} = f _{ADC10OSC} | 2 V to 3.6 V | 4.5 | 4.5 | 5.5 | MHz |
| t _{CONVERT} | Conversion time | REFON = 0, Internal oscillator, 12 ADC10CLK cycles, 10-bit mode, f _{ADC10OSC} = 4.5 MHz to 5.5 MHz | 2 V to 3.6 V | 2.18 | | 2.67 | μs |
| | | External f _{ADC10CLK} from ACLK, MCLK, or SMCLK, ADC10SSEL ≠ 0 | 2 V to 3.6 V | | (1) | | |
| t _{ADC10ON} | Turnon settling time of the ADC | The error in a conversion started after t _{ADC10ON} is less than ±0.5 LSB, Reference and input signal already settled | | | | 100 | ns |
| t _{Sample} | Sampling time | R _S = 1000 Ω, R _I = 36000 Ω, C _I = 3.5 pF, Approximately eight Tau (τ) are required to get an error of less than ±0.5 LSB | 2 V | 1.5 | | | μs |
| | | | 3 V | 2.0 | | | |

(1) 12 × ADC10DIV × 1/f_{ADC10CLK}

5.31 10-Bit ADC, Linearity Parameters

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------|---|--|-----------------|------|-----|-----|------|
| E _I | Integral linearity error | 1.4 V ≤ (V _{eREF+} - V _{REF-/V_{eREF-}})min ≤ 1.6 V | 2 V to 3.6 V | -1.4 | | 1.4 | LSB |
| | | 1.6 V < (V _{eREF+} - V _{REF-/V_{eREF-}})min ≤ V _{AVCC} | | -1.1 | | 1.1 | |
| E _D | Differential linearity error | (V _{eREF+} - V _{REF-/V_{eREF-}})min ≤ (V _{eREF+} - V _{REF-/V_{eREF-}}) | 2 V to 3.6 V | -1 | | 1 | LSB |
| E _O | Offset error | (V _{eREF+} - V _{REF-/V_{eREF-}})min ≤ (V _{eREF+} - V _{REF-/V_{eREF-}}) | 2 V to 3.6 V | -6.5 | | 6.5 | mV |
| E _G | Gain error, external reference | (V _{eREF+} - V _{REF-/V_{eREF-}})min ≤ (V _{eREF+} - V _{REF-/V_{eREF-}}) | 2 V to 3.6 V | -1.2 | | 1.2 | LSB |
| | Gain error, internal reference ⁽¹⁾ | | | -4% | | 4% | |
| E _T | Total unadjusted error, external reference | (V _{eREF+} - V _{REF-/V_{eREF-}})min ≤ (V _{eREF+} - V _{REF-/V_{eREF-}}) | 2 V to 3.6 V | -2 | | 2 | LSB |
| | Total unadjusted error, internal reference ⁽¹⁾ | | | -4% | | 4% | |

(1) Error is dominated by the internal reference.

5.32 REF, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) ⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|---|---|-----------------|-----|-----|------------------|------|
| V _{eREF+} | Positive external reference voltage input | V _{eREF+} > V _{eREF-} ⁽²⁾ | | 1.4 | | AV _{CC} | V |
| V _{eREF-} | Negative external reference voltage input | V _{eREF+} > V _{eREF-} ⁽³⁾ | | 0 | | 1.2 | V |
| (V _{eREF+} - V _{eREF-}) | Differential external reference voltage input | V _{eREF+} > V _{eREF-} ⁽⁴⁾ | | 1.4 | | AV _{CC} | V |
| I _{vREF+} , I _{vREF-} | Static input current | 1.4 V ≤ V _{eREF+} ≤ V _{AVCC} , V _{eREF-} = 0 V, f _{ADC10CLK} = 5 MHz, ADC10SHTx = 1h, Conversion rate 200 ksp/s | 2.2 V, 3 V | -6 | | 6 | μA |
| | | 1.4 V ≤ V _{eREF+} ≤ V _{AVCC} , V _{eREF-} = 0 V, f _{ADC10CLK} = 5 MHz, ADC10SHTx = 8h, Conversion rate 20 ksp/s | 2.2 V, 3 V | -1 | | 1 | |
| C _{vREF+} , C _{vREF-} | Capacitance at VREF+ or VREF- terminal ⁽⁵⁾ | | | 10 | | | μF |

- (1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C_i, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
- (2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
- (3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
- (4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
- (5) Two decoupling capacitors, 10 μF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_B. Also see the [MSP430FR57xx Family User's Guide](#).

5.33 REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|--|--|-----------------|------|------|------|------------|
| V _{REF+} | Positive built-in reference voltage output | REFVSEL = {2} for 2.5 V, REFON = 1 | 3 V | 2.4 | 2.5 | 2.6 | V |
| | | REFVSEL = {1} for 2 V, REFON = 1 | 3 V | 1.92 | 2.0 | 2.08 | |
| | | REFVSEL = {0} for 1.5 V, REFON = 1 | 3 V | 1.44 | 1.5 | 1.56 | |
| AV _{CC(min)} | AV _{CC} minimum voltage, Positive built-in reference active | REFVSEL = {0} for 1.5 V | | 2.0 | | | V |
| | | REFVSEL = {1} for 2 V | | 2.2 | | | |
| | | REFVSEL = {2} for 2.5 V | | 2.7 | | | |
| I _{REF+} | Operating supply current into AV _{CC} terminal ⁽¹⁾ | f _{ADC10CLK} = 5 MHz, REFON = 1, REFBURST = 0 | 3 V | | 33 | 45 | μA |
| T _{REF+} | Temperature coefficient of built-in reference | REFVSEL = {0, 1, 2}, REFON = 1 | | | ±35 | | ppm/ °C |
| PSRR _{DC} | Power supply rejection ratio (DC) | AV _{CC} = AV _{CC(min)} - AV _{CC(max)} , T _A = 25°C, REFON = 1, REFVSEL = {0} for 1.5 V | | | 1600 | | μV/V |
| | | AV _{CC} = AV _{CC(min)} - AV _{CC(max)} , T _A = 25°C, REFON = 1, REFVSEL = {1} for 2 V | | | 1900 | | |
| | | AV _{CC} = AV _{CC(min)} - AV _{CC(max)} , T _A = 25°C, REFON = 1, REFVSEL = {2} for 2.5 V | | | 3600 | | |
| t _{SETTLE} | Settling time of reference voltage ⁽²⁾ | AV _{CC} = AV _{CC(min)} - AV _{CC(max)} , REFVSEL = {0, 1, 2}, REFON = 0 → 1 | | | 30 | | μs |

- (1) The internal reference current is supplied by terminal AV_{CC}. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.
- (2) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB.

5.34 REF, Temperature Sensor and Built-In V_{MID}

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|----------------------|---|---|----------|------|------|------|----------------|
| V_{SENSOR} | See ⁽¹⁾ | ADC10ON = 1, INCH = 0Ah, $T_A = 0^\circ C$ | 2 V, 3 V | | 790 | | mV |
| TC_{SENSOR} | | ADC10ON = 1, INCH = 0Ah | 2 V, 3 V | | 2.55 | | mV/ $^\circ C$ |
| $t_{SENSOR(sample)}$ | Sample time required if channel 10 is selected ⁽²⁾ | ADC10ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB | 2 V | | 30 | | μs |
| | | | 3 V | | 30 | | |
| V_{MID} | AV_{CC} divider at channel 11 | ADC10ON = 1, INCH = 0Bh, V_{MID} is $\sim 0.5 \times V_{AVCC}$ | 2 V | 0.97 | 1.0 | 1.03 | V |
| | | | 3 V | 1.46 | 1.5 | 1.54 | |
| $t_{VMID(sample)}$ | Sample time required if channel 11 is selected ⁽³⁾ | ADC10ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB | 2 V, 3 V | | 1000 | | ns |

- (1) The temperature sensor offset can vary significantly. A single-point calibration is recommended to minimize the offset error of the built-in temperature sensor.
- (2) The typical equivalent impedance of the sensor is 51 k Ω . The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
- (3) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

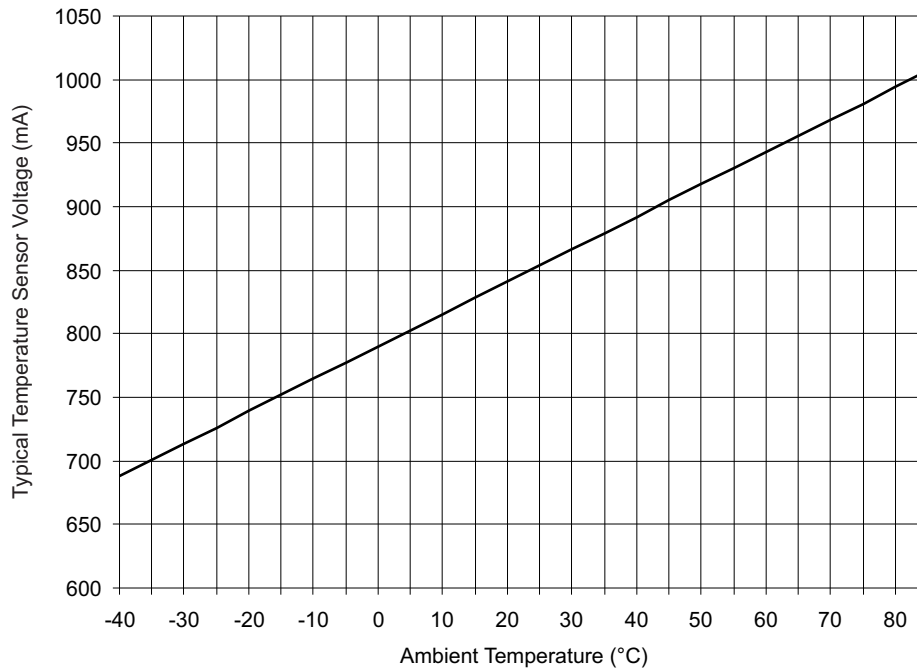


Figure 5-11. Typical Temperature Sensor Voltage

5.35 Comparator_D

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|----------------------------|--------------------------|----------------------------|------|
| t _{pd} Propagation delay, AVCC = 2 V to 3.6 V | Overdrive = 10 mV, VIN- = (VIN+ - 400 mV) to (VIN+ + 10 mV) | 50 | 100 | 200 | ns |
| | Overdrive = 100 mV, VIN- = (VIN+ - 400 mV) to (VIN+ + 100 mV) | | 80 | | |
| | Overdrive = 250 mV, (VIN+ - 400 mV) to (VIN+ + 250 mV) | | 50 | | |
| t _{filter} Filter timer added to the propagation delay of the comparator | CDF = 1, CDFDLY = 00 | 0.3 | 0.5 | 0.9 | μs |
| | CDF = 1, CDFDLY = 01 | 0.5 | 0.9 | 1.5 | |
| | CDF = 1, CDFDLY = 10 | 0.9 | 1.6 | 2.8 | |
| | CDF = 1, CDFDLY = 11 | 1.6 | 3.0 | 5.5 | |
| V _{offset} Input offset | AVCC = 2 V to 3.6 V | -20 | | 20 | mV |
| V _{ic} Common mode input range | AVCC = 2 V to 3.6 V | 0 | | AVCC - 1 | V |
| I _{comp(AVCC)} Comparator only | CDON = 1, AVCC = 2 V to 3.6 V | | 29 | 34 | μA |
| I _{ref(AVCC)} Reference buffer and R-ladder | CDREFLx = 01, AVCC = 2 V to 3.6 V | | 20 | 24 | μA |
| t _{enable,comp} Comparator enable time | CDON = 0 to CDON = 1, AVCC = 2 V to 3.6 V | | 1.1 | 2.0 | μs |
| t _{enable,r ladder} Resistor ladder enable time | CDON = 0 to CDON = 1, AVCC = 2 V to 3.6 V | | 1.1 | 2.0 | μs |
| V _{CB_REF} Reference voltage for a tap | VIN = voltage input to the R-ladder, n = 0 to 31 | VIN × (n + 0.5) / 32 | VIN × (n + 1) / 32 | VIN × (n + 1.5) / 32 | V |

5.36 FRAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--------------------------|-----|-----|------------------|--------|
| DV _{CC(WRITE)} Write supply voltage | | 2.0 | | 3.6 | V |
| t _{WRITE} Word or byte write time | | | | 120 | ns |
| t _{ACCESS} Read access time ⁽¹⁾ | | | | 60 | ns |
| t _{PRECHARGE} Precharge time ⁽¹⁾ | | | | 60 | ns |
| t _{CYCLE} Cycle time, read or write operation ⁽¹⁾ | | 120 | | | ns |
| | Read and write endurance | | | 10 ¹⁵ | cycles |
| t _{Retention} Data retention duration | T _J = 25°C | | | 100 | years |
| | T _J = 70°C | | | 40 | |
| | T _J = 85°C | | | 10 | |

(1) When using manual wait state control, see the [MSP430FR57xx Family User's Guide](#) for recommended settings for common system frequencies.

5.37 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

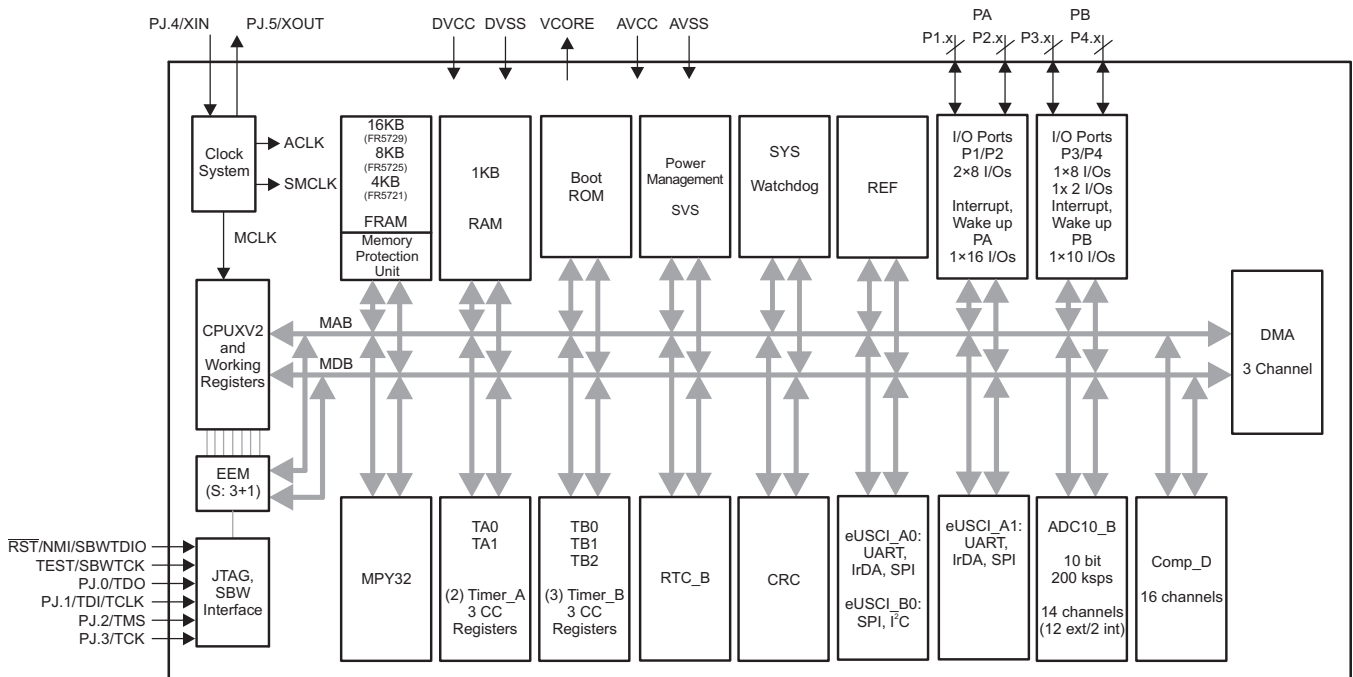
| PARAMETER | | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|--|-----------------|-------|-----|-----|------|
| f _{SBW} | Spy-Bi-Wire input frequency | 2 V, 3 V | 0 | | 20 | MHz |
| t _{SBW,Low} | Spy-Bi-Wire low clock pulse duration | 2 V, 3 V | 0.025 | | 15 | μs |
| t _{SBW,En} | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) ⁽¹⁾ | 2 V, 3 V | | | 1 | μs |
| t _{SBW,Rst} | Spy-Bi-Wire return to normal operation time | | 19 | | 35 | μs |
| f _{TCK} | TCK input frequency, 4-wire JTAG ⁽²⁾ | 2 V | 0 | | 5 | MHz |
| | | 3 V | 0 | | 10 | |
| R _{internal} | Internal pulldown resistance on TEST | 2 V, 3 V | 20 | 35 | 50 | kΩ |

- (1) Tools that access the Spy-Bi-Wire and BSL interfaces must wait for the t_{SBW,En} time after the first transition of the TEST/SBWTCK pin (low to high), before the second transition of the pin (high to low) during the entry sequence.
- (2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

6 Detailed Description

6.1 Functional Block Diagrams

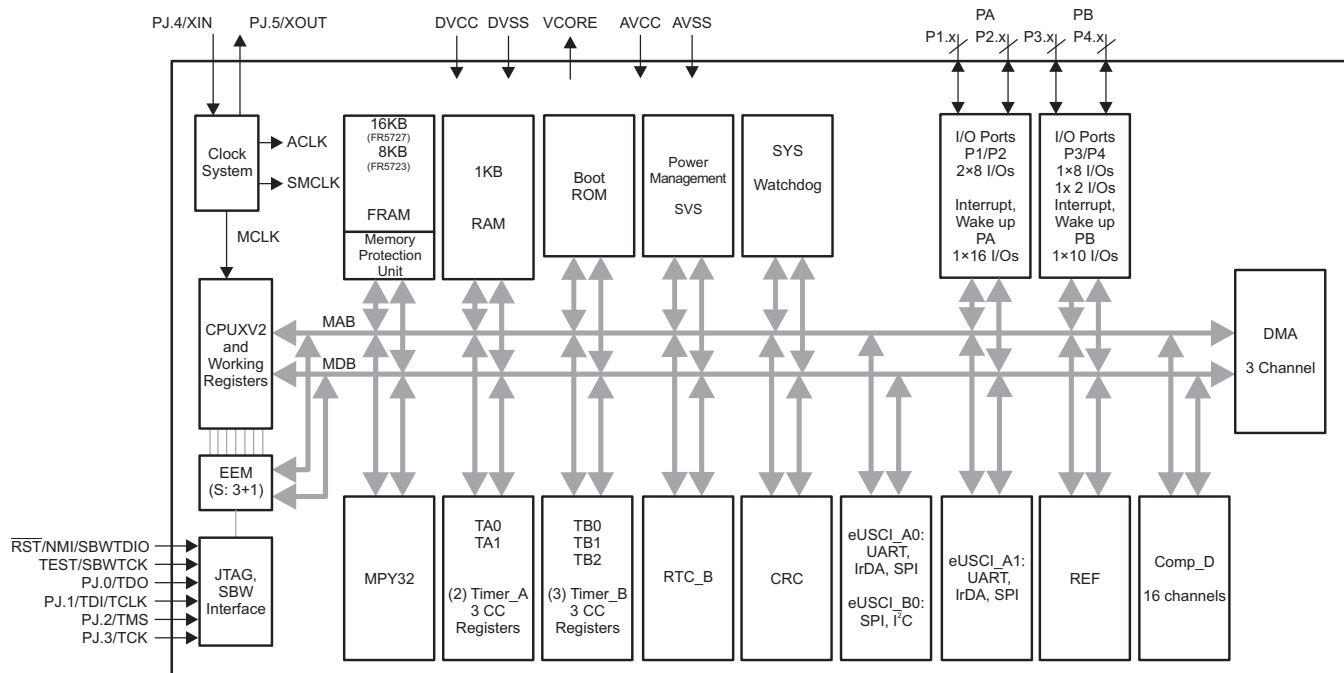
Figure 6-1 shows the functional block diagram for the MSP430FR5721, MSP430FR5725, and MSP430FR5729 in the RHA package.



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Figure 6-1. Functional Block Diagram – RHA Package – MSP430FR5721, MSP430FR5725, MSP430FR5729

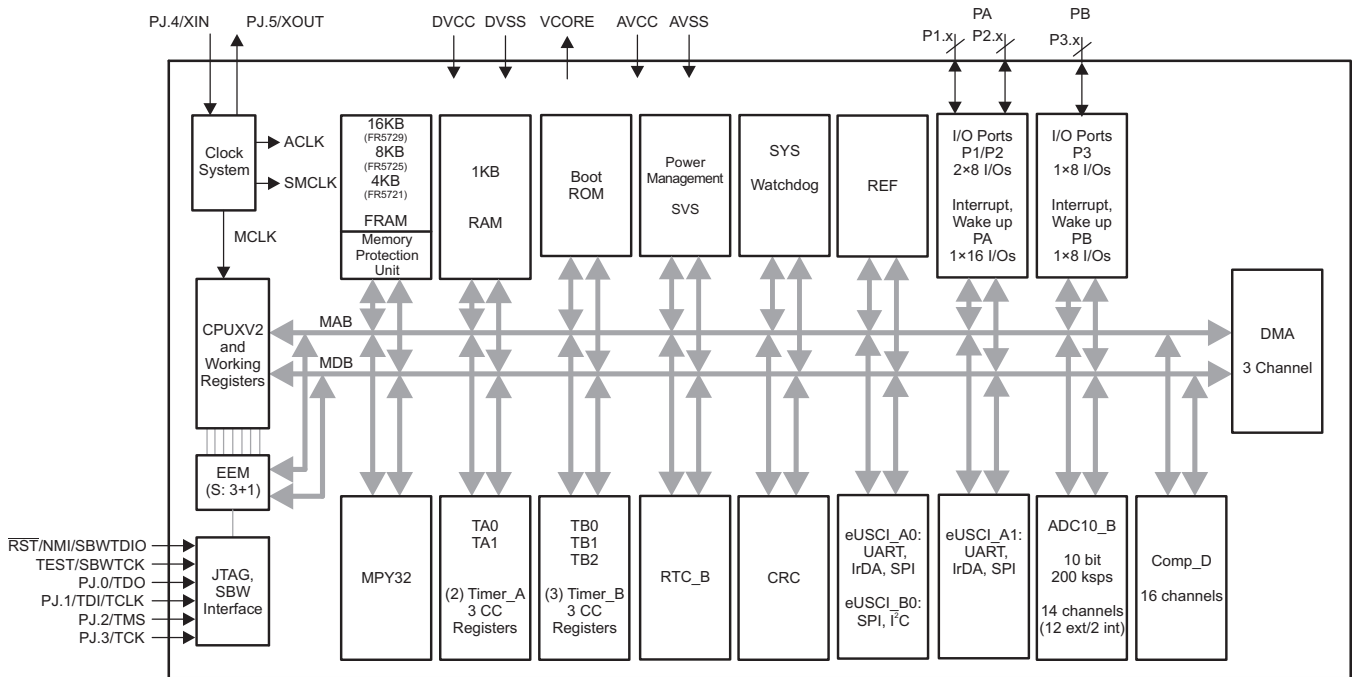
Figure 6-2 shows the functional block diagram for the MSP430FR5723 and MSP430FR5727 devices in the RHA package.



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Figure 6-2. Functional Block Diagram – RHA Package – MSP430FR5723, MSP430FR5727

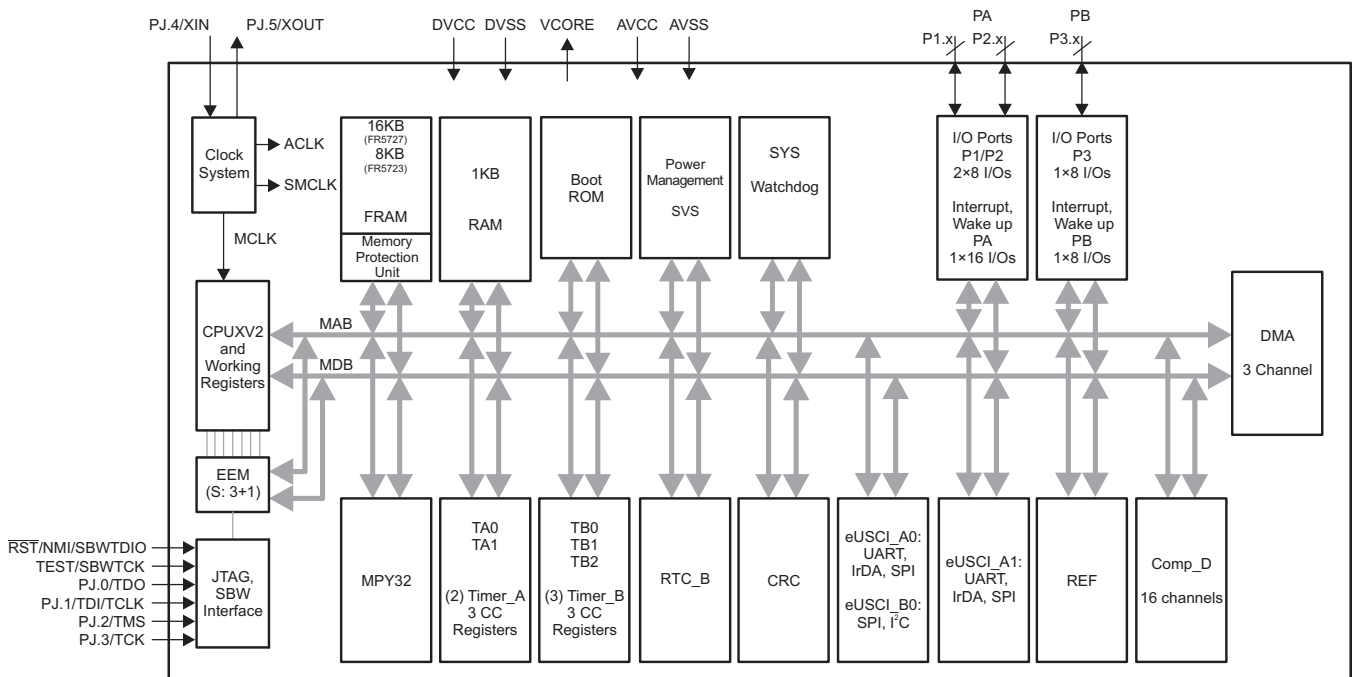
Figure 6-3 shows the functional block diagram for the MSP430FR5721, MSP430FR5725, and MSP430FR5729 devices in the DA package.



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Figure 6-3. Functional Block Diagram – DA Package – MSP430FR5721, MSP430FR5725, MSP430FR5729

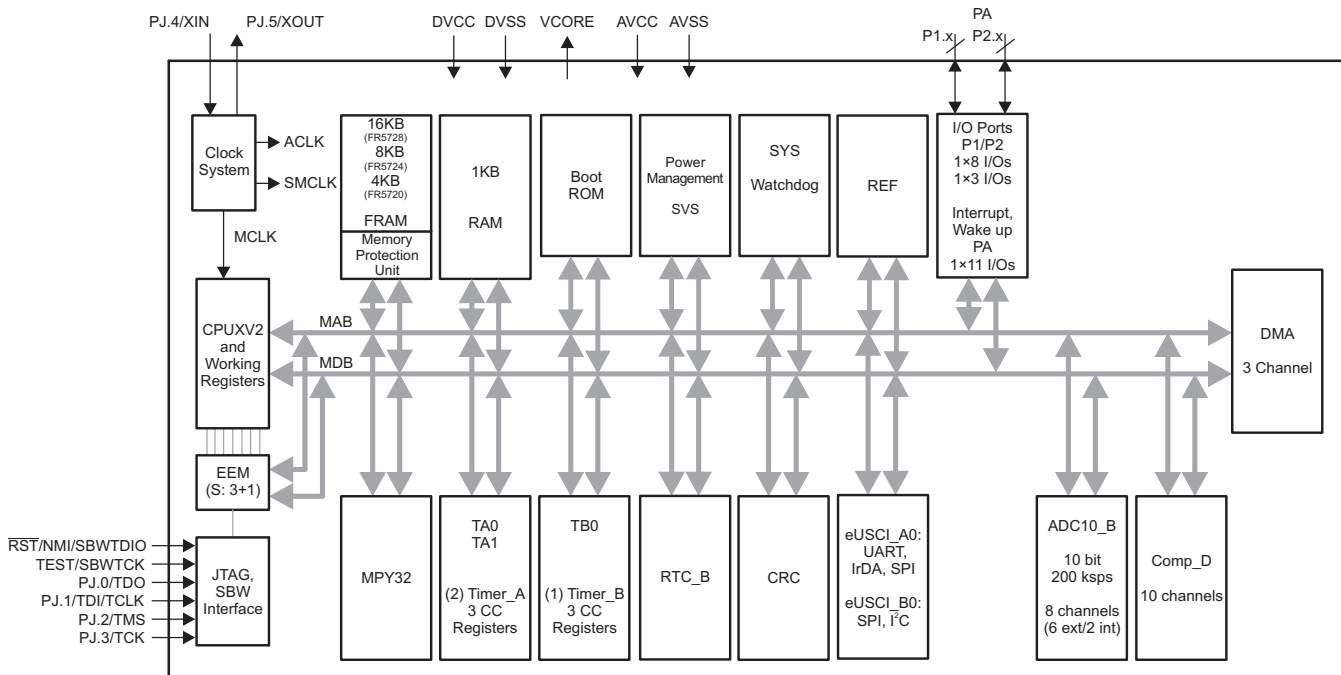
Figure 6-4 shows the functional block diagram for the MSP430FR5723 and MSP430FR5727 devices in the DA package.



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Figure 6-4. Functional Block Diagram – DA Package – MSP430FR5723, MSP430FR5727

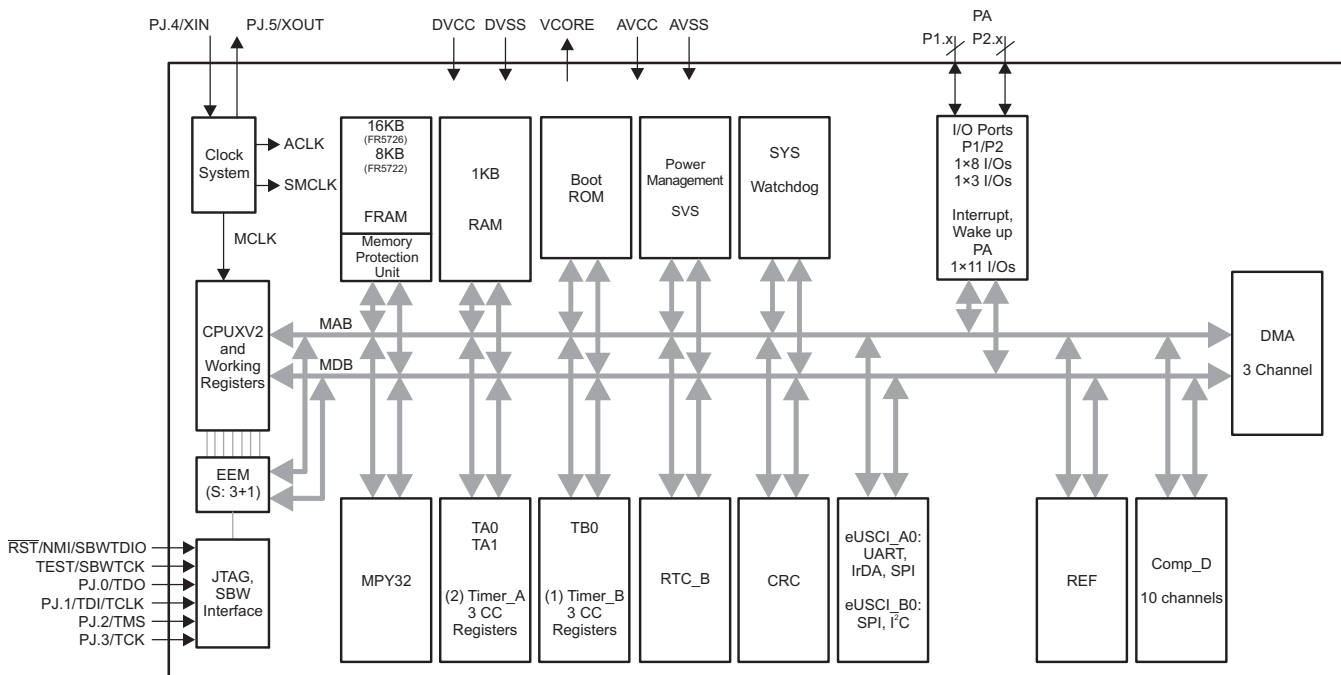
Figure 6-5 shows the functional block diagram for the MSP430FR5720, MSP430FR5724, and MSP430FR5728 devices in the RGE package.



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Figure 6-5. Functional Block Diagram – RGE Package – MSP430FR5720, MSP430FR5724, MSP430FR5728

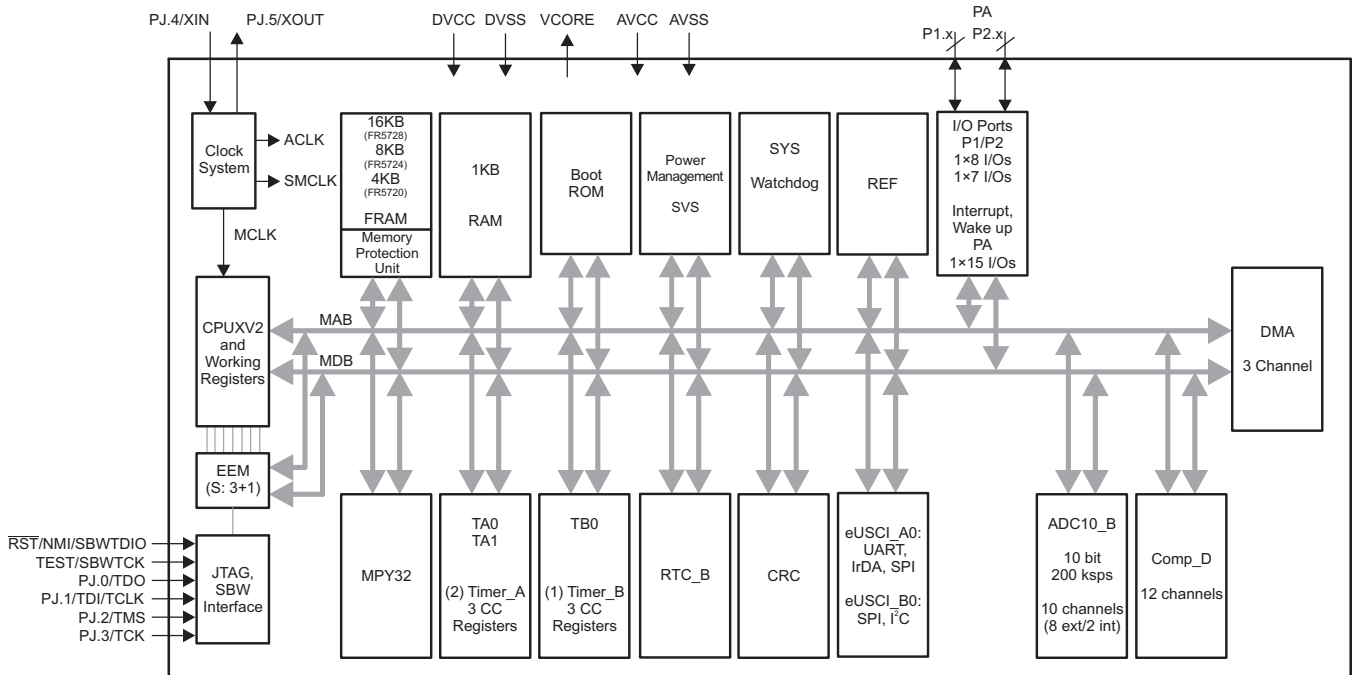
Figure 6-6 shows the functional block diagram for the MSP430FR5722 and MSP430FR5726 devices in the RGE package.



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Figure 6-6. Functional Block Diagram – RGE Package – MSP430FR5722, MSP430FR5726

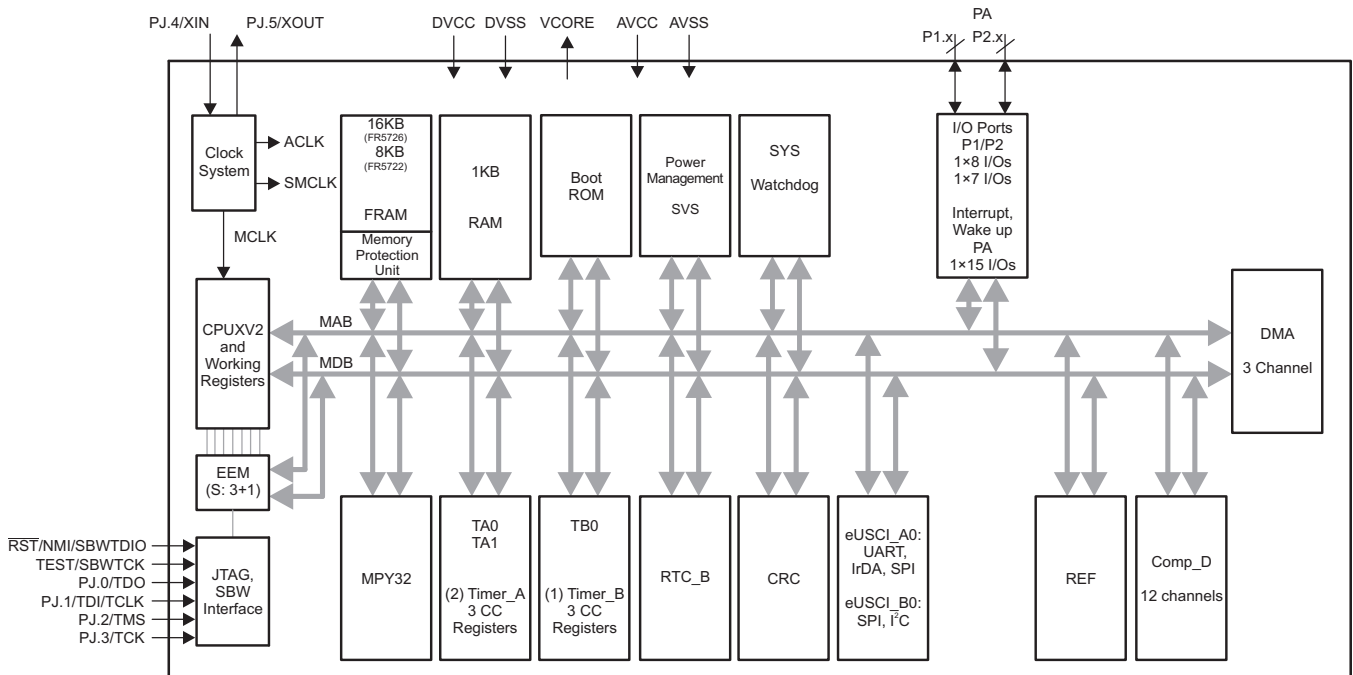
Figure 6-7 shows the functional block diagram for the MSP430FR5720, MSP430FR5724, and MSP430FR5728 devices in the PW package.



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Figure 6-7. Functional Block Diagram – PW Package – MSP430FR5720, MSP430FR5724, MSP430FR5728

Figure 6-8 shows the functional block diagram for the MSP430FR5722 and MSP430FR5726 devices in the PW package.



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Figure 6-8. Functional Block Diagram – PW Package – MSP430FR5722, MSP430FR5726

6.2 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

6.3 Operating Modes

The MSP430 has one active mode and seven software-selectable low-power modes of operation. An interrupt event can wake up the device from low-power modes LPM0 through LPM4, service the request, and restore back to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

The following eight operating modes can be configured by software:

- Active mode (AM)
 - All clocks are active
- Low-power mode 0 (LPM0)
 - CPU is disabled
 - ACLK active
 - MCLK disabled
 - SMCLK optionally active
 - Complete data retention
- Low-power mode 1 (LPM1)
 - CPU is disabled
 - ACLK active
 - MCLK disabled
 - SMCLK optionally active
 - DCO disabled
 - Complete data retention
- Low-power mode 2 (LPM2)
 - CPU is disabled
 - ACLK active
 - MCLK disabled
 - SMCLK optionally active
 - DCO disabled
 - Complete data retention
- Low-power mode 3 (LPM3)
 - CPU is disabled
 - ACLK active
 - MCLK and SMCLK disabled
 - DCO disabled
 - Complete data retention
- Low-power mode 4 (LPM4)
 - CPU is disabled
 - ACLK, MCLK, SMCLK disabled
 - Complete data retention
- Low-power mode 3.5 (LPM3.5)
 - RTC operation
 - Internal regulator disabled
 - No data retention
 - I/O pad state retention
 - Wake-up input from $\overline{\text{RST}}$, general-purpose I/O, RTC events
- Low-power mode 4.5 (LPM4.5)
 - Internal regulator disabled
 - No data retention
 - I/O pad state retention
 - Wake-up input from $\overline{\text{RST}}$ and general-purpose I/O

6.4 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see [Table 6-1](#)). The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 6-1. Interrupt Sources, Flags, and Vectors

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|--|--|------------------|--------------|-------------|
| System Reset Power-Up, Brownout, Supply Supervisors External Reset \overline{RST} Watchdog Time-out (Watchdog mode) WDT, FRCTL MPU, CS, PMM Password Violation FRAM double bit error detection MPU segment violation Software POR, BOR | SVSLIFG, SVSHIFG PMMRSTIFG WDTIFG WDTPW, FRCTLPW, MPUPW, CSPW, PMMPW DBDIFG MPUSEG1IFG, MPUSEG2IFG, MPUSEG3IFG PMPORIFG, PMMBORIFG (SYSRSTIV) ^{(1) (2)} | Reset | 0FFFEh | 63, highest |
| System NMI Vacant Memory Access JTAG Mailbox FRAM access time error FRAM single, double bit error detection | VMAIFG JMBNIFG, JMBOUTIFG ACCTIMIFG SBDIFG, DBDIFG (SYSSNIV) ⁽¹⁾ | (Non)maskable | 0FFFCh | 62 |
| User NMI External NMI Oscillator Fault | NMIIFG, OFIFG (SYSUNIV) ^{(1) (2)} | (Non)maskable | 0FFFAh | 61 |
| Comparator_D | Comparator_D interrupt flags (CBIV) ^{(1) (3)} | Maskable | 0FFF8h | 60 |
| TB0 | TB0CCR0 CCIFG0 ⁽³⁾ | Maskable | 0FFF6h | 59 |
| TB0 | TB0CCR1 CCIFG1 to TB0CCR2 CCIFG2, TB0IFG (TB0IV) ^{(1) (3)} | Maskable | 0FFF4h | 58 |
| Watchdog Timer (Interval Timer Mode) | WDTIFG | Maskable | 0FFF2h | 57 |
| eUSCI_A0 Receive and Transmit | UCA0RXIFG, UCA0TXIFG (SPI mode) UCA0STTIFG, UCA0XCPTIFG, UCA0RXIFG, UXA0TXIFG (UART mode) (UCA0IV) ^{(1) (3)} | Maskable | 0FFF0h | 56 |
| eUSCI_B0 Receive and Transmit | UCB0STTIFG, UCB0XCPTIFG, UCB0RXIFG, UCB0TXIFG (SPI mode) UCB0ALIFG, UCB0NACKIFG, UCB0STTIFG, UCB0STPIFG, UCB0RXIFG0, UCB0TXIFG0, UCB0RXIFG1, UCB0TXIFG1, UCB0RXIFG2, UCB0TXIFG2, UCB0RXIFG3, UCB0TXIFG3, UCB0CNTIFG, UCB0BIT9IFG (I ² C mode) (UCB0IV) ^{(1) (3)} | Maskable | 0FFEEh | 55 |
| ADC10_B | ADC10OVIFG, ADC10TOVIFG, ADC10HIIFG, ADC10LOIFG ADC10INIFG, ADC10IFG0 (ADC10IV) ^{(1) (3) (4)} | Maskable | 0FFECCh | 54 |
| TA0 | TA0CCR0 CCIFG0 ⁽³⁾ | Maskable | 0FFEAh | 53 |
| TA0 | TA0CCR1 CCIFG1 to TA0CCR2 CCIFG2, TA0IFG (TA0IV) ^{(1) (3)} | Maskable | 0FFE8h | 52 |

(1) Multiple source flags

(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space.

(Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.

(3) Interrupt flags are located in the module.

(4) Only on devices with ADC, otherwise reserved.

Table 6-1. Interrupt Sources, Flags, and Vectors (continued)

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|-------------------------------|---|------------------|-----------------------|----------------------|
| eUSCI_A1 Receive and Transmit | UCA1RXIFG, UCA1TXIFG (SPI mode) UCA1STTIFG, UCA1TXCPTIFG, UCA1RXIFG, UXA1TXIFG (UART mode) (UCA1IV) ^{(1) (3)} | Maskable | 0FFE6h | 51 |
| DMA | DMA0IFG, DMA1IFG, DMA2IFG (DMAIV) ^{(1) (3)} | Maskable | 0FFE4h | 50 |
| TA1 | TA1CCR0 CCIFG0 ⁽³⁾ | Maskable | 0FFE2h | 49 |
| TA1 | TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV) ^{(1) (3)} | Maskable | 0FFE0h | 48 |
| I/O Port P1 | P1IFG.0 to P1IFG.7 (P1IV) ^{(1) (3)} | Maskable | 0FFDEh | 47 |
| TB1 | TB1CCR0 CCIFG0 ⁽³⁾ | Maskable | 0FFDCh | 46 |
| TB1 | TB1CCR1 CCIFG1 to TB1CCR2 CCIFG2, TB1IFG (TB1IV) ^{(1) (3)} | Maskable | 0FFDAh | 45 |
| I/O Port P2 | P2IFG.0 to P2IFG.7 (P2IV) ^{(1) (3)} | Maskable | 0FFD8h | 44 |
| TB2 | TB2CCR0 CCIFG0 ⁽³⁾ | Maskable | 0FFD6h | 43 |
| TB2 | TB2CCR1 CCIFG1 to TB2CCR2 CCIFG2, TB2IFG (TB2IV) ^{(1) (3)} | Maskable | 0FFD4h | 42 |
| I/O Port P3 | P3IFG.0 to P3IFG.7 (P3IV) ^{(1) (3)} | Maskable | 0FFD2h | 41 |
| I/O Port P4 | P4IFG.0 to P4IFG.2 (P4IV) ^{(1) (3)} | Maskable | 0FFD0h | 40 |
| RTC_B | RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG, RTCOFIFG (RTCIV) ^{(1) (3)} | Maskable | 0FFCEh | 39 |
| Reserved | Reserved ⁽⁵⁾ | | 0FFCCh : 0FF80h | 38 : 0, lowest |

(5) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, it is recommended to reserve these locations.

6.5 Memory Organization

Table 6-2 describes the memory organization for all device variants.

Table 6-2. Memory Organization⁽¹⁾⁽²⁾

| | | MSP430FR5726 MSP430FR5727 MSP430FR5728 MSP430FR5729 | MSP430FR5722 MSP430FR5723 MSP430FR5724 MSP430FR5725 | MSP430FR5720 MSP430FR5721 |
|---|------------|--|--|---|
| Memory (FRAM) Main: interrupt vectors Main: code memory | Total Size | 15.5KB 00FFFFh–00FF80h 00FF7Fh–00C200h | 8.0KB 00FFFFh–00FF80h 00FF7Fh–00E000h | 4KB 00FFFFh–00FF80h 00FF7Fh–00F000h |
| RAM | | 1KB 001FFFh–001C00h | 1KB 001FFFh–001C00h | 1KB 001FFFh–001C00h |
| Device Descriptor Info (TLV) (FRAM) | | 128 B 001A7Fh–001A00h | 128 B 001A7Fh–001A00h | 128 B 001A7Fh–001A00h |
| Information memory (FRAM) | N/A | 0019FFh–001980h Address space mirrored to Info A | 0019FFh–001980h Address space mirrored to Info A | 0019FFh–001980h Address space mirrored to Info A |
| | N/A | 00197Fh–001900h Address space mirrored to Info B | 00197Fh–001900h Address space mirrored to Info B | 00197Fh–001900h Address space mirrored to Info B |
| | Info A | 128 B 0018FFh–001880h | 128 B 0018FFh–001880h | 128 B 0018FFh–001880h |
| | Info B | 128 B 00187Fh–001800h | 128 B 00187Fh–001800h | 128 B 00187Fh–001800h |
| Bootloader (BSL) memory (ROM) | BSL 3 | 512 B 0017FFh–001600h | 512 B 0017FFh–001600h | 512 B 0017FFh–001600h |
| | BSL 2 | 512 B 0015FFh–001400h | 512 B 0015FFh–001400h | 512 B 0015FFh–001400h |
| | BSL 1 | 512 B 0013FFh–001200h | 512 B 0013FFh–001200h | 512 B 0013FFh–001200h |
| | BSL 0 | 512 B 0011FFh–001000h | 512 B 0011FFh–001000h | 512 B 0011FFh–001000h |
| Peripherals | Size | 4KB 000FFFh–0h | 4KB 000FFFh–0h | 4KB 000FFFh–0h |

(1) N/A = Not available

(2) All address space not listed in this table is considered vacant memory.

6.6 Bootloader (BSL)

The BSL enables users to program the FRAM or RAM using a UART serial interface. Access to the device memory by the BSL is protected by an user-defined password. Use of the BSL requires four pins (see [Table 6-3](#)). BSL entry requires a specific entry sequence on the $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ and $\text{TEST}/\text{SBWTCK}$ pins. For complete description of the features of the BSL and its implementation, see the [MSP430 Programming With the Bootloader User's Guide](#).

Table 6-3. BSL Pin Requirements and Functions

| DEVICE SIGNAL | BSL FUNCTION |
|---|-----------------------|
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | Entry sequence signal |
| $\text{TEST}/\text{SBWTCK}$ | Entry sequence signal |
| P2.0 | Data transmit |
| P2.1 | Data receive |
| VCC | Power supply |
| VSS | Ground supply |

6.7 JTAG Operation

6.7.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The $\text{TEST}/\text{SBWTCK}$ pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ is required to interface with MSP430 development tools and device programmers. [Table 6-4](#) lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For a complete description of the features of the JTAG interface and its implementation, see [MSP430 Programming Via the JTAG Interface](#).

Table 6-4. JTAG Pin Requirements and Functions

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|---|-----------|-----------------------------|
| PJ.3/TCK | IN | JTAG clock input |
| PJ.2/TMS | IN | JTAG state control |
| PJ.1/TDI/TCLK | IN | JTAG data input, TCLK input |
| PJ.0/TDO | OUT | JTAG data output |
| $\text{TEST}/\text{SBWTCK}$ | IN | Enable JTAG pins |
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | IN | External reset |
| VCC | | Power supply |
| VSS | | Ground supply |

6.7.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the 2-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. [Table 6-5](#) lists the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For a complete description of the features of the JTAG interface and its implementation, see [MSP430 Programming Via the JTAG Interface](#).

Table 6-5. Spy-Bi-Wire Pin Requirements and Functions

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|-------------------------------------|-----------|-----------------------------------|
| TEST/SBWTCK | IN | Spy-Bi-Wire clock input |
| $\overline{\text{RST}}$ /NMI/SBWDIO | IN, OUT | Spy-Bi-Wire data input and output |
| VCC | | Power supply |
| VSS | | Ground supply |

6.8 FRAM

The FRAM can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. Features of the FRAM include:

- Low-power ultra-fast write nonvolatile memory
- Byte and word access capability
- Programmable and automated wait state generation
- Error correction coding (ECC) with single bit detection and correction, double bit detection

For important software design information regarding FRAM including but not limited to partitioning the memory layout according to application-specific code, constant, and data space requirements, the use of FRAM to optimize application energy consumption, and the use of the memory protection unit (MPU) to maximize application robustness by protecting the program code against unintended write accesses, see [MSP430™ FRAM Technology – How To and Best Practices](#).

6.9 Memory Protection Unit (MPU)

The FRAM can be protected from inadvertent CPU execution or write access by the MPU. Features of the MPU include:

- Main memory partitioning programmable up to three segments
- Access rights for each segment (main and information memory) can be individually selected
- Access violation flags with interrupt capability for easy servicing of access violations

6.10 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be managed using all instructions. For complete module descriptions, see the [MSP430FR57xx Family User's Guide](#).

6.10.1 Digital I/O

Up to four 8-bit I/O ports are implemented:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt and LPM3.5 and LPM4.5 wake-up input capability is available for all ports.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise in pairs.

6.10.2 Oscillator and Clock System (CS)

The clock system includes support for a 32-kHz watch crystal oscillator XT1 (LF mode), an internal very-low-power low-frequency oscillator (VLO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator XT1 (HF mode). The clock system module is designed to meet the requirements of both low system cost and low power consumption. A fail-safe mechanism exists for all crystal sources. The clock system module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal (XT1 LF mode), a high-frequency crystal (XT1 HF mode), the internal VLO, or the internal DCO.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by the same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by the same sources made available to ACLK.

6.10.3 Power-Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device. The PMM also includes supply voltage supervisor (SVS) and brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS circuitry detects if the supply voltage drops below a user-selectable safe level. SVS circuitry is available on the primary and core supplies.

6.10.4 Hardware Multiplier (MPY)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

6.10.5 Real-Time Clock (RTC_B)

The RTC_B module contains an integrated real-time clock (RTC) (calendar mode). Calendar mode integrates an internal calendar which compensates for months with fewer than 31 days and includes leap year correction. The RTC_B also supports flexible alarm functions and offset-calibration hardware. RTC operation is available in LPM3.5 mode to minimize power consumption.

6.10.6 Watchdog Timer (WDT_A)

The primary function of the WDT_A module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

6.10.7 System Module (SYS)

The SYS module handles many of the system functions within the device. These include power-on reset (POR) and power-up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators (see [Table 6-6](#)), bootloader entry mechanisms, and configuration management (device descriptors). It also includes a data exchange mechanism using JTAG called a JTAG mailbox that can be used in the application.

Table 6-6. System Module Interrupt Vector Registers

| INTERRUPT VECTOR REGISTER | ADDRESS | INTERRUPT EVENT | VALUE | PRIORITY |
|---------------------------|------------|--|------------|----------------------|
| SYSRSTIV, System Reset | 019Eh | No interrupt pending | 00h | |
| | | Brownout (BOR) | 02h | Highest |
| | | RSTIFG \overline{RST} /NMI (BOR) | 04h | |
| | | PMMSWBOR software BOR (BOR) | 06h | |
| | | LPMx.5 wake up (BOR) | 08h | |
| | | Security violation (BOR) | 0Ah | |
| | | SVSLIFG SVSL event (BOR) | 0Ch | |
| | | SVSHIFG SVSH event (BOR) | 0Eh | |
| | | Reserved | 10h | |
| | | Reserved | 12h | |
| | | PMMSWPOR software POR (POR) | 14h | |
| | | WDTIFG watchdog time-out (PUC) | 16h | |
| | | WDTPW password violation (PUC) | 18h | |
| | | FRCTLPW password violation (PUC) | 1Ah | |
| | | DBDIFG FRAM double bit error (PUC) | 1Ch | |
| | | Peripheral area fetch (PUC) | 1Eh | |
| | | PMMPW PMM password violation (PUC) | 20h | |
| | | MPUPW MPU password violation (PUC) | 22h | |
| | | CSPW CS password violation (PUC) | 24h | |
| | | MPUSEGIIIFG information memory segment violation (PUC) | 26h | |
| | | MPUSEG1IFG segment 1 memory violation (PUC) | 28h | |
| | | MPUSEG2IFG segment 2 memory violation (PUC) | 2Ah | |
| | | MPUSEG3IFG segment 3 memory violation (PUC) | 2Ch | |
| | | Reserved | 2Eh | |
| Reserved | 30h to 3Eh | Lowest | | |
| SYSSNIV, System NMI | 019Ch | No interrupt pending | 00h | |
| | | DBDIFG FRAM double bit error | 02h | Highest |
| | | ACCTIMIFG access time error | 04h | |
| | | Reserved | 0Eh | |
| | | VMAIFG Vacant memory access | 10h | |
| | | JMBINIFG JTAG mailbox input | 12h | |
| | | JMBOUTIFG JTAG mailbox output | 14h | |
| | | SBDIFG FRAM single bit error | 16h | |
| | | Reserved | 18h to 1Eh | Lowest |
| | | SYSUNIV, User NMI | 019Ah | No interrupt pending |
| NMIIFG NMI pin | 02h | | | Highest |
| OFIFG oscillator fault | 04h | | | |
| Reserved | 06h | | | |
| Reserved | 08h | | | |
| Reserved | 0Ah to 1Eh | | | Lowest |

6.10.8 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC10_B conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral. [Table 6-7](#) lists all triggers to start DMA transfers.

Table 6-7. DMA Trigger Assignments ⁽¹⁾

| TRIGGER | CHANNEL 0 | CHANNEL 1 | CHANNEL 2 |
|---------|------------------------------|------------------------------|------------------------------|
| 0 | DMAREQ | DMAREQ | DMAREQ |
| 1 | TA0CCR0 CCIFG | TA0CCR0 CCIFG | TA0CCR0 CCIFG |
| 2 | TA0CCR2 CCIFG | TA0CCR2 CCIFG | TA0CCR2 CCIFG |
| 3 | TA1CCR0 CCIFG | TA1CCR0 CCIFG | TA1CCR0 CCIFG |
| 4 | TA1CCR2 CCIFG | TA1CCR2 CCIFG | TA1CCR2 CCIFG |
| 5 | Reserved | Reserved | Reserved |
| 6 | Reserved | Reserved | Reserved |
| 7 | TB0CCR0 CCIFG | TB0CCR0 CCIFG | TB0CCR0 CCIFG |
| 8 | TB0CCR2 CCIFG | TB0CCR2 CCIFG | TB0CCR2 CCIFG |
| 9 | TB1CCR0 CCIFG ⁽²⁾ | TB1CCR0 CCIFG ⁽²⁾ | TB1CCR0 CCIFG ⁽²⁾ |
| 10 | TB1CCR2 CCIFG ⁽²⁾ | TB1CCR2 CCIFG ⁽²⁾ | TB1CCR2 CCIFG ⁽²⁾ |
| 11 | TB2CCR0 CCIFG ⁽³⁾ | TB2CCR0 CCIFG ⁽³⁾ | TB2CCR0 CCIFG ⁽³⁾ |
| 12 | TB2CCR2 CCIFG ⁽³⁾ | TB2CCR2 CCIFG ⁽³⁾ | TB2CCR2 CCIFG ⁽³⁾ |
| 13 | Reserved | Reserved | Reserved |
| 14 | UCA0RXIFG | UCA0RXIFG | UCA0RXIFG |
| 15 | UCA0TXIFG | UCA0TXIFG | UCA0TXIFG |
| 16 | UCA1RXIFG ⁽⁴⁾ | UCA1RXIFG ⁽⁴⁾ | UCA1RXIFG ⁽⁴⁾ |
| 17 | UCA1TXIFG ⁽⁴⁾ | UCA1TXIFG ⁽⁴⁾ | UCA1TXIFG ⁽⁴⁾ |
| 18 | UCB0RXIFG0 | UCB0RXIFG0 | UCB0RXIFG0 |
| 19 | UCB0TXIFG0 | UCB0TXIFG0 | UCB0TXIFG0 |
| 20 | UCB0RXIFG1 | UCB0RXIFG1 | UCB0RXIFG1 |
| 21 | UCB0TXIFG1 | UCB0TXIFG1 | UCB0TXIFG1 |
| 22 | UCB0RXIFG2 | UCB0RXIFG2 | UCB0RXIFG2 |
| 23 | UCB0TXIFG2 | UCB0TXIFG2 | UCB0TXIFG2 |
| 24 | UCB0RXIFG3 | UCB0RXIFG3 | UCB0RXIFG3 |
| 25 | UCB0TXIFG3 | UCB0TXIFG3 | UCB0TXIFG3 |
| 26 | ADC10IFGx ⁽⁵⁾ | ADC10IFGx ⁽⁵⁾ | ADC10IFGx ⁽⁵⁾ |
| 27 | Reserved | Reserved | Reserved |
| 28 | Reserved | Reserved | Reserved |
| 29 | MPY ready | MPY ready | MPY ready |
| 30 | DMA2IFG | DMA0IFG | DMA1IFG |
| 31 | DMAE0 | DMAE0 | DMAE0 |

- (1) If a reserved trigger source is selected, no trigger is generated.
 (2) Only on devices with TB1, otherwise reserved
 (3) Only on devices with TB2, otherwise reserved
 (4) Only on devices with eUSCI_A1, otherwise reserved
 (5) Only on devices with ADC, otherwise reserved

6.10.9 Enhanced Universal Serial Communication Interface (eUSCI)

The eUSCI modules are used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3-pin or 4-pin) and I²C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA. Each eUSCI module contains two portions, A and B.

The eUSCI_An module provides support for SPI (3-pin or 4-pin), UART, enhanced UART, or IrDA.

The eUSCI_Bn module provides support for SPI (3-pin or 4-pin) or I²C.

The MSP430FR572x series include one or two eUSCI_An modules (eUSCI_A0, eUSCI_A1) and one eUSCI_Bn module (eUSCI_B).

6.10.10 TA0, TA1

TA0 and TA1 are 16-bit timers/counters (Timer_A type) with three capture/compare registers each. TA0 and TA1 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-8 and Table 6-9). TA0 and TA1 have extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-8. TA0 Signal Connections

| INPUT PIN NUMBER | | | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | | | |
|------------------|---------|---------|---------|---------------------|---------------------|--------------|----------------------|----------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|
| RHA | RGE | DA | PW | | | | | | RHA | RGE | DA | PW |
| 3-P1.2 | 3-P1.2 | 7-P1.2 | 7-P1.2 | TA0CLK | TACLK | Timer | N/A | N/A | | | | |
| | | | | ACLK (internal) | ACLK | | | | | | | |
| | | | | SMCLK (internal) | SMCLK | | | | | | | |
| 3-P1.2 | 3-P1.2 | 7-P1.2 | 7-P1.2 | TA0CLK | TACLK | | | | | | | |
| 28-P1.6 | 16-P1.6 | 30-P1.6 | 22-P1.6 | TA0.0 | CCI0A | CCR0 | TA0 | TA0.0 | 28-P1.6 | 16-P1.6 | 30-P1.6 | 22-P1.6 |
| 34-P2.3 | N/A | 36-P2.3 | 27-P2.3 | TA0.0 | CCI0B | | | | 34-P2.3 | N/A | 36-P2.3 | 27-P2.3 |
| | | | | DV _{SS} | GND | | | | | | | |
| | | | | DV _{CC} | V _{CC} | | | | | | | |
| 1-P1.0 | 1-P1.0 | 5-P1.0 | 5-P1.0 | TA0.1 | CCI1A | CCR1 | TA1 | TA0.1 | 1-P1.0 | 1-P1.0 | 5-P1.0 | 5-P1.0 |
| | | | | CDOUT (internal) | CCI1B | | | | ADC10 (internal) ⁽¹⁾ | ADC10 (internal) ⁽¹⁾ | ADC10 (internal) ⁽¹⁾ | ADC10 (internal) ⁽¹⁾ |
| | | | | DV _{SS} | GND | | | | ADC10SHSx = {1} | ADC10SHSx = {1} | ADC10SHSx = {1} | ADC10SHSx = {1} |
| | | | | DV _{CC} | V _{CC} | | | | | | | |
| 2-P1.1 | 2-P1.1 | 6-P1.1 | 6-P1.1 | TA0.2 | CCI2A | CCR2 | TA2 | TA0.2 | 2-P1.1 | 2-P1.1 | 6-P1.1 | 6-P1.1 |
| | | | | ACLK (internal) | CCI2B | | | | | | | |
| | | | | DV _{SS} | GND | | | | | | | |
| | | | | DV _{CC} | V _{CC} | | | | | | | |

(1) Only on devices with ADC

Table 6-9. TA1 Signal Connections

| INPUT PIN NUMBER | | | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | | | |
|------------------|---------|---------|---------|---------------------------|---------------------------|-----------------|----------------------------|----------------------------|-------------------|---------|---------|---------|
| RHA | RGE | DA | PW | | | | | | RHA | RGE | DA | PW |
| 2-P1.1 | 2-P1.1 | 6-P1.1 | 6-P1.1 | TA1CLK | TACLK | Timer | N/A | N/A | | | | |
| | | | | ACLK (internal) | ACLK | | | | | | | |
| | | | | SMCLK (internal) | SMCLK | | | | | | | |
| 2-P1.1 | 2-P1.1 | 6-P1.1 | 6-P1.1 | TA1CLK | $\overline{\text{TACLK}}$ | CCR0 | TA0 | TA1.0 | | | | |
| 29-P1.7 | 17-P1.7 | 31-P1.7 | 23-P1.7 | TA1.0 | CCI0A | | | | 29-P1.7 | 17-P1.7 | 31-P1.7 | 23-P1.7 |
| 35-P2.4 | N/A | 37-P2.4 | 28-P2.4 | TA1.0 | CCI0B | | | | 35-P2.4 | N/A | 37-P2.4 | 28-P2.4 |
| | | | | DV _{SS} | GND | | | | | | | |
| | | | | DV _{CC} | V _{CC} | | | | | | | |
| 3-P1.2 | 3-P1.2 | 7-P1.2 | 7-P1.2 | TA1.1 | CCI1A | CCR1 | TA1 | TA1.1 | 3-P1.2 | 3-P1.2 | 7-P1.2 | 7-P1.2 |
| | | | | CDOUT (internal) | CCI1B | | | | | | | |
| | | | | DV _{SS} | GND | | | | | | | |
| | | | | DV _{CC} | V _{CC} | | | | | | | |
| 8-P1.3 | 4-P1.3 | 12-P1.3 | 8-P1.3 | TA1.2 | CCI2A | CCR2 | TA2 | TA1.2 | 8-P1.3 | 4-P1.3 | 12-P1.3 | 8-P1.3 |
| | | | | ACLK (internal) | CCI2B | | | | | | | |
| | | | | DV _{SS} | GND | | | | | | | |
| | | | | DV _{CC} | V _{CC} | | | | | | | |

6.10.11 TB0, TB1, TB2

TB0, TB1, and TB2 are 16-bit timers/counters (Timer_B type) with three capture/compare registers each. TB0, TB1, and TB2 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-10 through Table 6-12). TB0, TB1, and TB2 have extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-10. TB0 Signal Connections

| INPUT PIN NUMBER | | | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | | | |
|------------------|---------|---------|---------|---------------------|---------------------|--------------|----------------------|----------------------|--|--|--|--|
| RHA | RGE | DA | PW | | | | | | RHA | RGE | DA | PW |
| 21-P2.0 | 13-P2.0 | 23-P2.0 | 19-P2.0 | TB0CLK | TBCLK | Timer | N/A | N/A | | | | |
| | | | | ACLK (internal) | ACLK | | | | | | | |
| | | | | SMCLK (internal) | SMCLK | | | | | | | |
| 21-P2.0 | 13-P2.0 | 23-P2.0 | 19-P2.0 | TB0CLK | TBCLK | CCR0 | TB0 | TB0.0 | | | | |
| 22-P2.1 | 14-P2.1 | 24-P2.1 | 20-P2.1 | TB0.0 | CCI0A | | | | 22-P2.1 | 14-P2.1 | 24-P2.1 | 20-P2.1 |
| 17-P2.5 | N/A | 19-P2.5 | 15-P2.5 | TB0.0 | CCI0B | | | | 17-P2.5 | N/A | 19-P2.5 | 15-P2.5 |
| | | | | DV _{SS} | GND | | | | ADC10 (internal) ⁽¹⁾ ADC10SHSx = {2} | ADC10 (internal) ⁽¹⁾ ADC10SHSx = {2} | ADC10 (internal) ⁽¹⁾ ADC10SHSx = {2} | ADC10 (internal) ⁽¹⁾ ADC10SHSx = {2} |
| | | | | DV _{CC} | V _{CC} | | | | | | | |
| 9-P1.4 | 5-P1.4 | 13-P1.4 | 9-P1.4 | TB0.1 | CCI1A | CCR1 | TB1 | TB0.1 | 9-P1.4 | 5-P1.4 | 13-P1.4 | 9-P1.4 |
| | | | | CDOUT (internal) | CCI1B | | | | ADC10 (internal) ⁽¹⁾ ADC10SHSx = {3} | ADC10 (internal) ⁽¹⁾ ADC10SHSx = {3} | ADC10 (internal) ⁽¹⁾ ADC10SHSx = {3} | ADC10 (internal) ⁽¹⁾ ADC10SHSx = {3} |
| | | | | DV _{SS} | GND | | | | | | | |
| | | | | DV _{CC} | V _{CC} | | | | | | | |
| 10-P1.5 | 6-P1.5 | 14-P1.5 | 19-P1.5 | TB0.2 | CCI2A | CCR2 | TB2 | TB0.2 | 10-P1.5 | 6-P1.5 | 14-P1.5 | 19-P1.5 |
| | | | | ACLK (internal) | CCI2B | | | | | | | |
| | | | | DV _{SS} | GND | | | | | | | |
| | | | | DV _{CC} | V _{CC} | | | | | | | |

(1) Only on devices with ADC

Table 6-11. TB1 Signal Connections ⁽¹⁾

| INPUT PIN NUMBER | | | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | | | |
|------------------|-------------------------|---------|-------------------------|---------------------|---------------------------|--------------|----------------------|----------------------|-------------------|-----|---------|-----|
| RHA | RGE | DA | PW | | | | | | RHA | RGE | DA | PW |
| 26-P3.6 | N/A (DV _{SS}) | 28-P3.6 | N/A (DV _{SS}) | TB1CLK | TBCLK | Timer | N/A | N/A | | | | |
| | | | | ACLK (internal) | ACLK | | | | | | | |
| | | | | SMCLK (internal) | SMCLK | | | | | | | |
| 26-P3.6 | N/A (DV _{SS}) | 28-P3.6 | N/A (DV _{SS}) | TB1CLK | $\overline{\text{TBCLK}}$ | CCR0 | TB0 | TB1.0 | | | | |
| 23-P2.2 | N/A (DV _{SS}) | 25-P2.2 | N/A (DV _{SS}) | TB1.0 | CCI0A | | | | 23-P2.2 | N/A | 25-P2.2 | N/A |
| 18-P2.6 | N/A (DV _{SS}) | 20-P2.6 | N/A (DV _{SS}) | TB1.0 | CCI0B | | | | 18-P2.6 | N/A | 20-P2.6 | N/A |
| | | | | DV _{SS} | GND | | | | | | | |
| | | | | DV _{CC} | V _{CC} | | | | | | | |
| 28-P1.6 | N/A (DV _{SS}) | 30-P1.6 | N/A (DV _{SS}) | TB1.1 | CC1A | CCR1 | TB1 | TB1.1 | 28-P1.6 | N/A | 30-P1.6 | N/A |
| 24-P3.4 | N/A (DV _{SS}) | 26-P3.4 | N/A (DV _{SS}) | TB1.1 | CC1B | | | | 24-P3.4 | N/A | 26-P3.4 | N/A |
| | | | | DV _{SS} | GND | | | | | | | |
| | | | | DV _{CC} | V _{CC} | | | | | | | |
| 29-P1.7 | N/A (DV _{SS}) | 31-P1.7 | N/A (DV _{SS}) | TB1.2 | CC12A | CCR2 | TB2 | TB1.2 | 29-P1.7 | N/A | 31-P1.7 | N/A |
| 25-P3.5 | N/A (DV _{SS}) | 27-P3.5 | N/A (DV _{SS}) | TB1.2 | CC12B | | | | 25-P3.5 | N/A | 27-P3.5 | N/A |
| | | | | DV _{SS} | GND | | | | | | | |
| | | | | DV _{CC} | V _{CC} | | | | | | | |

(1) TB1 is not present on all device types.

Table 6-12. TB2 Signal Connections ⁽¹⁾

| INPUT PIN NUMBER | | | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | | | |
|------------------|-------------------------|-------------------------|-------------------------|---------------------|---------------------------|--------------|----------------------|----------------------|-------------------|-----|---------|-----|
| RHA | RGE | DA | PW | | | | | | RHA | RGE | DA | PW |
| 24-P3.4 | N/A (DV _{SS}) | 26-P3.4 | N/A (DV _{SS}) | TB2CLK | TBCLK | Timer | N/A | N/A | | | | |
| | | | | ACLK (internal) | ACLK | | | | | | | |
| | | | | SMCLK (internal) | SMCLK | | | | | | | |
| 24-P3.4 | N/A (DV _{SS}) | 26-P3.4 | N/A (DV _{SS}) | TB2CLK | $\overline{\text{TBCLK}}$ | CCR0 | TB0 | TB2.0 | | | | |
| 21-P2.0 | N/A (DV _{SS}) | 23-P2.0 | N/A (DV _{SS}) | TB2.0 | CCI0A | | | | 21-P2.0 | N/A | 23-P2.0 | N/A |
| 15-P4.0 | N/A (DV _{SS}) | N/A (DV _{SS}) | N/A (DV _{SS}) | TB2.0 | CCI0B | | | | 15-P4.0 | N/A | 36-P4.0 | N/A |
| | | | | DV _{SS} | GND | | | | | | | |
| | | | | DV _{CC} | V _{CC} | | | | | | | |
| 22-P2.1 | N/A (DV _{SS}) | 24-P2.1 | N/A (DV _{SS}) | TB2.1 | CC1A | CCR1 | TB1 | TB2.1 | 22-P2.1 | N/A | 24-P2.1 | N/A |
| 26-P3.6 | N/A (DV _{SS}) | 28-P3.6 | N/A (DV _{SS}) | TB2.1 | CC1B | | | | 26-P3.6 | N/A | 28-P3.6 | N/A |
| | | | | DV _{SS} | GND | | | | | | | |
| | | | | DV _{CC} | V _{CC} | | | | | | | |
| 23-P2.2 | N/A (DV _{SS}) | 25-P2.2 | N/A (DV _{SS}) | TB2.2 | CC12A | CCR2 | TB2 | TB2.2 | 23-P2.2 | N/A | 25-P2.2 | N/A |
| 27-P3.7 | N/A (DV _{SS}) | 29-P3.7 | N/A (DV _{SS}) | TB2.2 | CC12B | | | | 27-P3.7 | N/A | 29-P3.7 | N/A |
| | | | | DV _{SS} | GND | | | | | | | |
| | | | | DV _{CC} | V _{CC} | | | | | | | |

(1) TB2 is not present on all device types.

6.10.12 *ADC10_B*

The ADC10_B module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and a conversion result buffer. A window comparator with lower and an upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

6.10.13 *Comparator_D*

The primary function of the Comparator_D module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

6.10.14 *CRC16*

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

6.10.15 *Shared Reference (REF)*

The REF module generates all of the critical reference voltages that can be used by the various analog peripherals in the device.

6.10.16 *Embedded Emulation Module (EEM)*

The EEM supports real-time in-system debugging. The S version of the EEM has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

6.10.17 Peripheral File Map

Table 6-13 lists the base address and offset range of all available peripherals.

Table 6-13. Peripherals

| MODULE NAME | BASE ADDRESS | OFFSET ADDRESS RANGE |
|--|--------------|----------------------|
| Special Functions (see Table 6-14) | 0100h | 000h–01Fh |
| PMM (see Table 6-15) | 0120h | 000h–010h |
| FRAM Control (see Table 6-16) | 0140h | 000h–00Fh |
| CRC16 (see Table 6-17) | 0150h | 000h–007h |
| Watchdog (see Table 6-18) | 015Ch | 000h–001h |
| CS (see Table 6-19) | 0160h | 000h–00Fh |
| SYS (see Table 6-20) | 0180h | 000h–01Fh |
| Shared Reference (see Table 6-21) | 01B0h | 000h–001h |
| Port P1, P2 (see Table 6-22) | 0200h | 000h–01Fh |
| Port P3, P4 (see Table 6-23) | 0220h | 000h–01Fh |
| Port PJ (see Table 6-24) | 0320h | 000h–01Fh |
| TA0 (see Table 6-25) | 0340h | 000h–02Fh |
| TA1 (see Table 6-26) | 0380h | 000h–02Fh |
| TB0 (see Table 6-27) | 03C0h | 000h–02Fh |
| TB1 (see Table 6-28) | 0400h | 000h–02Fh |
| TB2 (see Table 6-29) | 0440h | 000h–02Fh |
| Real-Time Clock (RTC_B) (see Table 6-30) | 04A0h | 000h–01Fh |
| 32-Bit Hardware Multiplier (see Table 6-31) | 04C0h | 000h–02Fh |
| DMA General Control (see Table 6-32) | 0500h | 000h–00Fh |
| DMA Channel 0 (see Table 6-32) | 0510h | 000h–00Ah |
| DMA Channel 1 (see Table 6-32) | 0520h | 000h–00Ah |
| DMA Channel 2 (see Table 6-32) | 0530h | 000h–00Ah |
| MPU Control (see Table 6-33) | 05A0h | 000h–00Fh |
| eUSCI_A0 (see Table 6-34) | 05C0h | 000h–01Fh |
| eUSCI_A1 (see Table 6-35) | 05E0h | 000h–01Fh |
| eUSCI_B0 (see Table 6-36) | 0640h | 000h–02Fh |
| ADC10_B (see Table 6-37) | 0700h | 000h–03Fh |
| Comparator_D (see Table 6-38) | 08C0h | 000h–00Fh |

Table 6-14. Special Function Registers (Base Address: 0100h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-----------------------|----------|--------|
| SFR interrupt enable | SFRIE1 | 00h |
| SFR interrupt flag | SFRIFG1 | 02h |
| SFR reset pin control | SFRRPCR | 04h |

Table 6-15. PMM Registers (Base Address: 0120h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| PMM Control 0 | PMMCTL0 | 00h |
| PMM interrupt flags | PMMIFG | 0Ah |
| PM5 control 0 | PM5CTL0 | 10h |

Table 6-16. FRAM Control Registers (Base Address: 0140h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|-----------|--------|
| FRAM control 0 | FRCTLCTL0 | 00h |
| General control 0 | GCCTL0 | 04h |
| General control 1 | GCCTL1 | 06h |

Table 6-17. CRC16 Registers (Base Address: 0150h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|-----------|--------|
| CRC data input | CRC16DI | 00h |
| CRC data input reverse byte | CRCDIRB | 02h |
| CRC initialization and result | CRCINIRES | 04h |
| CRC result reverse byte | CRCRESR | 06h |

Table 6-18. Watchdog Registers (Base Address: 015Ch)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------|----------|--------|
| Watchdog timer control | WDTCTL | 00h |

Table 6-19. CS Registers (Base Address: 0160h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| CS control 0 | CSCTL0 | 00h |
| CS control 1 | CSCTL1 | 02h |
| CS control 2 | CSCTL2 | 04h |
| CS control 3 | CSCTL3 | 06h |
| CS control 4 | CSCTL4 | 08h |
| CS control 5 | CSCTL5 | 0Ah |
| CS control 6 | CSCTL6 | 0Ch |

Table 6-20. SYS Registers (Base Address: 0180h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-----------------------------|-----------|--------|
| System control | SYSTCTL | 00h |
| JTAG mailbox control | SYSJMBC | 06h |
| JTAG mailbox input 0 | SYSJMBIO | 08h |
| JTAG mailbox input 1 | SYSJMBI1 | 0Ah |
| JTAG mailbox output 0 | SYSJMBO0 | 0Ch |
| JTAG mailbox output 1 | SYSJMBO1 | 0Eh |
| Bus Error vector generator | SYSBERRIV | 18h |
| User NMI vector generator | SYSUNIV | 1Ah |
| System NMI vector generator | SYSSNIV | 1Ch |
| Reset vector generator | SYSRSTIV | 1Eh |

Table 6-21. Shared Reference Registers (Base Address: 01B0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------|----------|--------|
| Shared reference control | REFCTL | 00h |

Table 6-22. Port P1, P2 Registers (Base Address: 0200h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port P1 input | P1IN | 00h |
| Port P1 output | P1OUT | 02h |
| Port P1 direction | P1DIR | 04h |
| Port P1 pullup/pulldown enable | P1REN | 06h |
| Port P1 selection 0 | P1SEL0 | 0Ah |
| Port P1 selection 1 | P1SEL1 | 0Ch |
| Port P1 interrupt vector word | P1IV | 0Eh |
| Port P1 complement selection | P1SELC | 16h |
| Port P1 interrupt edge select | P1IES | 18h |
| Port P1 interrupt enable | P1IE | 1Ah |
| Port P1 interrupt flag | P1IFG | 1Ch |
| Port P2 input | P2IN | 01h |
| Port P2 output | P2OUT | 03h |
| Port P2 direction | P2DIR | 05h |
| Port P2 pullup/pulldown enable | P2REN | 07h |
| Port P2 selection 0 | P2SEL0 | 0Bh |
| Port P2 selection 1 | P2SEL1 | 0Dh |
| Port P2 complement selection | P2SELC | 17h |
| Port P2 interrupt vector word | P2IV | 1Eh |
| Port P2 interrupt edge select | P2IES | 19h |
| Port P2 interrupt enable | P2IE | 1Bh |
| Port P2 interrupt flag | P2IFG | 1Dh |

Table 6-23. Port P3, P4 Registers (Base Address: 0220h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port P3 input | P3IN | 00h |
| Port P3 output | P3OUT | 02h |
| Port P3 direction | P3DIR | 04h |
| Port P3 pullup/pulldown enable | P3REN | 06h |
| Port P3 selection 0 | P3SEL0 | 0Ah |
| Port P3 selection 1 | P3SEL1 | 0Ch |
| Port P3 interrupt vector word | P3IV | 0Eh |
| Port P3 complement selection | P3SELC | 16h |
| Port P3 interrupt edge select | P3IES | 18h |
| Port P3 interrupt enable | P3IE | 1Ah |
| Port P3 interrupt flag | P3IFG | 1Ch |
| Port P4 input | P4IN | 01h |
| Port P4 output | P4OUT | 03h |
| Port P4 direction | P4DIR | 05h |
| Port P4 pullup/pulldown enable | P4REN | 07h |
| Port P4 selection 0 | P4SEL0 | 0Bh |
| Port P4 selection 1 | P4SEL1 | 0Dh |
| Port P4 complement selection | P4SELC | 17h |
| Port P4 interrupt vector word | P4IV | 1Eh |
| Port P4 interrupt edge select | P4IES | 19h |
| Port P4 interrupt enable | P4IE | 1Bh |
| Port P4 interrupt flag | P4IFG | 1Dh |

Table 6-24. Port J Registers (Base Address: 0320h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|----------|--------|
| Port PJ input | PJIN | 00h |
| Port PJ output | PJOUT | 02h |
| Port PJ direction | PJDIR | 04h |
| Port PJ pullup/pulldown enable | PJREN | 06h |
| Port PJ selection 0 | PJSEL0 | 0Ah |
| Port PJ selection 1 | PJSEL1 | 0Ch |
| Port PJ complement selection | PJSELC | 16h |

Table 6-25. TA0 Registers (Base Address: 0340h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TA0 control | TA0CTL | 00h |
| Capture/compare control 0 | TA0CCTL0 | 02h |
| Capture/compare control 1 | TA0CCTL1 | 04h |
| Capture/compare control 2 | TA0CCTL2 | 06h |
| TA0 counter | TA0R | 10h |
| Capture/compare 0 | TA0CCR0 | 12h |
| Capture/compare 1 | TA0CCR1 | 14h |
| Capture/compare 2 | TA0CCR2 | 16h |
| TA0 expansion 0 | TA0EX0 | 20h |
| TA0 interrupt vector | TA0IV | 2Eh |

Table 6-26. TA1 Registers (Base Address: 0380h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TA1 control | TA1CTL | 00h |
| Capture/compare control 0 | TA1CCTL0 | 02h |
| Capture/compare control 1 | TA1CCTL1 | 04h |
| Capture/compare control 2 | TA1CCTL2 | 06h |
| TA1 counter | TA1R | 10h |
| Capture/compare 0 | TA1CCR0 | 12h |
| Capture/compare 1 | TA1CCR1 | 14h |
| Capture/compare 2 | TA1CCR2 | 16h |
| TA1 expansion 0 | TA1EX0 | 20h |
| TA1 interrupt vector | TA1IV | 2Eh |

Table 6-27. TB0 Registers (Base Address: 03C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TB0 control | TB0CTL | 00h |
| Capture/compare control 0 | TB0CCTL0 | 02h |
| Capture/compare control 1 | TB0CCTL1 | 04h |
| Capture/compare control 2 | TB0CCTL2 | 06h |
| TB0 counter | TB0R | 10h |
| Capture/compare 0 | TB0CCR0 | 12h |
| Capture/compare 1 | TB0CCR1 | 14h |
| Capture/compare 2 | TB0CCR2 | 16h |
| TB0 expansion 0 | TB0EX0 | 20h |
| TB0 interrupt vector | TB0IV | 2Eh |

Table 6-28. TB1 Registers (Base Address: 0400h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TB1 control | TB1CTL | 00h |
| Capture/compare control 0 | TB1CCTL0 | 02h |
| Capture/compare control 1 | TB1CCTL1 | 04h |
| Capture/compare control 2 | TB1CCTL2 | 06h |
| TB1 counter | TB1R | 10h |
| Capture/compare 0 | TB1CCR0 | 12h |
| Capture/compare 1 | TB1CCR1 | 14h |
| Capture/compare 2 | TB1CCR2 | 16h |
| TB1 expansion 0 | TB1EX0 | 20h |
| TB1 interrupt vector | TB1IV | 2Eh |

Table 6-29. TB2 Registers (Base Address: 0440h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TB2 control | TB2CTL | 00h |
| Capture/compare control 0 | TB2CCTL0 | 02h |
| Capture/compare control 1 | TB2CCTL1 | 04h |
| Capture/compare control 2 | TB2CCTL2 | 06h |
| TB2 counter | TB2R | 10h |
| Capture/compare 0 | TB2CCR0 | 12h |
| Capture/compare 1 | TB2CCR1 | 14h |
| Capture/compare 2 | TB2CCR2 | 16h |
| TB2 expansion 0 | TB2EX0 | 20h |
| TB2 interrupt vector | TB2IV | 2Eh |

Table 6-30. Real-Time Clock Registers (Base Address: 04A0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-----------------------------------|-----------------|--------|
| RTC control 0 | RTCCTL0 | 00h |
| RTC control 1 | RTCCTL1 | 01h |
| RTC control 2 | RTCCTL2 | 02h |
| RTC control 3 | RTCCTL3 | 03h |
| RTC prescaler 0 control | RTCPS0CTL | 08h |
| RTC prescaler 1 control | RTCPS1CTL | 0Ah |
| RTC prescaler 0 | RTCPS0 | 0Ch |
| RTC prescaler 1 | RTCPS1 | 0Dh |
| RTC interrupt vector word | RTCIV | 0Eh |
| RTC seconds, RTC counter 1 | RTCSEC, RTCNT1 | 10h |
| RTC minutes, RTC counter 2 | RTCMIN, RTCNT2 | 11h |
| RTC hours, RTC counter 3 | RTCHOUR, RTCNT3 | 12h |
| RTC day of week, RTC counter 4 | RTCROW, RTCNT4 | 13h |
| RTC days | RTCDAY | 14h |
| RTC month | RTCMON | 15h |
| RTC year low | RTCYEARL | 16h |
| RTC year high | RTCYEARH | 17h |
| RTC alarm minutes | RTCAMIN | 18h |
| RTC alarm hours | RTCAHOUR | 19h |
| RTC alarm day of week | RTCADOW | 1Ah |
| RTC alarm days | RTCADAY | 1Bh |
| Binary-to-BCD conversion register | BIN2BCD | 1Ch |
| BCD-to-binary conversion register | BCD2BIN | 1Eh |

Table 6-31. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|-----------|--------|
| 16-bit operand 1 – multiply | MPY | 00h |
| 16-bit operand 1 – signed multiply | MPYS | 02h |
| 16-bit operand 1 – multiply accumulate | MAC | 04h |
| 16-bit operand 1 – signed multiply accumulate | MACS | 06h |
| 16-bit operand 2 | OP2 | 08h |
| 16 × 16 result low word | RESLO | 0Ah |
| 16 × 16 result high word | RESHI | 0Ch |
| 16 × 16 sum extension register | SUMEXT | 0Eh |
| 32-bit operand 1 – multiply low word | MPY32L | 10h |
| 32-bit operand 1 – multiply high word | MPY32H | 12h |
| 32-bit operand 1 – signed multiply low word | MPYS32L | 14h |
| 32-bit operand 1 – signed multiply high word | MPYS32H | 16h |
| 32-bit operand 1 – multiply accumulate low word | MAC32L | 18h |
| 32-bit operand 1 – multiply accumulate high word | MAC32H | 1Ah |
| 32-bit operand 1 – signed multiply accumulate low word | MACS32L | 1Ch |
| 32-bit operand 1 – signed multiply accumulate high word | MACS32H | 1Eh |
| 32-bit operand 2 – low word | OP2L | 20h |
| 32-bit operand 2 – high word | OP2H | 22h |
| 32 × 32 result 0 – least significant word | RES0 | 24h |
| 32 × 32 result 1 | RES1 | 26h |
| 32 × 32 result 2 | RES2 | 28h |
| 32 × 32 result 3 – most significant word | RES3 | 2Ah |
| MPY32 control register 0 | MPY32CTL0 | 2Ch |

Table 6-32. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|----------|--------|
| DMA channel 0 control | DMA0CTL | 00h |
| DMA channel 0 source address low | DMA0SAL | 02h |
| DMA channel 0 source address high | DMA0SAH | 04h |
| DMA channel 0 destination address low | DMA0DAL | 06h |
| DMA channel 0 destination address high | DMA0DAH | 08h |
| DMA channel 0 transfer size | DMA0SZ | 0Ah |
| DMA channel 1 control | DMA1CTL | 00h |
| DMA channel 1 source address low | DMA1SAL | 02h |
| DMA channel 1 source address high | DMA1SAH | 04h |
| DMA channel 1 destination address low | DMA1DAL | 06h |
| DMA channel 1 destination address high | DMA1DAH | 08h |
| DMA channel 1 transfer size | DMA1SZ | 0Ah |
| DMA channel 2 control | DMA2CTL | 00h |
| DMA channel 2 source address low | DMA2SAL | 02h |
| DMA channel 2 source address high | DMA2SAH | 04h |
| DMA channel 2 destination address low | DMA2DAL | 06h |
| DMA channel 2 destination address high | DMA2DAH | 08h |
| DMA channel 2 transfer size | DMA2SZ | 0Ah |
| DMA module control 0 | DMACTL0 | 00h |
| DMA module control 1 | DMACTL1 | 02h |
| DMA module control 2 | DMACTL2 | 04h |
| DMA module control 3 | DMACTL3 | 06h |
| DMA module control 4 | DMACTL4 | 08h |
| DMA interrupt vector | DMAIV | 0Ah |

Table 6-33. MPU Control Registers (Base Address: 05A0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-----------------------|----------|--------|
| MPU control 0 | MPUCTL0 | 00h |
| MPU control 1 | MPUCTL1 | 02h |
| MPU segmentation | MPUSEG | 04h |
| MPU access management | MPUSAM | 06h |

Table 6-34. eUSCI_A0 Registers (Base Address: 05C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|------------|--------|
| eUSCI_A control word 0 | UCA0CTLW0 | 00h |
| eUSCI_A control word 1 | UCA0CTLW1 | 02h |
| eUSCI_A baud rate 0 | UCA0BR0 | 06h |
| eUSCI_A baud rate 1 | UCA0BR1 | 07h |
| eUSCI_A modulation control | UCA0MCTLW | 08h |
| eUSCI_A status | UCA0STAT | 0Ah |
| eUSCI_A receive buffer | UCA0RXBUF | 0Ch |
| eUSCI_A transmit buffer | UCA0TXBUF | 0Eh |
| eUSCI_A LIN control | UCA0ABCTL | 10h |
| eUSCI_A IrDA transmit control | UCA0IRTCTL | 12h |
| eUSCI_A IrDA receive control | UCA0IRRCTL | 13h |
| eUSCI_A interrupt enable | UCA0IE | 1Ah |
| eUSCI_A interrupt flags | UCA0IFG | 1Ch |
| eUSCI_A interrupt vector word | UCA0IV | 1Eh |

Table 6-35. eUSCI_A1 Registers (Base Address: 05E0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|------------|--------|
| eUSCI_A control word 0 | UCA1CTLW0 | 00h |
| eUSCI_A control word 1 | UCA1CTLW1 | 02h |
| eUSCI_A baud rate 0 | UCA1BR0 | 06h |
| eUSCI_A baud rate 1 | UCA1BR1 | 07h |
| eUSCI_A modulation control | UCA1MCTLW | 08h |
| eUSCI_A status | UCA1STAT | 0Ah |
| eUSCI_A receive buffer | UCA1RXBUF | 0Ch |
| eUSCI_A transmit buffer | UCA1TXBUF | 0Eh |
| eUSCI_A LIN control | UCA1ABCTL | 10h |
| eUSCI_A IrDA transmit control | UCA1IRTCTL | 12h |
| eUSCI_A IrDA receive control | UCA1IRRCTL | 13h |
| eUSCI_A interrupt enable | UCA1IE | 1Ah |
| eUSCI_A interrupt flags | UCA1IFG | 1Ch |
| eUSCI_A interrupt vector word | UCA1IV | 1Eh |

Table 6-36. eUSCI_B0 Registers (Base Address: 0640h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|-------------|--------|
| eUSCI_B control word 0 | UCB0CTLW0 | 00h |
| eUSCI_B control word 1 | UCB0CTLW1 | 02h |
| eUSCI_B bit rate 0 | UCB0BR0 | 06h |
| eUSCI_B bit rate 1 | UCB0BR1 | 07h |
| eUSCI_B status word | UCB0STATW | 08h |
| eUSCI_B byte counter threshold | UCB0TBCNT | 0Ah |
| eUSCI_B receive buffer | UCB0RXBUF | 0Ch |
| eUSCI_B transmit buffer | UCB0TXBUF | 0Eh |
| eUSCI_B I2C own address 0 | UCB0I2COA0 | 14h |
| eUSCI_B I2C own address 1 | UCB0I2COA1 | 16h |
| eUSCI_B I2C own address 2 | UCB0I2COA2 | 18h |
| eUSCI_B I2C own address 3 | UCB0I2COA3 | 1Ah |
| eUSCI_B received address | UCB0ADDRX | 1Ch |
| eUSCI_B address mask | UCB0ADDMASK | 1Eh |
| eUSCI I2C slave address | UCB0I2CSA | 20h |
| eUSCI interrupt enable | UCB0IE | 2Ah |
| eUSCI interrupt flags | UCB0IFG | 2Ch |
| eUSCI interrupt vector word | UCB0IV | 2Eh |

Table 6-37. ADC10_B Registers (Base Address: 0700h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|------------|--------|
| ADC10_B control 0 | ADC10CTL0 | 00h |
| ADC10_B control 1 | ADC10CTL1 | 02h |
| ADC10_B control 2 | ADC10CTL2 | 04h |
| ADC10_B window comparator low threshold | ADC10LO | 06h |
| ADC10_B window comparator high threshold | ADC10HI | 08h |
| ADC10_B memory control 0 | ADC10MCTL0 | 0Ah |
| ADC10_B conversion memory | ADC10MEM0 | 12h |
| ADC10_B Interrupt enable | ADC10IE | 1Ah |
| ADC10_B interrupt flags | ADC10IGH | 1Ch |
| ADC10_B interrupt vector word | ADC10IV | 1Eh |

Table 6-38. Comparator_D Registers (Base Address: 08C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------------|----------|--------|
| Comparator_D control 0 | CDCTL0 | 00h |
| Comparator_D control 1 | CDCTL1 | 02h |
| Comparator_D control 2 | CDCTL2 | 04h |
| Comparator_D control 3 | CDCTL3 | 06h |
| Comparator_D interrupt | CDINT | 0Ch |
| Comparator_D interrupt vector word | CDIV | 0Eh |

6.11 Input/Output Diagrams

6.11.1 Port P1 (P1.0 to P1.2) Input/Output With Schmitt Trigger

Figure 6-9 shows the port diagram. Table 6-39 summarizes the selection of the pin functions.

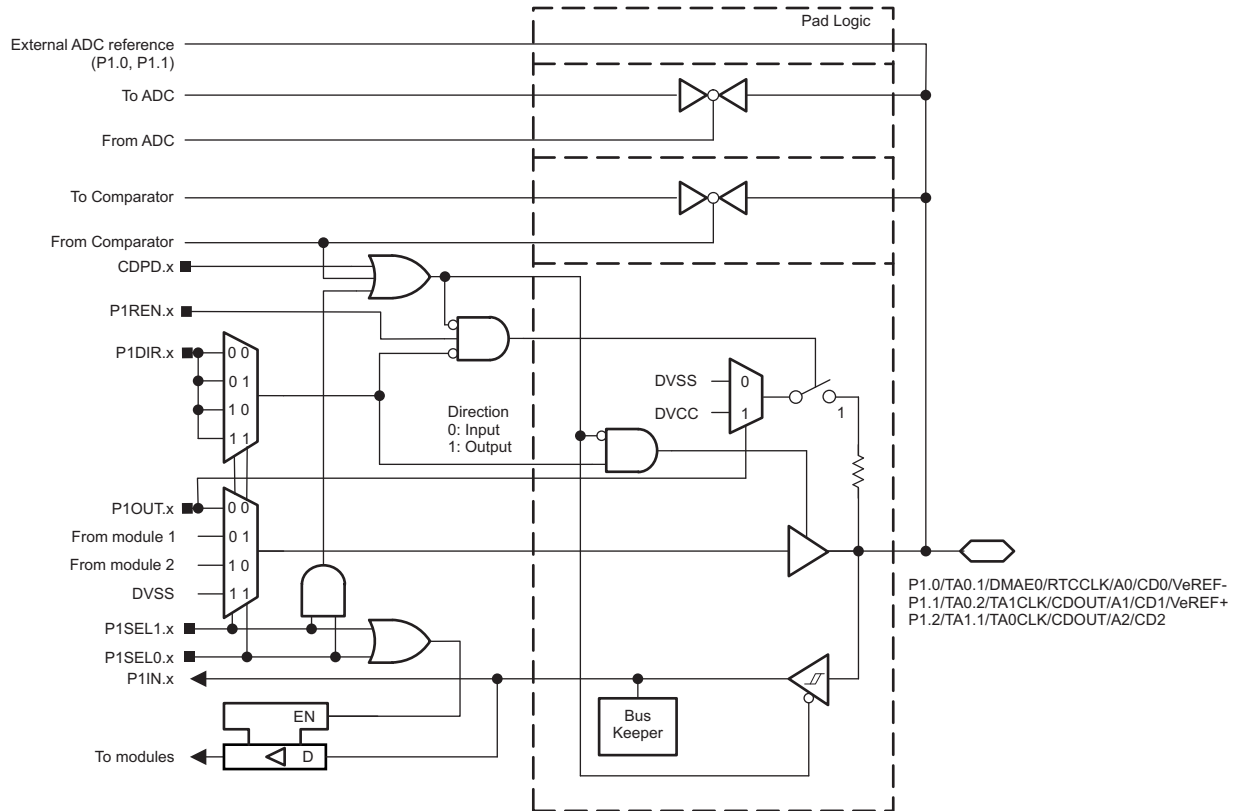


Figure 6-9. Port P1 (P1.0 to P1.2) Diagram

Table 6-39. Port P1 (P1.0 to P1.2) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | | |
|---------------------------------------|---|---|-------------------------|----------|----------|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x |
| P1.0/TA0.1/DMAE0/RTCCLK/A0/CD0/VeREF- | 0 | P1.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA0.CC1A | 0 | 0 | 1 |
| | | TA0.1 | 1 | | |
| | | DMAE0 | 0 | 1 | 0 |
| | | RTCCLK | 1 | | |
| | | A0 ⁽¹⁾ ⁽²⁾ CD0 ⁽¹⁾ ⁽³⁾ VeREF- ⁽¹⁾ ⁽²⁾ | X | 1 | 1 |
| P1.1/TA0.2/TA1CLK/CDOUT/A1/CD1/VeREF+ | 1 | P1.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA0.CC1A | 0 | 0 | 1 |
| | | TA0.2 | 1 | | |
| | | TA1CLK | 0 | 1 | 0 |
| | | CDOUT | 1 | | |
| | | A1 ⁽¹⁾ ⁽²⁾ CD1 ⁽¹⁾ ⁽³⁾ VeREF+ ⁽¹⁾ ⁽²⁾ | X | 1 | 1 |
| P1.2/TA1.1/TA0CLK/CDOUT/A2/CD2 | 2 | P1.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA1.CC1A | 0 | 0 | 1 |
| | | TA1.1 | 1 | | |
| | | TA0CLK | 0 | 1 | 0 |
| | | CDOUT | 1 | | |
| | | A2 ⁽¹⁾ ⁽²⁾ CD2 ⁽¹⁾ ⁽³⁾ | X | 1 | 1 |

- (1) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
- (2) Not available on all devices and package types.
- (3) Setting the CDPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CDx input pin to the comparator multiplexer with the CDx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CDPD.x bit.

6.11.2 Port P1 (P1.3 to P1.5) Input/Output With Schmitt Trigger

Figure 6-10 shows the port diagram. Table 6-40 summarizes the selection of the pin functions.

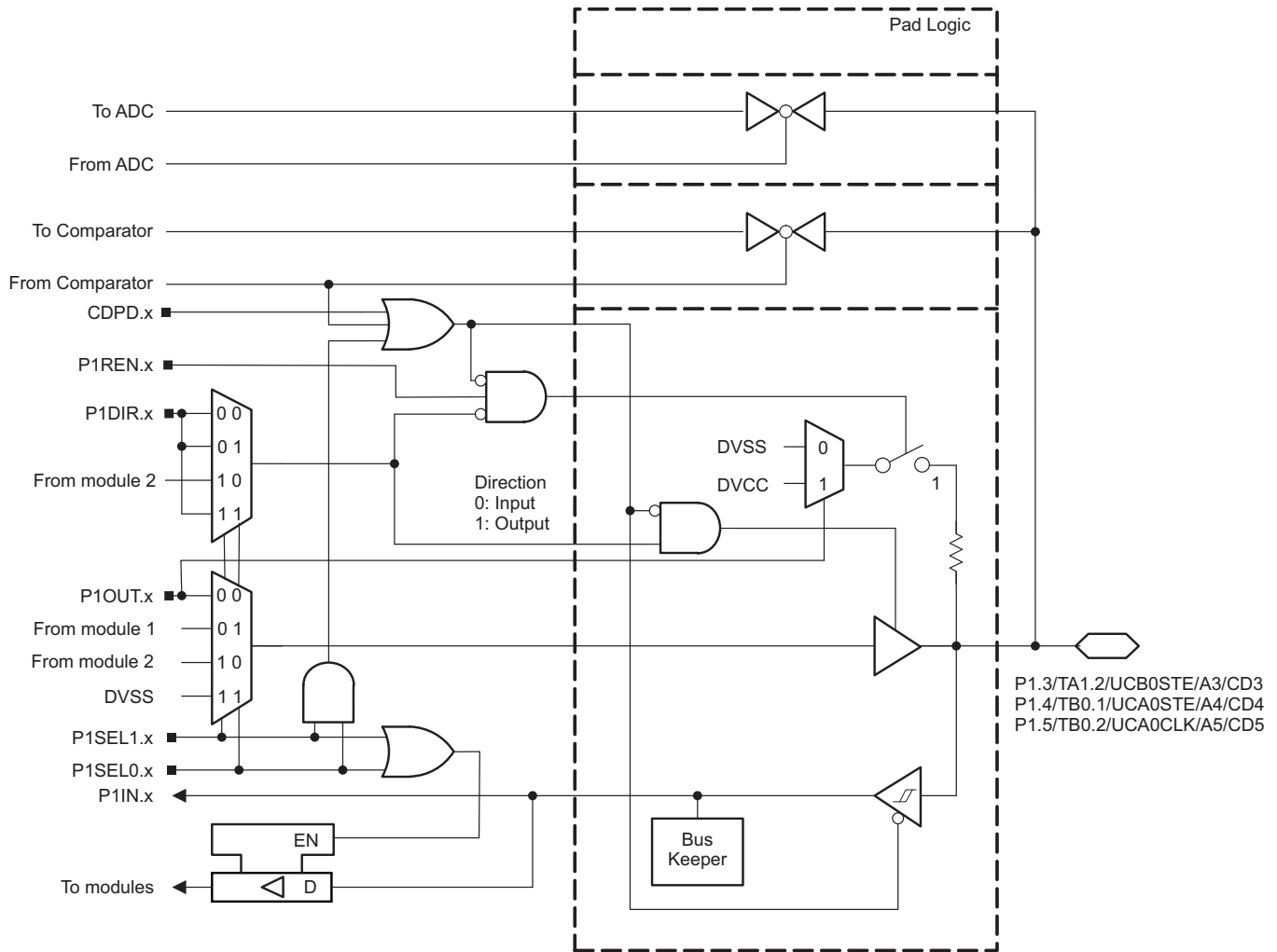


Figure 6-10. Port P1 (P1.3 to P1.5) Diagram

Table 6-40. Port P1 (P1.3 to P1.5) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | | |
|---------------------------|---|---|-------------------------|----------|----------|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x |
| P1.3/TA1.2/UCB0STE/A3/CD3 | 3 | P1.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA1.CCI2A | 0 | 0 | 1 |
| | | TA1.2 | 1 | | |
| | | UCB0STE | X ⁽¹⁾ | 1 | 0 |
| | | A3 ^{(2) (3)} CD3 ^{(2) (4)} | X | 1 | 1 |
| P1.4/TB0.1/UCA0STE/A4/CD4 | 4 | P1.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TB0.CCI1A | 0 | 0 | 1 |
| | | TB0.1 | 1 | | |
| | | UCA0STE | X ⁽⁵⁾ | 1 | 0 |
| | | A4 ^{(2) (3)} CD4 ^{(2) (4)} | X | 1 | 1 |
| P1.5/TB0.2/UCA0CLK/A5/CD5 | 5 | P1.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TB0.CCI2A | 0 | 0 | 1 |
| | | TB0.2 | 1 | | |
| | | UCA0CLK | X ⁽⁵⁾ | 1 | 0 |
| | | A5 ^{(2) (3)} CD5 ^{(2) (4)} | X | 1 | 1 |

- (1) Direction controlled by eUSCI_B0 module.
- (2) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
- (3) Not available on all devices and package types.
- (4) Setting the CDPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CDx input pin to the comparator multiplexer with the CDx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CDPD.x bit
- (5) Direction controlled by eUSCI_A0 module.

6.11.3 Port P1 (P1.6 and P1.7) Input/Output With Schmitt Trigger

Figure 6-11 shows the port diagram. Table 6-41 summarizes the selection of the pin functions.

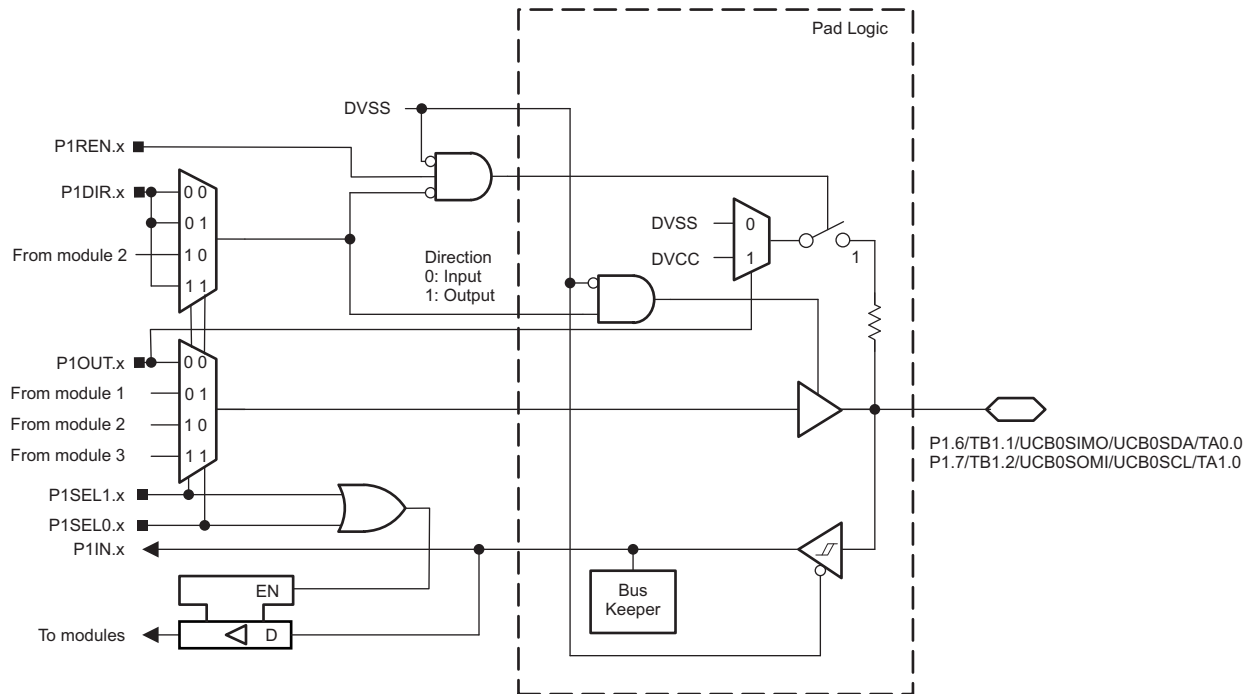


Figure 6-11. Port P1 (P1.6 and P1.7) Diagram

Table 6-41. Port P1 (P1.6 and P1.7) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | | |
|-----------------------------------|---|--------------------------|-------------------------|----------|----------|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x |
| P1.6/TB1.1/UCB0SIMO/UCB0SDA/TA0.0 | 6 | P1.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TB1.CCI1A ⁽¹⁾ | 0 | 0 | 1 |
| | | TB1.1 ⁽¹⁾ | 1 | | |
| | | UCB0SIMO/UCB0SDA | X ⁽²⁾ | 1 | 0 |
| | | TA0.CCI0A | 0 | 1 | 1 |
| | | TA0.0 | 1 | | |
| P1.7/TB1.2/UCB0SOMI/UCB0SCL/TA1.0 | 7 | P1.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TB1.CCI2A ⁽¹⁾ | 0 | 0 | 1 |
| | | TB1.2 ⁽¹⁾ | 1 | | |
| | | UCB0SOMI/UCB0SCL | X ⁽²⁾ | 1 | 0 |
| | | TA1.CCI0A | 0 | 1 | 1 |
| | | TA1.0 | 1 | | |

(1) Not available on all devices and package types.
(2) Direction controlled by eUSCI_B0 module.

6.11.4 Port P2 (P2.0 to P2.2) Input/Output With Schmitt Trigger

Figure 6-12 shows the port diagram. Table 6-42 summarizes the selection of the pin functions.

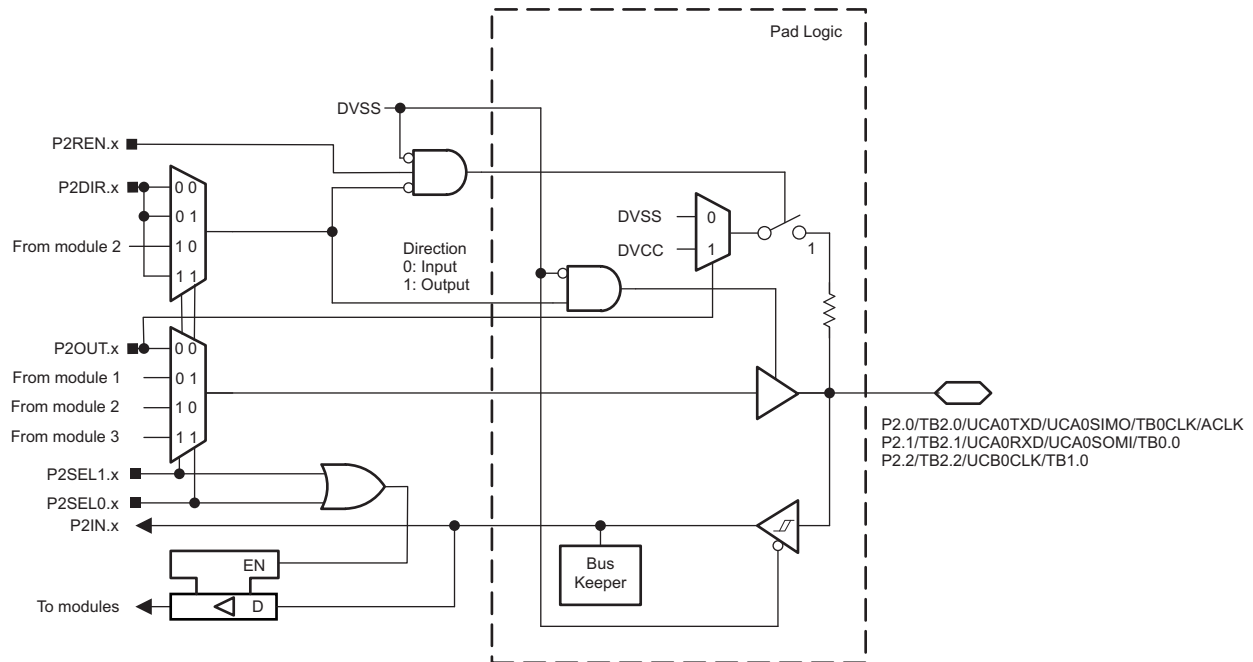


Figure 6-12. Port P2 (P2.0 to P2.2) Diagram

Table 6-42. Port P2 (P2.0 to P2.2) Pin Functions

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | | |
|---|---|--------------------------|-------------------------|----------|----------|
| | | | P2DIR.x | P2SEL1.x | P2SEL0.x |
| P2.0/TB2.0/UCA0TXD/UCA0SIMO/TB0CLK/ACLK | 0 | P2.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TB2.CCI0A ⁽¹⁾ | 0 | 0 | 1 |
| | | TB2.0 ⁽¹⁾ | 1 | | |
| | | UCA0TXD/UCA0SIMO | X ⁽²⁾ | 1 | 0 |
| | | TB0CLK | 0 | 1 | 1 |
| | | ACLK | 1 | | |
| P2.1/TB2.1/UCA0RXD/UCA0SOMI/TB0.0 | 1 | P2.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TB2.CCI1A ⁽¹⁾ | 0 | 0 | 1 |
| | | TB2.1 ⁽¹⁾ | 1 | | |
| | | UCA0RXD/UCA0SOMI | X ⁽²⁾ | 1 | 0 |
| | | TB0.CCI0A | 0 | 1 | 1 |
| | | TB0.0 | 1 | | |
| P2.2/TB2.2/UCB0CLK/TB1.0 | 2 | P2.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TB2.CCI2A ⁽¹⁾ | 0 | 0 | 1 |
| | | TB2.2 ⁽¹⁾ | 1 | | |
| | | UCB0CLK | X ⁽³⁾ | 1 | 0 |
| | | TB1.CCI0A ⁽¹⁾ | 0 | 1 | 1 |
| | | TB1.0 ⁽¹⁾ | 1 | | |

(1) Not available on all devices and package types.
 (2) Direction controlled by eUSCI_A0 module.
 (3) Direction controlled by eUSCI_B0 module.

6.11.5 Port P2 (P2.3 and P2.4) Input/Output With Schmitt Trigger

Figure 6-13 shows the port diagram. Table 6-43 summarizes the selection of the pin functions.

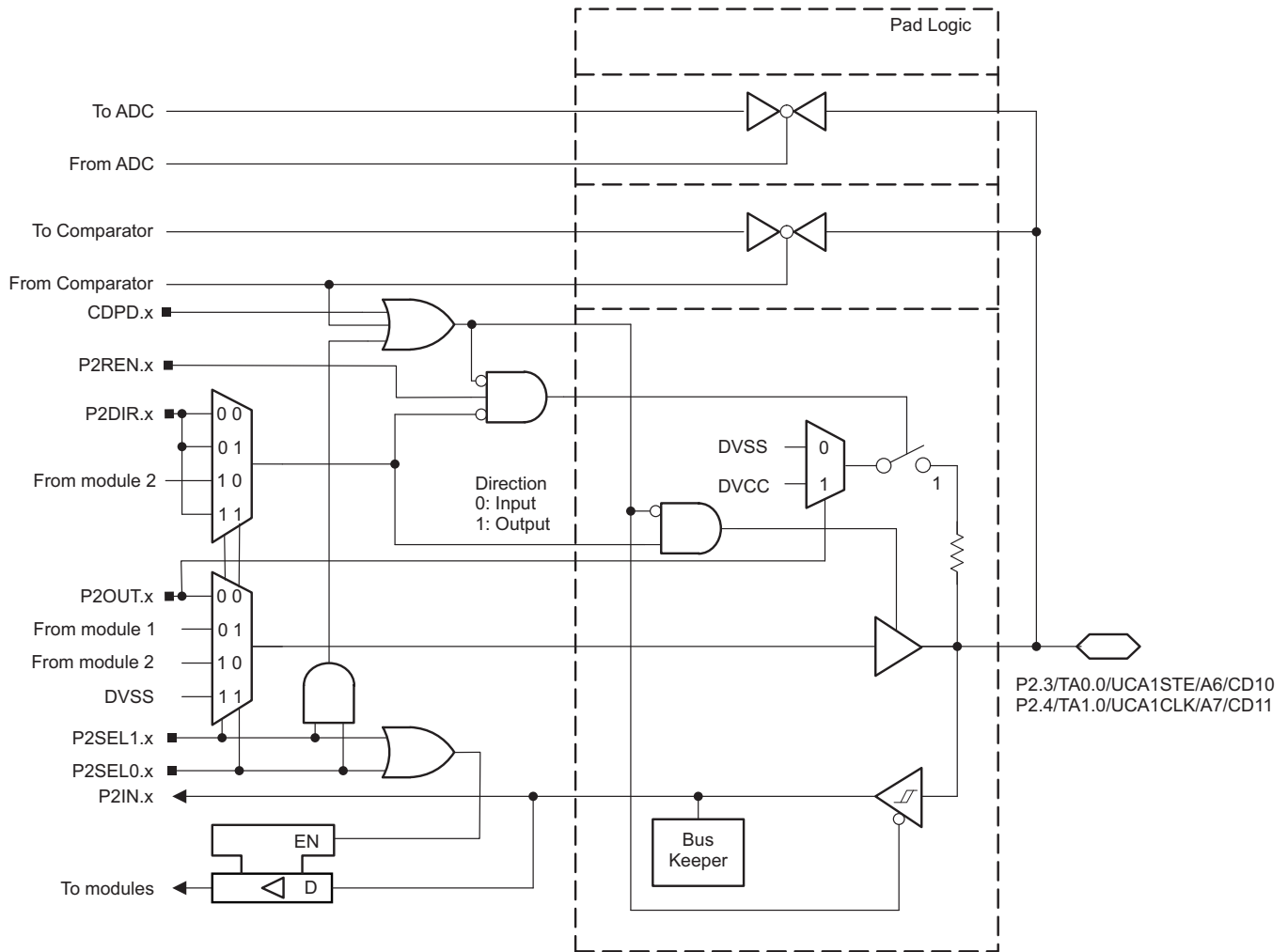


Figure 6-13. Port P2 (P2.3 and P2.4) Diagram

Table 6-43. Port P2 (P2.3 and P2.4) Pin Functions

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | | |
|----------------------------|---|--|-------------------------|----------|----------|
| | | | P2DIR.x | P2SEL1.x | P2SEL0.x |
| P2.3/TA0.0/UCA1STE/A6/CD10 | 3 | P2.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA0.CCI0B | 0 | 0 | 1 |
| | | TA0.0 | 1 | | |
| | | UCA1STE | X ⁽¹⁾ | 1 | 0 |
| | | A6 ^{(2) (3)} CD10 ^{(2) (4)} | X | 1 | 1 |
| P2.4/TA1.0/UCA1CLK/A7/CD11 | 4 | P2.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA1.CCI0B | 0 | 0 | 1 |
| | | TA1.0 | 1 | | |
| | | UCA1CLK | X ⁽¹⁾ | 1 | 0 |
| | | A7 ^{(2) (3)} CD11 ^{(2) (4)} | X | 1 | 1 |

- (1) Direction controlled by eUSCI_A1 module.
- (2) Setting P2SEL1.x and P2SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
- (3) Not available on all devices and package types.
- (4) Setting the CDPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CDx input pin to the comparator multiplexer with the CDx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CDPD.x bit.

6.11.6 Port P2 (P2.5 and P2.6) Input/Output With Schmitt Trigger

Figure 6-14 shows the port diagram. Table 6-44 summarizes the selection of the pin functions.

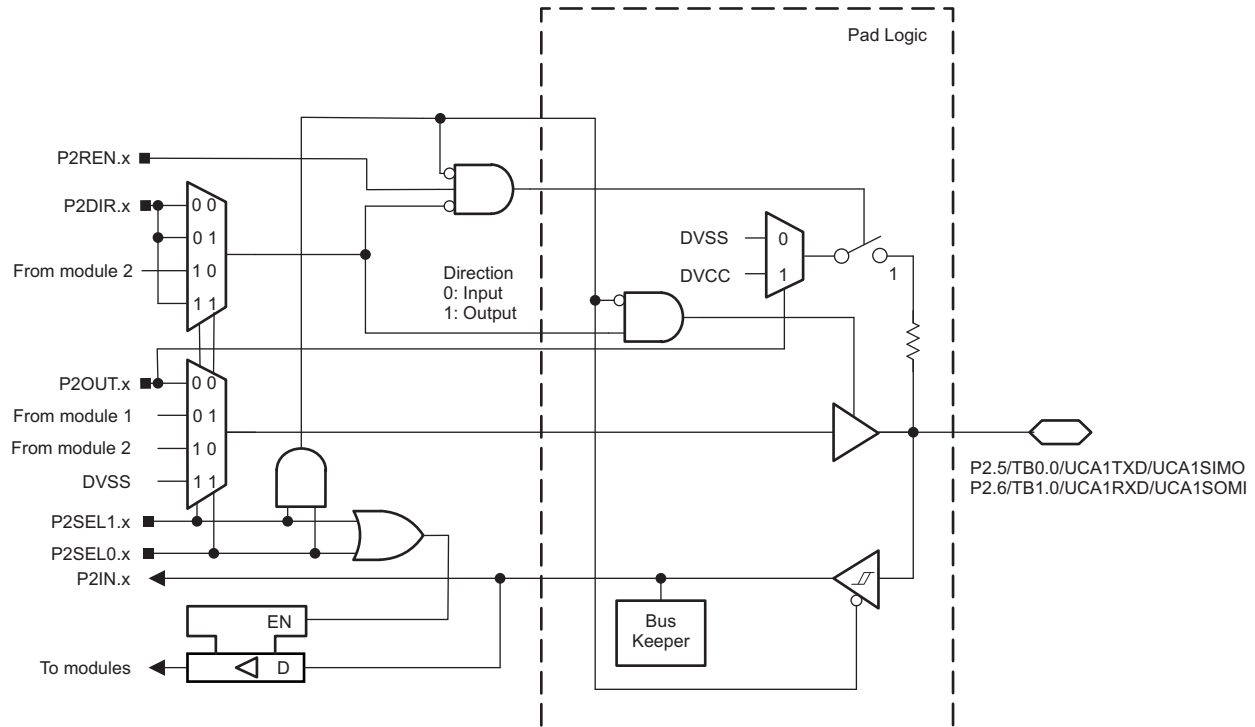


Figure 6-14. Port P2 (P2.5 and P2.6) Diagram

Table 6-44. Port P2 (P2.5 and P2.6) Pin Functions

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | | |
|-----------------------------|---|---------------------------------|-------------------------|----------|----------|
| | | | P2DIR.x | P2SEL1.x | P2SEL0.x |
| P2.5/TB0.0/UCA1TXD/UCA1SIMO | 5 | P2.5(I/O) ⁽¹⁾ | I: 0; O: 1 | 0 | 0 |
| | | TB0.CCI0B ⁽¹⁾ | 0 | 0 | 1 |
| | | TB0.0 ⁽¹⁾ | 1 | | |
| | | UCA1TXD/UCA1SIMO ⁽¹⁾ | X ⁽²⁾ | 1 | 0 |
| P2.6/TB1.0/UCA1RXD/UCA1SOMI | 6 | P2.6(I/O) ⁽¹⁾ | I: 0; O: 1 | 0 | 0 |
| | | TB1.CCI0B ⁽¹⁾ | 0 | 0 | 1 |
| | | TB1.0 ⁽¹⁾ | 1 | | |
| | | UCA1RXD/UCA1SOMI ⁽¹⁾ | X ⁽²⁾ | 1 | 0 |

(1) Not available on all devices and package types.

(2) Direction controlled by eUSCI_A1 module.

6.11.7 Port P2 (P2.7) Input/Output With Schmitt Trigger

Figure 6-15 shows the port diagram. Table 6-45 summarizes the selection of the pin functions.

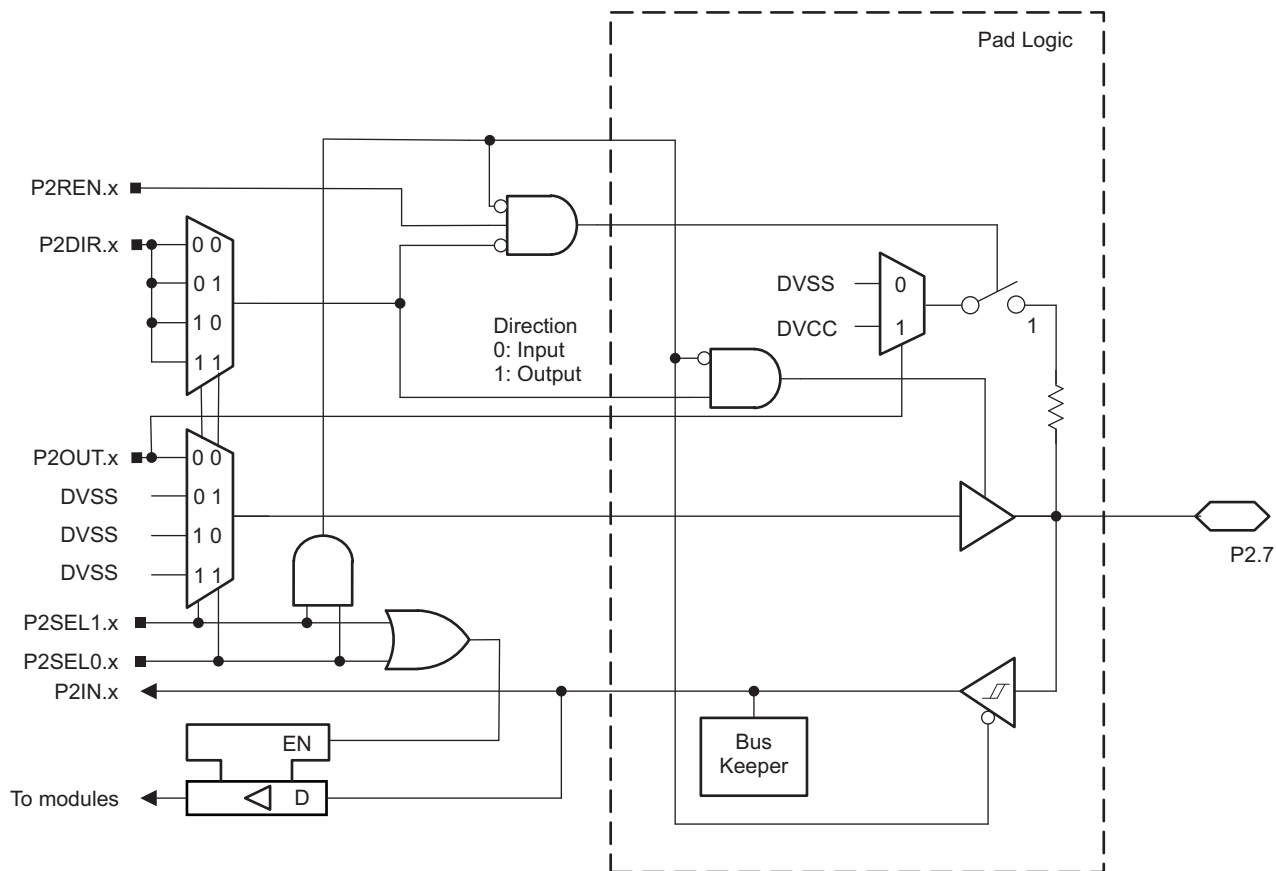


Figure 6-15. Port P2 (P2.7) Diagram

Table 6-45. Port P2 (P2.7) Pin Functions

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | | |
|-----------------|---|--------------------------|-------------------------|----------|----------|
| | | | P2DIR.x | P2SEL1.x | P2SEL0.x |
| P2.7 | 7 | P2.7(I/O) ⁽¹⁾ | I: 0; O: 1 | 0 | 0 |

(1) Not available on all devices and package types.

6.11.8 Port P3 (P3.0 to P3.3) Input/Output With Schmitt Trigger

Figure 6-16 shows the port diagram. Table 6-46 summarizes the selection of the pin functions.

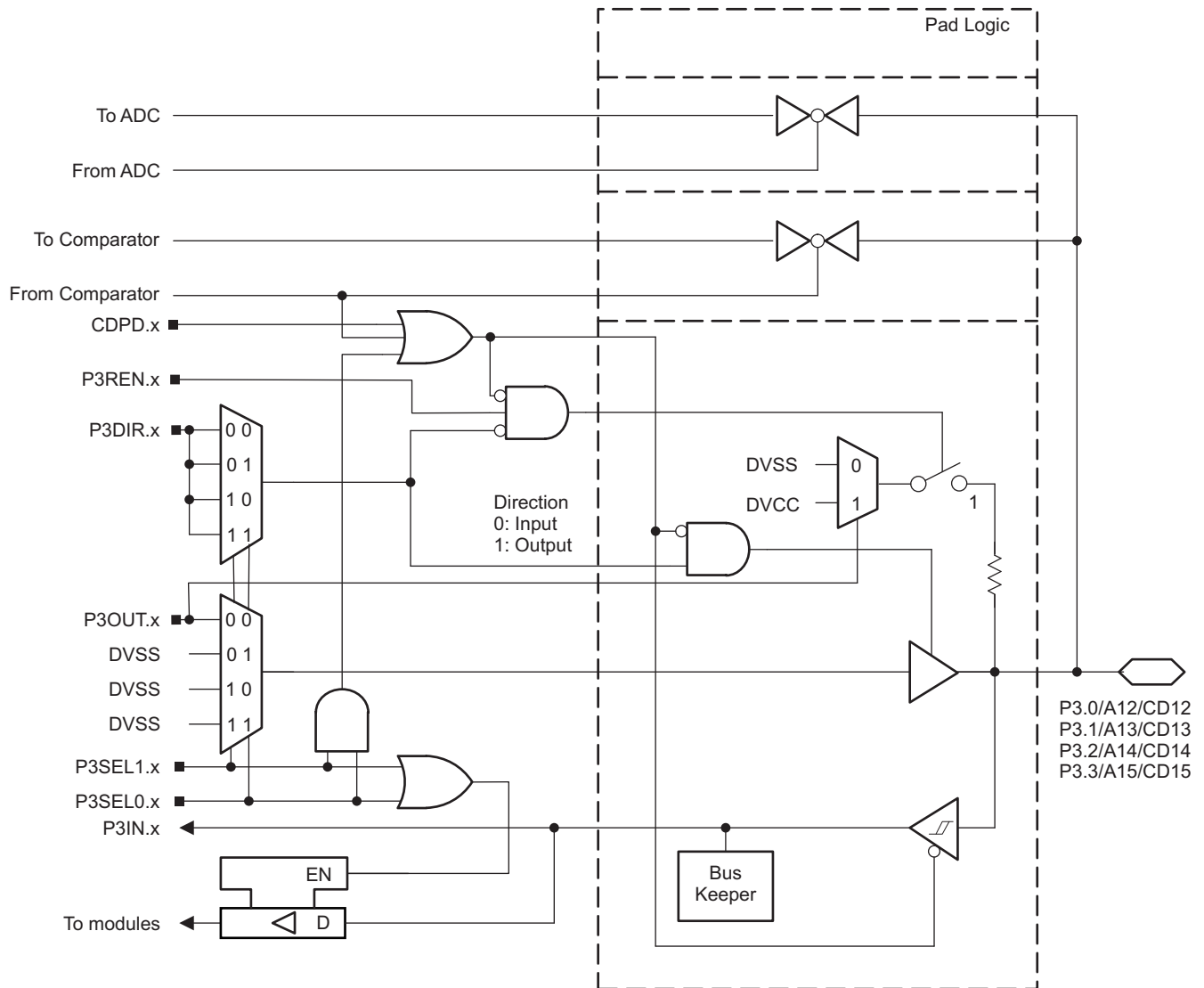


Figure 6-16. Port P3 (P3.0 to P3.3) Diagram

Table 6-46. Port P3 (P3.0 to P3.3) Pin Functions

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | | |
|-----------------|---|---|-------------------------|----------|----------|
| | | | P3DIR.x | P3SEL1.x | P3SEL0.x |
| P3.0/A12/CD12 | 0 | P3.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A12 ⁽¹⁾ ⁽²⁾ CD12 ⁽¹⁾ ⁽³⁾ | X | 1 | 1 |
| P3.1/A13/CD13 | 1 | P3.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A13 ⁽¹⁾ ⁽²⁾ CD13 ⁽¹⁾ ⁽³⁾ | X | 1 | 1 |
| P3.2/A14/CD14 | 2 | P3.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A14 ⁽¹⁾ ⁽²⁾ CD14 ⁽¹⁾ ⁽³⁾ | X | 1 | 1 |
| P3.3/A15/CD15 | 3 | P3.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A15 ⁽¹⁾ ⁽²⁾ CD15 ⁽¹⁾ ⁽³⁾ | X | 1 | 1 |

- (1) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
- (2) Not available on all devices and package types.
- (3) Setting the CDPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CDx input pin to the comparator multiplexer with the CDx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CDPD.x bit.

6.11.9 Port P3 (P3.4 to P3.6) Input/Output With Schmitt Trigger

Figure 6-17 shows the port diagram. Table 6-47 summarizes the selection of the pin functions.

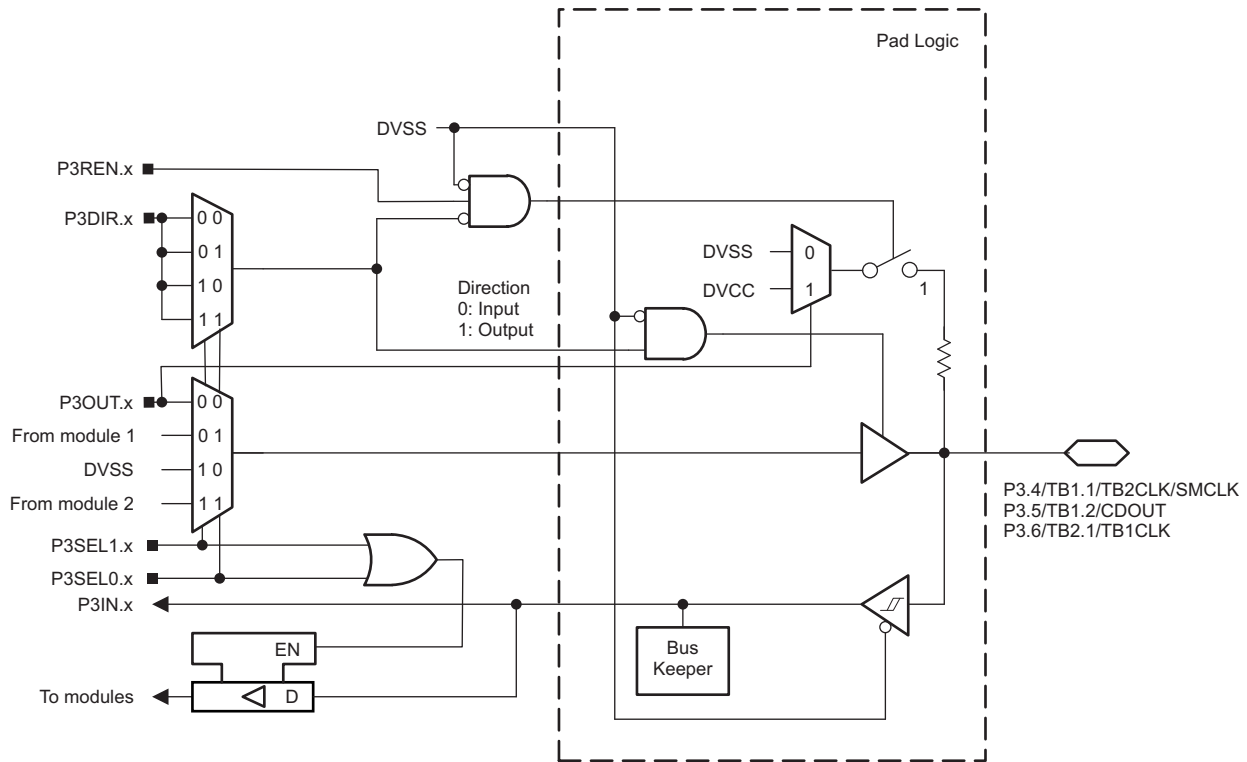


Figure 6-17. Port P3 (P3.4 to P3.6) Diagram

Table 6-47. Port P3 (P3.4 to P3.6) Pin Functions

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | | |
|-------------------------|---|---------------------------|-------------------------|----------|----------|
| | | | P3DIR.x | P3SEL1.x | P3SEL0.x |
| P3.4/TB1.1/TB2CLK/SMCLK | 4 | P3.4 (I/O) ⁽¹⁾ | I: 0; O: 1 | 0 | 0 |
| | | TB1.CCI1B ⁽¹⁾ | 0 | 0 | 1 |
| | | TB1.1 ⁽¹⁾ | 1 | | |
| | | TB2CLK ⁽¹⁾ | 0 | 1 | 1 |
| | | SMCLK ⁽¹⁾ | 1 | | |
| P3.5/TB1.2/CDOOUT | 5 | P3.5 (I/O) ⁽¹⁾ | I: 0; O: 1 | 0 | 0 |
| | | TB1.CCI2B ⁽¹⁾ | 0 | 0 | 1 |
| | | TB1.2 ⁽¹⁾ | 1 | | |
| | | CDOOUT ⁽¹⁾ | 1 | 1 | 1 |
| P3.6/TB2.1/TB1CLK | 6 | P3.6 (I/O) ⁽¹⁾ | I: 0; O: 1 | 0 | 0 |
| | | TB2.CCI1B ⁽¹⁾ | 0 | 0 | 1 |
| | | TB2.1 ⁽¹⁾ | 1 | | |
| | | TB1CLK ⁽¹⁾ | 0 | 1 | 1 |

(1) Not available on all devices and package types.

6.11.10 Port Port P3 (P3.7) Input/Output With Schmitt Trigger

Figure 6-18 shows the port diagram. Table 6-48 summarizes the selection of the pin functions.

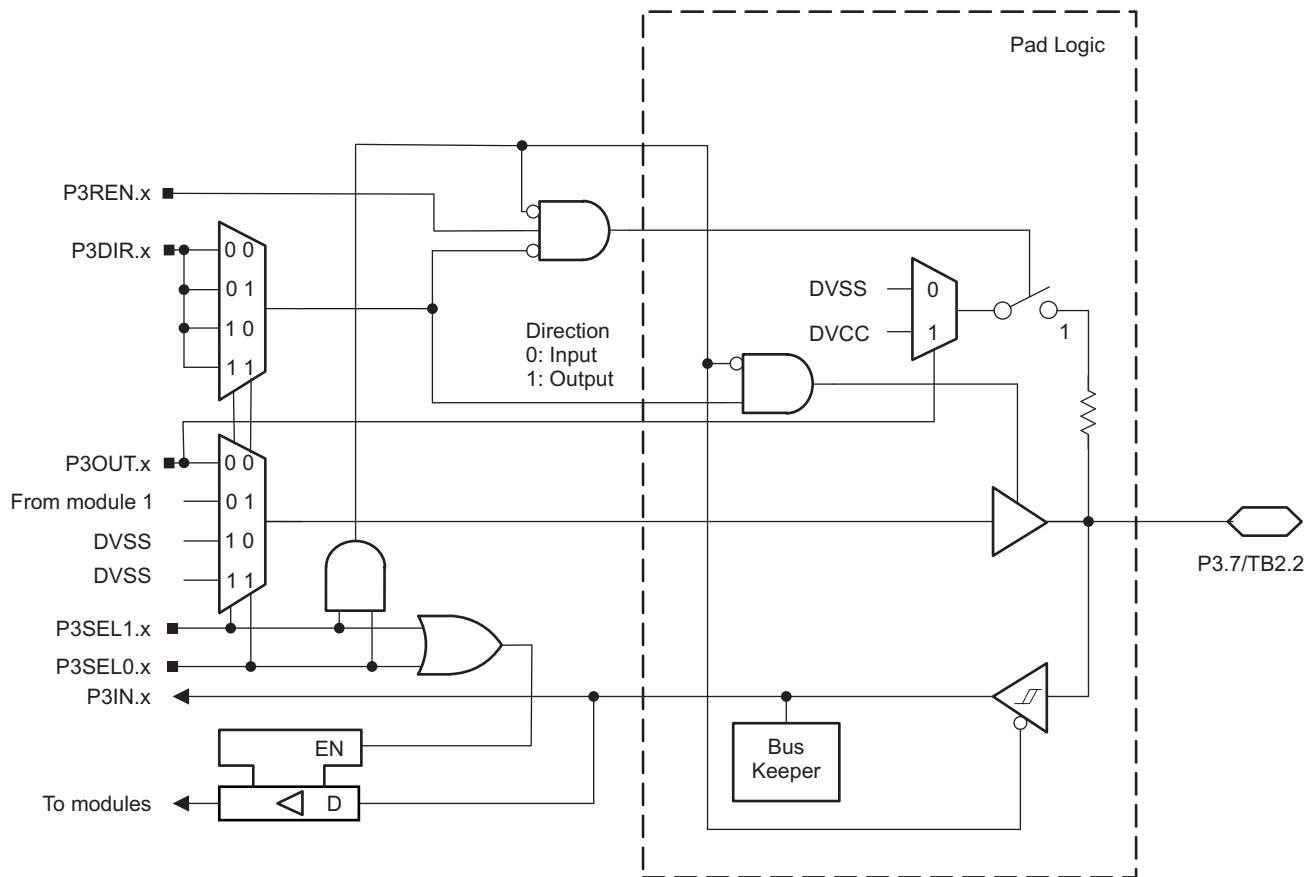


Figure 6-18. Port P3 (P3.7) Diagram

Table 6-48. Port P3 (P3.7) Pin Functions

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | | |
|-----------------|---|---------------------------|-------------------------|----------|----------|
| | | | P3DIR.x | P3SEL1.x | P3SEL0.x |
| P3.7/TB2.2 | 7 | P3.7 (I/O) ⁽¹⁾ | I: 0; O: 1 | 0 | 0 |
| | | TB2.CCI2B ⁽¹⁾ | 0 | 0 | 1 |
| | | TB2.2 ⁽¹⁾ | 1 | | |

(1) Not available on all devices and package types.

6.11.11 Port Port P4 (P4.0) Input/Output With Schmitt Trigger

Figure 6-19 shows the port diagram. Table 6-49 summarizes the selection of the pin functions.

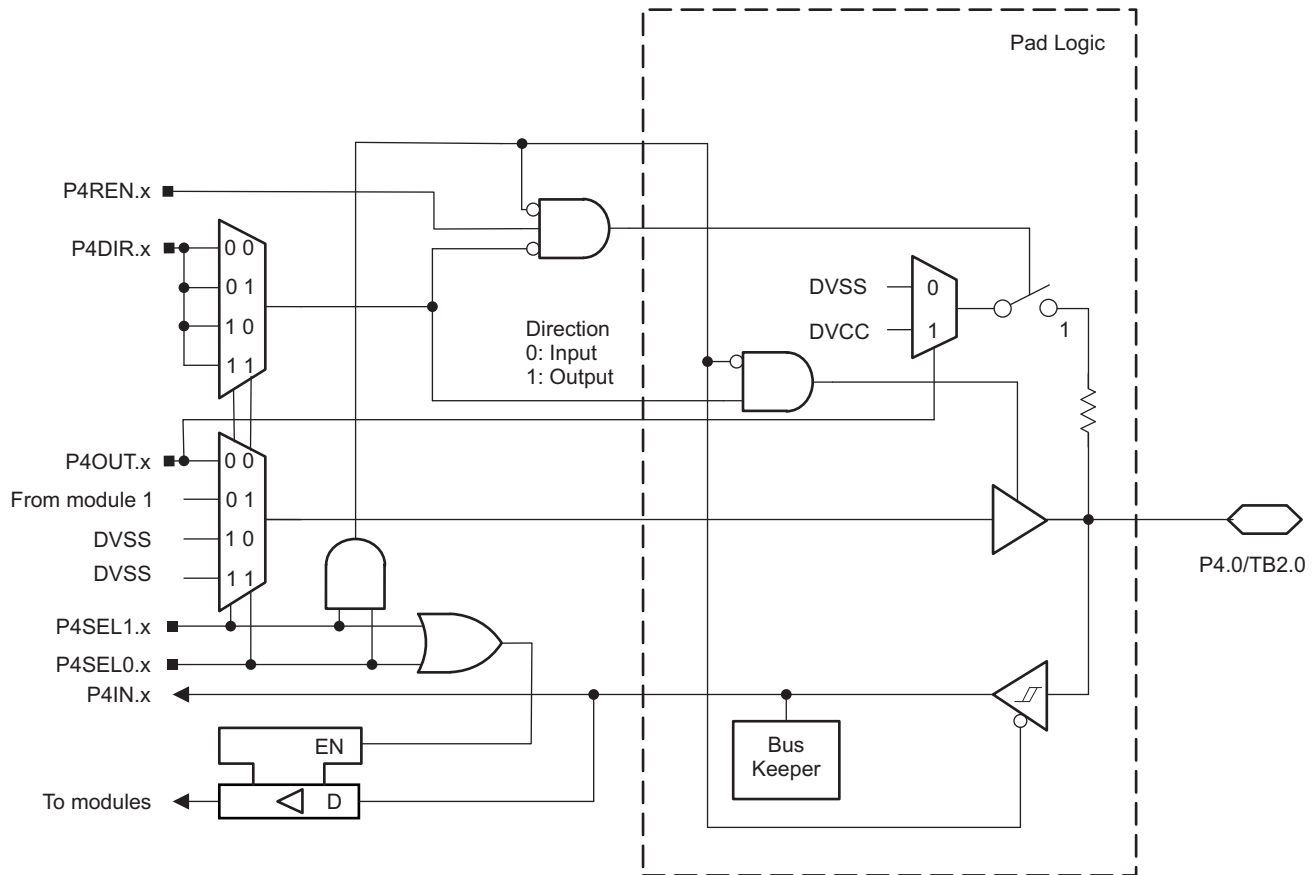


Figure 6-19. Port P4 (P4.0) Diagram

Table 6-49. Port P4 (P4.0) Pin Functions

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | | |
|-----------------|---|---------------------------|-------------------------|----------|----------|
| | | | P4DIR.x | P4SEL1.x | P4SEL0.x |
| P4.0/TB2.0 | 0 | P4.0 (I/O) ⁽¹⁾ | I: 0; O: 1 | 0 | 0 |
| | | TB2.CCI0B ⁽¹⁾ | 0 | 0 | 1 |
| | | TB2.0 ⁽¹⁾ | 1 | 0 | 1 |

(1) Not available on all devices and package types.

6.11.12 Port Port P4 (P4.1) Input/Output With Schmitt Trigger

Figure 6-20 shows the port diagram. Table 6-50 summarizes the selection of the pin functions.

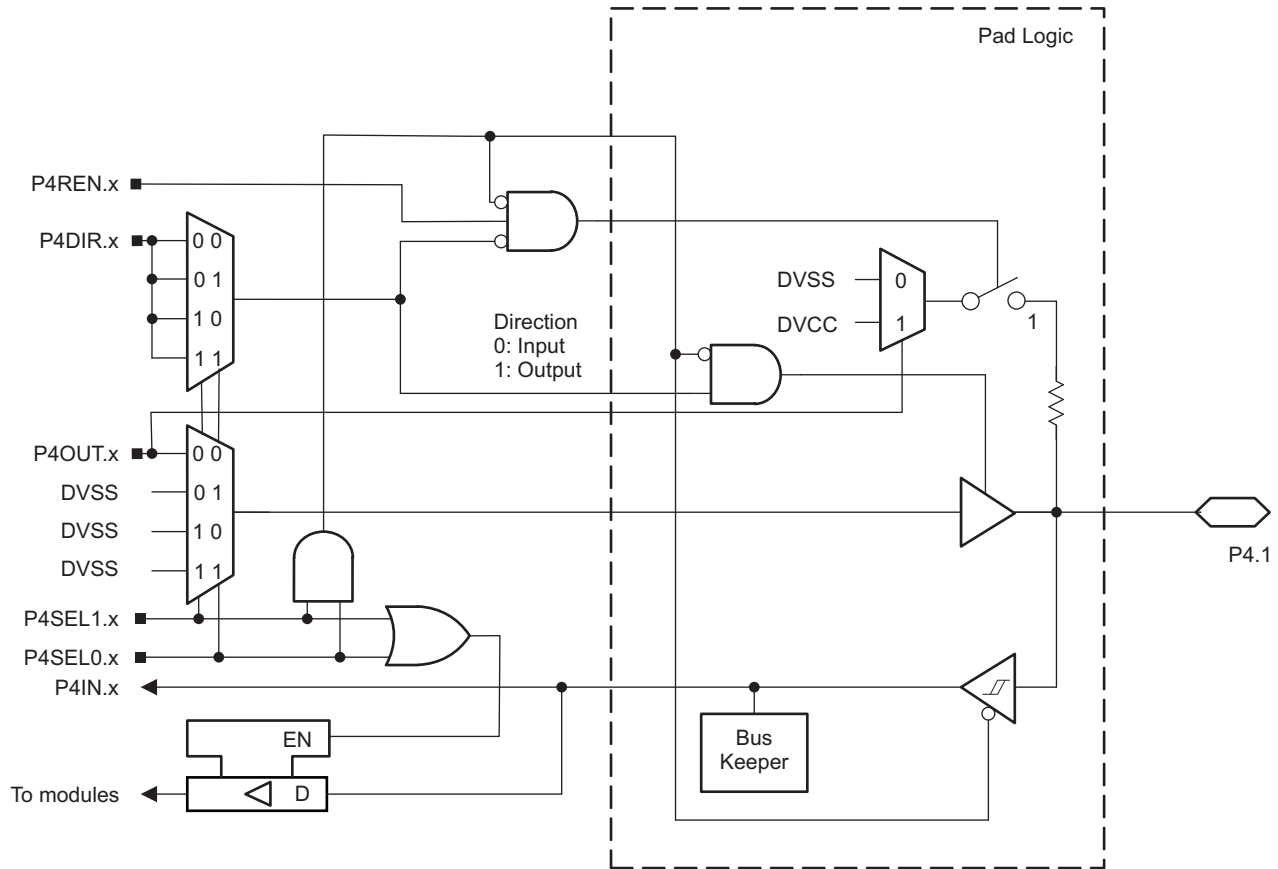


Figure 6-20. Port P4 (P4.1) Diagram

Table 6-50. Port P4 (P4.1) Pin Functions

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | | |
|-----------------|---|---------------------------|-------------------------|----------|----------|
| | | | P4DIR.x | P4SEL1.x | P4SEL0.x |
| P4.1 | 1 | P4.1 (I/O) ⁽¹⁾ | I: 0; O: 1 | 0 | 0 |

(1) Not available on all devices and package types.

6.11.13 Port Port PJ (PJ.0 to PJ.3) JTAG Pins TDO, TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

Figure 6-21 and Figure 6-22 show the port diagrams. Table 6-51 summarizes the selection of the pin functions.

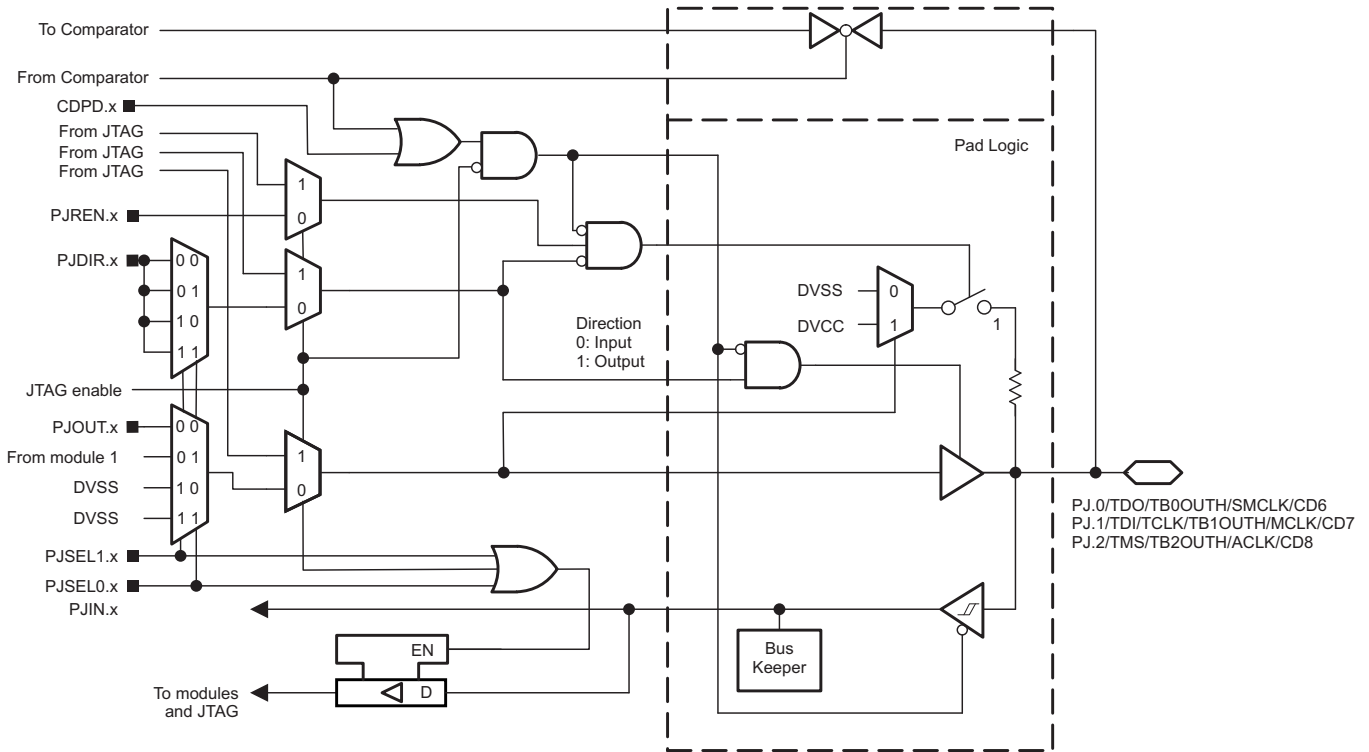


Figure 6-21. Port PJ (PJ.0 to PJ.2) Diagram

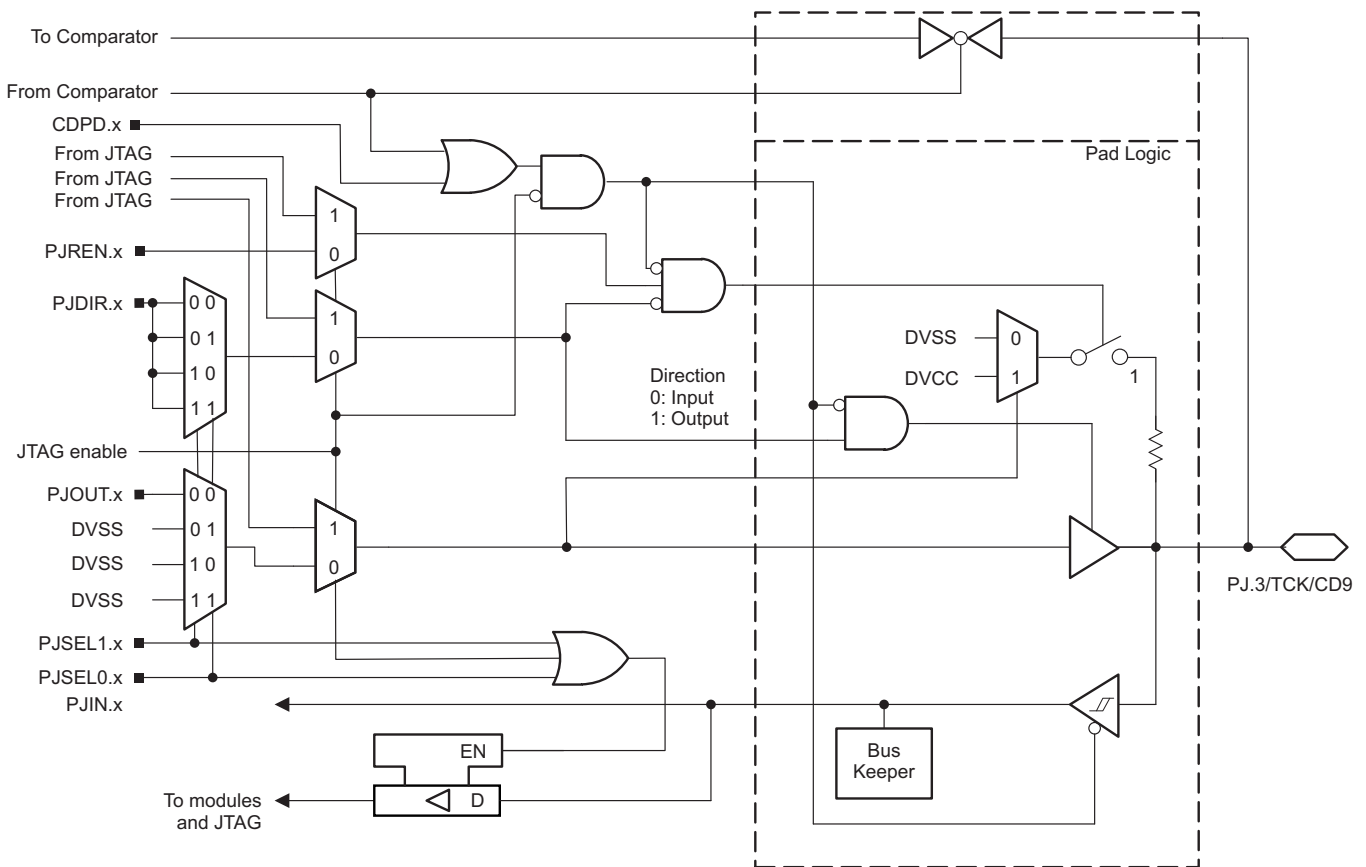


Figure 6-22. Port PJ (PJ.3) Diagram

Table 6-51. Port PJ (PJ.0 to PJ.3) Pin Functions

| PIN NAME (PJ.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|--------------------------------|---|-----------------------------|--|----------|----------|
| | | | PJDIR.x | PJSEL1.x | PJSEL0.x |
| PJ.0/TDO/TB0OUTH/SMCLK/CD6 | 0 | PJ.0 (I/O) ⁽²⁾ | I: 0; O: 1 | 0 | 0 |
| | | TDO ⁽³⁾ | X | X | X |
| | | TB0OUTH | 0 | 0 | 1 |
| | | SMCLK | 1 | | |
| | | CD6 | X | 1 | 1 |
| PJ.1/TDI/TCLK/TB1OUTH/MCLK/CD7 | 1 | PJ.1 (I/O) ⁽²⁾ | I: 0; O: 1 | 0 | 0 |
| | | TDI/TCLK ^{(3) (4)} | X | X | X |
| | | TB1OUTH | 0 | 0 | 1 |
| | | MCLK | 1 | | |
| | | CD7 | X | 1 | 1 |
| PJ.2/TMS/TB2OUTH/ACLK/CD8 | 2 | PJ.2 (I/O) ⁽²⁾ | I: 0; O: 1 | 0 | 0 |
| | | TMS ^{(3) (4)} | X | X | X |
| | | TB2OUTH | 0 | 0 | 1 |
| | | ACLK | 1 | | |
| | | CD8 | X | 1 | 1 |
| PJ.3/TCK/CD9 | 3 | PJ.3 (I/O) ⁽²⁾ | I: 0; O: 1 | 0 | 0 |
| | | TCK ^{(3) (4)} | X | X | X |
| | | CD9 | X | 1 | 1 |

(1) X = Don't care

(2) Default condition

(3) The pin direction is controlled by the JTAG module. JTAG mode selection is made by the SYS module or by the Spy-Bi-Wire four-wire entry sequence. PJSEL1.x and PJSEL0.x have no effect in these cases.

(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

6.11.14 Port Port PJ (PJ.4 and PJ.5) Input/Output With Schmitt Trigger

Figure 6-23 and Figure 6-24 show the port diagrams. Table 6-52 summarizes the selection of the pin functions.

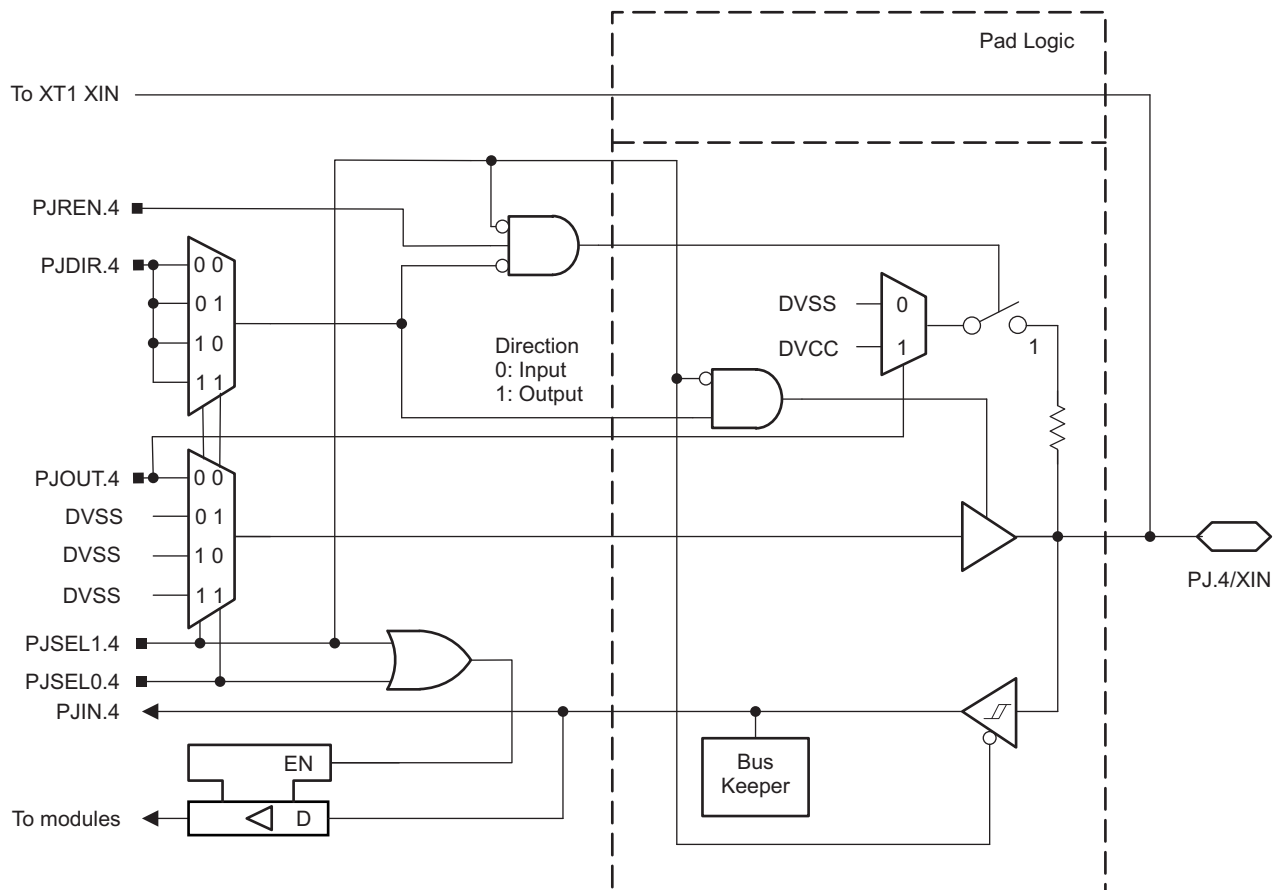


Figure 6-23. Port PJ (PJ.4) Diagram

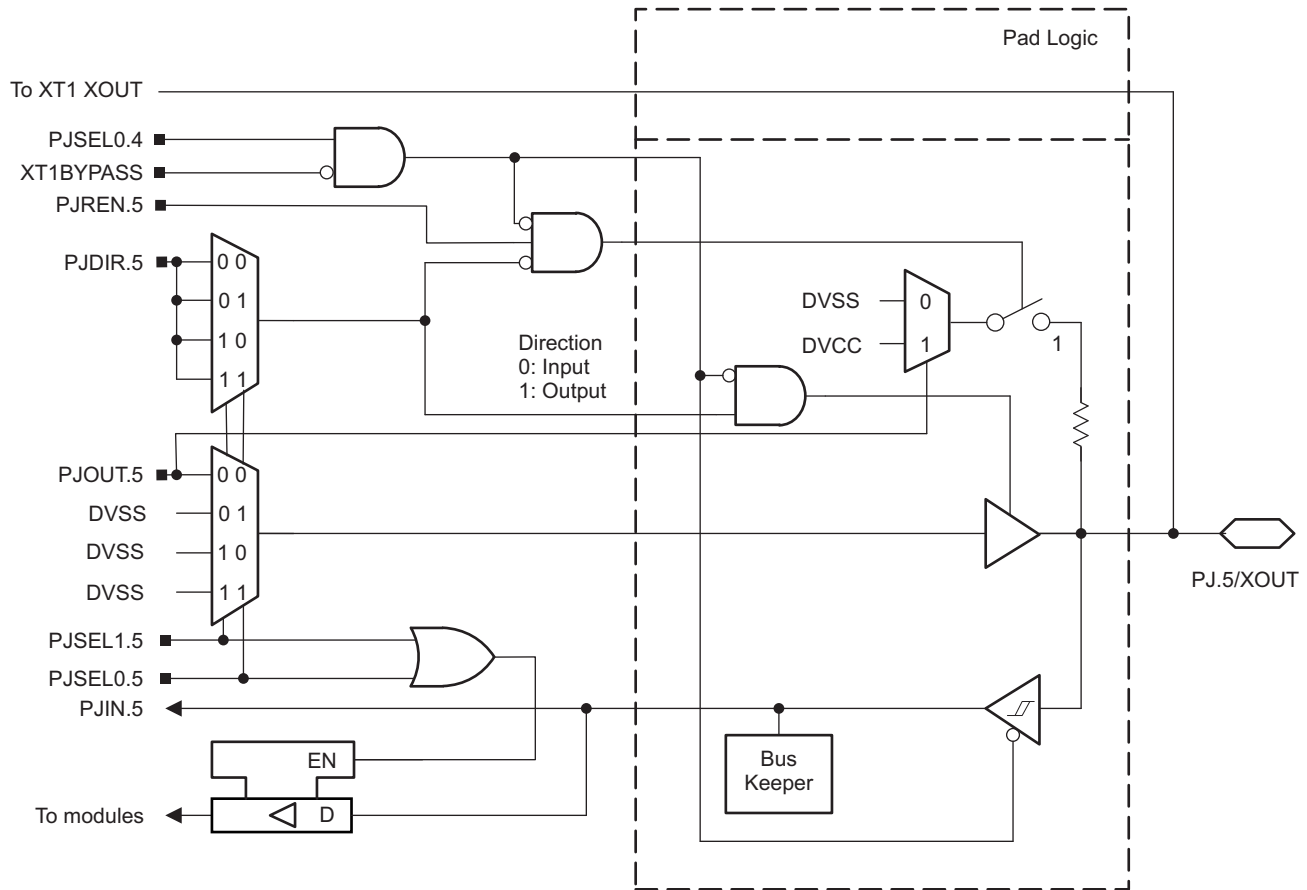


Figure 6-24. Port PJ (PJ.5) Diagram

Table 6-52. Port PJ (PJ.4 and PJ.5) Pin Functions

| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | | | |
|-----------------|---|----------------------------------|--|----------|----------|----------|----------|------------|
| | | | PJDIR.x | PJSEL1.5 | PJSEL0.5 | PJSEL1.4 | PJSEL0.4 | XT1 BYPASS |
| PJ.4/XIN | 4 | PJ.4 (I/O) | I: 0; O: 1 | X | X | 0 | 0 | X |
| | | XIN crystal mode ⁽²⁾ | X | X | X | 0 | 1 | 0 |
| | | XIN bypass mode ⁽²⁾ | X | X | X | 0 | 1 | 1 |
| PJ.5/XOUT | 5 | PJ.5 (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 | X |
| | | XOUT crystal mode ⁽²⁾ | X | X | X | 0 | 1 | 0 |
| | | PJ.5 (I/O) ⁽³⁾ | I: 0; O: 1 | X | X | 0 | 1 | 1 |

(1) X = Don't care

(2) Setting PJSEL1.4 = 0 and PJSEL0.4 = 1 causes the general-purpose I/O to be disabled. When XT1BYPASS = 0, PJ.4 and PJ.5 are configured for crystal operation and PJSEL1.5 and PJSEL0.5 are don't care. When XT1BYPASS = 1, PJ.4 is configured for bypass operation and PJ.5 is configured as general-purpose I/O.

(3) When PJ.4 is configured in bypass mode, PJ.5 is configured as general-purpose I/O.

6.12 Device Descriptors (TLV)

Table 6-53 and Table 6-54 list the complete contents of the device descriptor tag-length-value (TLV) structure for each device type.

Table 6-53. Device Descriptor Table ⁽¹⁾

| DESCRIPTION | | ADDRESS | VALUE | | | | |
|--|--|----------|----------|----------|----------|----------|----------|
| | | | FR5729 | FR5728 | FR5727 | FR5726 | FR5725 |
| Info Block | Info length | 01A00h | 05h | 05h | 05h | 05h | 05h |
| | CRC length | 01A01h | 05h | 05h | 05h | 05h | 05h |
| | CRC value | 01A02h | per unit | per unit | per unit | per unit | per unit |
| | | 01A03h | per unit | per unit | per unit | per unit | per unit |
| | Device ID | 01A04h | 7Bh | 7Ah | 79h | 74h | 78h |
| | Device ID | 01A05h | 80h | 80h | 80h | 81h | 80h |
| | Hardware revision | 01A06h | per unit | per unit | per unit | per unit | per unit |
| Firmware revision | 01A07h | per unit | per unit | per unit | per unit | per unit | |
| Die Record | Die Record Tag | 01A08h | 08h | 08h | 08h | 08h | 08h |
| | Die record length | 01A09h | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot/wafer ID | 01A0Ah | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Bh | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Ch | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Dh | per unit | per unit | per unit | per unit | per unit |
| | Die X position | 01A0Eh | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Fh | per unit | per unit | per unit | per unit | per unit |
| | Die Y position | 01A10h | per unit | per unit | per unit | per unit | per unit |
| | | 01A11h | per unit | per unit | per unit | per unit | per unit |
| Test results | 01A12h | per unit | per unit | per unit | per unit | per unit | |
| | 01A13h | per unit | per unit | per unit | per unit | per unit | |
| ADC10 Calibration | ADC10 calibration tag | 01A14h | 13h | 13h | 13h | 05h | 13h |
| | ADC10 calibration length | 01A15h | 10h | 10h | 10h | 10h | 10h |
| | ADC gain factor | 01A16h | per unit | per unit | NA | NA | per unit |
| | | 01A17h | per unit | per unit | NA | NA | per unit |
| | ADC offset | 01A18h | per unit | per unit | NA | NA | per unit |
| | | 01A19h | per unit | per unit | NA | NA | per unit |
| | ADC 1.5-V reference Temp. sensor 30°C | 01A1Ah | per unit | per unit | NA | NA | per unit |
| | | 01A1Bh | per unit | per unit | NA | NA | per unit |
| | ADC 1.5-V reference Temp. sensor 85°C | 01A1Ch | per unit | per unit | NA | NA | per unit |
| | | 01A1Dh | per unit | per unit | NA | NA | per unit |
| | ADC 2.0-V reference Temp. sensor 30°C | 01A1Eh | per unit | per unit | NA | NA | per unit |
| | | 01A1Fh | per unit | per unit | NA | NA | per unit |
| | ADC 2.0-V reference Temp. sensor 85°C | 01A20h | per unit | per unit | NA | NA | per unit |
| | | 01A21h | per unit | per unit | NA | NA | per unit |
| | ADC 2.5-V reference Temp. sensor 30°C | 01A22h | per unit | per unit | NA | NA | per unit |
| 01A23h | | per unit | per unit | NA | NA | per unit | |
| ADC 2.5-V reference Temp. sensor 85°C | 01A24h | per unit | per unit | NA | NA | per unit | |
| | 01A25h | per unit | per unit | NA | NA | per unit | |

(1) NA = Not applicable

Table 6-53. Device Descriptor Table ⁽¹⁾ (continued)

| DESCRIPTION | | ADDRESS | VALUE | | | | |
|-----------------|------------------------|----------|----------|----------|----------|----------|----------|
| | | | FR5729 | FR5728 | FR5727 | FR5726 | FR5725 |
| REF Calibration | REF calibration tag | 01A26h | 12h | 12h | 12h | 12h | 12h |
| | REF calibration length | 01A27h | 06h | 06h | 06h | 06h | 06h |
| | REF 1.5-V Reference | 01A28h | per unit | per unit | per unit | per unit | per unit |
| | | 01A29h | per unit | per unit | per unit | per unit | per unit |
| | REF 2.0-V reference | 01A2Ah | per unit | per unit | per unit | per unit | per unit |
| | | 01A2Bh | per unit | per unit | per unit | per unit | per unit |
| | REF 2.5-V reference | 01A2Ch | per unit | per unit | per unit | per unit | per unit |
| 01A2Dh | | per unit | per unit | per unit | per unit | per unit | |

Table 6-54. Device Descriptor Table ⁽¹⁾

| DESCRIPTION | | ADDRESS | VALUE | | | | |
|-------------------|-------------------|----------|----------|----------|----------|----------|----------|
| | | | FR5724 | FR5723 | FR5722 | FR5721 | FR5720 |
| Info Block | Info length | 01A00h | 05h | 05h | 05h | 05h | 05h |
| | CRC length | 01A01h | 05h | 05h | 05h | 05h | 05h |
| | CRC value | 01A02h | per unit | per unit | per unit | per unit | per unit |
| | | 01A03h | per unit | per unit | per unit | per unit | per unit |
| | Device ID | 01A04h | 73h | 72h | 71h | 77h | 70h |
| | Device ID | 01A05h | 81h | 81h | 81h | 80h | 81h |
| | Hardware revision | 01A06h | per unit | per unit | per unit | per unit | per unit |
| Firmware revision | 01A07h | per unit | per unit | per unit | per unit | per unit | |
| Die Record | Die record tag | 01A08h | 08h | 08h | 08h | 08h | 08h |
| | Die record length | 01A09h | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot/wafer ID | 01A0Ah | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Bh | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Ch | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Dh | per unit | per unit | per unit | per unit | per unit |
| | Die X position | 01A0Eh | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Fh | per unit | per unit | per unit | per unit | per unit |
| | Die Y position | 01A10h | per unit | per unit | per unit | per unit | per unit |
| | | 01A11h | per unit | per unit | per unit | per unit | per unit |
| Test results | 01A12h | per unit | per unit | per unit | per unit | per unit | |
| | 01A13h | per unit | per unit | per unit | per unit | per unit | |

(1) NA = Not applicable

Table 6-54. Device Descriptor Table ⁽¹⁾ (continued)

| DESCRIPTION | | ADDRESS | VALUE | | | | |
|--|--|----------|----------|----------|----------|----------|----------|
| | | | FR5724 | FR5723 | FR5722 | FR5721 | FR5720 |
| ADC10 Calibration | ADC10 calibration tag | 01A14h | 13h | 13h | 13h | 05h | 13h |
| | ADC10 calibration length | 01A15h | 10h | 10h | 10h | 10h | 10h |
| | ADC gain factor | 01A16h | per unit | NA | NA | per unit | per unit |
| | | 01A17h | per unit | NA | NA | per unit | per unit |
| | ADC offset | 01A18h | per unit | NA | NA | per unit | per unit |
| | | 01A19h | per unit | NA | NA | per unit | per unit |
| | ADC 1.5-V reference Temp. sensor 30°C | 01A1Ah | per unit | NA | NA | per unit | per unit |
| | | 01A1Bh | per unit | NA | NA | per unit | per unit |
| | ADC 1.5-V reference Temp. sensor 85°C | 01A1Ch | per unit | NA | NA | per unit | per unit |
| | | 01A1Dh | per unit | NA | NA | per unit | per unit |
| | ADC 2.0-V reference Temp. sensor 30°C | 01A1Eh | per unit | NA | NA | per unit | per unit |
| | | 01A1Fh | per unit | NA | NA | per unit | per unit |
| | ADC 2.0-V reference Temp. sensor 85°C | 01A20h | per unit | NA | NA | per unit | per unit |
| | | 01A21h | per unit | NA | NA | per unit | per unit |
| | ADC 2.5-V reference Temp. sensor 30°C | 01A22h | per unit | NA | NA | per unit | per unit |
| | | 01A23h | per unit | NA | NA | per unit | per unit |
| ADC 2.5-V reference Temp. sensor 85°C | 01A24h | per unit | NA | NA | per unit | per unit | |
| | 01A25h | per unit | NA | NA | per unit | per unit | |
| REF Calibration | REF calibration tag | 01A26h | 12h | 12h | 12h | 12h | 12h |
| | REF calibration length | 01A27h | 06h | 06h | 06h | 06h | 06h |
| | REF 1.5-V reference | 01A28h | per unit | per unit | per unit | per unit | per unit |
| | | 01A29h | per unit | per unit | per unit | per unit | per unit |
| | REF 2.0-V reference | 01A2Ah | per unit | per unit | per unit | per unit | per unit |
| | | 01A2Bh | per unit | per unit | per unit | per unit | per unit |
| | REF 2.5-V reference | 01A2Ch | per unit | per unit | per unit | per unit | per unit |
| | | 01A2Dh | per unit | per unit | per unit | per unit | per unit |

7 Device and Documentation Support

7.1 Getting Started

TI provides all of the hardware platforms and software components and tooling you need to get started today! Not only that, TI has many complementary components to meet your needs. For an overview of the MSP430™ MCU product line, the available development tools and evaluation kits, and advanced development resources, visit the [MSP430 Getting Started](#) page.

7.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP430 MCU devices and support tools. Each MSP430 MCU commercial family member has one of three prefixes: MSP, PMS, or XMS (for example, MSP430F5438A). TI recommends two of three possible prefix designators for its support tools: MSP and MSPX. These prefixes represent evolutionary stages of product development from engineering prototypes (with XMS for devices and MSPX for tools) through fully qualified production devices and tools (with MSP for devices and MSP for tools).

Device development evolutionary flow:

XMS – Experimental device that is not necessarily representative of the electrical specifications for the final device

PMS – Final silicon die that conforms to the electrical specifications for the device but has not completed quality and reliability verification

MSP – Fully qualified production device

Support tool development evolutionary flow:

MSPX – Development-support product that has not yet completed TI's internal qualification testing.

MSP – Fully-qualified development-support product

XMS and PMS devices and MSPX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices and MSP development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS and PMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PZP) and temperature range (for example, T). [Figure 7-1](#) provides a legend for reading the complete device name for any family member.

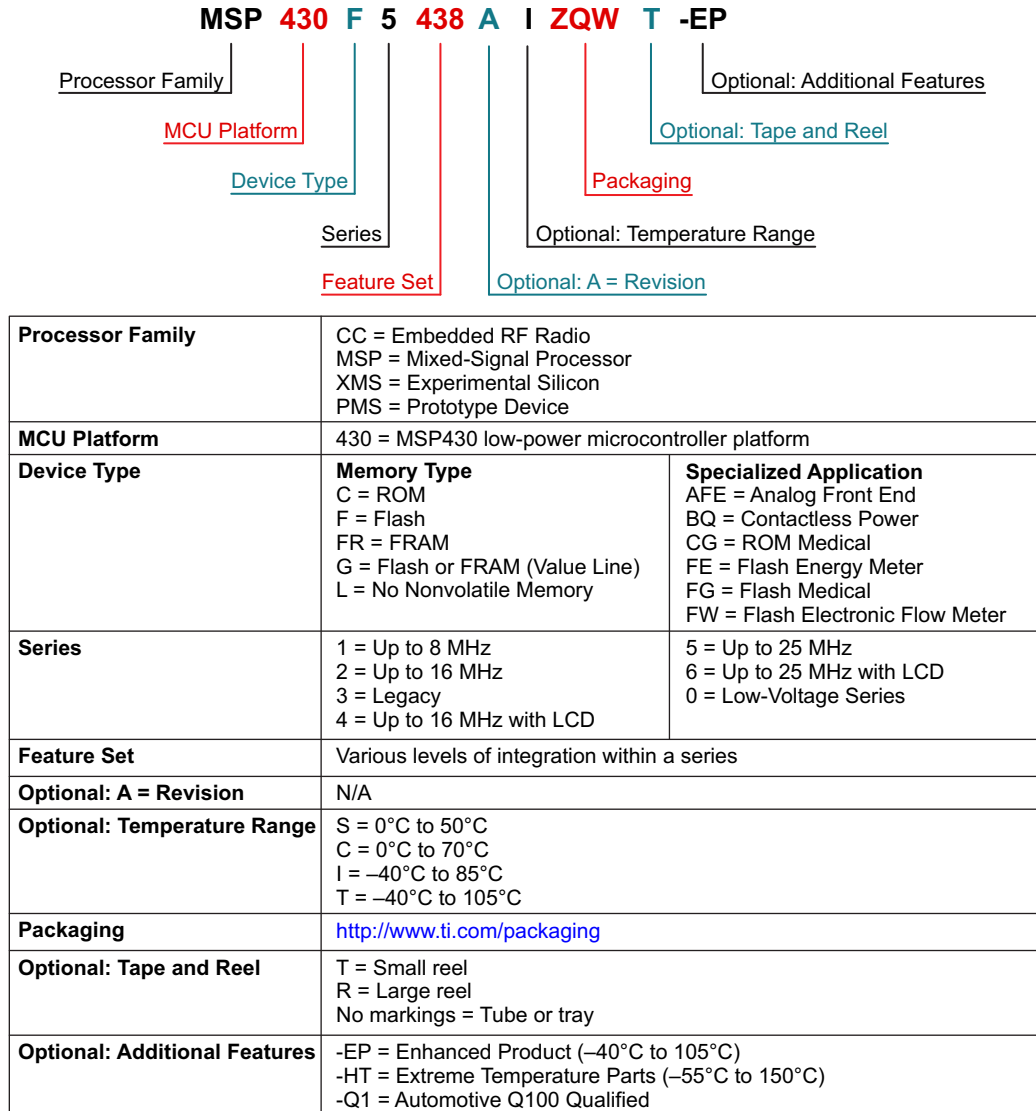


Figure 7-1. Device Nomenclature

7.3 Tools and Software

Table 7-1 lists the debug features supported by these microcontrollers. See the [Code Composer Studio for MSP430 User's Guide](#) for details on the available features.

Table 7-1. Hardware Features

| MSP430 ARCHITECTURE | 4-WIRE JTAG | 2-WIRE JTAG | BREAK-POINTS (N) | RANGE BREAK-POINTS | CLOCK CONTROL | STATE SEQUENCER | TRACE BUFFER | LPMx.5 DEBUGGING SUPPORT |
|---------------------|-------------|-------------|------------------|--------------------|---------------|-----------------|--------------|--------------------------|
| MSP430Xv2 | Yes | Yes | 3 | Yes | Yes | No | No | Yes |

Design Kits and Evaluation Modules

EEPROM Emulation and Sensing With MSP430 FRAM Microcontrollers This TI Design reference design describes an implementation of emulating EEPROM using Ferroelectric Random Access Memory (FRAM) technology on MSP430™ ultra-low-power microcontrollers (MCUs) combined with the additional sensing capabilities that can be enabled when using an MCU. The reference design supports both I2C and SPI interface to a host processor with multiple slave addressing.

MSP-EXP430FR5739 Experimenter Board The MSP-EXP430FR5739 Experimenter Board is a development platform for the MSP430FR57xx devices. It supports this new generation of MSP430 microcontroller devices with integrated Ferroelectric Random Access Memory (FRAM). The board is compatible with many TI low-power RF wireless evaluation modules such as the CC2520EMK. The Experimenter Board helps designers quickly learn and develop using the new MSP430FR57xx MCUs, which provide the industry's lowest overall power consumption, fast data read /write and unbeatable memory endurance. The MSP-EXP430FR5739 Experimenter Board can help evaluate and drive development for data logging applications, energy harvesting, wireless sensing, automatic metering infrastructure (AMI) and many others.

MSP-TS430RHA40A - 40-pin Target Development Board for MSP430FRxx FRAM MCUs The MSP-TS430RHA40A is a stand-alone 40-pin ZIF socket target board used to program and debug the MSP430 MCU in-system through the JTAG interface or the Spy Bi-Wire (2-wire JTAG) protocol.

Software

MSP430Ware™ Software MSP430Ware software is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 design resources, MSP430Ware software also includes a high-level API called MSP430 Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware software is available as a component of CCS or as a stand-alone package.

MSP430FR573x, MSP430FR572x C Code Examples C Code examples are available for every MSP device that configures each of the integrated peripherals for various application needs.

MSP Driver Library Driver Library's abstracted API keeps you above the bits and bytes of the MSP430 hardware by providing easy-to-use function calls. Thorough documentation is delivered through a helpful API Guide, which includes details on each function call and the recognized parameters. Developers can use Driver Library functions to write complete projects with minimal overhead.

MSP EnergyTrace™ Technology EnergyTrace technology for MSP430 microcontrollers is an energy-based code analysis tool that measures and displays the application's energy profile and helps to optimize it for ultra-low-power consumption.

ULP (Ultra-Low Power) Advisor ULP Advisor™ software is a tool for guiding developers to write more efficient code to fully utilize the unique ultra-low power features of MSP and MSP432 microcontrollers. Aimed at both experienced and new microcontroller developers, ULP Advisor checks your code against a thorough ULP checklist to squeeze every last nano amp out of your application. At build time, ULP Advisor will provide notifications and remarks to highlight areas of your code that can be further optimized for lower power.

IEC60730 Software Package The IEC60730 MSP430 software package was developed to be useful in assisting customers in complying with IEC 60730-1:2010 (Automatic Electrical Controls for Household and Similar Use – Part 1: General Requirements) for up to Class B products, which includes home appliances, arc detectors, power converters, power tools, e-bikes, and many others. The IEC60730 MSP430 software package can be embedded in customer applications running on MSP430s to help simplify the customer's certification efforts of functional safety-compliant consumer devices to IEC 60730-1:2010 Class B.

Fixed-Point Math Library for MSP The MSP IQmath and Qmath Libraries are a collection of highly optimized and high-precision mathematical functions for C programmers to seamlessly port a floating-point algorithm into fixed-point code on MSP430 and MSP432 devices. These routines are typically used in computationally intensive real-time applications where optimal execution speed, high accuracy, and ultra-low energy are critical. By using the IQmath and Qmath libraries, it is possible to achieve execution speeds considerably faster and energy consumption considerably lower than equivalent code written using floating-point math.

Floating-Point Math Library for MSP430 Continuing to innovate in the low power and low cost microcontroller space, TI brings you MSPMATHLIB. Leveraging the intelligent peripherals of our devices, this floating point math library of scalar functions brings you up to 26x better performance. Mathlib is easy to integrate into your designs. This library is free and is integrated in both Code Composer Studio and IAR IDEs. Read the user's guide for an in depth look at the math library and relevant benchmarks.

Development Tools

Code Composer Studio™ Integrated Development Environment for MSP Microcontrollers Code Composer Studio is an integrated development environment (IDE) that supports all MSP microcontroller devices. Code Composer Studio comprises a suite of embedded software utilities used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar utilities and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers. When using CCS with an MSP MCU, a unique and powerful set of plugins and embedded software utilities are made available to fully leverage the MSP microcontroller.

Command-Line Programmer MSP Flasher is an open-source shell-based interface for programming MSP microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP Flasher can download binary files (.txt or .hex) files directly to the MSP microcontroller without an IDE.

MSP MCU Programmer and Debugger The MSP-FET is a powerful emulation development tool – often called a debug probe – which allows users to quickly begin application development on MSP low-power microcontrollers (MCU). Creating MCU software usually requires downloading the resulting binary program to the MSP device for validation and debugging. The MSP-FET provides a debug communication pathway between a host computer and the target MSP. Furthermore, the MSP-FET also provides a Backchannel UART connection between the computer's USB interface and the MSP UART. This affords the MSP programmer a convenient method for communicating serially between the MSP and a terminal running on the computer. It also supports loading programs (often called firmware) to the MSP target using the BSL (bootloader) through the UART and I²C communication protocols.

MSP-GANG Production Programmer The MSP Gang Programmer is an MSP430 or MSP432 device programmer that can program up to eight identical MSP430 or MSP432 Flash or FRAM devices at the same time. The MSP Gang Programmer connects to a host PC using a standard RS-232 or USB connection and provides flexible programming options that allow the user to fully customize the process. The MSP Gang Programmer is provided with an expansion board, called the Gang Splitter, that implements the interconnections between the MSP Gang Programmer and multiple target devices. Eight cables are provided that connect the expansion board to eight target devices (through JTAG or Spy-Bi-Wire connectors). The programming can be done with a PC or as a stand-alone device. A PC-side graphical user interface is also available and is DLL-based.

7.4 Documentation Support

The following documents describe the [MSP430FR572x](#) MCUs. Copies of these documents are available on the Internet at www.ti.com.

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (for example, [MSP430FR5729](#)). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

Errata

[MSP430FR5729 Device Erratasheet](#) Describes the known exceptions to the functional specifications for each silicon revision of this device.

[MSP430FR5728 Device Erratasheet](#) Describes the known exceptions to the functional specifications for each silicon revision of this device.

[MSP430FR5727 Device Erratasheet](#) Describes the known exceptions to the functional specifications for each silicon revision of this device.

[MSP430FR5726 Device Erratasheet](#) Describes the known exceptions to the functional specifications for each silicon revision of this device.

[MSP430FR5725 Device Erratasheet](#) Describes the known exceptions to the functional specifications for each silicon revision of this device.

[MSP430FR5724 Device Erratasheet](#) Describes the known exceptions to the functional specifications for each silicon revision of this device.

[MSP430FR5723 Device Erratasheet](#) Describes the known exceptions to the functional specifications for each silicon revision of this device.

[MSP430FR5722 Device Erratasheet](#) Describes the known exceptions to the functional specifications for each silicon revision of this device.

[MSP430FR5721 Device Erratasheet](#) Describes the known exceptions to the functional specifications for each silicon revision of this device.

MSP430FR5720 Device Erratasheet Describes the known exceptions to the functional specifications for each silicon revision of this device.

User's Guides

MSP430FR57xx Family User's Guide Detailed description of all modules and peripherals available in this device family.

MSP430 Programming With the Bootloader (BSL) The MSP430 bootloader (BSL, formerly known as the bootstrap loader) allows users to communicate with embedded memory in the MSP430 microcontroller during the prototyping phase, final production, and in service. Both the programmable memory (flash memory) and the data memory (RAM) can be modified as required. Do not confuse the bootloader with the bootstrap loader programs found in some digital signal processors (DSPs) that automatically load program code (and data) from external memory to the internal memory of the DSP.

MSP430 Programming With the JTAG Interface This document describes the functions that are required to erase, program, and verify the memory module of the MSP430 flash-based and FRAM-based microcontroller families using the JTAG communication port. In addition, it describes how to program the JTAG access security fuse that is available on all MSP430 devices. This document describes device access using both the standard 4-wire JTAG interface and the 2-wire JTAG interface, which is also referred to as Spy-Bi-Wire (SBW).

MSP430 Hardware Tools User's Guide This manual describes the hardware of the TI MSP-FET430 Flash Emulation Tool (FET). The FET is the program development tool for the MSP430 ultra-low-power microcontroller. Both available interface types, the parallel port interface and the USB interface, are described.

Application Reports

MSP430 FRAM Technology – How To and Best Practices FRAM is a nonvolatile memory technology that behaves similar to SRAM while enabling a whole host of new applications, but also changing the way firmware should be designed. This application report outlines the how to and best practices of using FRAM technology in MSP430 from an embedded software development perspective. It discusses how to implement a memory layout according to application-specific code, constant, data space requirements, the use of FRAM to optimize application energy consumption, and the use of the Memory Protection Unit (MPU) to maximize application robustness by protecting the program code against unintended write accesses.

MSP430 FRAM Quality and Reliability FRAM is a nonvolatile embedded memory technology and is known for its ability to be ultra-low power while being the most flexible and easy-to-use universal memory solution available today. This application report is intended to give new FRAM users and those migrating from flash-based applications knowledge on how FRAM meets key quality and reliability requirements such as data retention and endurance.

Maximizing Write Speed on the MSP430™ FRAM Nonvolatile low-power ferroelectric RAM (FRAM) is capable of extremely high-speed write accesses. This application report discusses how to maximize FRAM write speeds specifically in the MSP430FRxx family using simple techniques. The document uses examples from bench tests performed on the MSP430FR5739 device, which can be extended to all MSP430™ FRAM-based devices, and discusses tradeoffs such as CPU clock frequency and block size and how they impact the FRAM write speed.

MSP430 System-Level ESD Considerations System-Level ESD has become increasingly demanding with silicon technology scaling towards lower voltages and the need for designing cost-effective and ultra-low-power components. This application report addresses three different ESD topics to help board designers and OEMs understand and design robust system-level designs: (1) Component-level ESD testing and system-level ESD testing, their differences and why component-level ESD rating does not ensure system-level robustness. (2) General design guidelines for system-level ESD protection at different levels including enclosures, cables, PCB layout, and on-board ESD protection devices. (3) Introduction to System Efficient ESD Design (SEED), a co-design methodology of on-board and on-chip ESD protection to achieve system-level ESD robustness, with example simulations and test results. A few real-world system-level ESD protection design examples and their results are also discussed.

MSP430 32-kHz Crystal Oscillators Selection of the right crystal, correct load circuit, and proper board layout are important for a stable crystal oscillator. This application report summarizes crystal oscillator function and explains the parameters to select the correct crystal for MSP430 ultra-

low-power operation. In addition, hints and examples for correct board layout are given. The document also contains detailed information on the possible oscillator tests to ensure stable oscillator operation in mass production.

7.5 Related Links

Table 7-2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7-2. Related Links

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|--------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| MSP430FR5729 | Click here | Click here | Click here | Click here | Click here |
| MSP430FR5728 | Click here | Click here | Click here | Click here | Click here |
| MSP430FR5727 | Click here | Click here | Click here | Click here | Click here |
| MSP430FR5726 | Click here | Click here | Click here | Click here | Click here |
| MSP430FR5725 | Click here | Click here | Click here | Click here | Click here |
| MSP430FR5724 | Click here | Click here | Click here | Click here | Click here |
| MSP430FR5723 | Click here | Click here | Click here | Click here | Click here |
| MSP430FR5722 | Click here | Click here | Click here | Click here | Click here |
| MSP430FR5721 | Click here | Click here | Click here | Click here | Click here |
| MSP430FR5720 | Click here | Click here | Click here | Click here | Click here |

7.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Community

TI's *Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki

Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.7 Trademarks

MSP430, MSP430Ware, EnergyTrace, ULP Advisor, Code Composer Studio, E2E are trademarks of Texas Instruments.

All other trademarks are the property of their respective owners.

7.8 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

7.10 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430FR5720IPW | ACTIVE | TSSOP | PW | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430FR5720 | Samples |
| MSP430FR5720IPWR | ACTIVE | TSSOP | PW | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430FR5720 | Samples |
| MSP430FR5720IRGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 430FR 5720 | Samples |
| MSP430FR5720IRGET | ACTIVE | VQFN | RGE | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 430FR 5720 | Samples |
| MSP430FR5721IDA | ACTIVE | TSSOP | DA | 38 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430FR5721 | Samples |
| MSP430FR5721IDAR | ACTIVE | TSSOP | DA | 38 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430FR5721 | Samples |
| MSP430FR5721IRHAR | ACTIVE | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430 FR5721 | Samples |
| MSP430FR5721IRHAT | ACTIVE | VQFN | RHA | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430 FR5721 | Samples |
| MSP430FR5722IPW | ACTIVE | TSSOP | PW | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430FR5722 | Samples |
| MSP430FR5722IRGET | NRND | VQFN | RGE | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 430FR 5722 | |
| MSP430FR5723IRHAR | ACTIVE | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430 FR5723 | Samples |
| MSP430FR5723IRHAT | ACTIVE | VQFN | RHA | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430 FR5723 | Samples |
| MSP430FR5724IPW | ACTIVE | TSSOP | PW | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430FR5724 | Samples |
| MSP430FR5724IPWR | ACTIVE | TSSOP | PW | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430FR5724 | Samples |
| MSP430FR5724IRGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 430FR 5724 | Samples |
| MSP430FR5724IRGET | ACTIVE | VQFN | RGE | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 430FR 5724 | Samples |
| MSP430FR5725IDA | ACTIVE | TSSOP | DA | 38 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430FR5725 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430FR5725IDAR | ACTIVE | TSSOP | DA | 38 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430FR5725 | Samples |
| MSP430FR5725IRHAR | ACTIVE | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430 FR5725 | Samples |
| MSP430FR5725IRHAT | ACTIVE | VQFN | RHA | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430 FR5725 | Samples |
| MSP430FR5726IPW | ACTIVE | TSSOP | PW | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430FR5726 | Samples |
| MSP430FR5726IRGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 430FR 5726 | Samples |
| MSP430FR5727IDAR | ACTIVE | TSSOP | DA | 38 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430FR5727 | Samples |
| MSP430FR5727IRHAT | NRND | VQFN | RHA | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430 FR5727 | |
| MSP430FR5728IPW | ACTIVE | TSSOP | PW | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430FR5728 | Samples |
| MSP430FR5728IPWR | ACTIVE | TSSOP | PW | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430FR5728 | Samples |
| MSP430FR5728IRGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 430FR 5728 | Samples |
| MSP430FR5728IRGET | ACTIVE | VQFN | RGE | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 430FR 5728 | Samples |
| MSP430FR5729IDA | ACTIVE | TSSOP | DA | 38 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430FR5729 | Samples |
| MSP430FR5729IDAR | ACTIVE | TSSOP | DA | 38 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430FR5729 | Samples |
| MSP430FR5729IRHAR | ACTIVE | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430 FR5729 | Samples |
| MSP430FR5729IRHAT | ACTIVE | VQFN | RHA | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430 FR5729 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

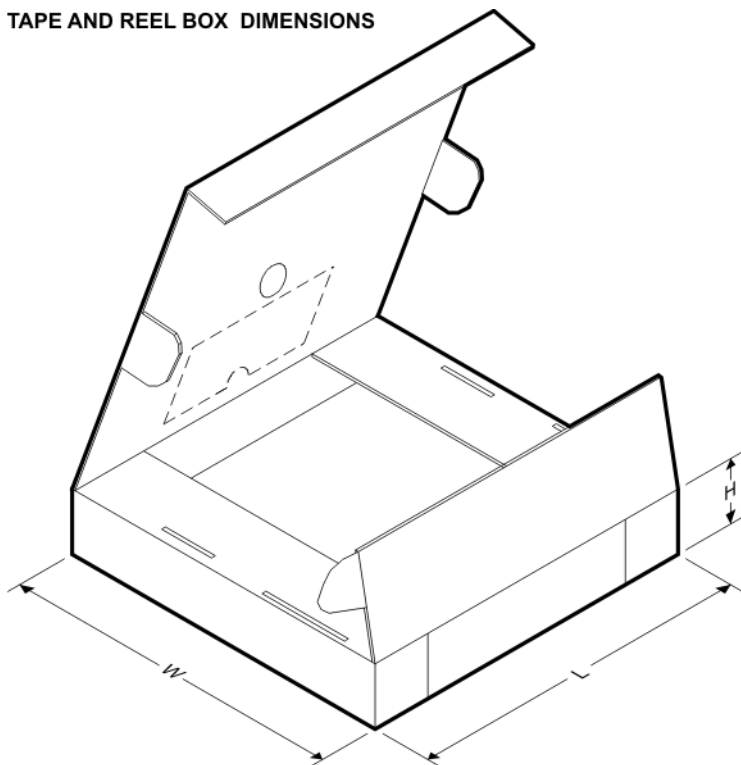
TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430FR5720IPWR | TSSOP | PW | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| MSP430FR5720IRGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430FR5720IRGET | VQFN | RGE | 24 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430FR5721IDAR | TSSOP | DA | 38 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |
| MSP430FR5721IRHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430FR5721IRHAT | VQFN | RHA | 40 | 250 | 180.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430FR5722IRGET | VQFN | RGE | 24 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430FR5723IRHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430FR5723IRHAT | VQFN | RHA | 40 | 250 | 180.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430FR5724IPWR | TSSOP | PW | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| MSP430FR5724IRGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430FR5724IRGET | VQFN | RGE | 24 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430FR5725IDAR | TSSOP | DA | 38 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |
| MSP430FR5725IRHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430FR5725IRHAT | VQFN | RHA | 40 | 250 | 180.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430FR5726IRGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430FR5727IDAR | TSSOP | DA | 38 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |
| MSP430FR5727IRHAT | VQFN | RHA | 40 | 250 | 180.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430FR5728IPWR | TSSOP | PW | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| MSP430FR5728IRGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430FR5728IRGET | VQFN | RGE | 24 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430FR5729IDAR | TSSOP | DA | 38 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |
| MSP430FR5729IRHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430FR5729IRHAT | VQFN | RHA | 40 | 250 | 180.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430FR5720IPWR | TSSOP | PW | 28 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430FR5720IRGER | VQFN | RGE | 24 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430FR5720IRGET | VQFN | RGE | 24 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430FR5721IDAR | TSSOP | DA | 38 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430FR5721IRHAR | VQFN | RHA | 40 | 2500 | 367.0 | 367.0 | 38.0 |
| MSP430FR5721IRHAT | VQFN | RHA | 40 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430FR5722IRGET | VQFN | RGE | 24 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430FR5723IRHAR | VQFN | RHA | 40 | 2500 | 367.0 | 367.0 | 38.0 |
| MSP430FR5723IRHAT | VQFN | RHA | 40 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430FR5724IPWR | TSSOP | PW | 28 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430FR5724IRGER | VQFN | RGE | 24 | 3000 | 367.0 | 367.0 | 35.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430FR5724IRGET | VQFN | RGE | 24 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430FR5725IDAR | TSSOP | DA | 38 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430FR5725IRHAR | VQFN | RHA | 40 | 2500 | 367.0 | 367.0 | 38.0 |
| MSP430FR5725IRHAT | VQFN | RHA | 40 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430FR5726IRGER | VQFN | RGE | 24 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430FR5727IDAR | TSSOP | DA | 38 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430FR5727IRHAT | VQFN | RHA | 40 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430FR5728IPWR | TSSOP | PW | 28 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430FR5728IRGER | VQFN | RGE | 24 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430FR5728IRGET | VQFN | RGE | 24 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430FR5729IDAR | TSSOP | DA | 38 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430FR5729IRHAR | VQFN | RHA | 40 | 2500 | 367.0 | 367.0 | 38.0 |
| MSP430FR5729IRHAT | VQFN | RHA | 40 | 250 | 210.0 | 185.0 | 35.0 |

RGE 24

GENERIC PACKAGE VIEW

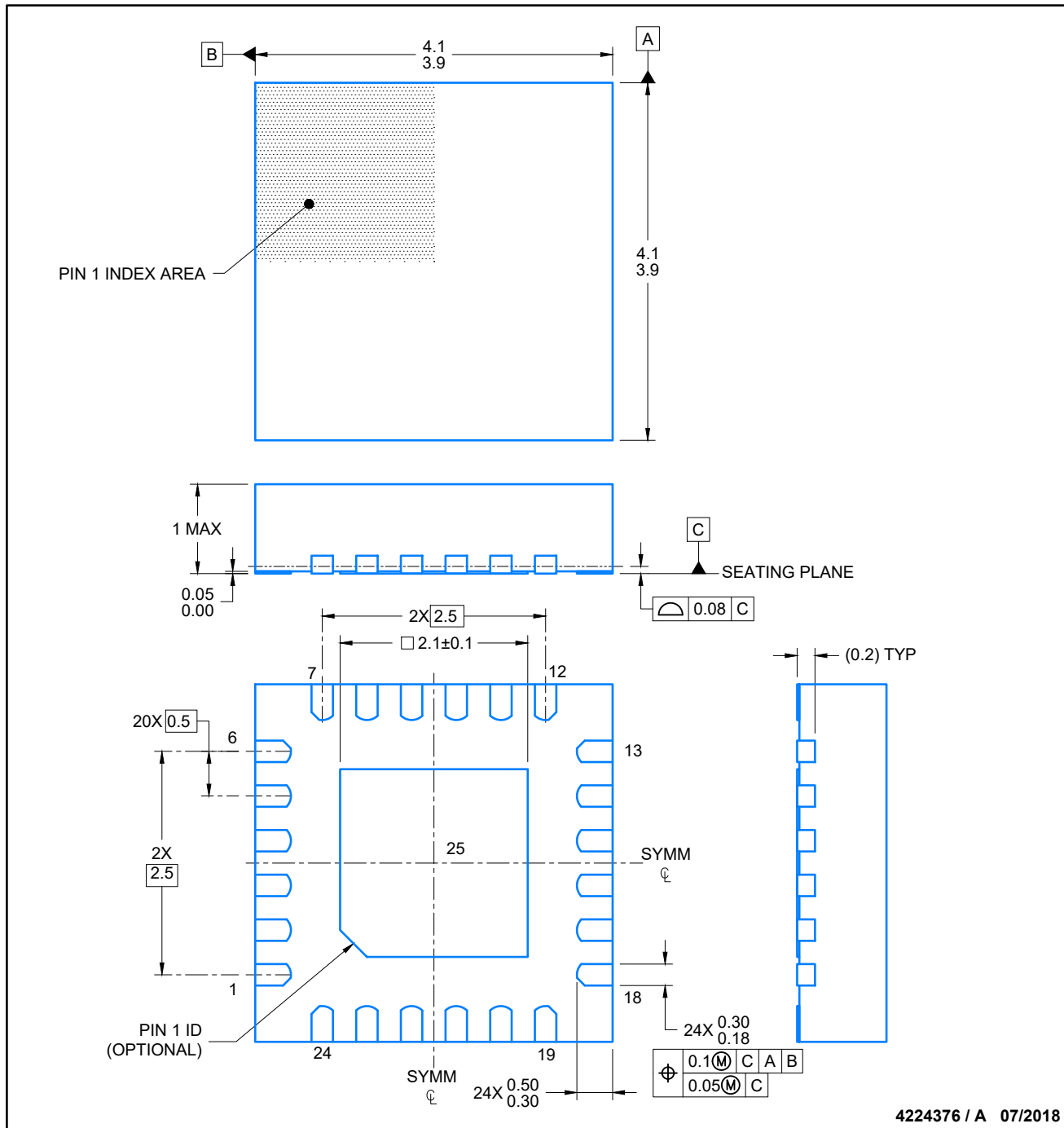
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

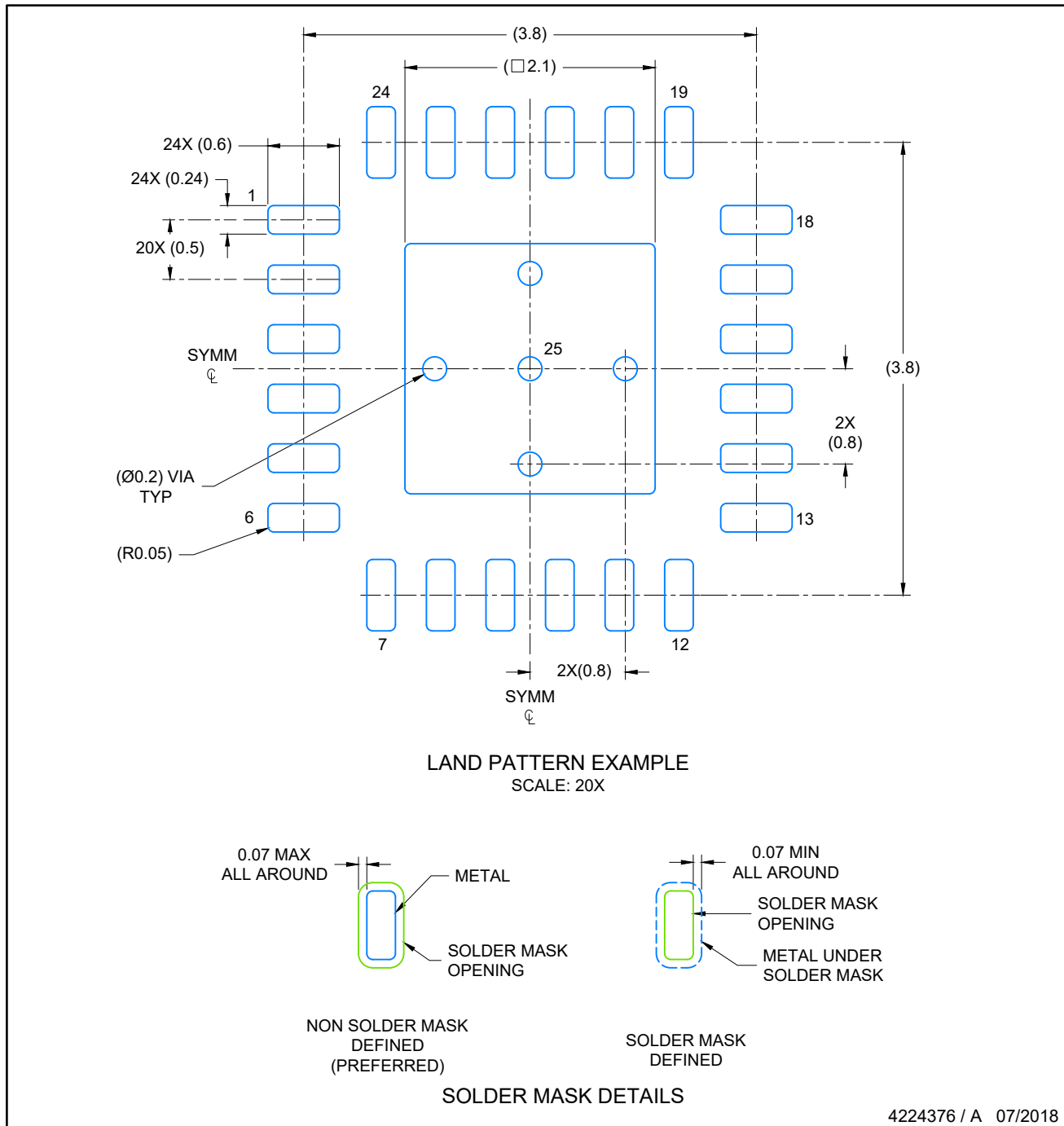
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4224376 / A 07/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



NOTES: (continued)

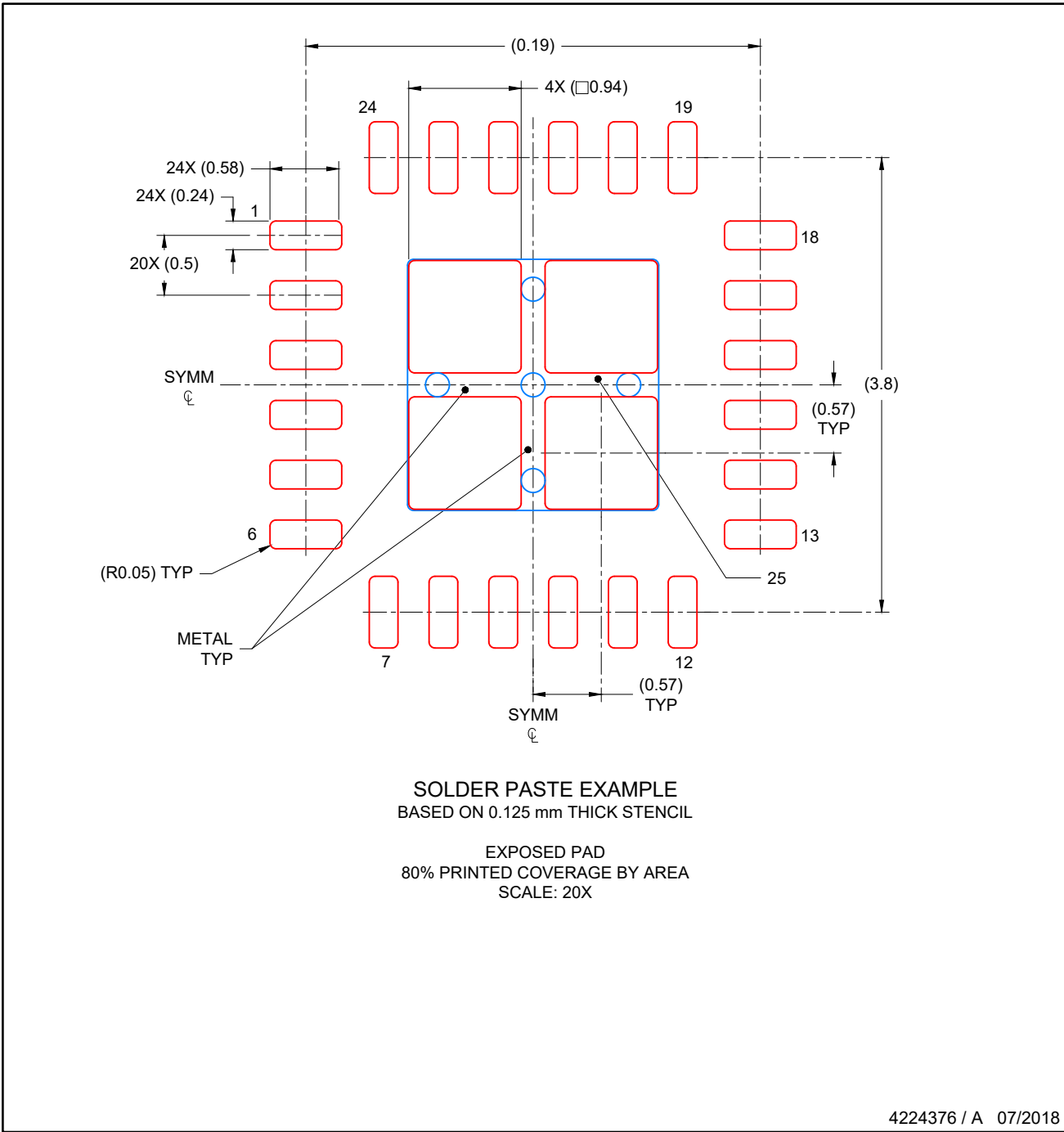
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

VQFN - 1 mm max height

RGE0024C

PLASTIC QUAD FLATPACK- NO LEAD



NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4204276/E 06/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) Package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Package complies to JEDEC MO-220 variation VJJD-2.

THERMAL PAD MECHANICAL DATA

RHA (S-PVQFN-N40)

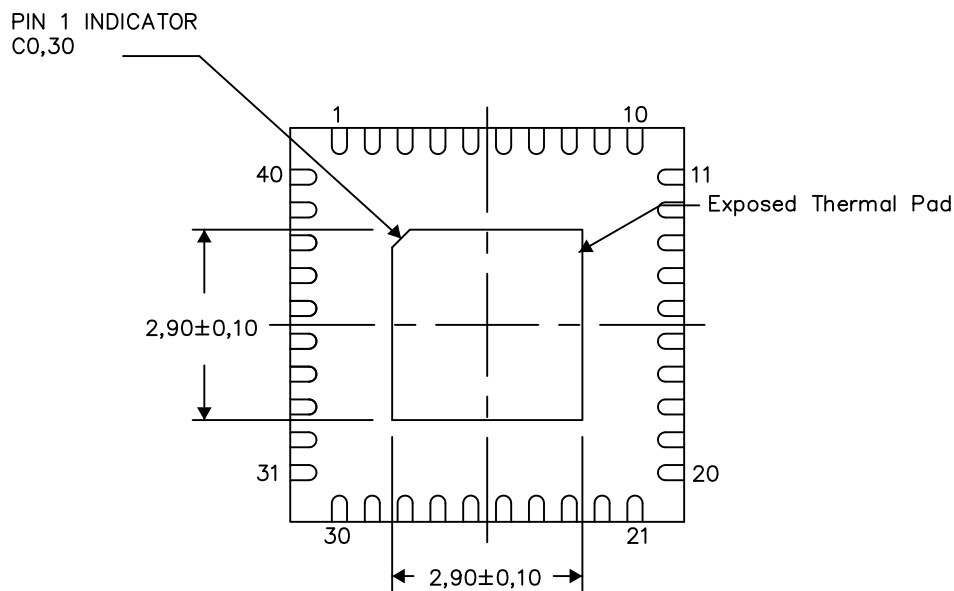
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

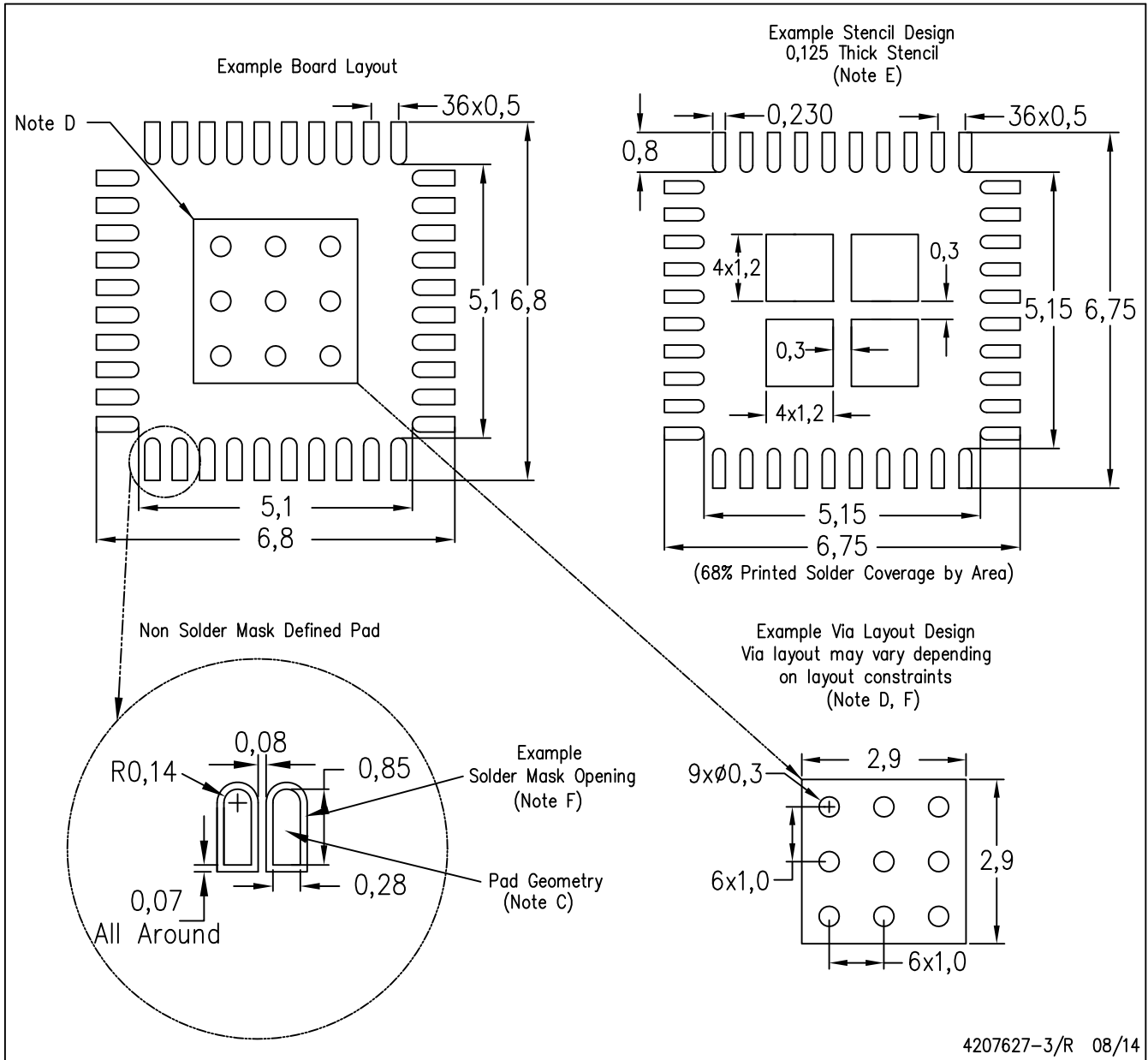
Exposed Thermal Pad Dimensions

4206355-3/X 08/14

NOTES: A. All linear dimensions are in millimeters

RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

DA (R-PDSO-G**)
 38 PIN SHOWN

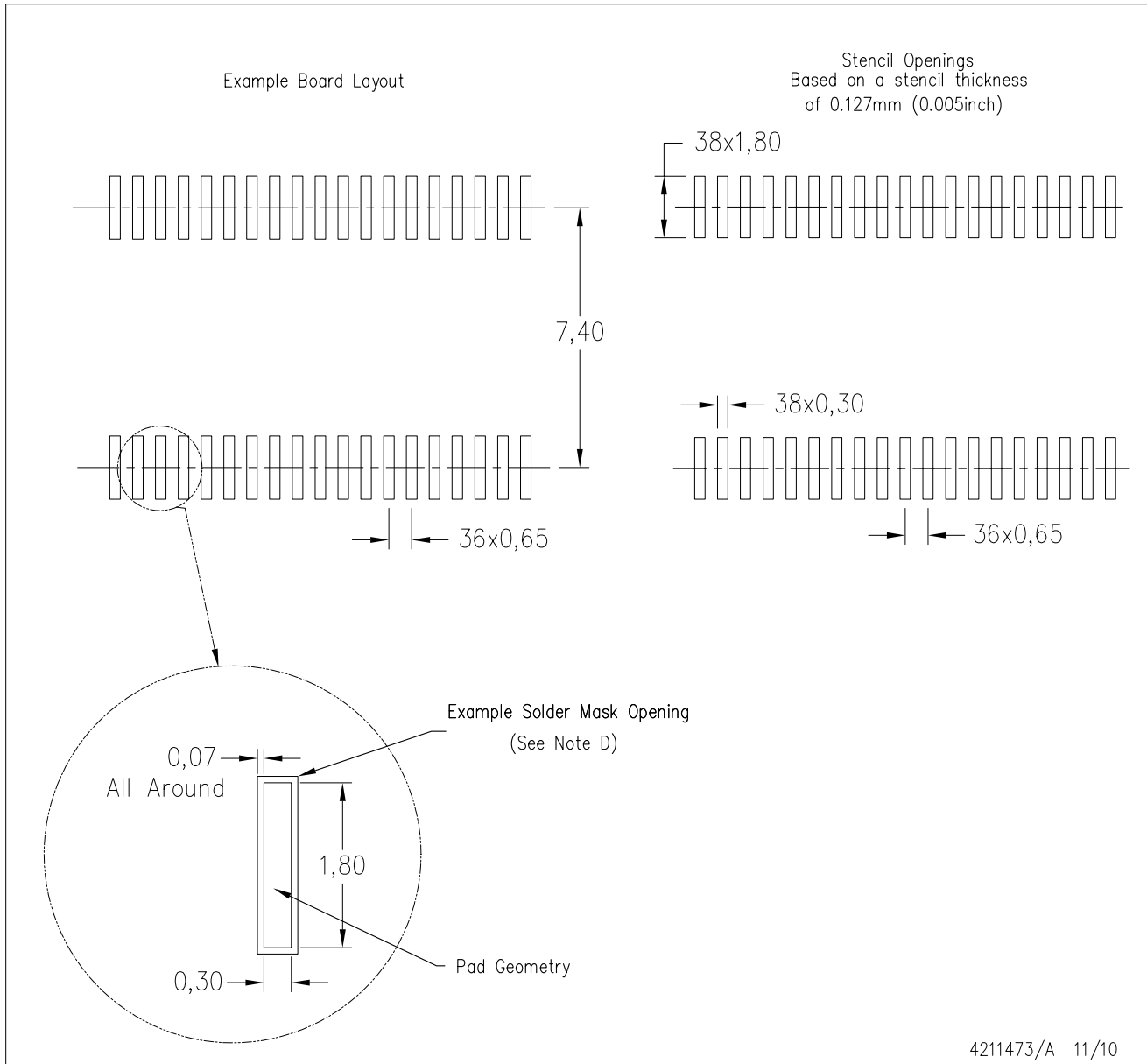
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-153, except 30 pin body length.

DA (R-PDSO-G38)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - D. Contact the board fabrication site for recommended soldermask tolerances.

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



4040064-7/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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