- Fully Programmable With Synchronous Counting and Loading
- SN74ALS867A and 'AS867 Have Asynchronous Clear; SN74ALS869 and 'AS869 Have Synchronous Clear
- Fully Independent Clock Circuit Simplifies Use
- Ripple-Carry Output for n-Bit Cascading
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

description

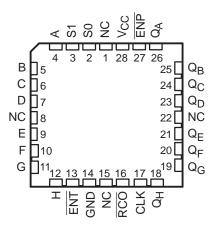
These synchronous, presettable, 8-bit up/down counters feature internal-carry look-ahead circuitry for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the eight flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; they may be preset to any number between 0 and 255. The load-input circuitry allows parallel loading of the cascaded counters. Because loading is synchronous, selecting the load mode disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

SN54AS867, SN54AS869 JT PACKAGE
SN74ALS867A, SN74ALS869, SN74AS867,
SN74AS869 DW OR NT PACKAGE
(TOP VIEW)

			1
S0 [S1 [1	U ₂₄	Vcc
S1 [2	23] ENP
A	3	22] Q _A
в[21] Q _B
С[20] Q _C
D [1	19	
E [7	18] Q _E
F [8	17] Q _F
G [9	16] Q _G
<u> </u>	10	15] Q _H
ENT [11	14	
GND [12	13] RCO

SN54AS867, SN54AS869 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Two count-enable (ENP and ENT) inputs and a ripple-carry (RCO) output are instrumental in accomplishing this function. Both ENP and ENT must be low to count. The direction of the count is determined by the levels of the select (S0, S1) inputs as shown in the function table. ENT is fed forward to enable RCO. RCO thus enabled produces a low-level pulse while the count is zero (all outputs low) counting down or 255 counting up (all outputs high). This low-level overflow-carry pulse can be used to enable successive cascaded stages. Transitions at ENP and ENT are allowed regardless of the level of CLK. All inputs are diode clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. With the exception of the asynchronous clear on the SN74ALS867A and 'AS867, changes at S0 and S1 that modify the operating mode have no effect on the Q outputs until clocking occurs. For the 'AS867 and 'AS869, any time ENP and/or ENT is taken high, RCO either goes or remains high. For the SN74ALS867A and SN74ALS869, any time ENT is taken high, RCO either goes or remains high. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description (continued)

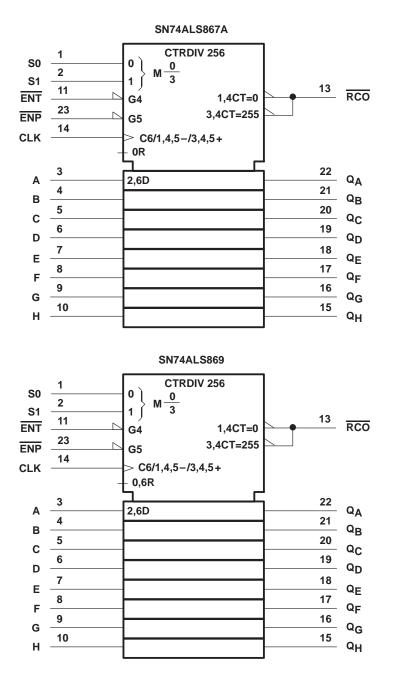
The SN54AS867 and SN54AS869 are characterized for operation over the full military temperature range of -55° C to 125° C. The SN74ALS867A, SN74ALS869, SN74AS867, and SN74AS869 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

S1	S0	FUNCTION
L	L	Clear
L	Н	Count down
н	L	Load
н	Н	Count up



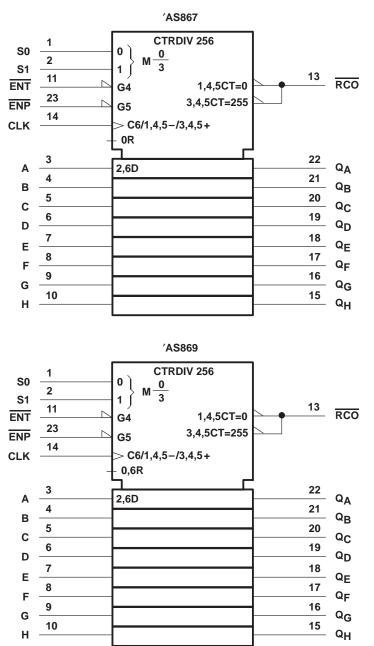
logic symbols[†]



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, JT, and NT packages.



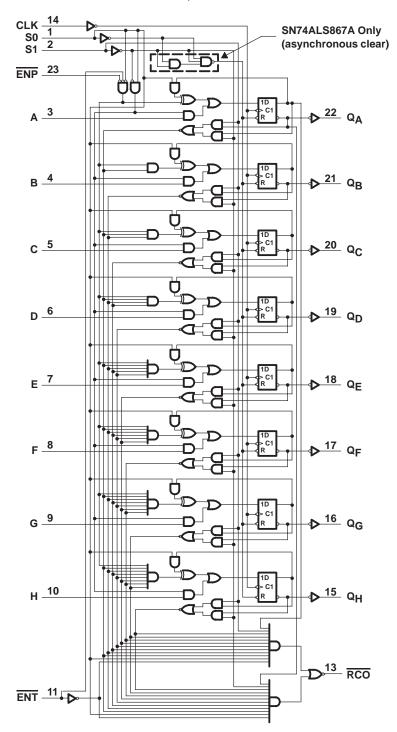
logic symbols (continued)[†]



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, JT, and NT packages.



logic diagram (positive logic)

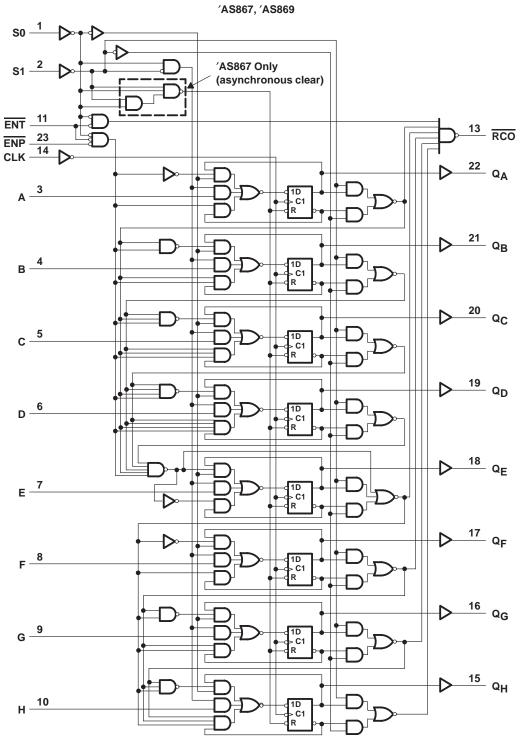


SN74ALS867A, SN74ALS869

Pin numbers shown are for the DW, JT, and NT packages.



logic diagram (positive logic)



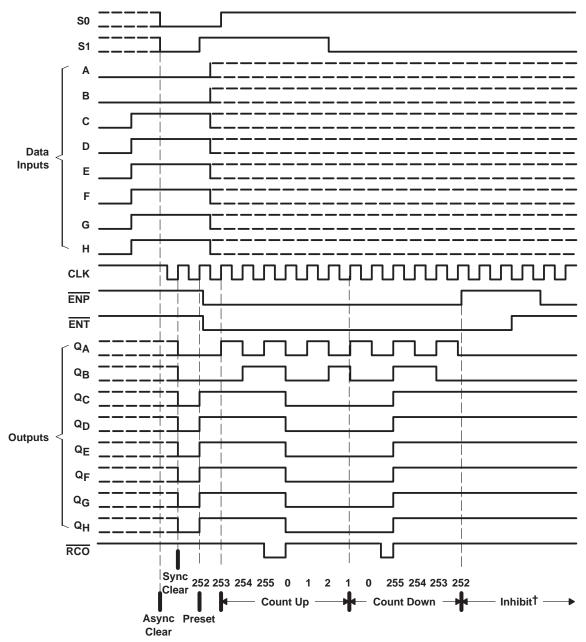
Pin numbers shown are for the DW, JT, and NT packages.



typical clear, preset, count, and inhibit sequences

The following sequence is illustrated below:

- 1. Clear outputs to zero (SN74ALS867A and 'AS867 are asynchronous; SN74ALS869 and 'AS869 are synchronous.)
- 2. Preset to binary 252
- 3. Count up to 253, 254, 255, 0, 1, and 2
- 4. Count down to 1, 0, 255, 254, 253, and 252
- 5. Inhibit



 $+\overline{\text{ENT}}$ and $\overline{\text{ENP}}$ both must be low for counting to occur.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{CC}	7 V
Input voltage, V _I	7V
Operating free-air temperature range, T _A : SN74ALS867A	C to 70°C
Storage temperature range	C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN74ALS867A			
			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.5	5	5.5	V
VIH	High-level input voltage		2			V
VIL	Low-level input voltage				0.8	V
IOH	High-level output current				-0.4	mA
IOL	Low-level output current				8	mA
fclock	Clock frequency		0		35	MHz
^t w(clock)	Pulse duration, CLK high or low		14			ns
^t w(clear)	Pulse duration of clear pulse, S0 and S1 low		10			ns
		Data inputs A-H	10			
		ENP or ENT	15			
t _{su}	Setup time before CLK [↑]	S0 low and S1 high (load)	12			ns
		S0 high and S1 low (count down)	12			
		S0 and S1 high (count up)	12			
t _h Hold time after CLK [↑]		S0 high after S1 \uparrow or S1 high after S0 \uparrow	3			ns
	Hold time after CLK	Data inputs A-H	0			115
TA	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS8	SN74ALS867A		
PARAMETER	TEST CON	IDITIONS	MIN TYP‡	MAX	UNIT	
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA		-1.2	V	
VOH	$V_{CC} = 4.5 V$ to 5.5 V,	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2		V	
Ver		$I_{OL} = 4 \text{ mA}$	0.25	0.4	V	
VOL	$V_{CC} = 4.5 V$	I _{OL} = 8 mA	0.35	0.5	v	
lı	$V_{CC} = 5.5 V,$	VI = 7 V		0.1	mA	
Чн	V _{CC} = 5.5 V,	VI = 2.7 V		20	μA	
Ι _{ΙL}	V _{CC} = 5.5 V,	VI = 0.4 V		-0.2	mA	
۱ ₀ §	V _{CC} = 5.5 V,	V _O = 2.25 V	-30	-112	mA	
ICC	V _{CC} = 5.5 V		28	45	mA	

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L = 50 pF R _L = 500 Ω T _A = MIN t	2,	UNIT
fmax			35		MHz
^t PLH	CLK		4	14	
^t PHL	CEK	RCO	4	14	ns
^t PLH	CLK	Apy 0	3	16	
^t PHL	CEK	Any Q	3	16	ns
^t PLH			3	14	
^t PHL	ENT	RCO	2	9	ns
^t PHL	S0 or S1 (clear mode)	Any Q	8	26	ns
^t PLH	S0 or S1		4	16	
^t PHL	(count up/down)	RCO	4	16	ns
^t PLH	S0 or S1 (clear mode)	RCO	4	16	ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{CC}	V
Input voltage, V ₁	' V
Operating free-air temperature range, T _A : SN74ALS869 0°C to 70°	°C
Storage temperature range	°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN74ALS869		UNIT	
			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
VIL	Low-level input voltage				0.8	V
IOH	High-level output current				-0.4	mA
IOL	Low-level output current				8	mA
fclock	Clock frequency		0		35	MHz
^t w(clock)	Pulse duration, CLK high or low		14			ns
		Data inputs A-H	10			
		ENP or ENT	15			
+	Satur time hafara CLIZ	S0 and S1 low (clear)	13			ns
t _{su}	Setup time before CLK↑	S0 low and S1 high (load)	13			115
		S0 high and S1 low (count down)	13			
		S0 and S1 high (count up)	13			
tu lalatima attar OLKA		S0 high after S1 \uparrow or S1 high after S0 \uparrow	3			ns
th	Hold time after CLK [↑]	Data inputs A-H	0			115
T _A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SI	SN74ALS869		
PARAMETER	TEST CON	IDITIONS	MIN	TYP‡	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	lj = -18 mA			-1.2	V
V _{OH}	$V_{CC} = 4.5 V$ to 5.5 V,	$I_{OH} = -0.4 \text{ mA}$	V _{CC} –	2		V
Ver		$I_{OL} = 4 \text{ mA}$		0.25	0.4	V
VOL	$V_{CC} = 4.5 V$	I _{OL} = 8 mA		0.35	0.5	v
Ι	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1	mA
Ιн	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20	μΑ
١ _{IL}	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.2	mA
١ _O §	V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	mA
ICC	$V_{CC} = 5.5 V$			28	45	mA

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L = 50 p R _L = 500 T _A = MIN	i V to 5.5 V, F, Ω, to MAX [†] ALS869 MAX	UNIT
fmax			35		MHz
^t PLH	CLK		4	14	
^t PHL	CER	RCO	4	14	ns
^t PLH	CLK	Any Q	3	16	ns
^t PHL	CER	Ally Q	3	16	115
^t PLH	ENT	RCO	3	14	ns
^t PHL	ENI	RCO	2	9	115
^t PLH	S1	RCO	4	15	ns
^t PHL	(count up/down)	RCO	4	15	
^t PLH	SO	RCO	4	16	ns
^t PHL	(clear/load)	Red	4	12	115

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{CC}	
Operating free-air temperature range, T _A : SN54AS867	
SN74AS867	0°C to 70°C
Storage temperature range	

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SI	N54AS86	67	SN74AS867		LINUT	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			0.8	V
IOH	High-level output current				-2			-2	mA
IOL	Low-level output current			20			20	mA	
fclock*	Clock frequency	0		40	0		50	MHz	
^t w(clock)*	Pulse duration, CLK high or I	12.5			10			ns	
^t w(clear)*	Pulse duration of clear pulse	12.5			10			ns	
		Data inputs A-H	5			4			
		ENP or ENT	9			8			
. *		S0 low and S1 high (load)	11			10			~~
t _{su} *	Setup time before CLK↑	S0 and S1 low (clear)	11			10			ns
		S0 high and S1 low (count down)	42			40			
		S0 and S1 high (count up)	42			40			
t _h *	Hold time after CLK↑	Data inputs A-H	0			0			ns
^t skew [*]	Skew time between S0 and S1 (maximum to avoid inadvertent clear)				8			7	ns
Тд	Operating free-air temperatur	e	-55		125	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54AS867			SN74AS867			
					TYP†	MAX	MIN	TYP†	MAX	UNIT	
VIK		V _{CC} = 4.5 V,	lj = -18 mA			-1.2			-1.2	V	
VOH		V_{CC} = 4.5 V to 5.5 V,	$I_{OH} = -2 \text{ mA}$	V _{CC} -2	2		V _{CC} -2	2		V	
V _{OL}	RCO	V _{CC} = 4.5 V	I _{OL} = 2 <u>0 m</u> A, V _{IL} on ENT = 0.7 V		0.34	0.5				V	
	Other outputs		I _{OL} = 20 mA					0.34			
Ιį	-	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA	
	ENT		V ₁ = 2.7 V			40			40		
IН	Other inputs	V _{CC} = 5.5 V,	$v_{1} = 2.7 v_{2}$			20			20	μA	
L.	ENT		\/. 0.4.\/			-4			-4	A	
ΊL	Other inputs	V _{CC} = 5.5 V,	$V_{I} = 0.4 V$			-2			-2	mA	
10‡	-	V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	-30		-112	mA	
ICC		V _{CC} = 5.5 V			134	195		134	195	mA	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _C CL RL TA	UNIT			
			SN54A	S867	SN74A	S867	
			MIN	MAX	MIN	MAX	
fmax*			40		50		MHz
^t PLH	CLK	RCO	5	31	5	22	ns
^t PHL	OER	RCU	6	19	6	16	115
tPLH	CLK	Any Q	3	12	3	11	ns
^t PHL	OER		4	16	4	15	115
^t PLH	ENT	RCO	3	19	3	10	ns
^t PHL	ENI	RCU	5	21	5	17	115
^t PLH	ENP	RCO	5	16	5	14	ns
t _{PHL}	ENP	KCU	5	21	5	17	115
tPHL .	Clear (S0 or S1 low)	Any Q	7	23	7	21	ns

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested. § For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{CC}	
Operating free-air temperature range, T _A : SN54AS869	
SN74AS869	0°C to 70°C
Storage temperature range	. −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54AS869			SN74AS869			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V
ЮН	High-level output current				-2			-2	mA
IOL	Low-level output current			20			20	mA	
^f clock [*]	Clock frequency			40			45	MHz	
^t w(clock)*	Pulse duration, CLK high or I	12.5			11			ns	
		Data inputs A-H	6			5			
		ENP or ENT	10			9			
L *		S0 low and S1 high (load)	13			11			
t _{su} *	Setup time before CLK↑	S0 and S1 low (clear)	13			11			ns
		S0 high and S1 low (count down)	52			50			
		S0 and S1 high (count up)	52			50			
t _h *	Hold time after CLK↑	Data inputs A-H	0			0			ns
Т _А	Operating free-air temperatu	re	-55		125	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54AS869			SN74AS869			
					TYP†	MAX	MIN	TYP†	MAX	UNIT	
VIK		V _{CC} = 4.5 V,	lj = -18 mA			-1.2			-1.2	V	
V _{OH}		V_{CC} = 4.5 V to 5.5 V,	$I_{OH} = -2 \text{ mA}$				V _{CC} -2	2		V	
		$V_{CC} = 4.5 \text{ V}, \qquad I_{OH} = -2 \text{ mA}$		V _{CC} -2	<u>2</u> *					v	
V _{OL}	RCO	V _{CC} = 4.5 V	I _{OL} = 2 <u>0 m</u> A, V _{IL} on ENT = 0.7 V		0.34	0.5				V	
	Other outputs	1	I _{OL} = 20 mA					0.34	0.5		
Ιį	-	V _{CC} = 5.5 V,	V ₁ = 7 V			0.1			0.1	mA	
	ENT		VI = 2.7 V			40			40	۵	
ЧΗ	Other inputs	V _{CC} = 5.5 V,	$v_{1} = 2.7 v_{1}$			20			20	μA	
1	ENT					-4			-4	mA	
ΊL	Other inputs	V _{CC} = 5.5 V,	V _I = 0.4 V	-2		-2			-2	2	
10‡		V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	-30		-112	mA	
ICC		V _{CC} = 5.5 V			134	195		134	195	mA	

[†] All typical values are at V_{CC} = 5 V, $T_A = 25^{\circ}$ C.

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

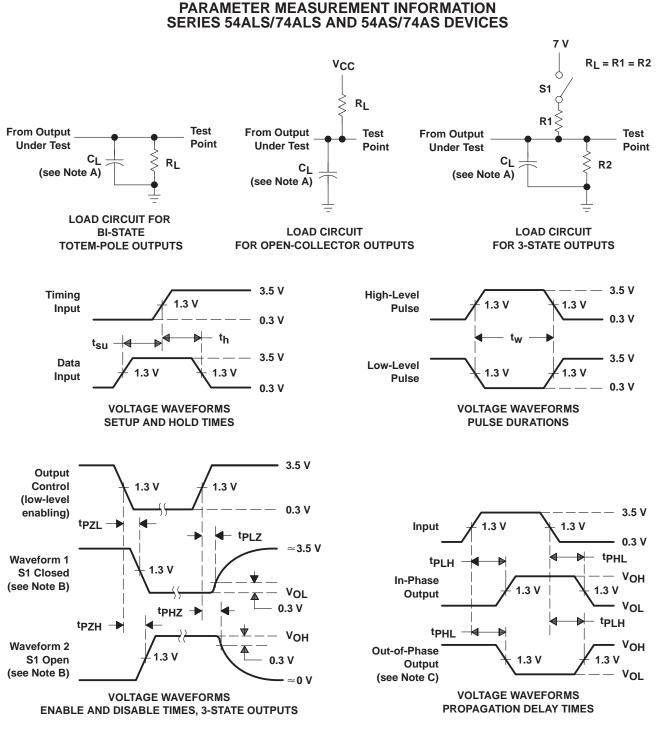
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _C C _L R _L T _A	UNIT			
			SN54A	S869	SN74AS869		
			MIN	MAX	MIN	MAX	
fmax*			40		45		MHz
^t PLH	CLK	RCO	6	35	6	35	ns
^t PHL	OLK	RCU	6	20	6	18	115
^t PLH	CLK	Any Q	3	12	3	11	
^t PHL	ULK	Ally Q	4	16	4	15	ns
^t PLH			3	25	3	15	20
^t PHL	ENT	RCO	6	21	6	17	ns
^t PLH	ENP	RCO	5	27	5	19	200
^t PHL	EINP	RCU	6	21	6	18	ns

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested. § For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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NOTES: A. CL includes probe and jig capacitance.

- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Β. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: $PRR \le 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms





28-Jul-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8952601LA	ACTIVE	CDIP	JT	24	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	5962-8952601LA SNJ54AS869JT	Samples
5962-8966801LA	ACTIVE	CDIP	JT	24	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	5962-8966801LA SNJ54AS867JT	Samples
SN54AS867JT	ACTIVE	CDIP	JT	24	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	SN54AS867JT	Samples
SN54AS869JT	ACTIVE	CDIP	JT	24	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	SN54AS869JT	Samples
SN74ALS867ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS867A	Samples
SN74ALS869DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS869	Samples
SN74ALS869DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS869	Samples
SN74AS867DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS867	Samples
SN74AS869DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS869	Samples
SNJ54AS867JT	ACTIVE	CDIP	JT	24	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	5962-8966801LA SNJ54AS867JT	Samples
SNJ54AS869JT	ACTIVE	CDIP	JT	24	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	5962-8952601LA SNJ54AS869JT	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.



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⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54AS867, SN54AS869, SN74AS867, SN74AS869 :

• Catalog: SN74AS867, SN74AS869

• Military: SN54AS867, SN54AS869

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

MECHANICAL DATA

MCER004A - JANUARY 1995 - REVISED JANUARY 1997

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AD.



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