## Features

- **32-kHz Crystal Oscillator**
- **1.1 V to 2.2 V Operating-voltage Range**
- **Integrated Capacitors for Digital Trimming**
- **Suitable for up to 12.5 pF Quartz**
- **Output Pulse Formers**
- **Mask Options for Motor Period and Pulse Width**
- **Low Resistance Output for Bipolar Stepping Motor**
- **Motor Fast-test Function**

## Description

The e1466D is an integrated circuit in CMOS Silicon Gate Technology for analog clocks. It consists of a 32-kHz oscillator, frequency divider, output pulse formers and push-pull motor drivers. Integrated capacitors are mask-selectable to accomodate the external quartz crystal. Additional capacitance can be selected through pad bonding for trimming the oscillator frequency.

**32-kHz Clock CMOS IC with Digital Trimming**

**e1466D**

## Pad Configuration

**Figure 1.** Pinning



$^{(1)}$ The pads VDD and OSCOUT are interchangeable per mask option

$^{(2)}$ The pads TEST and MOT1 are interchangeable per mask option

## Pin Description

| Name | Description |
|---|---|
| VDD | Positive supply voltage |
| VSS | Negative supply voltage |
| OSCIN | Oscillator input |
| OSCOUT | Oscillator output |
| MOT1/2 | Motor drive outputs |
| C1, C2, C3, C4 | Oscillator trimming inputs |
| TEST | TEST input/output |

# Functional Descripion

**Oscillator**

An oscillator inverter with feedback resistor is provided to generate the 32768 Hz clock frequency. Values for the fixed capacitors at OSCIN and OSCOUT are mask-selectable (see note 3 of "Operating Characteristics"). Four capacitor pads, C1 to C4, enable the users to add integrated trimming capacitors to OSCIN, providing 15 tuning steps.

**Trimming Capacitors**

A frequency variation of typically 4 ppm for each tuning step is obtained by bonding the capacitor pads to OSCIN. As none of these pads are bonded, the IC is in an untrimmed state. Figure 3 shows the trimming curve characteristic.

Note: For applications which utilize this integrated trimming feature, Atmel will determine optimum values for the integrated capacitors COSCIN and COSCOUT.

Capacitor pads C1 to C4: 0 = open, 1 = connected to OSCIN

Combination C1 + C4 is redundant and therefore eliminated from the list

**Table 1.** Frequency Trimming Table

| Capacitor Pads | | | | |
|---|---|---|---|---|
| **C4** | **C3** | **C2** | **C1** | **Trimming Step** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 1 | 0 | 0 | 3 |
| 1 | 0 | 0 | 0 | 4 |
| 0 | 0 | 1 | 1 | 5 |
| 0 | 1 | 0 | 1 | 6 |
| 0 | 1 | 1 | 0 | 7 |
| 1 | 0 | 1 | 0 | 8 |
| 1 | 1 | 0 | 0 | 9 |
| 0 | 1 | 1 | 1 | 10 |
| 1 | 0 | 1 | 1 | 11 |
| 1 | 1 | 0 | 1 | 12 |
| 1 | 1 | 1 | 0 | 13 |
| 1 | 1 | 1 | 1 | 14 |

**Motor Drive Output**

The e1466D contains two push-pull output buffers for driving bipolar stepping motors. During a motor pulse, the N-channel device of one buffer and the P-channel device of the other buffer will be activated. Both N-channel transistors are on and conducting between output pulses. The outputs are protected against inductive voltage spikes with diodes to both supply pins. The motor output period and pulse width are mask-programmable, as listed below:

Available motor periods ($T_M$): 125, 250, 500 ms and 2, 16 s

Available max. pulse widths ($t_M$): 15, 6, 23.4, 31.25, 46.9 ms and 1 s

Available motor periods for motor test ($T_{MT}$): 250, 500 ms and 1 s

Note: The following constraints for combination of motor period and pulse widths have to be considered: $T_M > 4 \times t_M$, $T_{MT} > 4 \times t_M$ or alternatively $T_M = 2 \times t_M$, $T_{MT} = 2 \times t_M$

**Test Functions**    For test purposes, the TEST pad is open. With a high resistance probe ($R \geq 10$ M$\Omega$, $C \geq 20$ pF), a test frequency $f_{TEST}$ of 128 Hz can be measured at the TEST pad. Connecting TEST (for at least 32 ms) to $V_{DD}$ changes the motor period from the selected value to $T_{MT}$ (mask-selectable) while the pulse width remains unaffected. This feature can be used for testing the mechanical parts of the clock.

## Absolute Maximum Ratings

Absolute maximum ratings define parameter limits which, if exceeded, may permanently change or damage the device.
All inputs and outputs on Atmel's circuits are protected against electrostatic discharges. However, precautions to minimize the build-up of electrostatic charges during handling are recommended.
The circuit is protected against supply voltage reversal for typically 5 minutes.

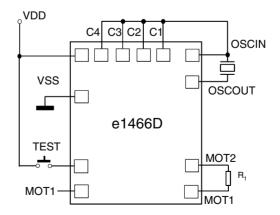| Parameters | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage | $V_{SS}$ | -0.3 to 5 V | V |
| Input voltage range, all inputs | $V_{IN}$ | $(V_{SS} - 0.3\ V) \leq V_{IN} \leq (V_{DD} + 0.3\ V)$ | V |
| Output short-circuit duration | | indefinite | |
| Power dissipation (DIL package) | $P_{tot}$ | 125 | mW |
| Operating ambient temperature range | $T_{amb}$ | -20 to +70 | °C |
| Storage temperature range | $T_{stg}$ | -40 to +125 | °C |
| Lead temperature during soldering at 2 mm distance, 10 s | $T_{sld}$ | 260 | °C |

# Operating Characteristics

$V_{SS} = 0$ V, $V_{DD} = 1.5$ V, $T_{amb} = +25°C$, unless otherwise specified.
All voltage levels are measured with reference to $V_{SS}$. Test crystal as specified below.

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operating voltage | | $V_{DD}$ | 1.1 | 1.5 | 2.2 | V |
| Operating temperature | | $T_{amb}$ | -20 | | +70 | °C |
| Operating current | $R_1 = \infty$ [2] | $I_{DD}$ | | 2 | 5 | mA |
| **Motor Drive Output** | | | | | | |
| Motor output current | $V_{DD} = 1.2$ V, $R_1 = 200$ Ω | $I_M$ | ±4.3 | | | mA |
| Motor period | | $T_M$ | See option list | | | |
| Motor period during motor test | | $T_{MT}$ | See option list | | | |
| Motor pulse width | | $t_M$ | See option list | | | |
| **Oscillator** | | | | | | |
| Startup voltage | Within 2 s | $V_{START}$ | 1.2 | | 2.2 | V |
| Frequency stability | $\Delta V_{DD} = 100$ mV, $V_{DD} = 1.1$ to 2.2 V | $\Delta f/f$ | | 1 | | ppm |
| Integrated input capacitance | [3] | $C_{OSCIN}$ | See option list | | | |
| Integrated output capacitance | | $C_{OSCOUT}$ | See option list | | | |
| Integrated capacitance for bond option [4] | | C1<br>C2<br>C3<br>C4 | | 3<br>4<br>5<br>6 | | pF<br>pF<br>pF<br>pF |
| **TEST Input** | | | | | | |
| Input current | TEST = $V_{DD}$ peak current | $I_{TINH}$ | 0.6 | 3 | 10 | µA |
| Input current | TEST = $V_{SS}$ peak current | $I_{TINL}$ | -0.6 | -3 | -10 | µA |
| Input debounce delay | | $t_{TIN}$ | 23.4 | | 31.2 | ms |

Notes:  1. Typical parameters represent the statistical mean values
2. See test circuit
3. Values can be selected in 1 pF steps. A total capacitance ($C_{OSCIN}$ + $C_{OSCOUT}$) of 38 pF is available
4. These values are valid for 10 pF quartz applications. For $C_L = 12.5$ pF these values change to 4.5, 6, 7.5, 9 pF

**Figure 2.**  Functional Test

## Test Crystal Specification

| | |
|---|---|
| Oscillation frequency | $f_{OSC}$ = 32768 Hz |
| Series resistance | $R_S$ = 30 kΩ |
| Static capacitance | $C_0$ = 1.5 pF |
| Dynamic capacitance | $C_1$ = 3.0 fF |
| Load capacitance | $C_L$ optionally 10 or 12.5 pF |

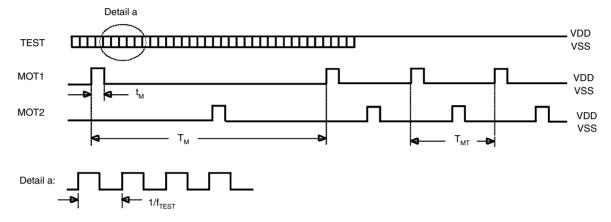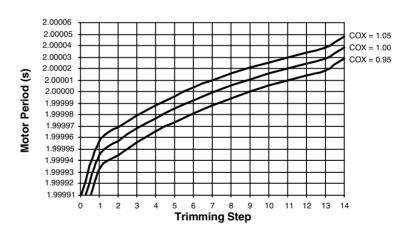**Figure 3.** Motor Output Signal During Normal Operation and During Motor Test



**Figure 4.** Typical Trimming Curve Characteristic for $T_M$ of 2 s



COX means frequency deviation due to production process variations.

Trimming inputs C1 ... C4 are binary weighted, i.e.,
C1 ... C4 = 0 corresponds to trimming step 0
C1 ... C4 = 1 corresponds to trimming step 15

LSB = C1

## Ordering Information

**Table 2.** Option List e1466Dx

| Option | Motor | | | Integrated Capacitance | | | | | | Load Capacitance |
|---|---|---|---|---|---|---|---|---|---|---|
| | Cycle (T_M) | Pulse (t_M) | Test (T_MT) | $C_{OSCIN}$[1] | $C_{OSCOUT}$[1] | C1 | C2 | C3 | C4 | |
| x | s | ms | ms | pF | pF | pF | pF | pF | pF | pF |
| A | 2 | 46.9 | 250 | 9 | 20 | 3 | 4 | 5 | 6 | 10 |
| AO | 2 | 46.9 | 250 | 9 | 20 | 3 | 4 | 5 | 6 | 10 |
| FO | 0.25 | 62.5 | 2000 | 9 | 20 | 3 | 4 | 5 | 6 | 10 |
| HO | 2 | 1000 | 500/250 | 9 | 20 | 3 | 4 | 5 | 6 | 10 |

Note:    1.  On-chip stray capacitance included

| Option | Pad Designation | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| x | Pad 1 | Pad 2 | Pad 3 | Pad 4 | Pad 5 | Pad 6 | Pad 7 | Pad 8 | Pad 8 | Pad 10 | Pad 11 | Pad 12 |
| A | OSCIN | OSCOUT | MOT2 | MOT1 | MOT1 | TEST | $V_{SS}$ | $V_{DD}$ | C4 | C3 | C2 | C1 |
| AO | OSCIN | OSCOUT | MOT2 | MOT1 | MOT1 | TEST | $V_{SS}$ | $V_{DD}$ | C4 | C3 | C2 | C1 |
| FO | OSCIN | OSCOUT | MOT2 | MOT1 | MOT1 | TEST | $V_{SS}$ | $V_{DD}$ | C4 | C3 | C2 | C1 |
| HO | OSCIN | OSCOUT | MOT2 | MOT1 | MOT1 | TEST | $V_{SS}$ | $V_{DD}$ | C4 | C3 | C2 | C1 |

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