THIS SPEC IS OBSOLETE

Spec No: 001-67737

Spec Title: CY7C199CN AUTOMOTIVE, 256-KBIT (32K X 8) STATIC RAM

Replaced by: None

CY7C199CN Automotive

256-Kbit (32K × 8) Static RAM

Features

- Fast access time: 12 ns
- Wide voltage range: 5.0 V ± 10% (4.5 V to 5.5 V)
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Low CMOS standby power
- Automated power down when deselected
- Available in 28-pin SOJ package

Functional Description

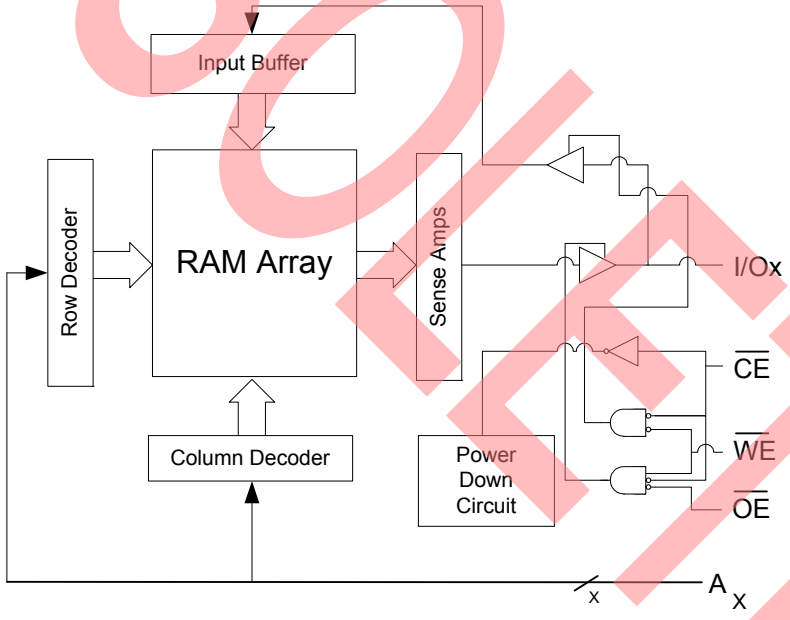
The CY7C199CN Automotive [1] is a high performance CMOS Asynchronous SRAM organized as 32K by 8 bits that supports an asynchronous memory interface. The device features an automatic power down feature that reduces power consumption when deselected.

See the Truth Table on page 4 in this data sheet for a complete description of read and write modes.

The CY7C199CN Automotive is available in 28-pin Molded SOJ package.

For a complete list of related resources, click here.

Logic Block Diagram



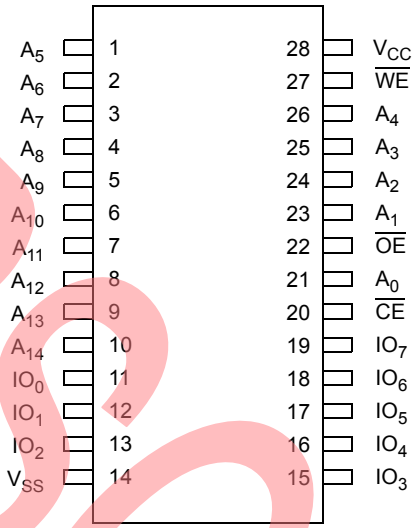
Product Portfolio

Description	-12	Unit
Maximum access time	12	ns
Maximum operating current	85	mA
Maximum CMOS standby current	10	mA

Contents

Pin Layout and Specifications

Figure 1. 28-pin SOJ pinout



Note
1. For best practices recommendations, refer to the Cypress application note *System Design Guidelines* on www.cypress.com.

Pin Description

Pin	Type	Description	SOJ
A_X	Input	Address inputs	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 21, 23, 24, 25, 26
$\overline{CE}$	Control	Chip enable	20
IO_X	Input or output	Data input outputs	11, 12, 13, 15, 16, 17, 18, 19
$\overline{OE}$	Control	Output enable	22
V_{CC}	Supply	Power (5.0V)	28
V_{SS}	Supply	Ground	14
$\overline{WE}$	Control	Write enable	27

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	IOx	Mode	Power
H	X	X	High-Z	Deselect/power-down	Stand by (I_{SB})
L	L	H	Data-out	Read	Active (I_{CC})
L	X	L	Data-in	Write	Active (I_{CC})
L	H	H	High-Z	Selected, outputs disabled	Active (I_{CC})

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Parameter [2]	Description	Value	Unit
T_{STG}	Storage temperature	–65 to +150	°C
T_{AMB}	Ambient temperature with power applied (that is, case temperature)	–55 to +125	°C
V_{CC}	Core supply voltage relative to V_{SS}	–0.5 to +7.0	V
V_{IN}, V_{OUT}	DC voltage applied to any pin relative to V_{SS}	–0.5 to V_{CC} + 0.5	V
I_{OUT}	Output short-circuit current	20	mA
V_{ESD}	Static discharge voltage (in accordance with MIL-STD-883, Method 3015)	> 2001	V
I_{LU}	Latch-up current	> 200	mA

Operating Range

Range	Ambient Temperature (T_A)	Voltage Range (V_{CC})
Automotive-A	–40 °C to 85 °C	5.0 V ± 10%

DC Electrical Characteristics

Over the Operating Range

Parameter [2]	Description	Condition	-12		Unit
			Min	Max	
V_{IH}	Input HIGH voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage		–0.5	0.8	V
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –4.0 mA	2.4	–	V
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 8.0 mA	–	0.4	V
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, I_{OUT} = 0 mA, f = F_{max} = $1/t_{RC}$	–	85	mA
I_{SB1}	Automatic $\overline{CE}$ power- down current – TTL Inputs	Max V_{CC}, $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = F_{max}	–	30	mA
I_{SB2}	Automatic $\overline{CE}$ power- down current – CMOS Inputs	Max V_{CC}, $\overline{CE} \geq V_{CC}$ – 0.3 V, $V_{IN} \geq V_{CC}$ – 0.3 V, or $V_{IN} \leq$ 0.3 V, f = 0	–	10	mA
I_{OZ}	Output leakage current	GND ≤ $V_I \leq V_{CC}$, Output disabled	–5	+5	µA
I_{IX}	Input leakage current	GND ≤ $V_I \leq V_{CC}$	–5	+5	µA

Note
2. $V_{IL(min)}$ = –2.0 V for pulse durations of less than 20 ns.

Capacitance

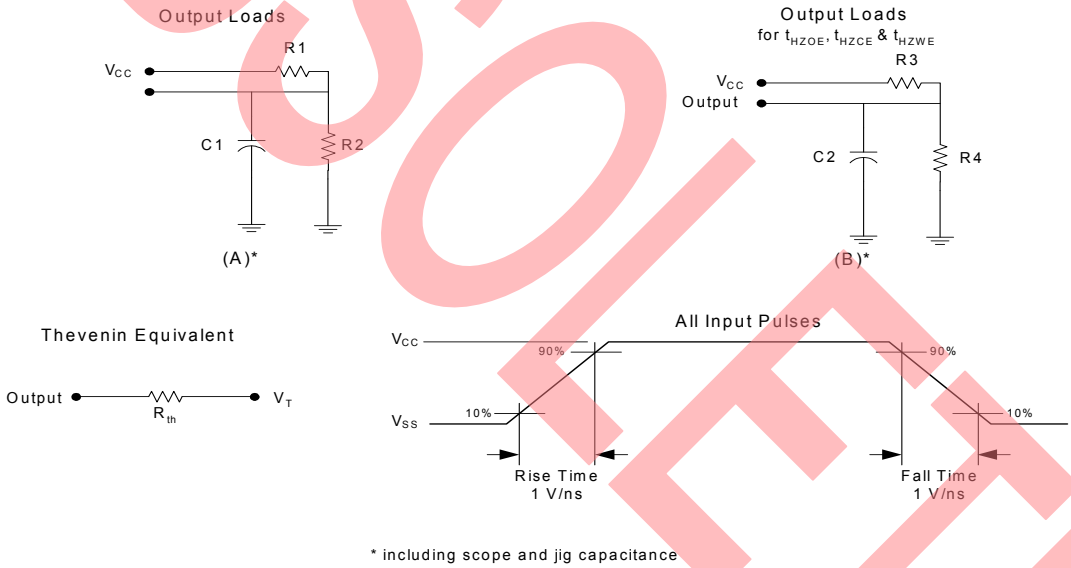
Parameter [3]	Description	Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	8	pF
C_{OUT}	Output capacitance		8	

Thermal Resistance

Parameter [3]	Description	Conditions	SOJ	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 square inch, two-layer printed circuit board	79	°C/W
Θ_{JC}	Thermal resistance (junction to case)		41.42	

AC Test Loads

Figure 2. AC Test Loads



* including scope and jig capacitance

AC Test Conditions

Parameter	Description	Nom	Unit
C1	Capacitor 1	30	pF
C2	Capacitor 2	5	
R1	Resistor 1	480	Ω
R2	Resistor 2	255	
R3	Resistor 3	480	
R4	Resistor 4	255	
R_{TH}	Resistor Thevenin	167	
V_{TH}	Voltage Thevenin	1.73	V

Note
3. Tested initially and after any design or process change that may affect these parameters.

AC Electrical Characteristics

Parameter [4, 5]	Description	-12		Unit
		Min	Max	
t_{RC}	Read cycle time	12	–	ns
t_{AA}	Address to data valid	–	12	ns
t_{OHA}	Data hold from address change	3	–	ns
t_{ACE}	$\overline{CE}$ to data valid	–	12	ns
t_{DOE}	$\overline{OE}$ to data valid	–	6	ns
t_{LZOE}	$\overline{OE}$ to low-Z [6]	0	–	ns
t_{HZOE}	$\overline{OE}$ to high-Z [6, 7]	–	5	ns
t_{LZCE}	$\overline{CE}$ to low-Z [6]	3	–	ns
t_{HZCE}	$\overline{CE}$ to high-Z [6, 7]	–	5	ns
t_{PU}	$\overline{CE}$ to power-up	0	–	ns
t_{PD}	$\overline{CE}$ to power-down	–	12	ns
t_{WC}	Write cycle time [8]	12	–	ns
t_{SCE}	$\overline{CE}$ to write end	9	–	ns
t_{AW}	Address setup to write end	9	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	8	–	ns
t_{SD}	Data setup to write end	8	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high-Z [6, 7]	–	7	ns
t_{LZWE}	$\overline{WE}$ HIGH to low-Z [6]	3	–	ns

Notes

4. Test Conditions are based on a transition time of 3 ns or less and timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.
5. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to sum of t_{SD} and t_{HZWE}.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE}, t_{HZCE}, t_{HZWE} are specified as in part (b) of Figure 2 on page 6. Transitions are measured ± 200 mV from steady state voltage.
8. The internal memory write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data setup and hold timing must be referenced to the leading edge of the signal that terminates the write.

Timing Waveforms

Figure 3. Read Cycle No. 1 [9, 10]

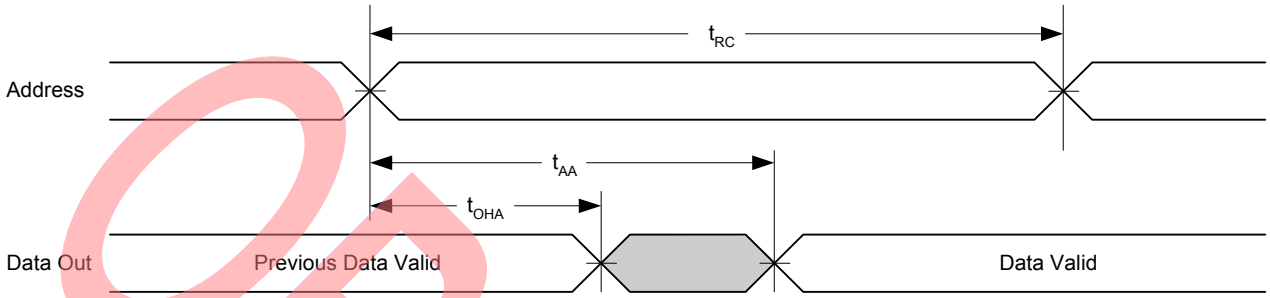
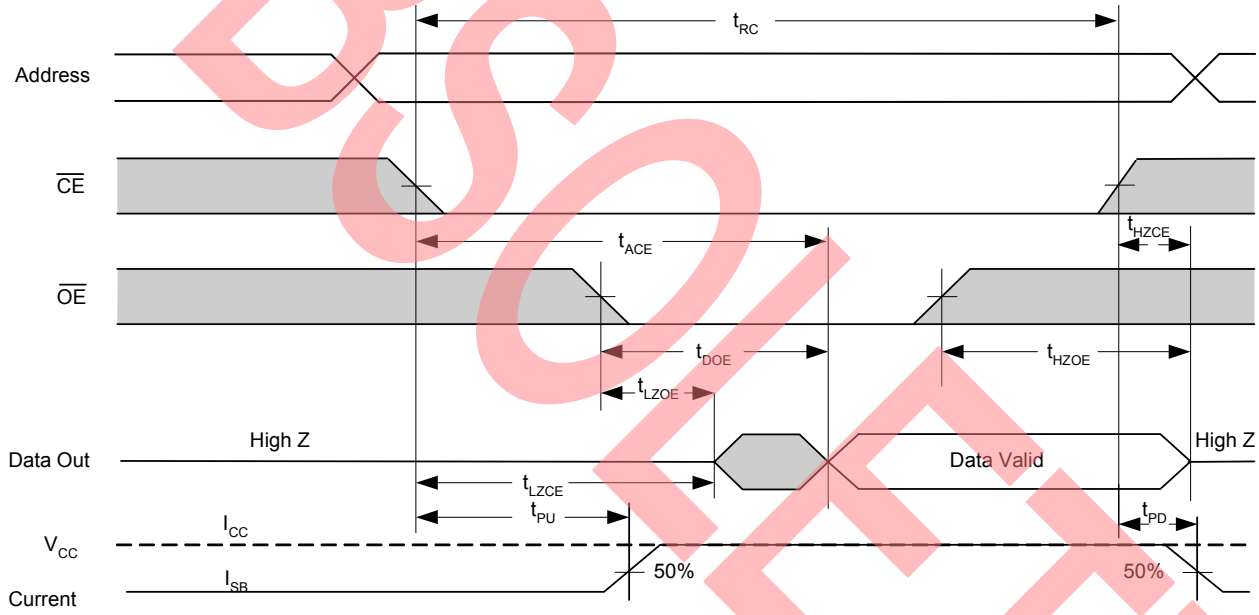


Figure 4. Read Cycle No. 2 [11, 12]



Notes
9. Device is continuously selected. $\overline{OE}$ = V_{IL} = $\overline{CE}$.
10. $\overline{WE}$ is HIGH for read cycle.
11. This cycle is $\overline{OE}$ controlled and $\overline{WE}$ is HIGH read cycle.
12. Address valid before or similar with $\overline{CE}$ transition LOW.

Timing Waveforms *(continued)*

Figure 5. Write Cycle No. 1 ($\overline{WE}$ Controlled) [13, 14, 15]

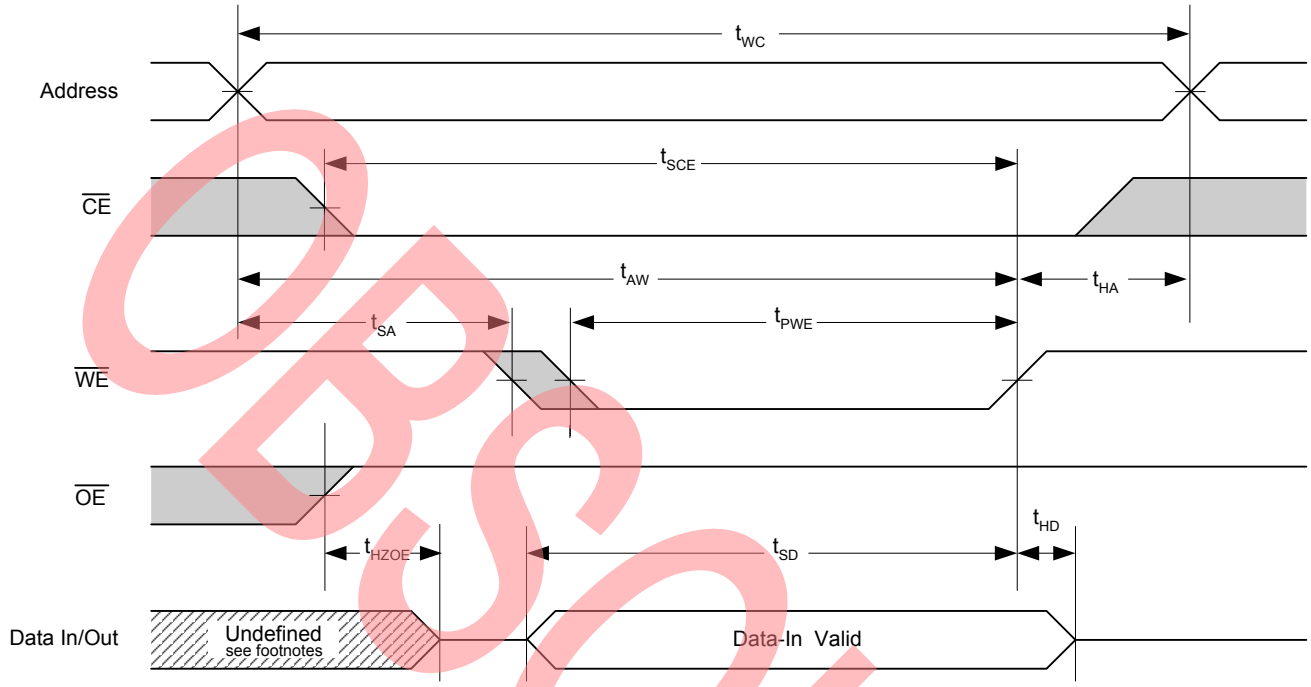
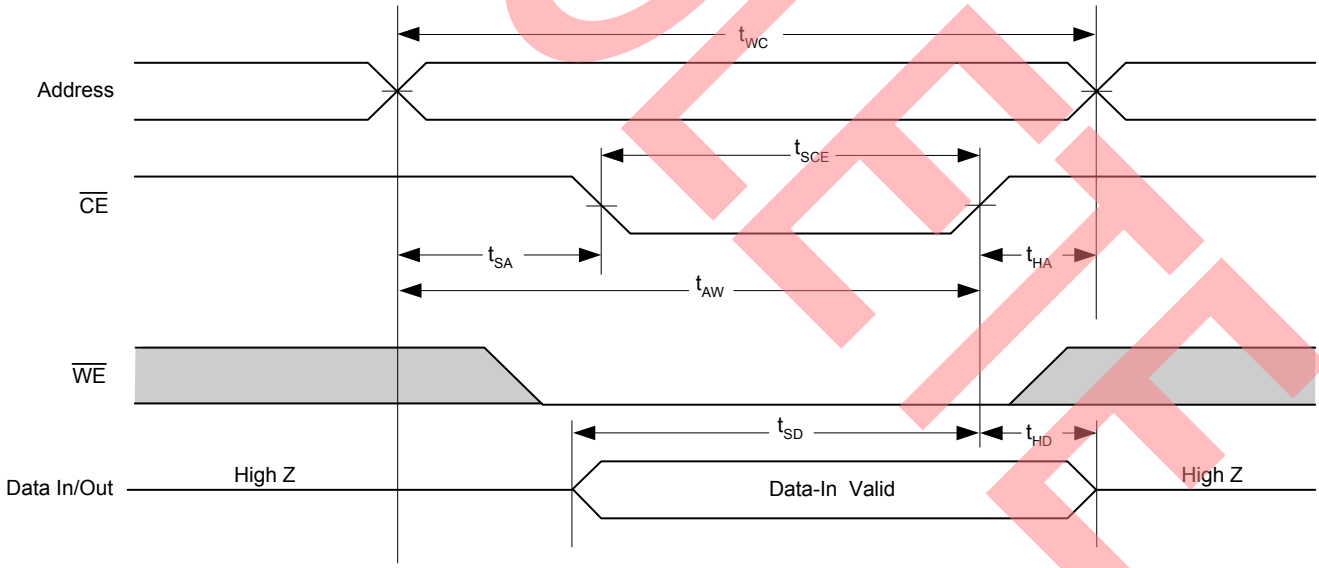


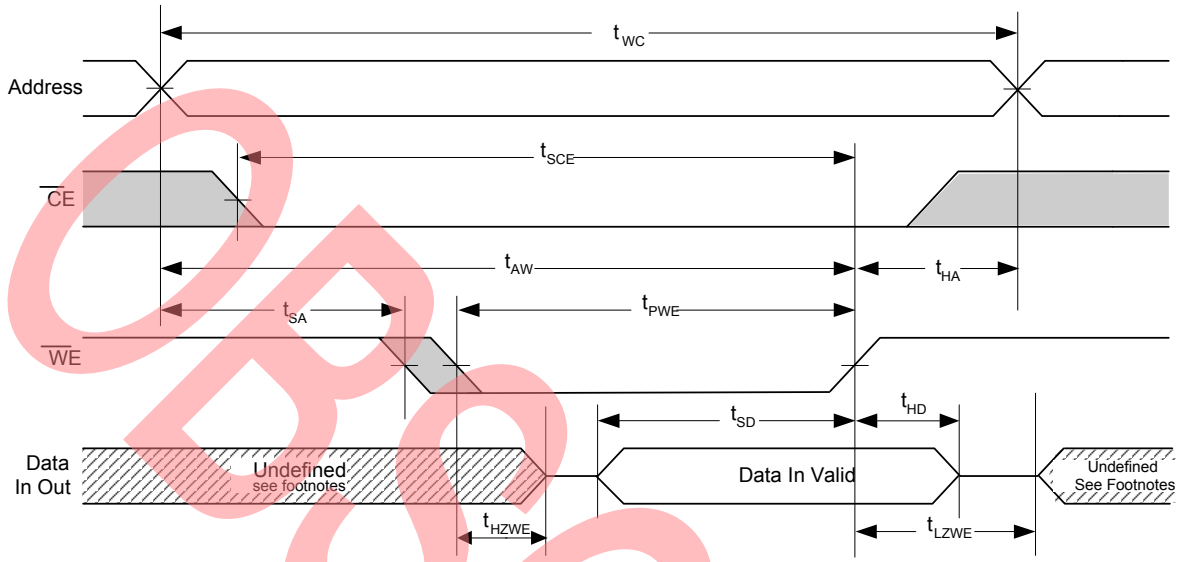
Figure 6. Write Cycle No. 2 ($\overline{CE}$ Controlled) [14, 16, 17]



Notes
13. This cycle is $\overline{WE}$ controlled, $\overline{OE}$ is HIGH during write.
14. Data in and/or out is high impedance if $\overline{OE}$ = V_{IH}.
15. During this period the IOs are in output state and input signals must not be applied.
16. This cycle is $\overline{CE}$ controlled.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

Timing Waveforms *(continued)*

Figure 7. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ Low) [18]

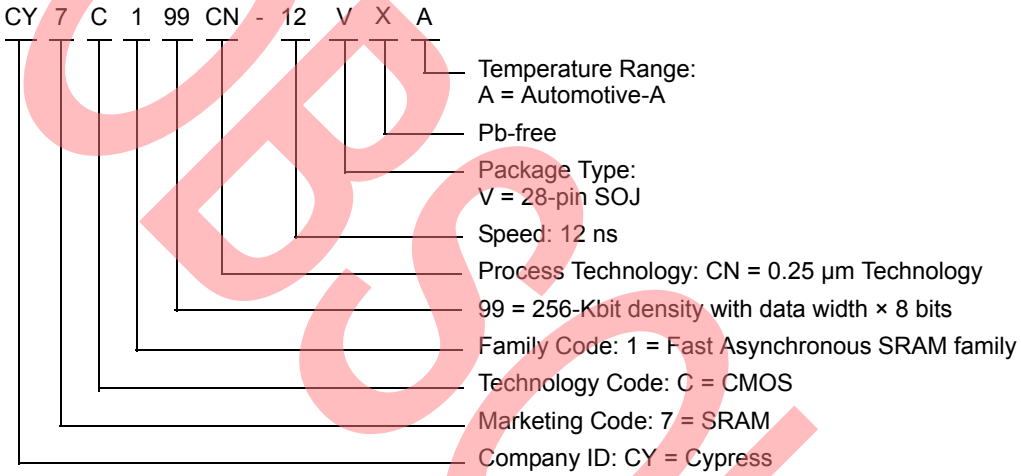


Note
18. The cycle is $\overline{WE}$ controlled, $\overline{OE}$ LOW. The minimum write cycle time is the sum of t_{HZWE} and t_{SD}.

Ordering Information

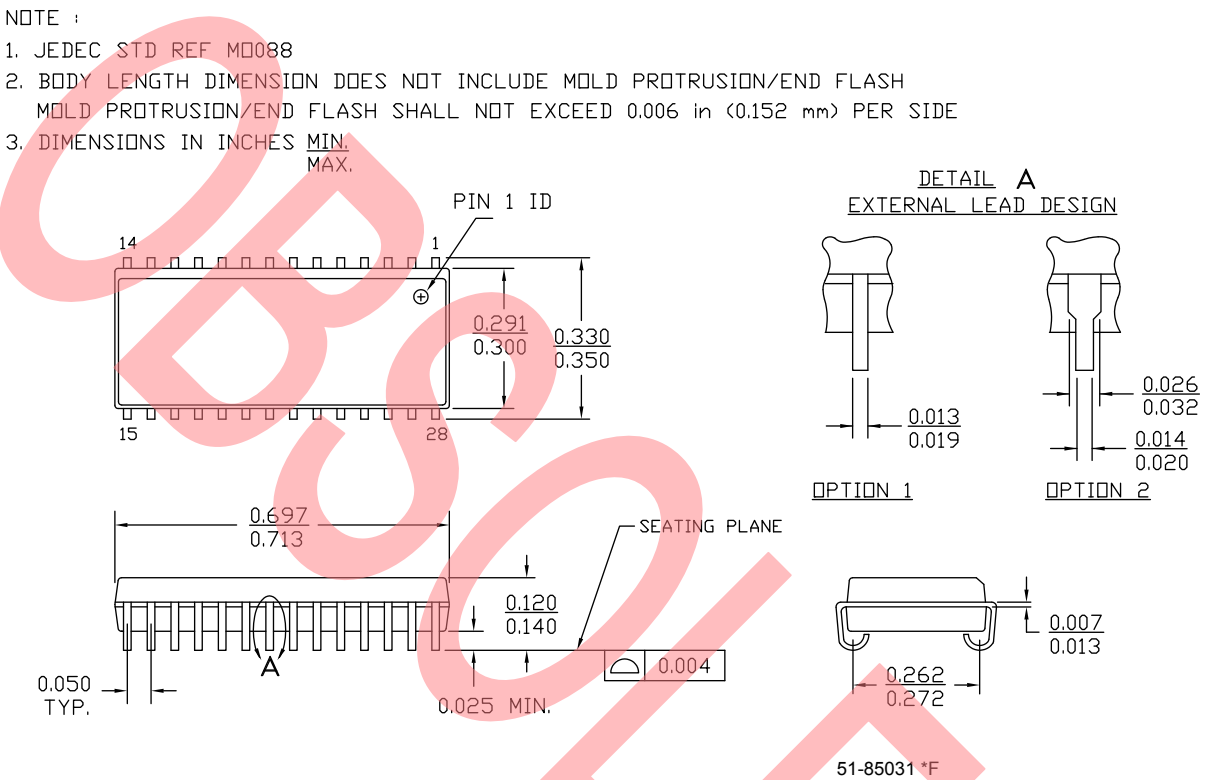
Speed (ns)	Ordering Code	Package Diagram	Package Type	Power Option	Operating Range
12	CY7C199CN-12VXA	51-85031	28-pin SOJ (300 Mils), Pb-free	Standard	Automotive-A

Ordering Code Definitions



Package Diagrams

Figure 8. 28-pin SOJ (300 Mils) V28.3 (Molded SOJ V21) Package Outline, 51-85031



Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
SOJ	Small Outline J-Lead
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C199CN Automotive, 256-Kbit (32K × 8) Static RAM Document Number: 001-67737				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3253367	PRAS	05/23/11	New data sheet. Separation of the automotive data sheet from CY7C199CN spec no. 001-06435 Rev. *D. Further rev of 001-06435 would include only industrial / commercial parts.
*A	4394563	VINI	05/30/2014	Updated Package Diagrams: spec 51-85031 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*B	4546472	VINI	10/28/2014	Updated Maximum Ratings: Referred Note 2 in “Parameter” column. Updated AC Electrical Characteristics: Added Note 5 and referred the same note in “Parameter” column.
*C	4745772	PSR	04/28/2015	Updated Functional Description: Added “For a complete list of related resources, click here.” at the end. Updated Package Diagrams: spec 51-85031 – Changed revision from *E to *F. Updated to new template. Completing Sunset Review.
*D	5307710	VINI	06/14/2016	Obsolete document. Completing Sunset Review.

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