EN6347QI 4A PowerSoC

Step-Down DC-DC Switching Converter with Integrated Inductor

DESCRIPTION

The EN6347QI is an Intel® Enpirion® Power System on a Chip (PowerSoC) DC-DC converter. It integrates the inductor, MOSFET switches, small-signal circuits and compensation in an advanced 4mm x 7mm x 1.85mm 38-pin QFN package.

The EN6347QI is specifically designed to meet the precise voltage and fast transient requirements of present and future high-performance, low-power processor, DSP, FPGA, memory boards and system level applications in distributed power architectures. The device's advanced circuit techniques, high switching frequency, and proprietary integrated inductor technology deliver high-quality, ultra compact, non-isolated DC-DC conversion.

Intel Enpirion Power Solutions significantly help in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, a reduction in the number of components required for the complete power solution helps to enable an overall system cost saving.

All Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

FEATURES

- Integrated Inductor, MOSFETs, Controller
- 1.5% V_{OUT} Accuracy (Over Load and Temperature)
- Up to 4A Continuous Operating Current
- 3 MHz Operating Frequency with Ext Clock Sync
- High Efficiency (Up to 95%)
- Frequency Synchronization to External Clock
- Input Voltage Range (2.5V to 6.6V)
- Programmable Light Load Mode
- Output Enable Pin and Power OK
- Programmable Soft-Start
- Thermal Shutdown, Over-Current, Short Circuit, and Under-Voltage Protection
- RoHS Compliant, MSL Level 3, 260°C Reflow

APPLICATIONS

- Point of Load Regulation for Low-Power, ASICs Multi-Core and Communication Processors, DSPs, FPGAs and Distributed Power Architectures
- Low Voltage, Distributed Power Architectures
- Blade Servers, RAID Storage, Industrial Automation, Embedded Computing, Wireless Communications
- Beat Frequency/Noise Sensitive Applications

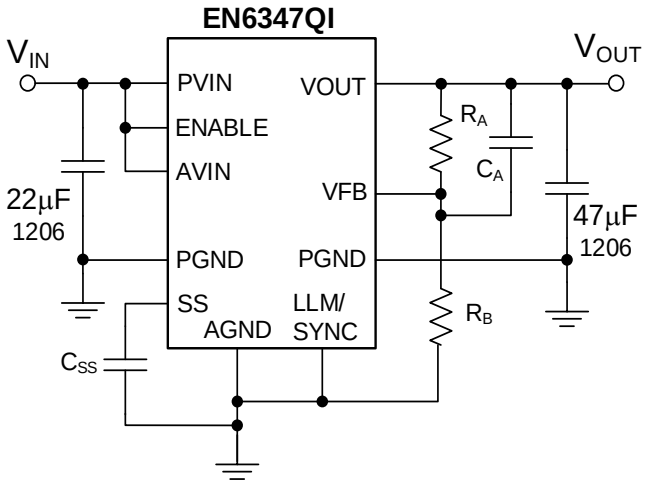


Figure 1: Simplified Applications Circuit

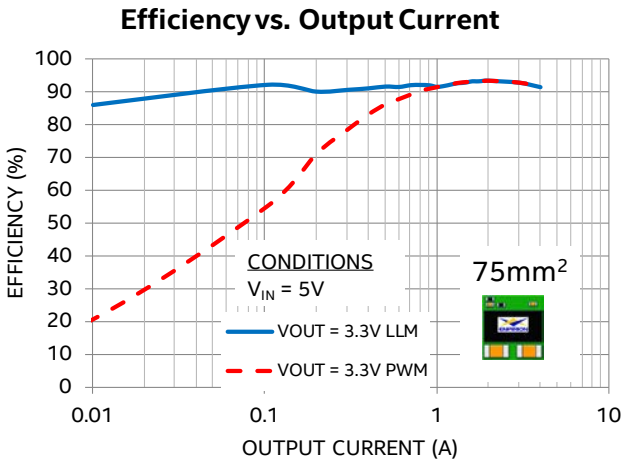


Figure 2: Highest Efficiency in Smallest Solution Size

ORDERING INFORMATION

Part Number	Package Markings	T_J Rating	Package Description
EN6347QI	EN6347QI	-40°C to +125°C	38-pin (4mm x 7mm x 1.85mm) QFN
EVB-EN6347QI	EN6347QI	QFN Evaluation Board	

Packing and Marking Information: https://www.altera.com/support/quality-and-reliability/packing.html

PIN FUNCTIONS

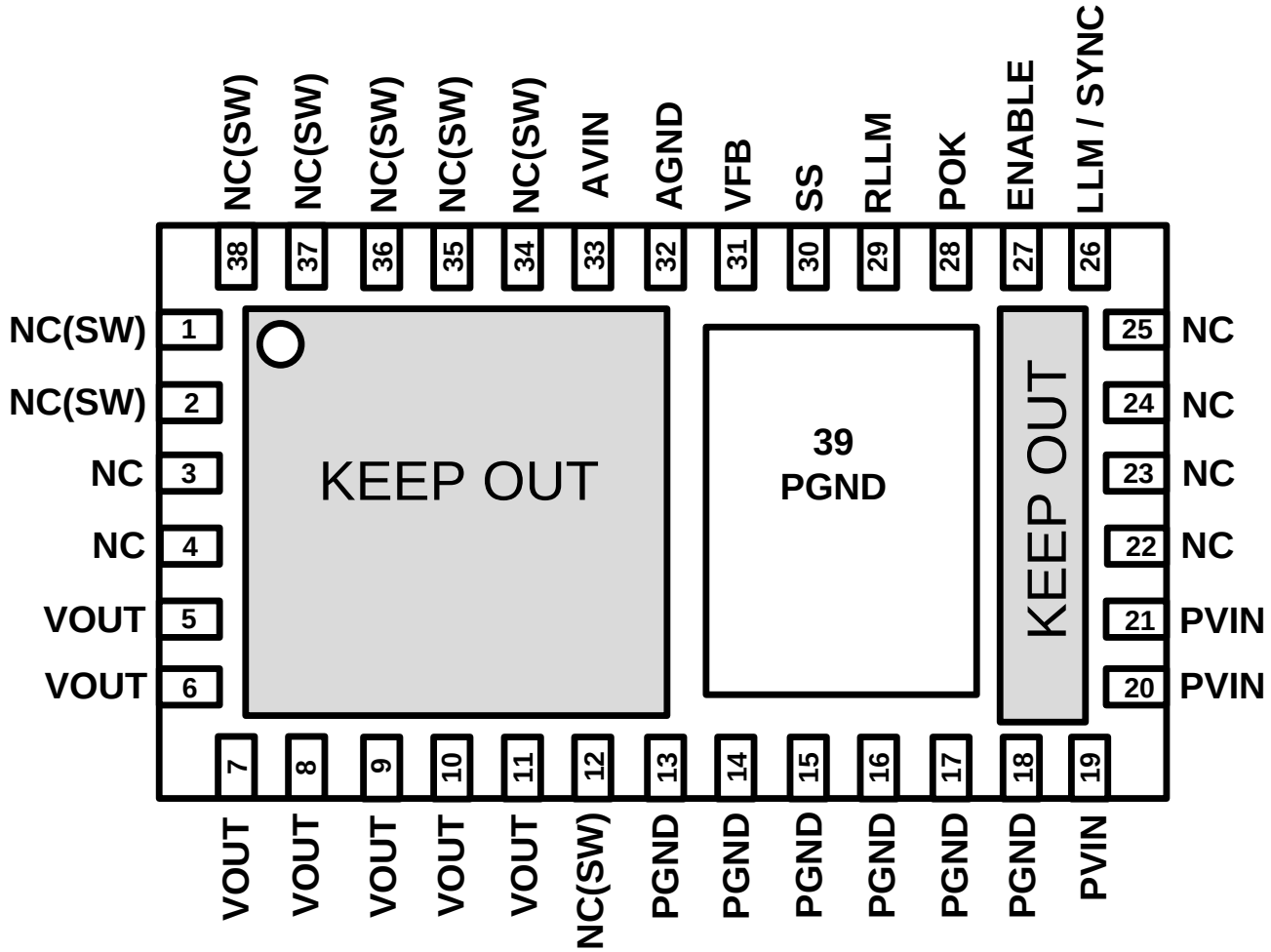


Figure 3: Pin Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: Shaded area highlights exposed metal below the package that is not to be mechanically or electrically connected to the PCB. Refer to Figure 11 for details.

NOTE C: White 'dot' on top left is pin 1 indicator on top of the device package.

PIN DESCRIPTIONS

PIN	NAME	TYPE	FUNCTION
1,2, 12, 34-38	NC(SW)	-	NO CONNECT – These pins are internally connected to the common switching node of the internal MOSFETs. They are not to be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in damage to the device.
3,4, 22-25	NC	-	NO CONNECT – These pins may be internally connected. Do not connect to each other or to any other electrical signal. Failure to follow this guideline may result in device damage.
5- 11	VOUT	Power	Regulated converter output. Connect to the load and place output filter capacitor(s) between these pins and PGND pins. Refer to the Layout Recommendation section.
13-18	PGND	Ground	Input/Output power ground. Connect to the ground electrode of the input and output filter capacitors. See VOUT and PVIN pin descriptions for more details.
19-21	PVIN	Power	Input power supply. Connect to input power supply. Decouple with input capacitor to PGND pin. Refer to the Layout Recommendation section.
26	LLM/SYNC	Analog	Dual function pin providing LLM Enable and External Clock Synchronization (see Application Section). At static Logic HIGH, device will allow automatic engagement of light load mode. At static logic LOW, the device is forced into PWM only. A clocked input to this pin will synchronize the internal switching frequency to the external signal. If this pin is left floating, it will pull to a static logic high, enabling LLM.
27	ENABLE	Analog	Input Enable. Applying logic high enables the output and initiates a soft-start. Applying logic low discharges the output through a soft-shutdown.
28	POK	Digital	Power OK is an open drain transistor used for power system state indication. POK is logic high when V_{OUT} is within ±10% of V_{OUT} nominal and has an internal 100kΩ pull-up resistance to AVIN.
29	RLLM	Analog	Programmable LLM engage resistor to AGND allows for adjustment of load current at which Light-Load Mode engages. Can be left open for PWM only operation.
30	SS	Analog	A soft-start capacitor is connected between this pin and AGND. The value of the capacitor controls the soft-start interval. Refer to Soft-Start Operation in the Functional Description section for more details.
31	VFB	Analog	External Feedback Input. The feedback loop is closed through this pin. A voltage divider at VOUT is used to set the output voltage. The midpoint of the divider is connected to VFB. A phase lead capacitor from this pin to VOUT is also required to stabilize the loop.
32	AGND	Power	Ground for internal control circuits. Connect to the power ground plane with a via right next to the pin.
33	AVIN	Power	Input power supply for the controller. Connect to input voltage at a quiet point. Refer to the Layout Recommendation section.

PIN	NAME	TYPE	FUNCTION
39	PGND	Ground	Power ground thermal pad. Not a perimeter pin. Connect thermal pad to the system GND plane for heat-sinking purposes. Refer to the Layout Recommendation section.

ABSOLUTE MAXIMUM RATINGS

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Absolute Maximum Pin Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
PVIN, AVIN, VOUT		-0.3	7.0	V
ENABLE, POK		-0.3	V_{IN}+0.3	V
VFB, SS		-0.3	2.5	V

Absolute Maximum Thermal Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
Maximum Operating Junction Temperature			+150	°C
Storage Temperature Range		-65	+150	°C
Reflow Peak Body Temperature	(10 Sec) MSL3 JEDEC J-STD-020A		+260	°C

Absolute Maximum ESD Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
HBM (Human Body Model)		±2000		V
CDM (Charged Device Model)		±500		V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.5	6.6	V
Output Voltage Range	V_{OUT}	0.75	$V_{IN} - V_{DO}$ (1)	V
Output Current Range	I_{OUT}		4	A
Operating Ambient Temperature Range	T_A	-40	+85	°C
Operating Junction Temperature	T_J	-40	+125	°C

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	TYPICAL	UNITS
Thermal Shutdown	T_{SD}	160	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	35	°C
Thermal Resistance: Junction to Ambient (0 LFM) (2)	θ_{JA}	30	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	3	°C/W

(1) V_{DO} (dropout voltage) is defined as (I_{LOAD} x Droput Resistance). Please refer to Electrical Characteristics Table.

(2) Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

ELECTRICAL CHARACTERISTICS

NOTE: V_{IN} = 5V, Minimum and Maximum values are over operating ambient temperature range unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}	PVIN = AVIN	2.5		6.6	V
Under Voltage Lock-Out – V_{IN} Rising	V_{UVLOR}	Voltage above which UVLO is not asserted		2.3		V
Under Voltage Lock-Out – V_{IN} Falling	V_{UVLOF}	Voltage below which UVLO is asserted		2.075		V
Shut-Down Supply Current	I_S	ENABLE = 0V		100		µA
Operating Quiescent Current	I_Q	LLM/SYNC = High		650		mA
Feedback Pin Voltage [3]	V_{FB}	VIN = 5V, ILOAD = 0, TA = 25°C	0.7425	0.75	0.7575	V
Feedback Pin Voltage (Load, Temp.)	V_{FB}	0A ≤ I_{LOAD} ≤ 4A -40°C ≤ T_A ≤ 85°C Starting Date Code: X501 or greater	0.739	0.75	0.761	V
Feedback Pin Voltage (Line, Load, Temp.)	V_{FB}	3.0V ≤ V_{IN} ≤ 6.0V 0A ≤ I_{LOAD} ≤ 4A	0.735	0.75	0.765	V
Feedback pin Input Leakage Current [4]	I_{FB}	VFB pin input leakage current	-5		5	nA
V_{OUT} Rise Time Range [4]	t_{RISE}	Measured from when V_{IN} > V_{UVLOR} & ENABLE pin voltage crosses its logic high threshold to when V_{OUT} reaches its final value. C_{SS} = 15 nF	0.9	1.2	1.5	ms
Soft Start Capacitance Range	C_{SS_RANGE}		10	47	68	nF
Drop-Out Voltage [4]	V_{DO}	V_{INMIN} - V_{OUT} at full load		240	360	mV
Drop-Out Resistance [4]	R_{DO}	Input to output resistance		60	90	mΩ
Continuous Output Current	I_{OUT}	PMM mode LLM mode [5]	0 0.002		4 4	A
Over Current Trip Level	I_{OCP}	V_{IN} = 5V, V_{OUT} = 1.2V		5		A

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Precision Disable Threshold	$V_{DISABLE}$	ENABLE pin logic going low	0		0.6	V
Precision Enable Threshold	V_{EN}	ENABLE pin logic going high $2.5V \le V_{IN} \le 6.6V$	1.8		V_{IN}	V
ENABLE Lockout Time	$T_{ENLOCKOUT}$			3.2		ms
ENABLE Pin Input Current (4)	I_{EN}	ENABLE pin has ~180kΩ pull down		40		µA
Switching Frequency (Free Running)	F_{SW}	Free running frequency of oscillator		3		MHz
External SYNC Clock Frequency Lock Range	F_{PLL_LOCK}	Range of SYNC clock frequency	2.5		3.5	MHz
SYNC Input Threshold – Low (LLM/SYNC PIN)	V_{SYNC_LO}	SYNC Clock Logic Level			0.8	V
SYNC Input Threshold – High (LLM/SYNC PIN) (6)	V_{SYNC_HI}	SYNC Clock Logic Level	1.8		2.5	V
POK Lower Threshold	POK_{LT}	Output voltage as a fraction of expected output voltage		90		%
POK Low Voltage	V_{POKL}	With 4mA current sink into POK			0.4	V
POK High Voltage	V_{POKH}	$2.5V \le V_{IN} \le 6.6V$			V_{IN}	V
POK Pin Leakage Current (4)	I_{POKH}	POK is high			1	µA
LLM Engage Headroom		Minimum V_{IN}-V_{OUT} to ensure proper LLM operation		800		mV
LLM Logic Low (LLM/SYNC PIN)	V_{LLM_LO}	LLM Static Logic Level			0.3	V
LLM Logic High (LLM/SYNC PIN)	V_{LLM_HI}	LLM Static Logic Level	1.5			V
LLM/SYNC Pin Current		LLM/SYNC Pin is <2.5V		<100		nA

(3) The VFB pin is a sensitive node. Do not touch VFB while the device is in regulation.

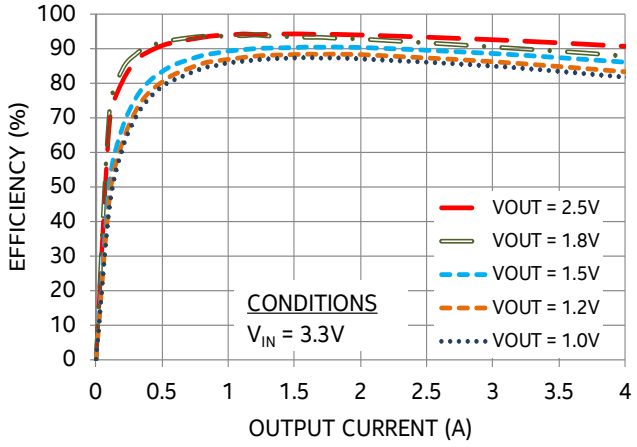
(4) Parameter not production tested but is guaranteed by design.

(5) LLM operation is normally only guaranteed above the minimum specified output current.

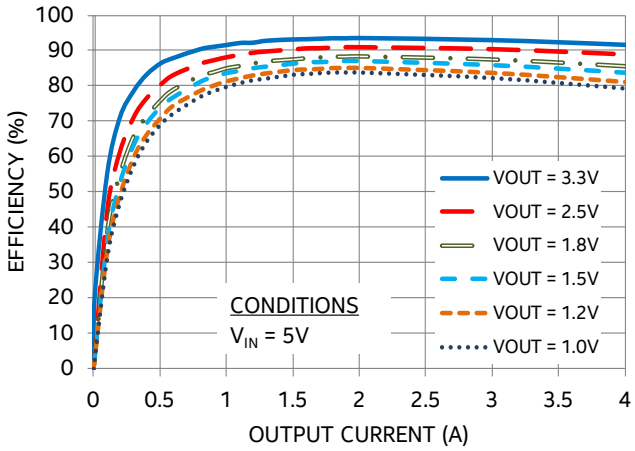
(6) For proper operation of the synchronization circuit, the high-level amplitude of the SYNC signal should not be above 2.5V.

TYPICAL PERFORMANCE CURVES

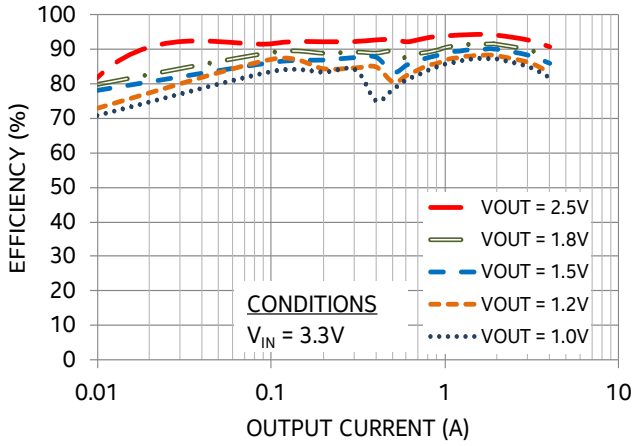
PWM Efficiency vs. I_{OUT} (V_{IN} = 3.3V)



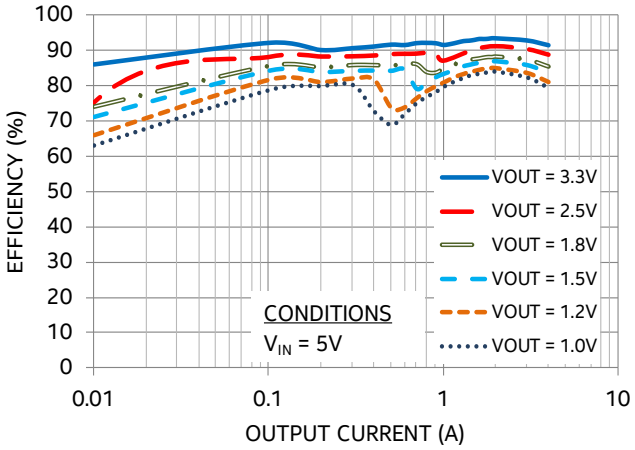
PWM Efficiency vs. I_{OUT} (V_{IN} = 5.0V)



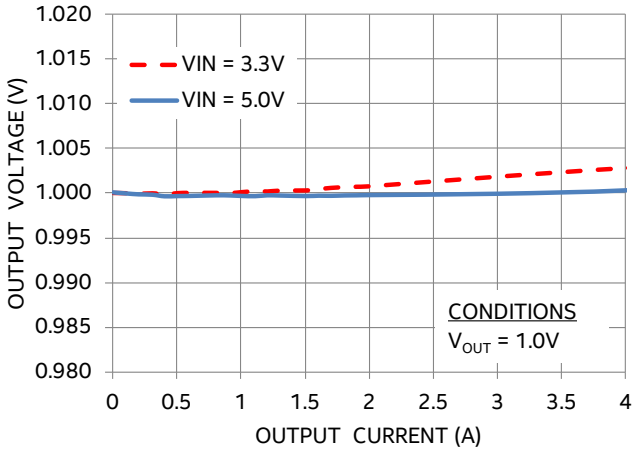
LLM Efficiency vs. I_{OUT} (V_{IN} = 3.3V)



LLM Efficiency vs. I_{OUT} (V_{IN} = 5.0V)



Output Voltage vs. Output Current



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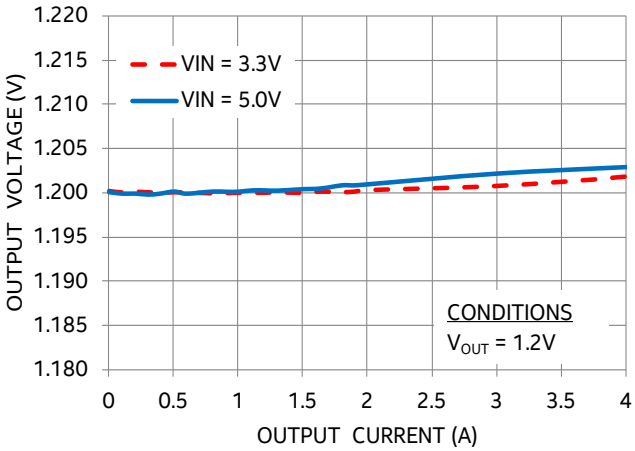
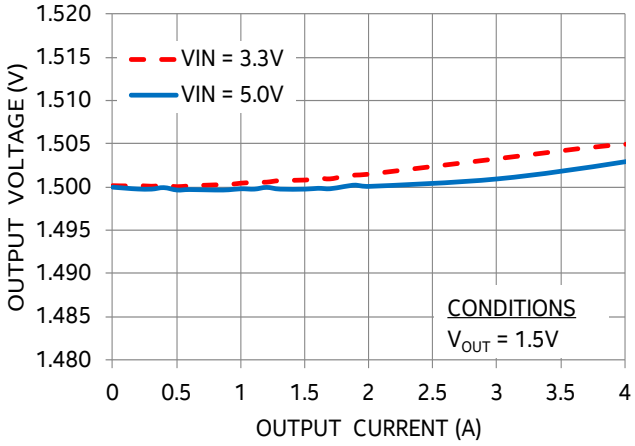


TYPICAL PERFORMANCE CURVES (CONTINUED)

Output Voltage vs. Output Current



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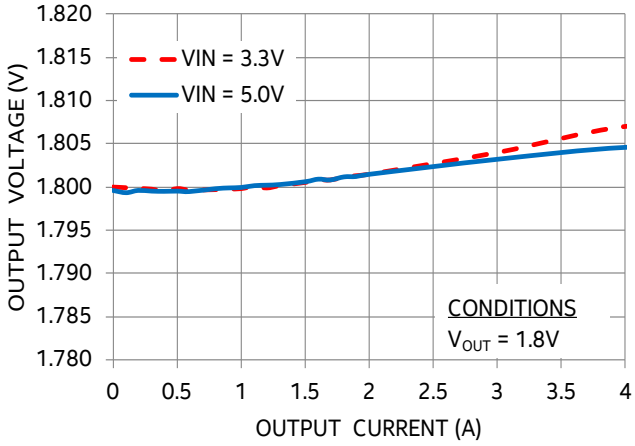

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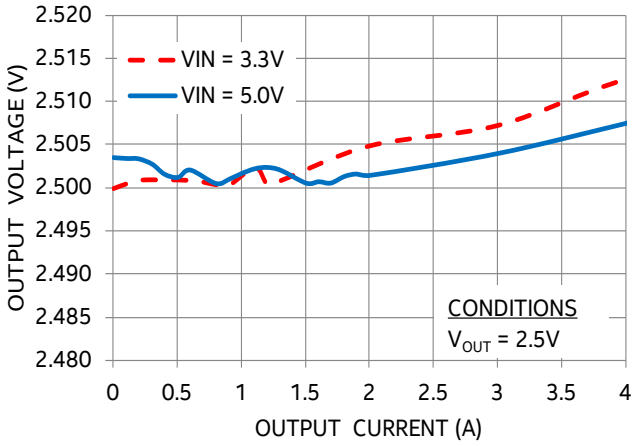

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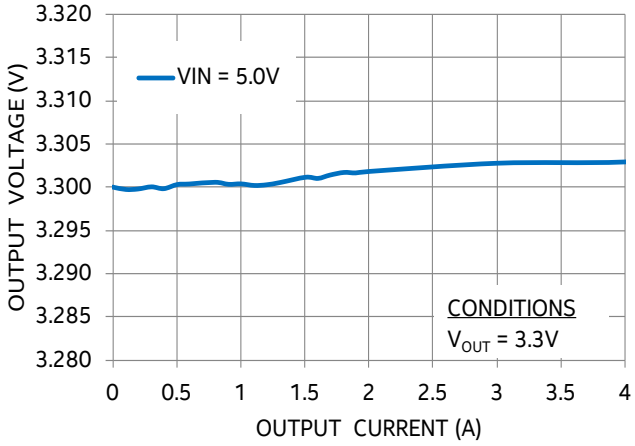
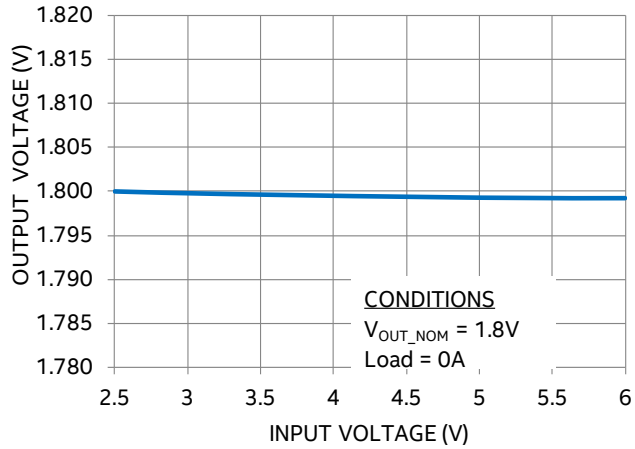
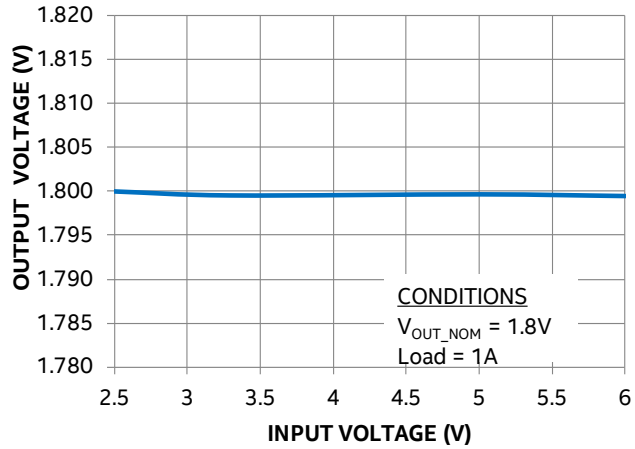


Output Voltage vs. Input Voltage

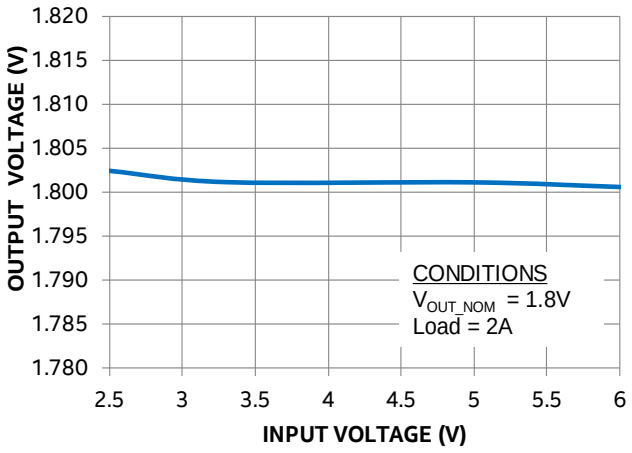


Output Voltage vs. Input Voltage

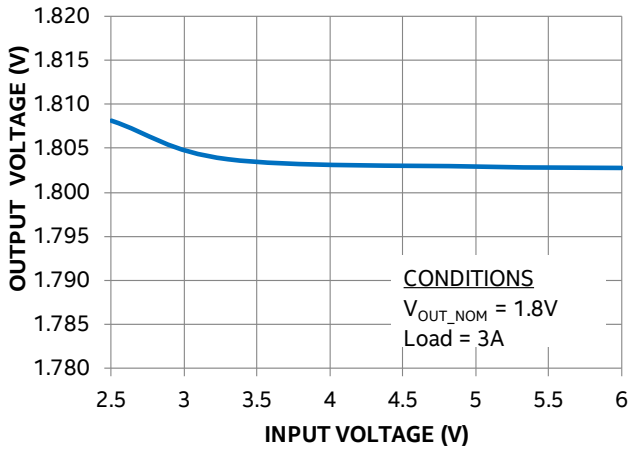


TYPICAL PERFORMANCE CURVES (CONTINUED)

Output Voltage vs. Input Voltage



Output Voltage vs. Input Voltage



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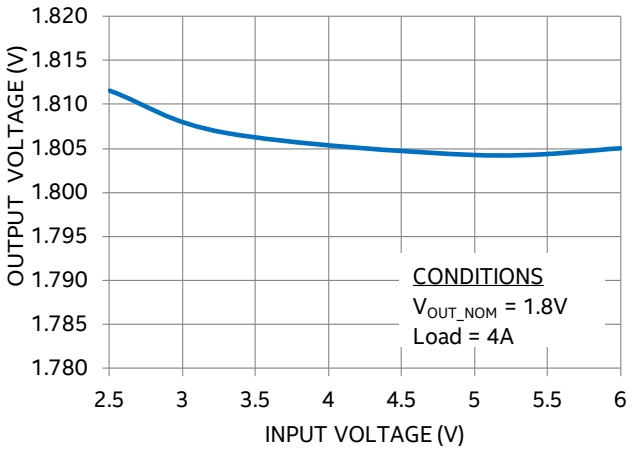
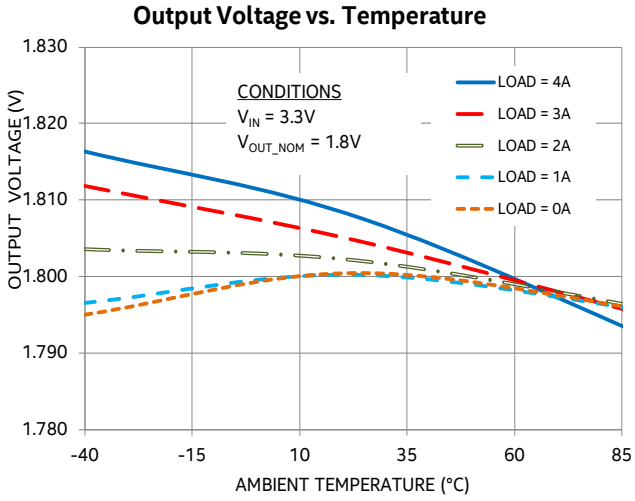
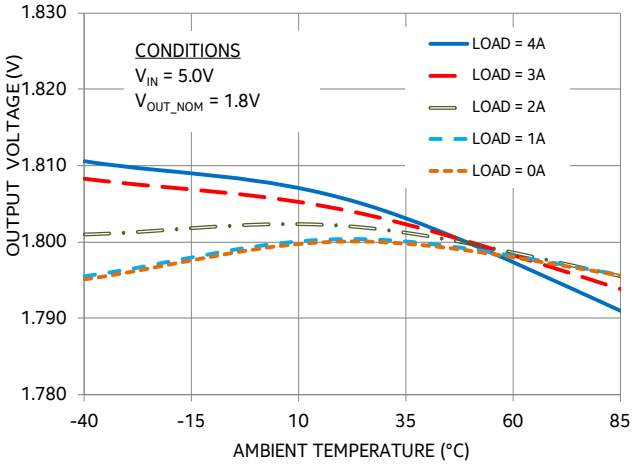


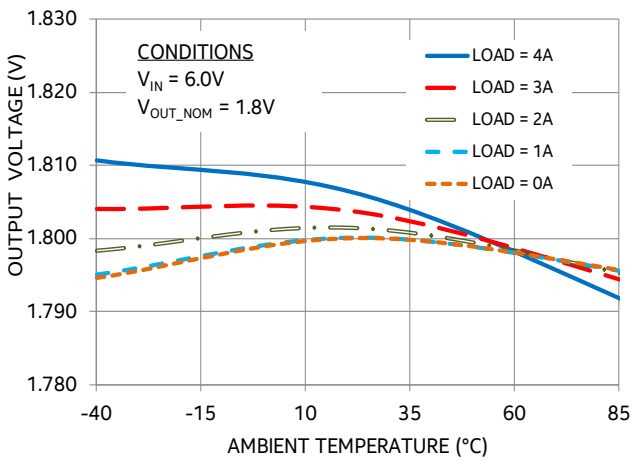
Output Voltage vs. Temperature



Output Voltage vs. Temperature

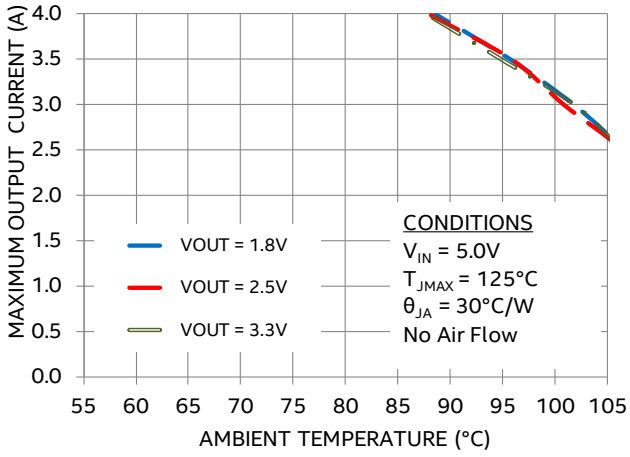


Output Voltage vs. Temperature

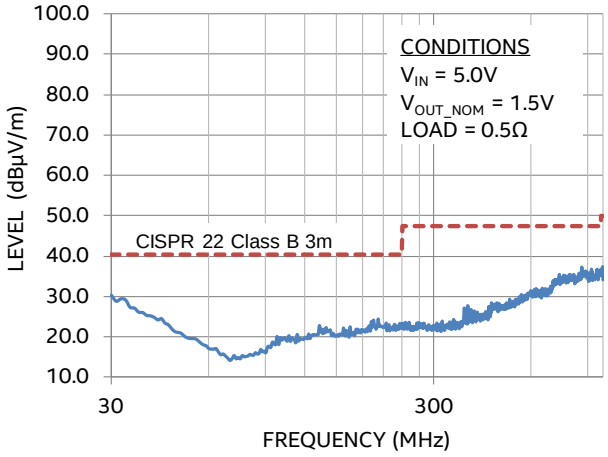


TYPICAL PERFORMANCE CHARACTERISTICS

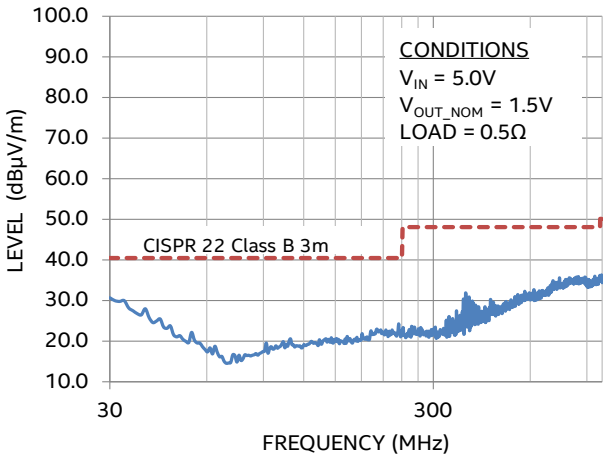
Output Current De-rating



EMI Performance (Horizontal Scan)

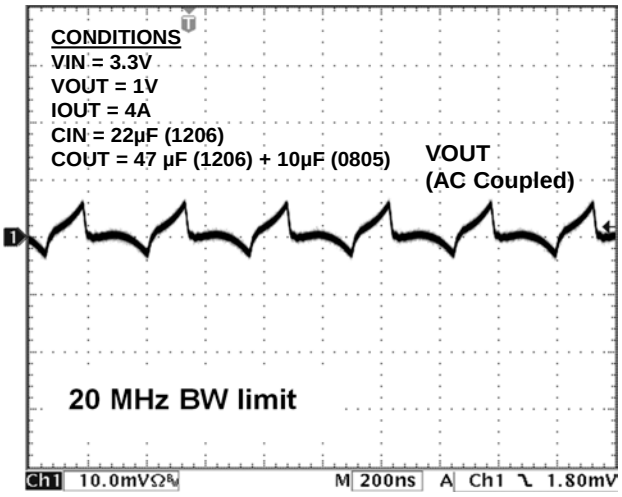


EMI Performance (Vertical Scan)

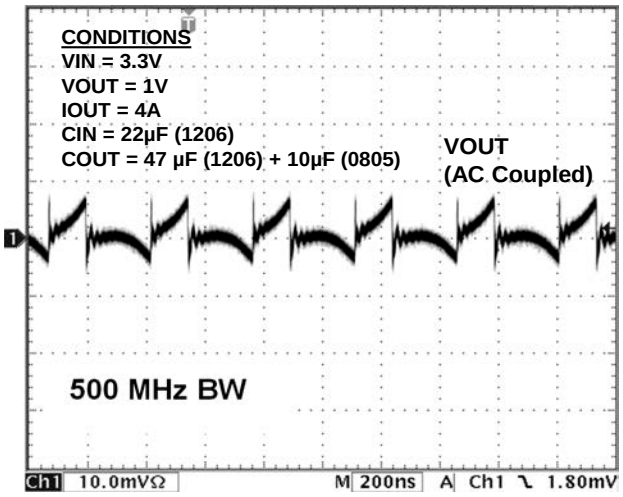


TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

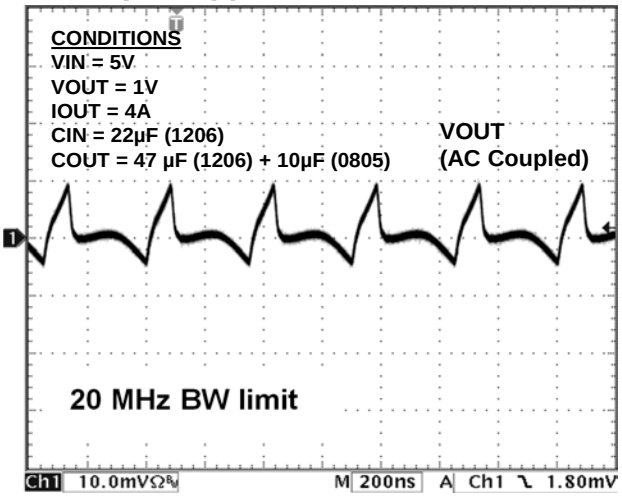
Output Ripple at 20MHz Bandwidth



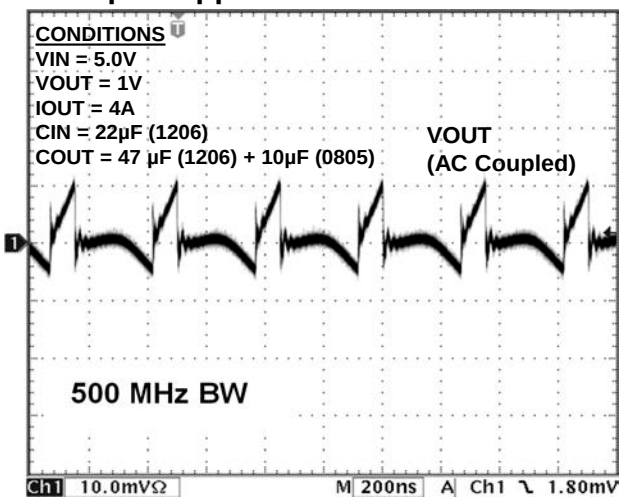
Output Ripple at 500MHz Bandwidth



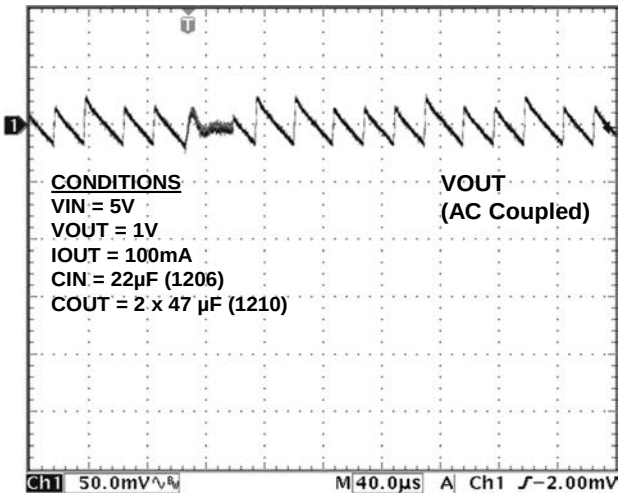
Output Ripple at 20MHz Bandwidth



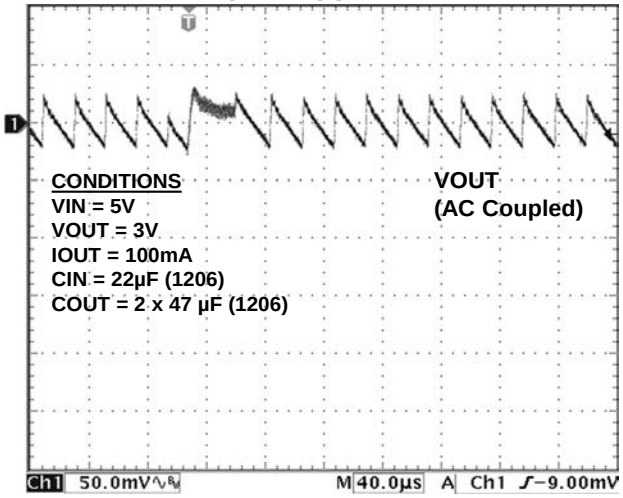
Output Ripple at 500MHz Bandwidth



LLM Output Ripple at 100mA

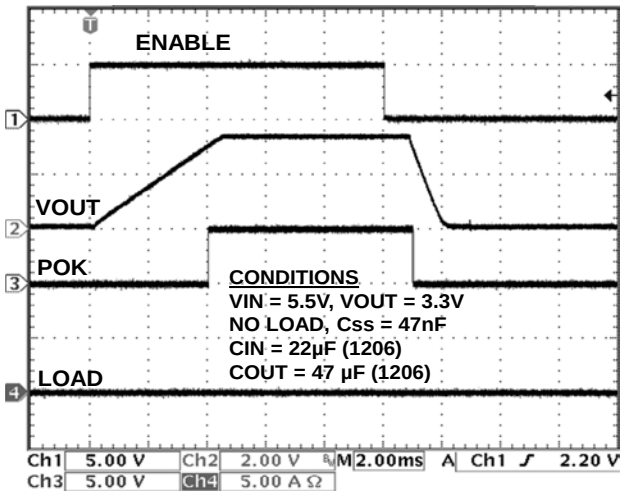


LLM Output Ripple at 100mA

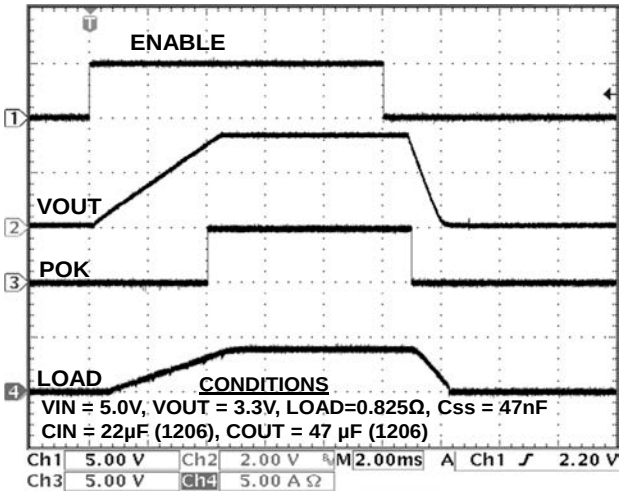


TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

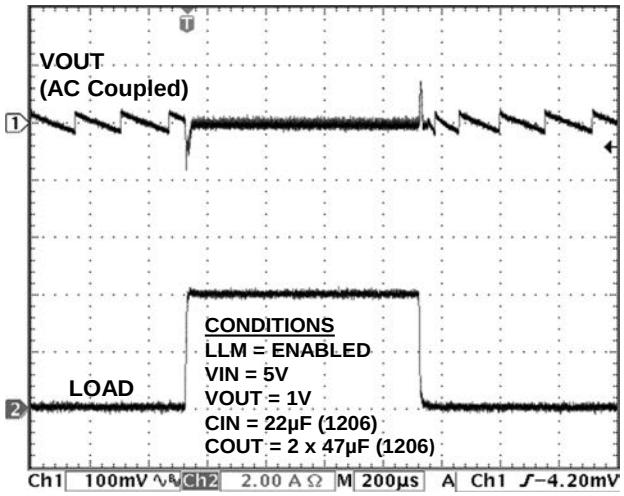
Enable Power Up/Down



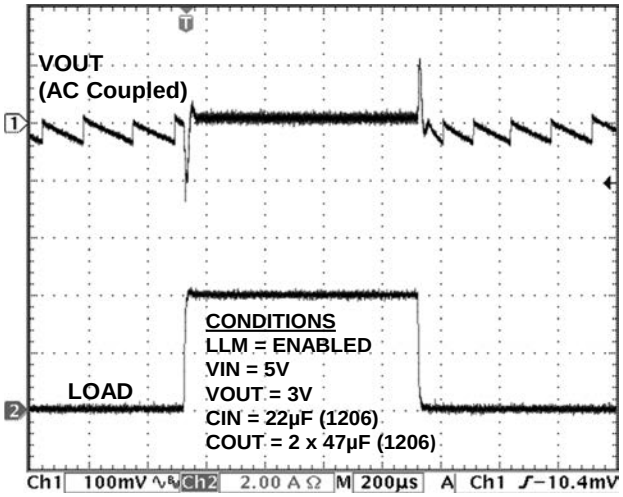
Enable Power Up/Down



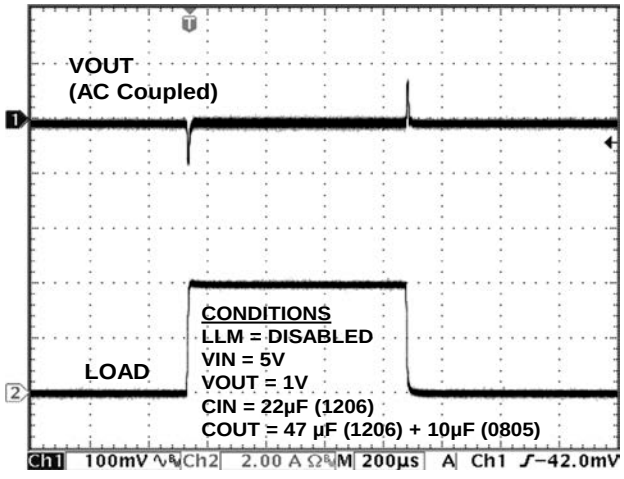
LLM Load Transient from 0.01 to 4A



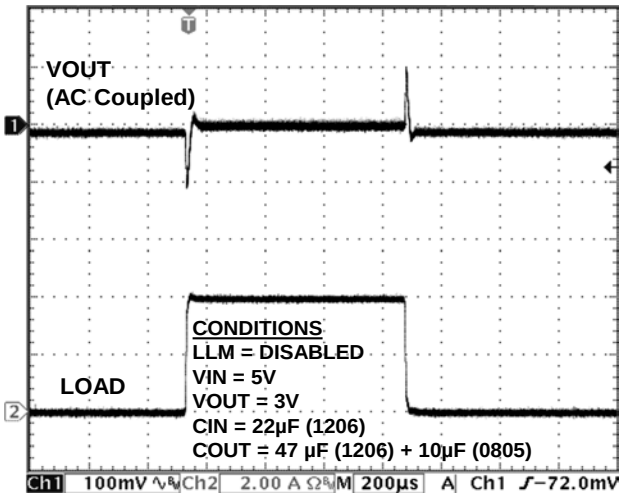
LLM Load Transient from 0.01 to 4A



PWM Load Transient from 0 to 4A



PWM Load Transient from 0 to 4A



FUNCTIONAL BLOCK DIAGRAM

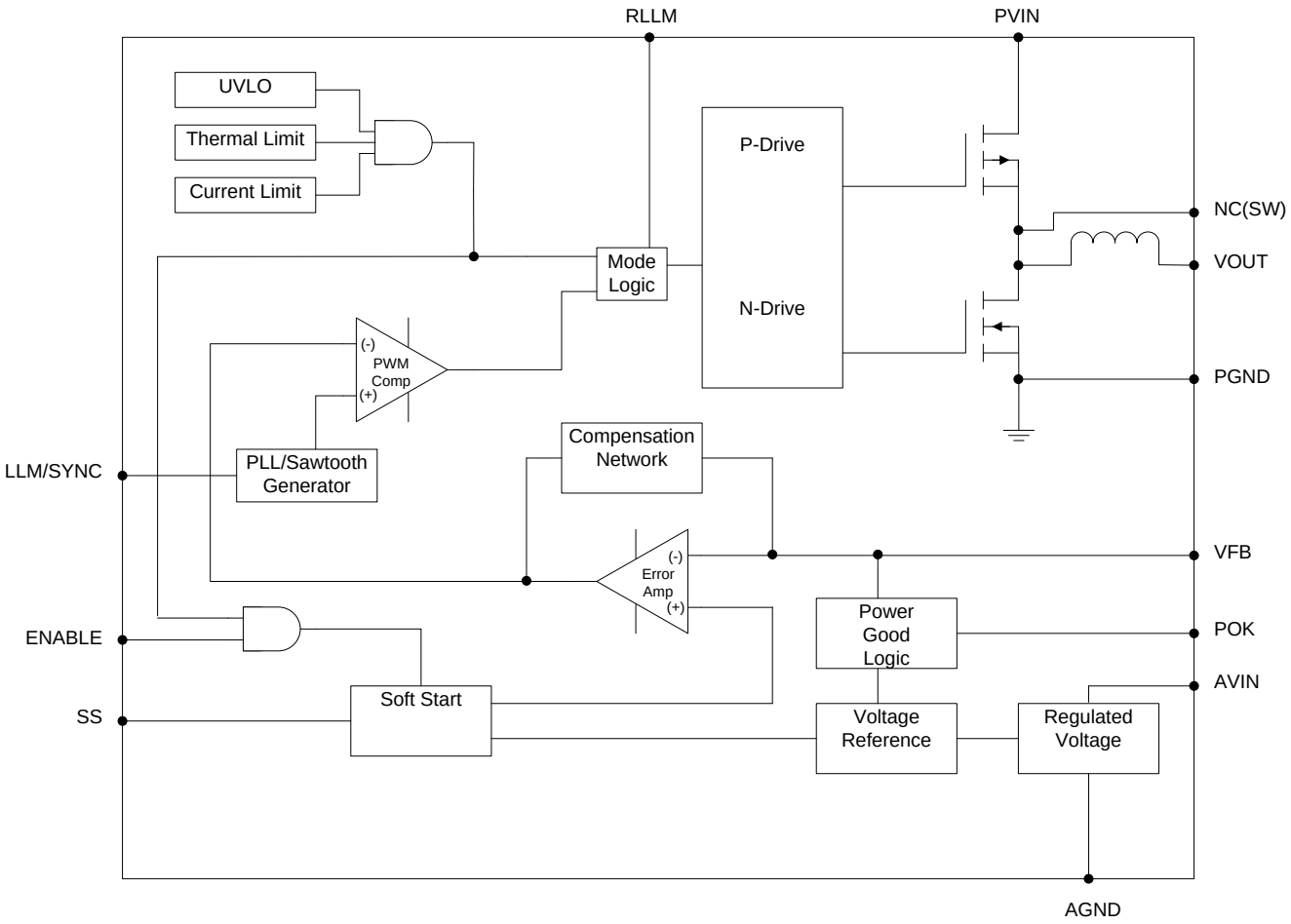


Figure 4: Functional Block Diagram

FUNCTIONAL DESCRIPTION

Synchronous DC-DC Step-Down PowerSoC

The EN6347QI is a synchronous, programmable power supply with integrated power MOSFET switches and integrated inductor. The nominal input voltage range is 2.5V to 6.6V. The output voltage is programmed using an external resistor divider network. The control loop is voltage-mode with a type III compensation network. Much of the compensation circuitry is internal to the device. However, a phase lead capacitor is required along with the output voltage feedback resistor divider to complete the type III compensation network. The device uses a low-noise PWM topology and also integrates a unique light-load mode (LLM) to improve efficiency at light output load currents. LLM can be disabled with a logic pin. Up to 4A of continuous output current can be drawn from this converter. The 3MHz switching frequency allows the use of small size input / output capacitors, and enables wide loop bandwidth within a small foot print.

Protection Features:

The power supply has the following protection features:

- Over-current protection (to protect the IC from excessive load current)
- Thermal shutdown with hysteresis.
- Under-voltage lockout circuit to keep the converter output off while the input voltage is less than 2.3V.

Additional Features:

- The switching frequency can be phase-locked to an external clock to eliminate or move beat frequency tones out of band.
- Soft-start circuit allowing controlled startup when the converter is initially powered up. The soft start time is programmable with an appropriate choice of soft start capacitor.
- Power good circuit indicating the output voltage is greater than 90% of programmed value as long as feedback loop is closed.
- To maintain high efficiency at low output current, the device incorporates automatic light load mode operation.

Precision Enable Operation

The ENABLE pin provides a means to enable normal operation or to shut down the device. When the ENABLE pin is asserted (high) the device will undergo a normal soft-start. A logic low on this pin will power the device down in a controlled manner. From the moment ENABLE goes low, there is a fixed lock out time before the output will respond to the ENABLE pin re-asserted (high). This lock out is activated for even very short logic low pulses on the ENABLE pin. The ENABLE signal must be pulled high at a slew rate faster than 1V/5µs in order to meet startup time specifications; otherwise, the device may experience a delay of 4.2ms (lock-out time) before startup occurs. See the Electrical Characteristics Table for technical specifications for this pin. See the Electrical Characteristics Table for technical specifications for the ENABLE pin.

LLM/SYNC Pin

This is a dual function pin providing LLM Enable and External Clock Synchronization. At static Logic HIGH, device will allow automatic engagement of light load mode. At static logic LOW, the device is forced into PWM only. A clocked input to this pin will synchronize the internal switching frequency – LLM mode is not available if this input is clocked. If this pin is left floating, it will pull to a static logic high, enabling LLM.

Frequency Synchronization

The switching frequency of the DC-DC converter can be phase-locked to an external clock source to move unwanted beat frequencies out of band. To avail this feature, the clock source should be connected to the LLM/SYNC pin. An activity detector recognizes the presence of an external clock signal and automatically phase-locks the internal oscillator to this external clock. Phase-lock will occur as long as the clock frequency is in the range specified in the Electrical Characteristics Table. For proper operation of the synchronization circuit, the high-level amplitude of the SYNC signal should not be above 2.5V. Please note LLM is not available when synchronizing to an external frequency.

Spread Spectrum Mode

The external clock frequency may be swept between the limits specified in the Electrical Characteristics Table at repetition rates of up to 10kHz in order to reduce EMI frequency components.

Soft-Start Operation

During Soft-start, the output voltage is ramped up gradually upon start-up. The output rise time is controlled by the choice of soft-start capacitor, which is placed between the SS pin (30) and the AGND pin (32).

$$\text{Rise Time: } T_R \approx (C_{SS} * 80k\Omega) \pm 25\%$$

During start-up of the converter, the reference voltage to the error amplifier is linearly increased to its final level by an internal current source of approximately 10µA. Typical soft-start rise time is ~3.8ms with SS capacitor value of 47nF. The rise time is measured from when $V_{IN} > V_{UVLOR}$ and ENABLE pin voltage crosses its logic high threshold to when V_{OUT} reaches its programmed value. Please note LLM function is disabled during the soft-start ramp-up time.

POK Operation

The POK signal is an open drain signal (requires a pull up resistor to V_{IN} or similar voltage) from the converter indicating the output voltage is within the specified range. The POK signal will be logic high (V_{IN}) when the output voltage is above 90% of programmed V_{OUT}. If the output voltage goes below this threshold, the POK signal will be logic low.

Light Load Mode (LLM) Operation

The EN6347QI uses a proprietary light load mode to provide high efficiency at low output currents. When the LLM/SYNC pin is high, the device is in automatic LLM "Detection" mode. When the LLM/SYNC pin is low, the device is forced into PWM mode. In automatic LLM "Detection" mode (LLM connected to AVIN with 50kΩ), when a light load condition is detected, the device will:

(1) Step V_{OUT} up by approximately 1.0% above the nominal operating output voltage setting, V_{NOM} and as low as -0.5% below V_{NOM}, and then

(2) Shut down unnecessary circuitry, and then

(3) Monitor V_{OUT}.

When V_{OUT} falls below V_{NOM}, the device will repeat (1), (2), and (3). The voltage step up, or pre-positioning, improves transient droop when a load transient causes a transition from LLM mode to PWM mode. If a load transient occurs, causing V_{OUT} to fall below the threshold V_{MIN}, the device will exit LLM operation and begin normal PWM operation. Figure 5 demonstrates V_{OUT} behavior during transition into and out of LLM operation. Many multi-mode DC-DC converters suffer from a condition that occurs when the load current increases only slowly so that there is no load transient driving V_{OUT} below the V_{MIN} threshold. In this condition, the device would never exit LLM operation. This could adversely affect efficiency and cause unwanted ripple. To prevent this from occurring, the EN6347QI periodically exits LLM mode into PWM mode and measures the load current. If the load current is above the LLM threshold current, the device will remain in PWM mode. If the load current is below the LLM threshold, the device will re-enter LLM operation. There may be a small overshoot or undershoot in V_{OUT} when the device exits and re-enters LLM.

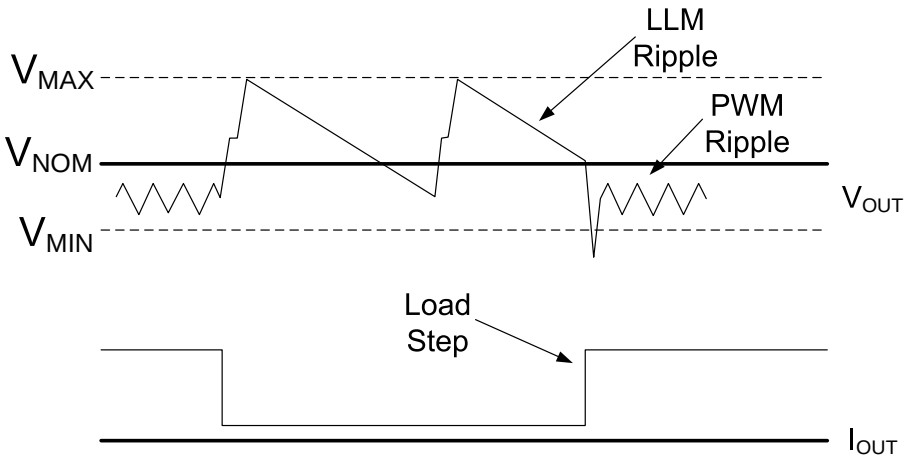


Figure 5. VOUT behavior in LLM operation

The load current at which the device will enter LLM mode is a function of input and output voltage, inductance variation and the RLLM pin resistor. The lower the RLLM resistor value, the lower the current when the device transitions from LLM into PWM mode. A 60kΩ resistor from RLLM to ground is recommended for most applications. For PWM only operation, the RLLM pin can be left open.

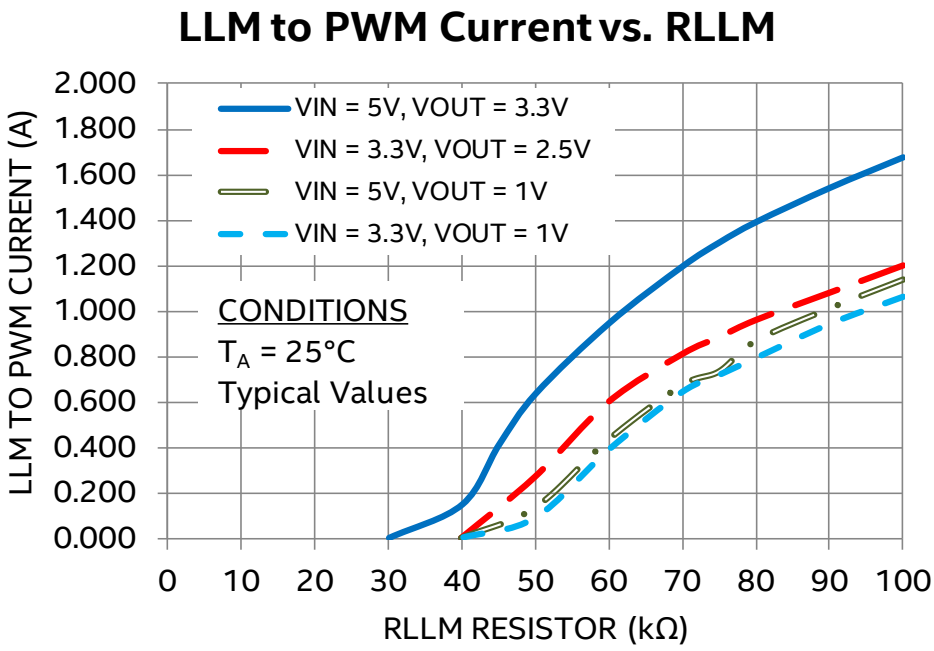


Figure 6. Typical LLM to PWM Current vs. RLLM

To ensure normal LLM operation, LLM mode should be enabled and disabled with specific sequencing. For applications with explicit LLM pin control, enable LLM after V_{IN} ramp up is complete. For applications with only ENABLE controlled, tie LLM to ENABLE. Enable the device after VIN ramps up into regulation and disable the device before VIN ramps. For designs with ENABLE and LLM tied to V_{IN}, make sure the device soft-start time is longer than the V_{IN} ramp-up time. LLM will start operating after the soft-start time is completed.

NOTE: For proper LLM operation the EN6347QI requires a minimum difference between V_{IN} and V_{OUT}, and a minimum LLM load requirement as specified in the Electrical Characteristics Table.

Over-Current Protection (OCP)

The current limit function is achieved by sensing the current flowing through the Power PFET. When the sensed current exceeds the over current trip point, both power FETs are turned off for the remainder of the switching cycle. If the over-current condition is removed, the over-current protection circuit will enable normal PWM operation. If the over-current condition persists, the soft start capacitor will gradually discharge causing the output voltage to fall. When the OCP fault is removed, the output voltage will ramp back up to the desired voltage. This circuit is designed to provide high noise immunity.

Thermal Protection

Thermal shutdown circuit will disable device operation when the Junction temperature exceeds the thermal shutdown temperature. After a thermal shutdown event, when the junction temperature drops to a safe operating level, the converter will re-start with a normal soft-start. The specific thermal shutdown junction temperature and hysteresis can be found in the Thermal Characteristics Table.

Input Under-Voltage Lock-Out (UVLO)

Internal circuits ensure that the converter will not start switching until the input voltage is above the specified minimum voltage. Hysteresis and input de-glitch circuits ensure high noise immunity and prevent false UVLO triggers.

APPLICATION INFORMATION

Output Voltage Setting

The EN6347QI uses a Type III voltage mode control compensation network. As noted earlier, a piece of the compensation network is the phase lead capacitor C_A equal 10pF in Figure 7. This network is optimized for use with about 50-100µF.

The EN6347QI output voltage is programmed using a simple resistor divider network. Since VFB is a sensitive node, do not touch the VFB node while the device is in operation as doing so may introduce parasitic capacitance into the control loop that causes the device to behave abnormally and damage may occur Figure 7 shows the resistor divider configuration. An additional compensation capacitor C_A is also required in parallel with the upper resistor.

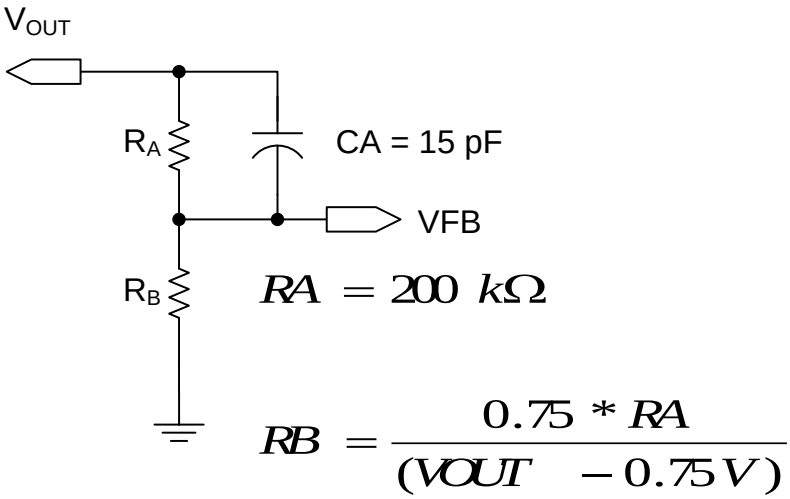


Figure 7. VOUT Resistor Divider & Compensation Capacitor

The EN6347QI output voltage is programmed using a simple resistor divider network (R_A and R_B). Figure 7 shows the resistor divider configuration.

The recommended R_A resistor value is 200kΩ and the feedback voltage is typically 0.75V. Depending on the output voltage (V_{OUT}), the R_B resistor value may be calculated as shown in Figure 7. Since the accuracy of the output voltage setting is dependent upon the feedback voltage and the external ressitors, 1% or better resistors are recommended. The external compensation capacitor (C_A) is also required in parallel with R_A, depending on input voltage and output voltage setting.

Table 1: Best Performance Solution

C_{OUT}= 47µF 1206, C_{IN}= 22µF (10V,1206), R_A= 200kΩ

V_{OUT}	V_{IN}	C_A
3.3V	6.6V	18pF
	≤5.0V	22pF
2.5V	6.6V	22pF
	≤5.0V	33pF
1.8V	6.6V	27pF
	5.0V	33pF
	3.3V	39pF
	2.5V	47pF
1.5V	6.6V	27pF
	5.0V	33pF
	≤3.3V	47pF
≤1.2V	6.6V	15pF
	5.0V	12pF
	≤3.3V	12pF

Table 2: Small Footprint Solution

C_{OUT}= 47µF (1206), C_{IN}= 22µF (10V,1206), R_A= 200kΩ

V_{OUT}	V_{IN}	C_A
3.3V	ALL V_{IN}	10pF
2.5V	> 5.0V	12pF
	≤ 5.0V	15pF
1.8V	6.6V	12pF
	5.0V	15pF
	3.3V	22pF
	2.5V	27pF
1.5V	> 3.3V	15pF
	≤ 3.3V	27pF
≤ 1.2V	6.6V	15pF
	5.0V	18pF
	≤ 3.3V	27pF

Input Capacitor Selection

The EN6347QI requires at least a 22µF X5R/X7R ceramic input capacitor. Additional input capacitors may be used in parallel to reduce input voltage spikes caused by parasitic line inductance. For applications where the input of the EN6347QI is far from the input power source, be sure to use sufficient bulk capacitors to mitigate the extra line inductance. Low-cost, low-ESR ceramic capacitors should be used as input capacitors for this converter. The dielectric must be X5R/X7R rated. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage. In some applications, lower value capacitors are needed in parallel with the larger, capacitors in order to provide high frequency decoupling.

Table 3: Recommended Input Capacitors

Description	MFG	P/N
22µF, 10V, X7R, 1206	Murata	GRM31CR71A226ME15
	Taiyo Yuden	LMK316AB7226KL-TR
	AVX	1206ZC226KAT2A
22µF, 10V, X5R, 1206	Murata	GRM31CR61A226ME19L
	Taiyo Yuden	LMK316BJ226ML-T
22µF, 16V, X5R, 0805	Murata	GRM21BR61C226ME44L
	Taiyo Yuden	EMK212BBJ226MG-T
22µF, 10V, X7R, 1206	Murata	GRM31CR71A226ME15
	Taiyo Yuden	LMK316AB7226KL-TR

Output Capacitor Selection

The EN6347QI requires at least one 22µF 0805 case size ceramic output capacitor. Additional output capacitors may be used in parallel near the load (>4mΩ away) to improve transient response as well as lower output ripple. In some cases modifications to the compensation or output filter capacitance may be required to optimize device performance such as transient response, ripple, or hold-up time. The EN6347QI provides the capability to modify the control loop response to allow for customization for such applications. Note that in Type III Voltage Mode Control, the double pole of the output filter is around $1/2\pi\sqrt{L_O \cdot C_{out}}$, where C_{out} is the equivalent capacitance of all the output capacitors including the minimum required output capacitors that Altera recommended and the extra bulk capacitors customers added based on their design requirement. While the compensation network was designed based on the capacitors that Altera recommended, increasing the output capacitance will shift the double pole to the direction of lower frequency, which will lower the loop bandwidth and phase margin. In most cases, this will not cause the instability due to adequate phase margin already in the design. In order to maintain a higher bandwidth as well as adequate phase margin, a slight modification of the external compensation is necessary. This can be easily implemented by increasing the leading capacitor value, Ca. In addition the ESR of the output capacitors also helps since the ESR and output capacitance forms a zero which also helps to boost the phase.

Table 4: C_A and Minimum ESR for Output Capacitors Ranges

Total C_{OUT} Range	Recommended C_A	Min ESR
100µF to 250µF	27pF	0
250µF to 450µF	33pF	0
450µF to 1000µF	47pF	>4mΩ

Table 5: Recommended Output Capacitors

Description	MFG	P/N
47µF, 6.3V, X7R, 1210	Murata	GRM32ER70J476ME20
	Taiyo Yuden	LMK325B7476KM-TR
47uF, 6.3V, X5R, 1206	Murata	GRM31CR60J476ME19L
	Taiyo Yuden	JMK316BJ476ML-T
22µF, 10V, X7R, 1206	Murata	GRM31CR71A226ME15
	Taiyo Yuden	LMK316AB7226KL-TR
	AVX	1206ZC226KAT2A
22 µF, 10V, X5R, 1206	Murata	GRM31CR61A226ME19L
	Taiyo Yuden	LMK316BJ226ML-T
22 µF, 10V, X5R, 0805	Murata	GRM219R61A226MEA0D
	Taiyo Yuden	LMK212BJ226MG-T
10µF, 10V, X7R, 0805	Murata	GRM21BR71A106KE51
	Taiyo Yuden	LMK212AB7106MG-T
	AVX	0805ZC106KAT2A

Low ESR ceramic capacitors are required with X5R/X7R rated dielectric formulation. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage.

Output ripple voltage is determined by the aggregate output capacitor impedance. Output impedance, denoted as Z, is comprised of effective series resistance, ESR, and effective series inductance, ESL:

Z = ESR + ESL

Placing output capacitors in parallel reduces the impedance and will hence result in lower PWM ripple voltage. In addition, higher output capacitance will improve overall regulation and ripple in light-load mode.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \ldots + \frac{1}{Z_n}$$

For best LLM performance, we recommend using just 2x47µF capacitors mentioned in the above table, and no 10µF capacitor.

The V_{OUT} sense point should be just after the last output filter capacitor right next to the device. Additional bulk output capacitance beyond the above recommendations can be used on the output node of the

EN6347QI as long as the bulk capacitors are far enough from the V_{OUT} sense point such that they don't interfere with the control loop operation.

Table 6: Typical PWM Ripple Voltages

Output Capacitor Configuration	Typical Output Ripple (mVp-p) (as measured on EN6347QI Evaluation Board)*
1 x 47 µF	25
47 µF + 10 µF	14

* Note: 20 MHz BW limit

Power-Up Sequencing

During power-up, ENABLE should not be asserted before PVIN, and PVIN should not be asserted before AVIN. It is recommended to enable the device after input voltage is stable.

Pre-Bias Start-up

The EN6347QI supports startup into a pre-biased output of up to 1.5V. The output of the EN6347QI can be pre-biased with a voltage up to 1.5V when it is first enabled.

THERMAL CONSIDERATIONS

Thermal considerations are important power supply design facts that cannot be avoided in the real world. Whenever there are power losses in a system, the heat that is generated by the power dissipation needs to be accounted for. The Enpirion PowerSoC helps alleviate some of those concerns.

The Enpirion EN6347QI DC-DC converter is packaged in a 4x7x1.85mm 38-pin QFN package. The QFN package is constructed with copper lead frames that have exposed thermal pads. The exposed thermal pad on the package should be soldered directly on to a copper ground pad on the printed circuit board (PCB) to act as a heat sink. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C may reduce long-term reliability. The device has a thermal overload protection circuit designed to turn off the device at an approximate junction temperature value of 160°C.

The following example and calculations illustrate the thermal performance of the EN6347QI.

Example:

V_{IN} = 5V

V_{OUT} = 3.3V

I_{OUT} = 4A

First calculate the output power.

P_{OUT} = 3.3V x 4A = 13.2W

Next, determine the input power based on the efficiency (η) shown in Figure 8.

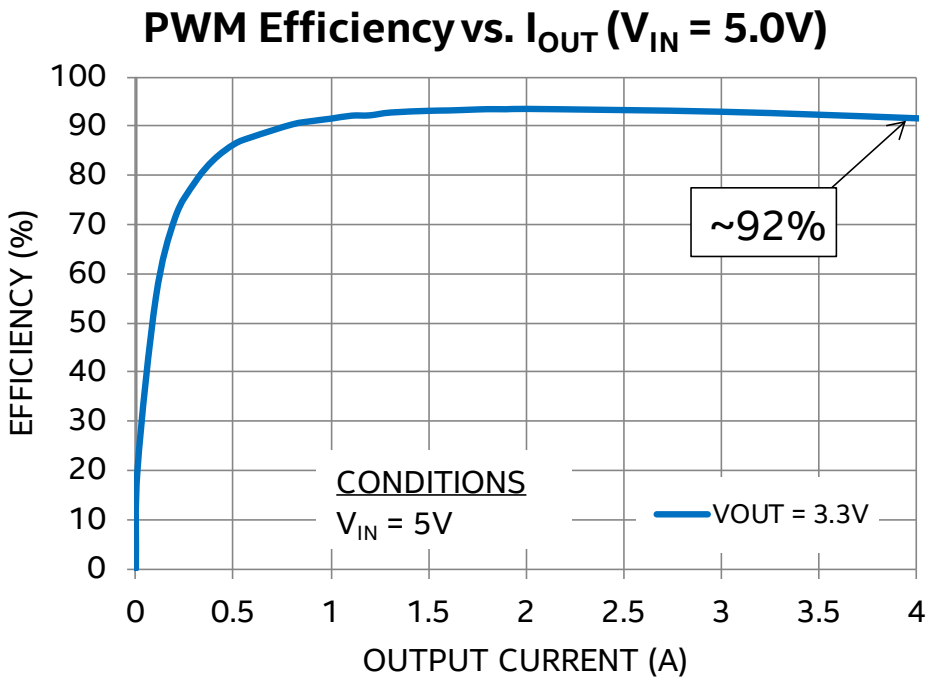


Figure 8: Efficiency vs. Output Current

For V_{IN} = 5V, V_{OUT} = 3.3V at 4A, η ≈ 92%

η = P_{OUT} / P_{IN} = 92% = 0.92

P_{IN} = P_{OUT} / η

P_{IN} ≈ 13.2W / 0.92 ≈ 14.35W

The power dissipation (P_D) is the power loss in the system and can be calculated by subtracting the output power from the input power.

P_D = P_{IN} – P_{OUT}

≈ 14.35W – 13.2W ≈ 1.148W

With the power dissipation known, the temperature rise in the device may be estimated based on the theta JA value (θ_{JA}). The θ_{JA} parameter estimates how much the temperature will rise in the device for every watt of power dissipation. The EN6347QI has a θ_{JA} value of 30 ºC/W without airflow.

Determine the change in temperature (ΔT) based on P_D and θ_{JA}.

ΔT = P_D x θ_{JA}

ΔT ≈ 1.148W x 30°C/W = 34.43°C ≈ 35°C

The junction temperature (T_J) of the device is approximately the ambient temperature (T_A) plus the change in temperature. We assume the initial ambient temperature to be 25°C.

T_J = T_A + ΔT

T_J ≈ 25°C + 35°C ≈ 60°C

The maximum operating junction temperature (T_{JMAX}) of the device is 125°C, so the device can operate at a higher ambient temperature. The maximum ambient temperature (T_{AMAX}) allowed can be calculated.

T_{AMAX} = T_{JMAX} – P_D x θ_{JA}

≈ 125°C – 35°C ≈ 90°C

The maximum ambient temperature (before de-rating) the device can reach is 90°C given the input and output conditions. Note that the efficiency will be slightly lower at higher temperatures and this calculation is an estimate.

APPLICATION CIRCUITS

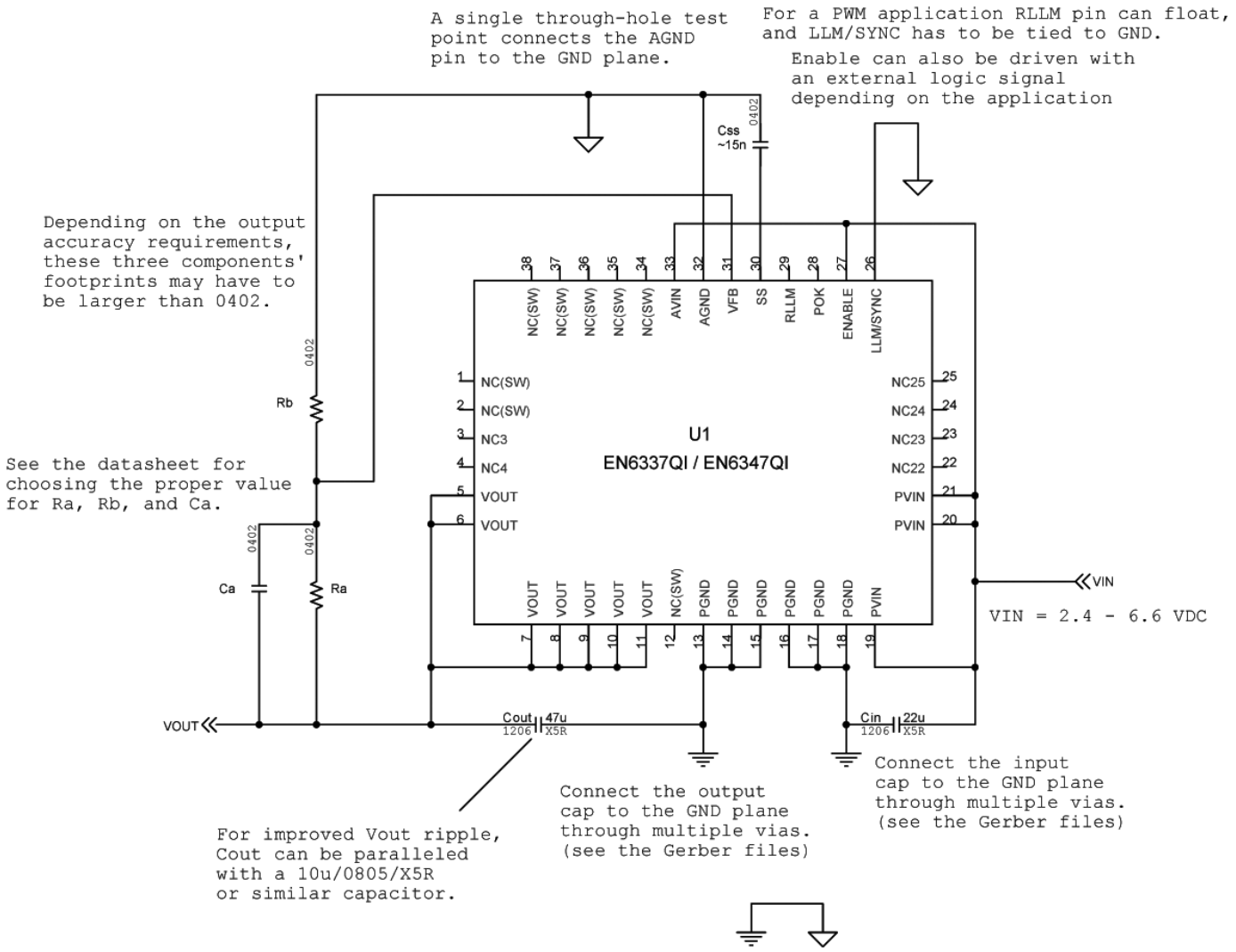


Figure 9: Engineering Schematic with Engineering Notes

LAYOUT RECOMMENDATIONS

Figure 9 shows critical components and layer 1 traces of a typical EN6347QI layout with ENABLE tied to V_{IN} in PWM mode. Alternate ENABLE configurations and other small signal pins need to be connected and routed according to specific customer application. Please see the Gerber files on the Altera website www.altera.com/powersoc for exact dimensions and other layers. Please refer to this Figure while reading the layout recommendations in this section.

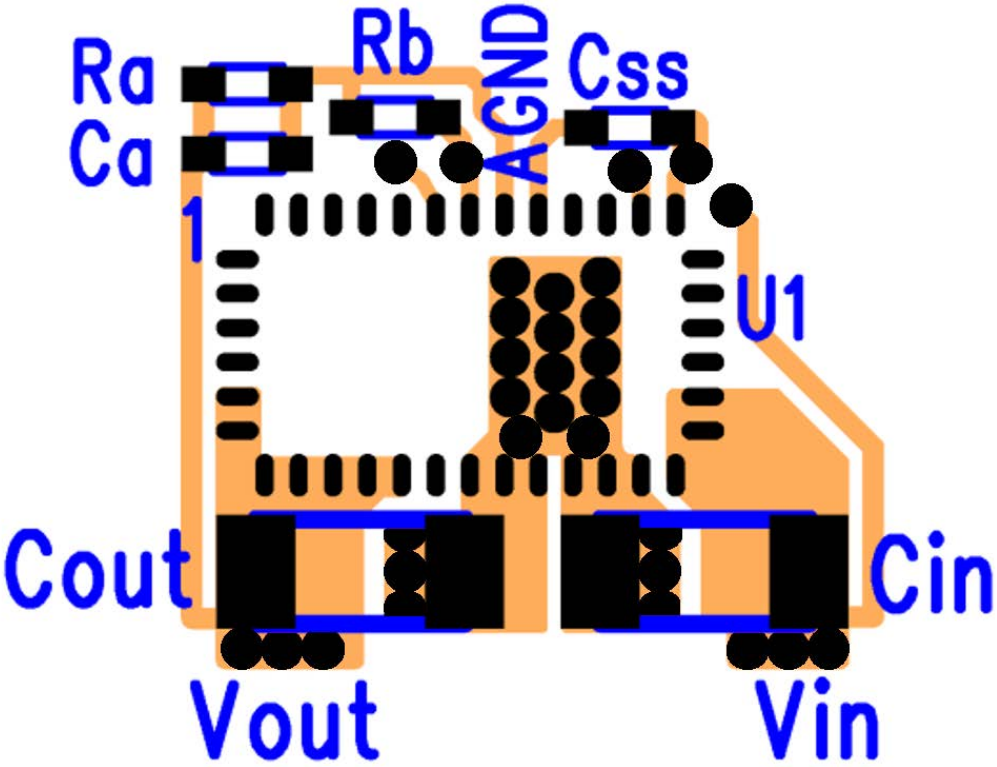


Figure 10: Top PCB Layer Critical Components and Copper for Minimum Footprint (Top View)

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EN6347QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EN6347QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: Three PGND pins are dedicated to the input circuit, and three to the output circuit. The slit in Figure 10 separating the input and output GND circuits helps minimize noise coupling between the converter input and output switching loops.

Recommendation 3: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors. Please see the Gerber files on the Altera website www.altera.com/powersoc.

Recommendation 4: The large thermal pad underneath the component must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter.

Recommendation 5: Multiple small vias (the same size as the thermal vias discussed in recommendation 4 should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias under the capacitors along the edge of the GND copper closest to the +V copper. Please see Figure 10. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops. If the vias cannot be placed under C_{IN} and C_{OUT}, then put them just outside the capacitors along the GND slit separating the two components. Do not use thermal reliefs or spokes to connect these vias to the ground plane.

Recommendation 6: AVIN is the power supply for the internal small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 10 this connection is made at the input capacitor close to the V_{IN} connection.

Recommendation 7: The layer 1 metal under the device must not be more than shown in Figure 10. See the section regarding exposed metal on bottom of package. As with any switch-mode DC/DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

Recommendation 8: The V_{OUT} sense point should be just after the last output filter capacitor. Keep the sense trace as short as possible in order to avoid noise coupling into the control loop.

Recommendation 9: Keep R_A, C_A, and R_B close to the VFB pin (see Figures 7). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect R_B directly to the AGND pin instead of going through the GND plane.

DESIGN CONSIDERATIONS FOR LEAD-FRAME BASED MODULES

Exposed Metal on Bottom of Package

Lead-frames offer many advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. However, they do require some special considerations.

In the assembly process lead frame construction requires that, for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package, as shown in Figure 11.

Only the thermal pad and the perimeter pads are to be mechanically or electrically connected to the PC board. The PCB top layer under the EN6347QI should be clear of any metal (copper pours, traces, or vias) except for the thermal pad. The “shaded-out” area in Figure 11 represents the area that should be clear of any metal on the top layer of the PCB. Any layer 1 metal under the shaded-out area runs the risk of undesirable shorted connections even if it is covered by soldermask.

The solder stencil aperture should be smaller than the PCB ground pad. This will prevent excess solder from causing bridging between adjacent pins or other exposed metal under the package.

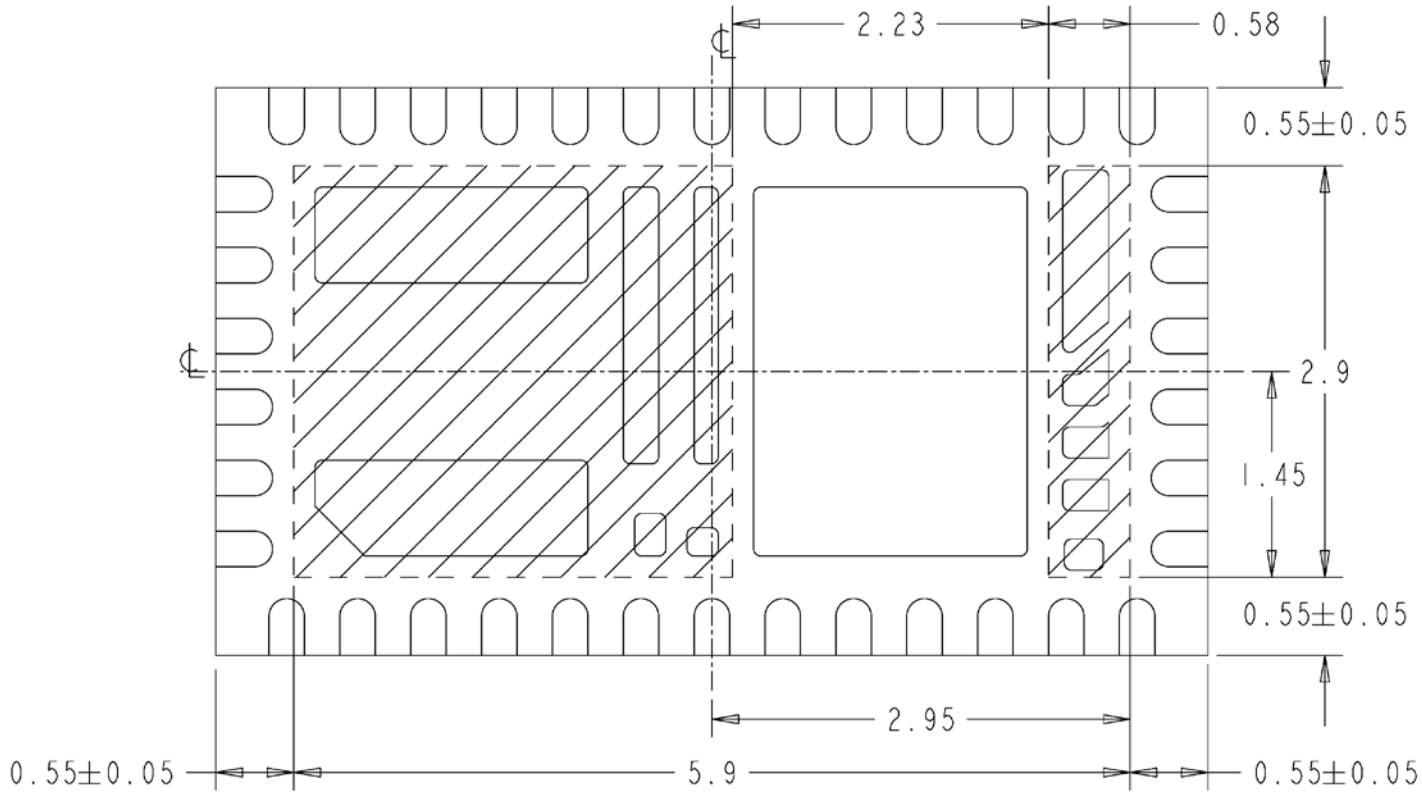


Figure 11: Lead-Frame exposed metal (Bottom View)

Shaded area highlights exposed metal that is not to be mechanically or electrically connected to the PCB.

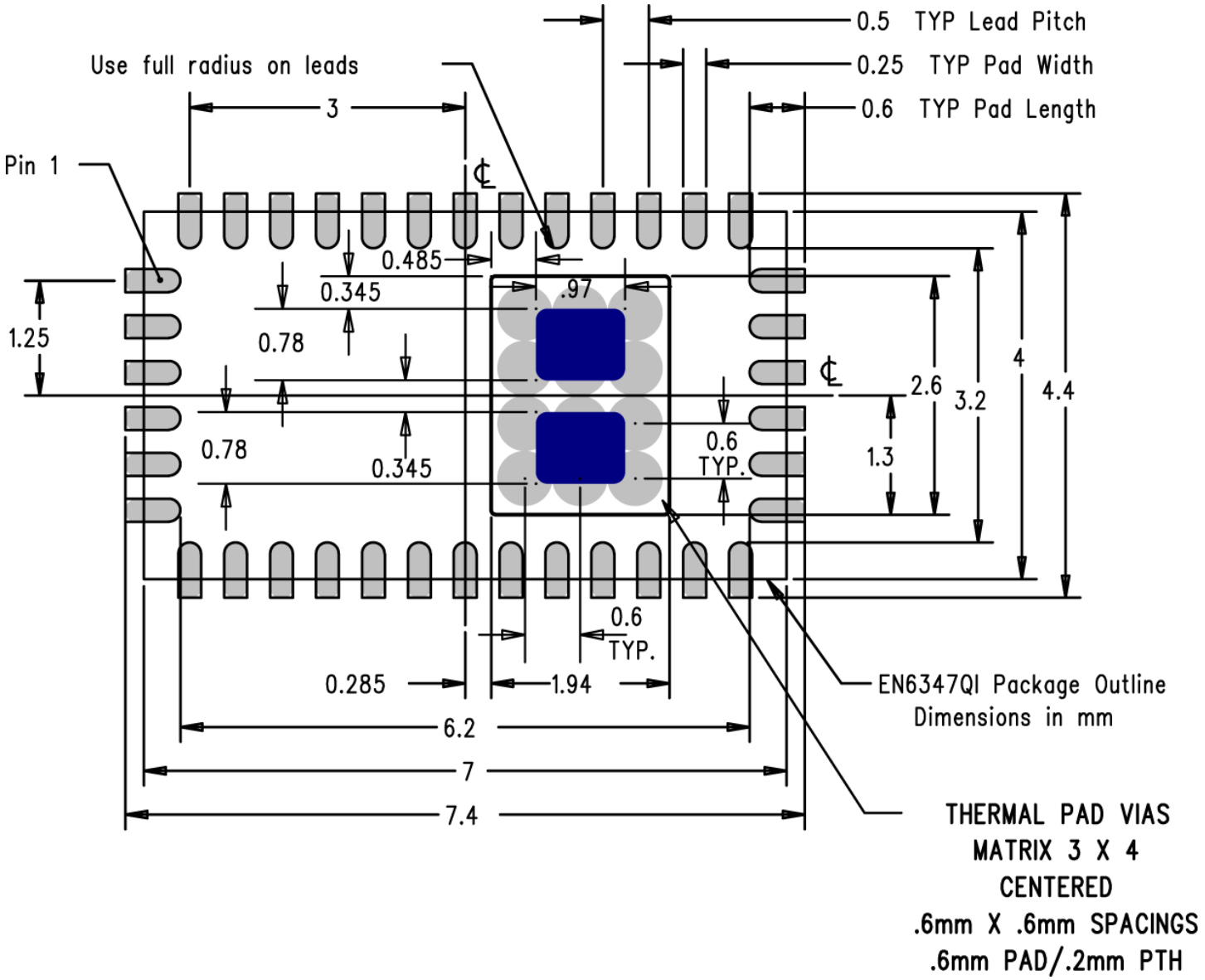


Figure 12: EN6347QI PCB Footprint (Top View)

The solder stencil aperture for the thermal pad is shown in blue and is based on Enpirion power product manufacturing specifications.

PACKAGE DIMENSIONS

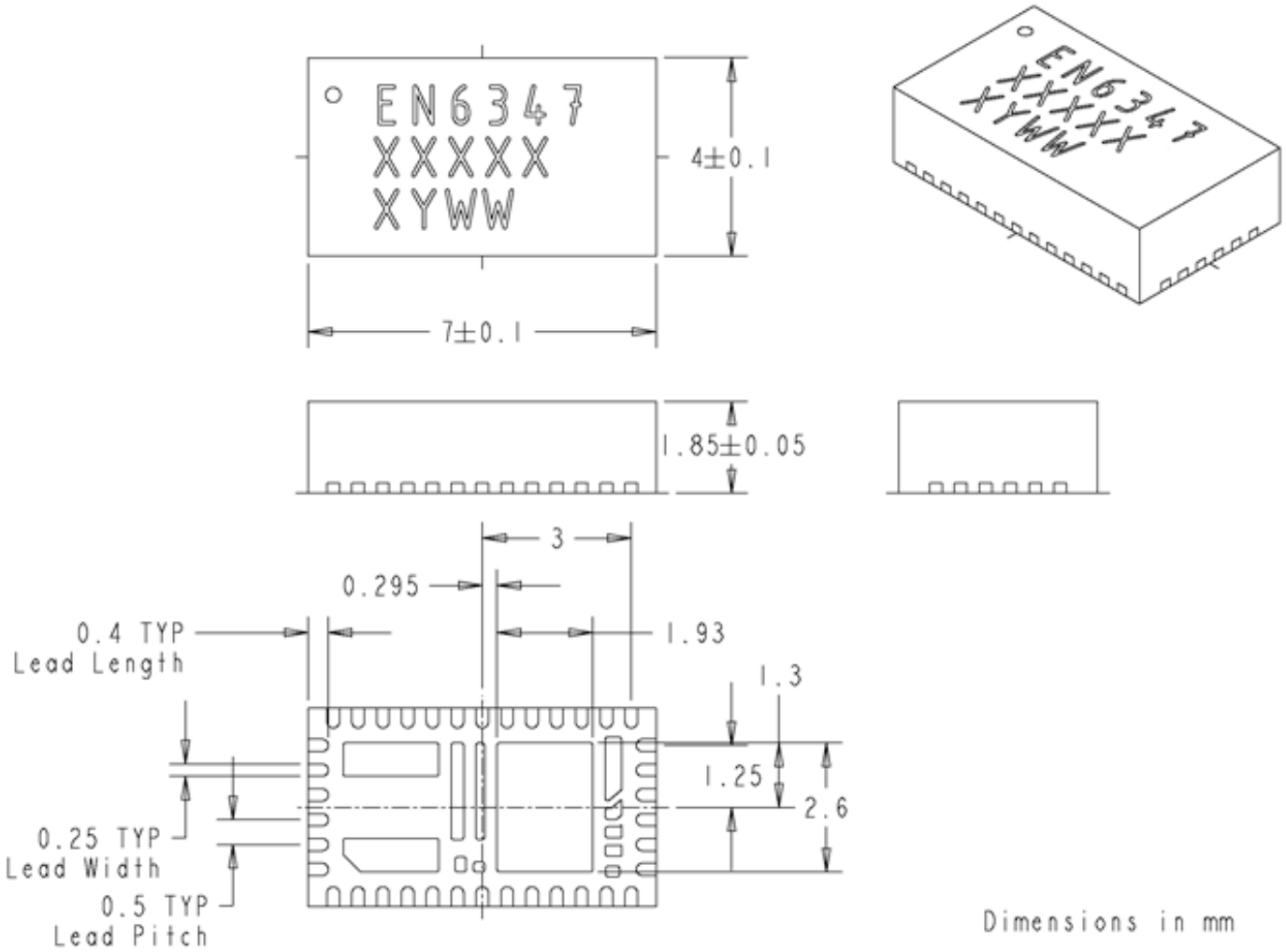


Figure 13: EN6347QI Package Dimensions

Packing and Marking Information: https://www.altera.com/support/quality-and-reliability/packing.html

REVISION HISTORY

Rev	Date	Change(s)
J	April, 2018	Changed datasheet into Intel format.
K	August, 2018	Correct some typos

WHERE TO GET MORE INFORMATION

For more information about Intel® and Enpirion® PowerSoCs, visit:

www.altera.com/enpirion

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