

## ISL6840, ISL6841, ISL6842, ISL6843, ISL6844

Improved Industry Standard Single-Ended Current Mode PWM Controller

The [ISL6840](#), [ISL6841](#), [ISL6842](#), [ISL6843](#), and [ISL6844](#) (ISL684x) family of adjustable frequency, low power, Pulse-Width Modulating (PWM) current mode controllers is designed for a wide range of power conversion applications including boost, flyback, and isolated output configurations. Peak current mode control effectively handles power transients and provides inherent overcurrent protection.

This advanced BiCMOS design is pin-compatible with the industry standard 384x family of controllers and offers significantly improved performance. Features include low operating current, 60µA start-up current, adjustable operating frequency to 2MHz, and high peak current drive capability with 20ns rise and fall times.

Part Number	Rising UVLO (V)	MAX. Duty Cycle (%)
ISL6840	7.0	100
ISL6841	7.0	50
ISL6842	14.4	100
ISL6843	8.4	100
ISL6844	14.4	50

### Related Literature

For a full list of related documents, visit our website:

[ISL6840](#), [ISL6841](#), [ISL6842](#), [ISL6843](#), [ISL6844](#) device pages

### Features

- 1A MOSFET gate driver
- 60µA start-up current, 100µA maximum
- 25ns propagation delay current sense to output
- Fast transient response with peak current mode control
- Adjustable switching frequency to 2MHz
- 20ns rise and fall times with 1nF output load
- Trimmed timing capacitor discharge current for accurate deadtime/maximum duty cycle control
- High bandwidth error amplifier
- Tight tolerance voltage reference over line, load, and temperature
- Tight tolerance current limit threshold
- Pb-free available (RoHS compliant)

### Applications

- Telecom and datacom power
- Wireless base station power
- File server power
- Industrial power systems
- PC power supplies
- Isolated buck and flyback regulators
- Boost regulators

# 1. Overview

## 1.1 Typical Applications

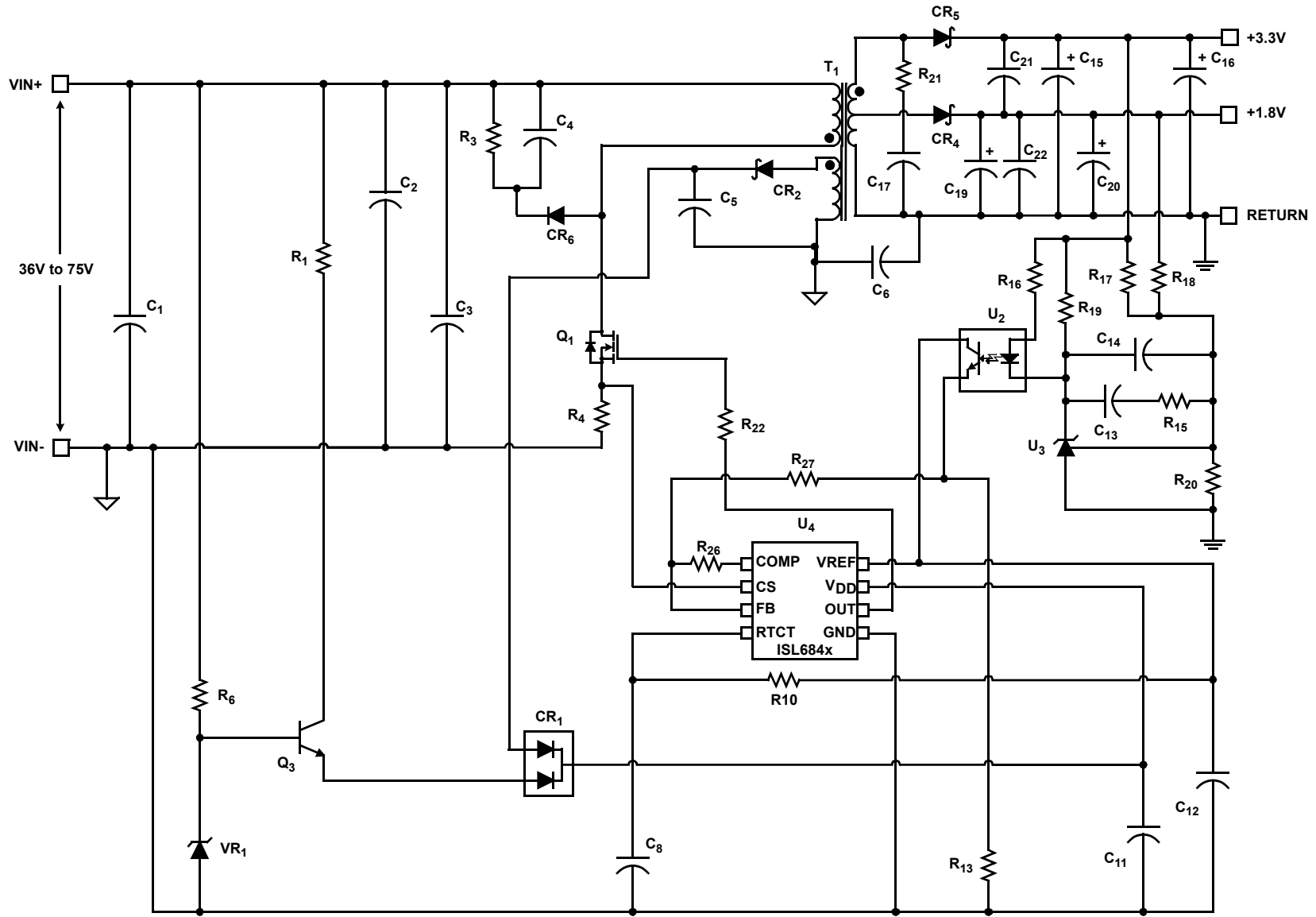


Figure 1. 48V Input Dual Output Flyback

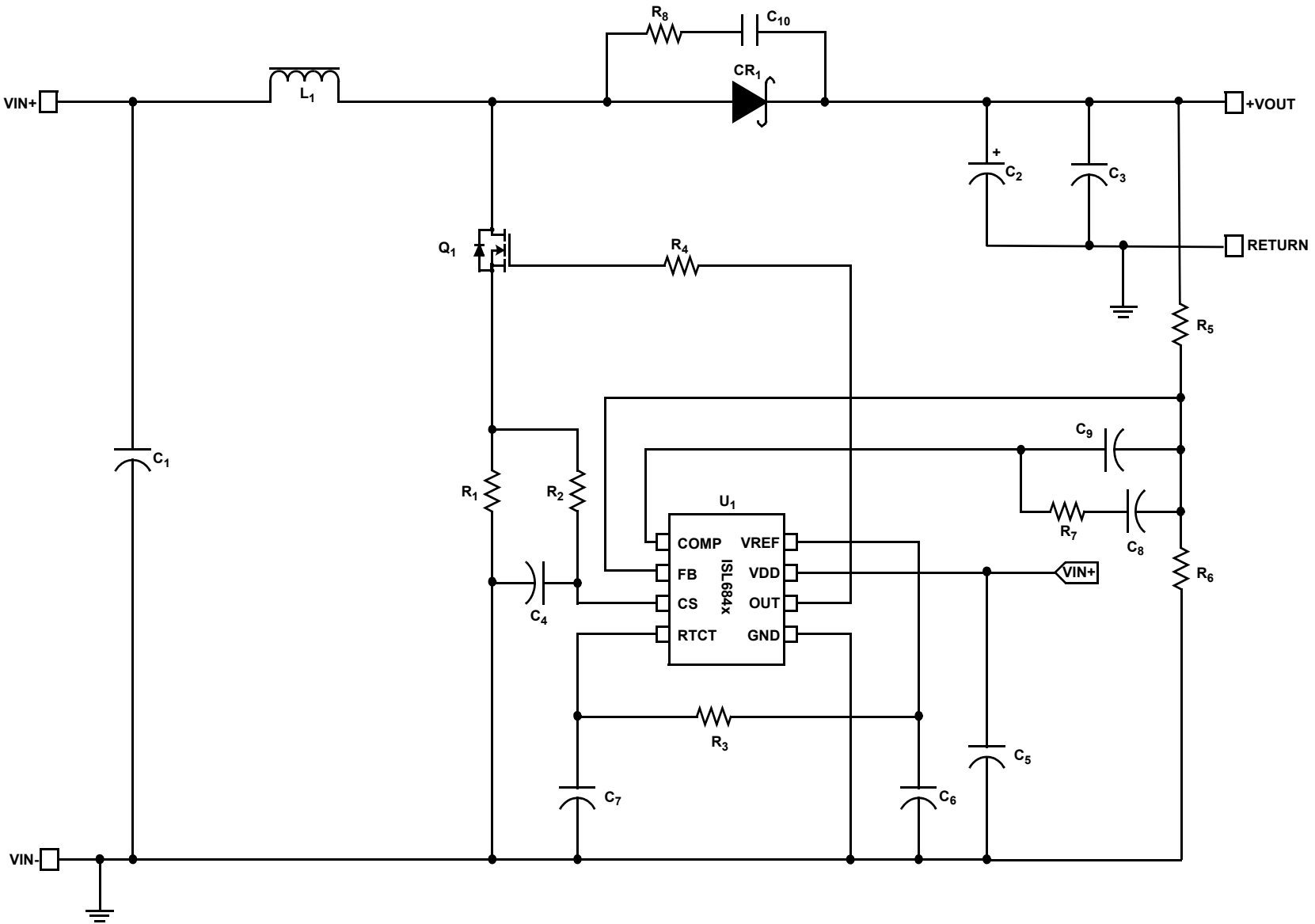


Figure 2. Boost Converter

## 1.2 Functional Block Diagram

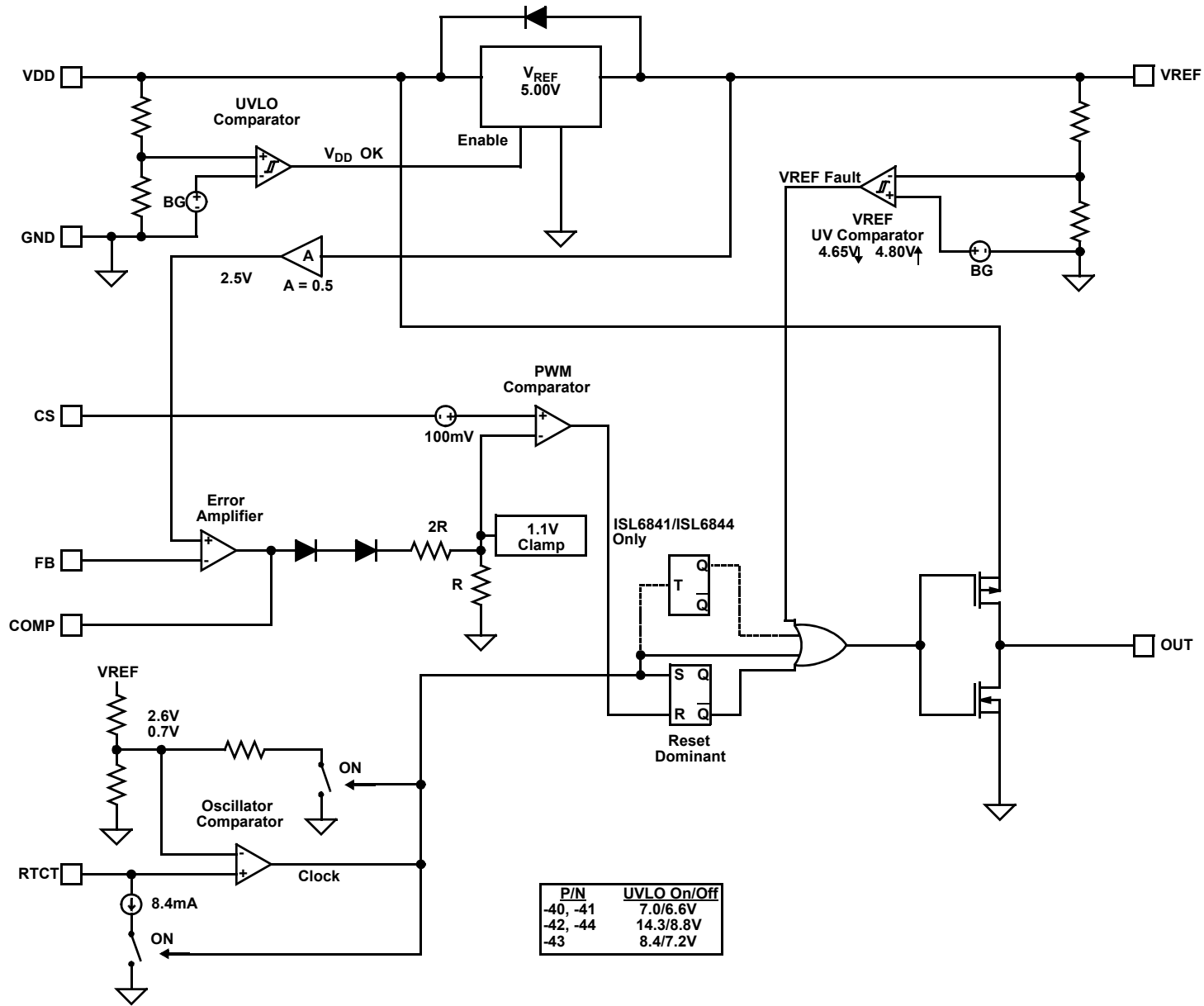


Figure 3. Block Diagram

### 1.3 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Temp Range (°C)	Tape and Reel (Units) (Note 1)	Package	Pkg. Dwg. #
ISL6840IBZ-T	6840 IBZ	-40 to +105	2.5k	8 Ld SOIC	M8.15
ISL6840IRZ-T	40Z	-40 to +105	6k	8 Ld 2x3 DFN	L8.2x3
ISL6840IUZ	6840Z	-40 to +105	-	8 Ld MSOP	M8.118
ISL6840IUZ-T	6840Z	-40 to +105	2.5k	8 Ld MSOP	M8.118
ISL6841IUZ (No longer available, recommended replacement: ISL8841AAUZ)	6841Z	-40 to +105	-	8 Ld MSOP	M8.118
ISL6841IUZ-T (No longer available, recommended replacement: ISL8841AAUZ-T)	6841Z	-40 to +105	2.5k	8 Ld MSOP	M8.118
ISL6842IBZ	6842 IBZ	-40 to +105	-	8 Ld SOIC	M8.15
ISL6842IBZ-T	6842 IBZ	-40 to +105	2.5k	8 Ld SOIC	M8.15
ISL6843IBZ	6843 IBZ	-40 to +105	-	8 Ld SOIC	M8.15
ISL6843IBZ-T	6843 IBZ	-40 to +105	2.5k	8 Ld SOIC	M8.15
ISL6843IUZ	6843Z	-40 to +105	-	8 Ld MSOP	M8.118
ISL6843IUZ-T	6843Z	-40 to +105	2.5k	8 Ld MSOP	M8.118
ISL6844IBZ (No longer available, recommended replacement: ISL8844AABZ)	6844 IBZ	-40 to +105	-	8 Ld SOIC	M8.15
ISL6841EVAL3Z (No longer available or supported)	Evaluation Board				

Notes:

- See [TB347](#) for details about reel specifications.
- These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
- For Moisture Sensitivity Level (MSL), see the [ISL6840](#), [ISL6841](#), [ISL6842](#), [ISL6843](#), and [ISL6844](#) device information pages. For more information about MSL, see [TB363](#).

### 1.4 Pin Configurations



## 1.5 Pin Descriptions

Pin Number	Pin Name	Description
1	COMP	The error amplifier output and the PWM comparator input. The control loop frequency compensation network is connected between the COMP and FB pins.
2	FB	The output voltage feedback is connected to the inverting input of the error amplifier through this pin. The non-inverting input of the error amplifier is internally tied to a reference voltage.
3	CS	The current sense input to the PWM comparator. The input signal range is nominally 0V to 1.0V and has an internal offset of 100mV.
4	RTCT	<p>The oscillator timing control pin. The operational frequency and maximum duty cycle are set by connecting a resistor, RT, between VREF and this pin and a timing capacitor, CT, from this pin to GND. The oscillator produces a sawtooth waveform with a programmable frequency range up to 2.0MHz. The charge time, t<sub>C</sub>, the discharge time, t<sub>D</sub>, the switching frequency, f, and the maximum duty cycle, D<sub>max</sub>, can be calculated from <a href="#">Equations 1, 2, 3 and 4</a>:</p> <p>(EQ. 1) <math>t_C \approx 0.583 \cdot RT \cdot CT</math></p> <p>(EQ. 2) <math>t_D \approx -RT \cdot CT \cdot \ln\left(\frac{0.0083 \cdot RT - 4.3}{0.0083 \cdot RT - 2.4}\right)</math></p> <p>(EQ. 3) <math>f = 1/(t_C + t_D)</math></p> <p>(EQ. 4) <math>D = t_C \cdot f</math></p> <p><a href="#">Figure 7 on page 10</a> can be used as a guideline in selecting the capacitor and resistor values required for a given frequency.</p>
5	GND	The power and small signal reference ground for all functions.
6	OUT	The drive output to the power switching device. It is a high current output capable of driving the gate of a power MOSFET with peak currents of 1.0A.
7	VDD	<p>The power connection for the devices. The total supply current depends on the load applied to OUT. Total I<sub>DD</sub> current is the sum of the operating current and the average output current. Knowing the operating frequency, f, and the MOSFET gate charge, Q<sub>g</sub>, the average output current can be calculated in <a href="#">Equation 5</a>:</p> <p>(EQ. 5) <math>I_{OUT} = Q_g \times f</math></p> <p>To optimize noise immunity, bypass V<sub>DD</sub> to GND with a ceramic capacitor as close to the VDD and GND pins as possible.</p>
8	VREF	The 5V reference voltage output. +1.0/-1.5% tolerance over line, load, and operating temperature. Bypass to GND with a 0.1μF to 3.3μF capacitor to filter this output as needed.

## 2. Specifications

### 2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Supply Voltage, $V_{DD}$	GND - 0.3	+20.0	V
OUT	GND - 0.3	$V_{DD} + 0.3$	V
Signal Pins	GND - 0.3	6.0	V
Peak GATE Current		1	A

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

### 2.2 Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
DFN Package ( <a href="#">Notes 5, 7</a> )	55	6
SOIC Package ( <a href="#">Notes 4, 6</a> )	100	60
MSOP Package ( <a href="#">Notes 4, 6</a> )	165	62

Notes:

- $\theta_{JA}$  is measured with the component mounted on a high-effective thermal conductivity test board in free air. See [TB379](#) for details.
- For  $\theta_{JC}$ , the "case temp" location is the center of the exposed metal pad on the package underside.
- For  $\theta_{JC}$ , the "case temp" location is taken at the package top center.
- $\theta_{JA}$  is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See [TB379](#).

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature	-55	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see <a href="#">TB493</a>		

### 2.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
<b>Supply Voltage Range (Typical, <a href="#">Note 8</a>)</b>			
ISL6840, ISL6841	7.5	14	V
ISL6843	9	16	V
ISL6842, ISL6844	15	18	V
<b>Temperature Range</b>			
ISL684xIx	-40	+105	°C

Note:

- All voltages are with respect to GND

## 2.4 Electrical Specifications

Recommended operating conditions unless otherwise noted. See [Functional Block Diagram](#) and [Typical Applications](#) schematics.  $V_{DD} = 15V$  ([Note 12](#)),  $R_t = 10k\Omega$ ,  $C_t = 3.3nF$ ,  $T_A = -40^\circ C$  to  $+105^\circ C$ , Typical values are at  $T_A = +25^\circ C$ . **Boldface limits apply across the operating temperature range,  $-40^\circ C$  to  $+105^\circ C$ .**

Parameter	Test Conditions	Min ( <a href="#">Note 9</a> )	Typ	Max ( <a href="#">Note 9</a> )	Unit
<b>Undervoltage Lockout</b>					
START Threshold (ISL6840, ISL6841)		<b>6.5</b>	7.0	<b>7.5</b>	V
START Threshold (ISL6843)		<b>7.8</b>	8.4	<b>9.0</b>	V
START Threshold (ISL6842, ISL6844)		<b>13.3</b>	14.3	<b>15.3</b>	V
STOP Threshold (ISL6840, ISL6841)		<b>6.1</b>	6.6	<b>6.9</b>	V
STOP Threshold (ISL6843)		<b>6.7</b>	7.2	<b>7.7</b>	V
STOP Threshold (ISL6842, ISL6844)		<b>8.0</b>	8.8	<b>9.6</b>	V
Hysteresis (ISL6840, ISL6841)			0.4		V
Hysteresis (ISL6843)			0.8		V
Hysteresis (ISL6842, ISL6844)			5.4		V
Start-Up Current, $I_{DD}$	$V_{DD} < \text{START threshold}$		60	<b>100</b>	$\mu A$
Operating Current, $I_{DD}$	<a href="#">(Note 10)</a>		3.3	<b>4.0</b>	mA
Operating Supply Current, $I_D$	Includes 1nF GATE loading		4.1	<b>5.5</b>	mA
<b>Reference Voltage</b>					
Overall Accuracy	Over line ( $V_{DD} = 12V$ to $18V$ ), load, temperature	<b>4.925</b>	5.000	<b>5.050</b>	V
Long Term Stability	$T_A = +125^\circ C$ , 1000 hours ( <a href="#">Note 11</a> )		5		mV
Fault Voltage		<b>4.40</b>	4.65	<b>4.85</b>	V
VREF Good Voltage		<b>4.60</b>	4.80	<b>VREF - 0.05</b>	V
Hysteresis		<b>50</b>	165	<b>250</b>	mV
Current Limit, Sourcing		<b>-20</b>			mA
Current Limit, Sinking		<b>5</b>			mA
<b>Current Sense</b>					
Input Bias Current	$V_{CS} = 1V$	<b>-1.0</b>		<b>1.0</b>	$\mu A$
CS Offset Voltage	$V_{CS} = 0V$ ( <a href="#">Note 11</a> )	<b>95</b>	100	<b>105</b>	mV
COMP to PWM Comparator Offset Voltage	$V_{CS} = 0V$ ( <a href="#">Note 11</a> )	<b>0.80</b>	1.15	<b>1.30</b>	V
Input Signal, Maximum		<b>0.91</b>	0.97	<b>1.03</b>	V
Gain, $A_{CS} = \Delta V_{COMP}/\Delta V_{CS}$	$0 < V_{CS} < 910mV$ , $V_{FB} = 0V$ ( <a href="#">Note 11</a> )	<b>2.5</b>	3.0	<b>3.5</b>	V/V
CS to OUT Delay	<a href="#">(Note 11)</a>		25	<b>40</b>	ns
<b>Error Amplifier</b>					
Open-Loop Voltage Gain	<a href="#">(Note 11)</a>	<b>60</b>	90		dB
Reference Voltage	$V_{FB} = V_{COMP}$	<b>2.475</b>	2.514	<b>2.55</b>	V
FB Input Bias Current	$V_{FB} = 0V$	<b>-1.0</b>	-0.2	<b>1.0</b>	$\mu A$
COMP Sink Current	$V_{COMP} = 1.5V$ , $V_{FB} = 2.7V$	<b>1.0</b>			mA
COMP Source Current	$V_{COMP} = 1.5V$ , $V_{FB} = 2.3V$	<b>-0.4</b>			mA
COMP $V_{OH}$	$V_{FB} = 2.3V$	<b>4.80</b>		<b>VREF</b>	V
COMP $V_{OL}$	$V_{FB} = 2.7V$	<b>0.4</b>		<b>1.0</b>	V
PSRR	Frequency = 120Hz, $V_{DD} = 12V$ to $18V$ ( <a href="#">Note 11</a> )	<b>60</b>	80		dB
<b>Oscillator</b>					
Frequency Accuracy	Initial, $T_J = +25^\circ C$	<b>49</b>	52	<b>55</b>	kHz
Frequency Variation with $V_{DD}$	$T = +25^\circ C$ ( $f_{18V} - f_{12V}$ )/ $f_{12V}$		0.2	<b>1.0</b>	%
Temperature Stability	<a href="#">(Note 11)</a>		-	<b>5</b>	%



Recommended operating conditions unless otherwise noted. See [Functional Block Diagram](#) and [Typical Applications](#) schematics.  $V_{DD} = 15V$  ([Note 12](#)),  $R_t = 10k\Omega$ ,  $C_t = 3.3nF$ ,  $T_A = -40^\circ C$  to  $+105^\circ C$ , Typical values are at  $T_A = +25^\circ C$ . **Boldface limits apply across the operating temperature range,  $-40^\circ C$  to  $+105^\circ C$ .** (Continued)

Parameter	Test Conditions	Min ( <a href="#">Note 9</a> )	Typ	Max ( <a href="#">Note 9</a> )	Unit
Amplitude, Peak-to-Peak			1.9		V
RTCT Discharge Voltage			0.7		V
Discharge Current	RTCT = 2.0V	<b>7.2</b>	8.4	<b>9.5</b>	mA
<b>Output</b>					
Gate VOH	$V_{DD}$ to OUT, $I_{OUT} = -200mA$		1.0	<b>2.0</b>	V
Gate VOL	OUT to GND, $I_{OUT} = 200mA$		1.0	<b>2.0</b>	V
Peak Output Current	$C_{OUT} = 1nF$ ( <a href="#">Note 11</a> )		1.0		A
Rise Time	$C_{OUT} = 1nF$ ( <a href="#">Note 11</a> )		20	<b>40</b>	ns
Fall Time	$C_{OUT} = 1nF$ ( <a href="#">Note 11</a> )		20	<b>40</b>	ns
<b>PWM</b>					
Maximum Duty Cycle	ISL6840, ISL6842, ISL6843	<b>94</b>	96		%
	ISL6841, ISL6844	<b>47</b>	48		%
Minimum Duty Cycle	ISL6840, ISL6842, ISL6843			<b>0</b>	%
	ISL6841, ISL6844			<b>0</b>	%

## Notes:

9. Parameters with MIN and/or MAX limits are 100% tested at  $+25^\circ C$ , unless otherwise specified. Temperature limits established by characterization and are not production tested.
10. This is the  $V_{DD}$  current consumed when the device is active but not switching. Does not include gate drive current.
11. Limits established by characterization and are not production tested.
12. Adjust  $V_{DD}$  above the start threshold and then lower to 15V.

### 3. Typical Performance Curves

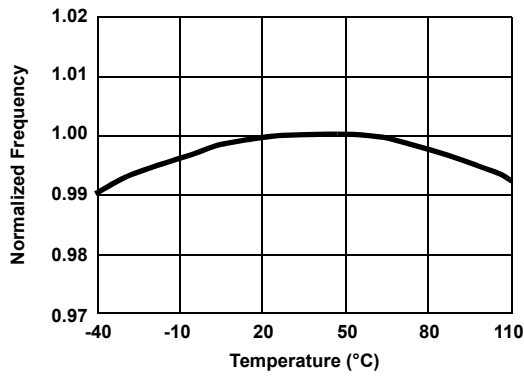


Figure 4. Frequency vs Temperature

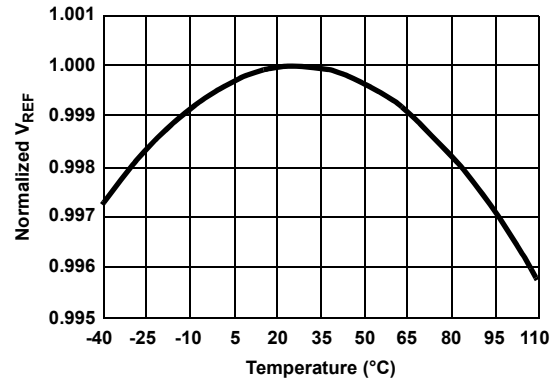


Figure 5. Reference Voltage vs Temperature

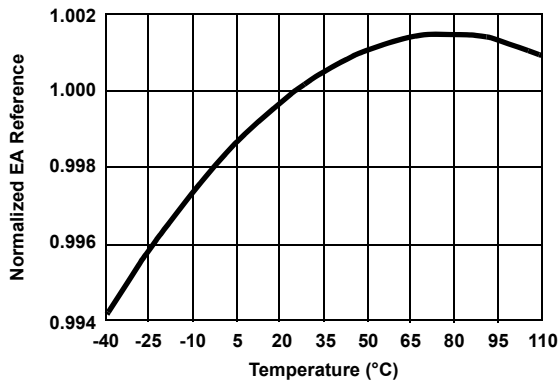


Figure 6. EA Reference vs Temperature

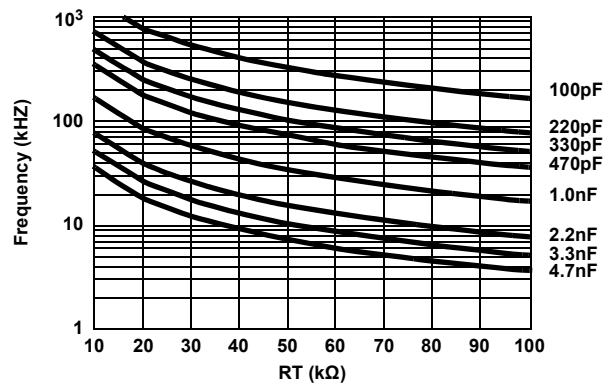


Figure 7. Resistance for CT Capacitor Values Given

## 4. Functional Description

### 4.1 Features

The ISL684x current mode PWMs make an ideal choice for low-cost flyback and forward topology applications. With its greatly improved performance over industry standard parts, it is the obvious choice for new designs or existing designs which require updating.

### 4.2 Oscillator

The ISL684x family of controllers have a sawtooth oscillator with a programmable frequency range to 2MHz, which can be programmed with a resistor from VREF and a capacitor to GND on the RTCT pin. (See [Figure 7 on page 10](#) for the resistor and capacitance required for a given frequency.)

### 4.3 Soft-Start Operation

Soft-start must be implemented externally. [Figure 8](#) shows one method that clamps the voltage on COMP.

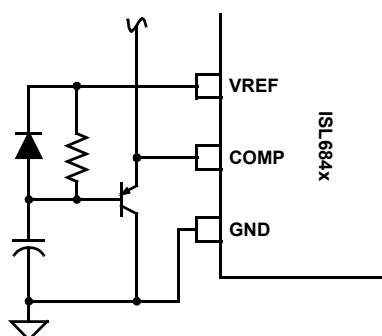


Figure 8. Soft-Start

### 4.4 Gate Drive

The ISL684x family is capable of sourcing and sinking 1A peak current. To limit the peak current through the ICs, an optional external resistor can be placed between the totem-pole output of the IC (OUT pin) and the gate of the MOSFET. This small series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the FET's input capacitance.

### 4.5 Slope Compensation

For applications where the maximum duty cycle is less than 50%, slope compensation can be used to improve noise immunity, particularly at lighter loads. The amount of slope compensation required for noise immunity is determined empirically, but is generally about 10% of the full scale current feedback signal. For applications where the duty cycle is greater than 50%, slope compensation is required to prevent instability. The minimum amount of slope compensation required corresponds to 1/2 the inductor downslope. Adding excessive slope compensation, however, results in a control loop that behaves more as a voltage mode controller than as a current mode controller.

Slope compensation may be added to the CS signal shown in [Figure 10 on page 12](#).

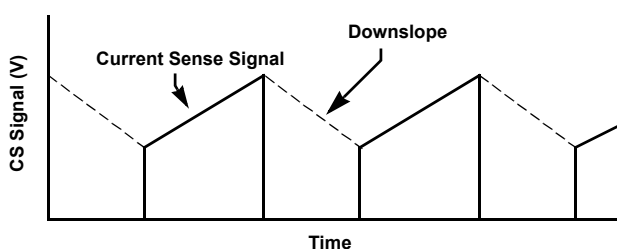


Figure 9. Current Sense Downslope

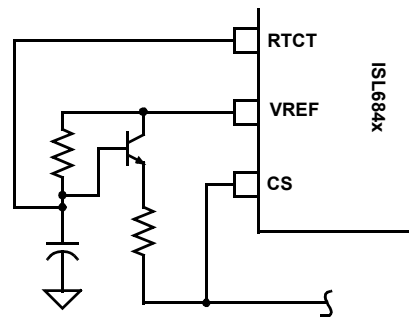


Figure 10. Slope Compensation

#### 4.6 Fault Conditions

A fault condition occurs if VREF falls below 4.65V. When a fault is detected, OUT is disabled. When VREF exceeds 4.80V, the fault condition clears, and OUT is enabled.

#### 4.7 Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stage. Bypass  $V_{DD}$  directly to GND with good high-frequency capacitors.

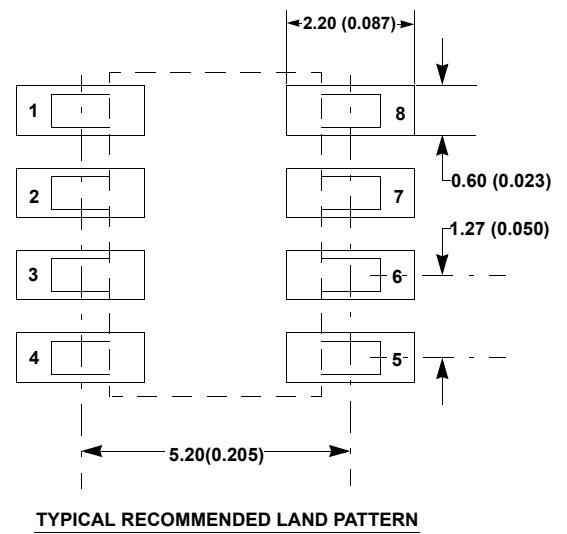
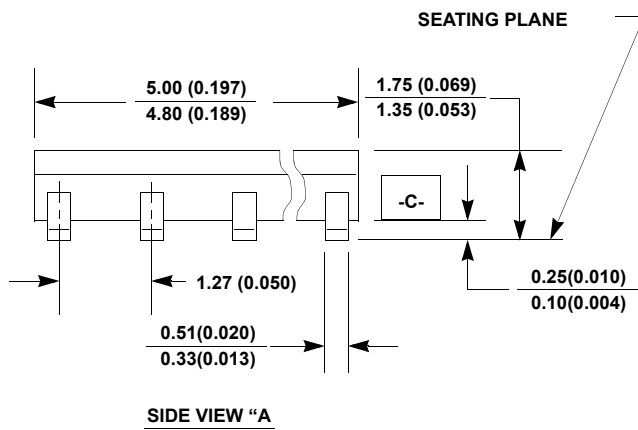
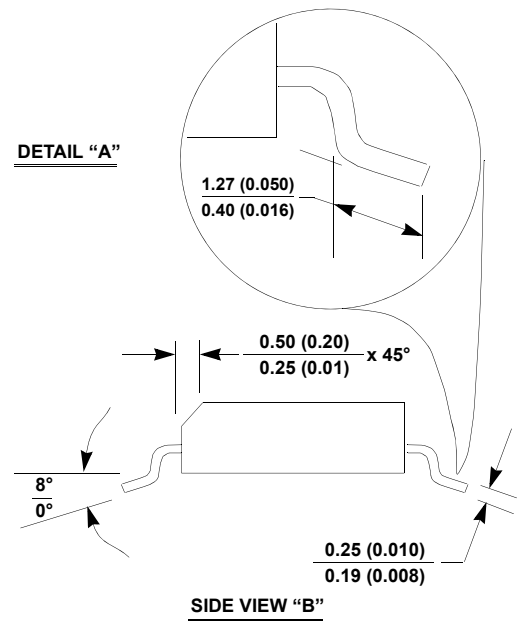
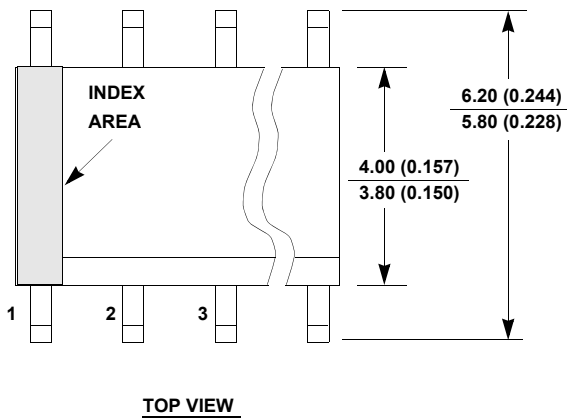
## 5. Revision History

Rev.	Date	Description
14	Jul.22.19	<p>Applied new formatting and template.            Added Related Literature section            Updated Ordering Information table by adding tape and reel information, removing retired parts, and updating notes.            Removed Note 2.            Updated Theta JA for DFN package changed from 77 to 55.            Updated Theta JC for SOIC package changed from N/A to 60.            Added Note 8 and updated references.            Removed ISL6843C information from document.            Removed ISL6845 information from document.            Updated the disclaimer.</p>
13	Feb.18.16	-Updated Ordering Information table on page 5
12	Sep.29.15	<ul style="list-style-type: none"> <li>- Updated Ordering Information Table on page 5.</li> <li>- Added Revision History.</li> <li>- Added About Intersil Verbiage.</li> <li>- Updated POD L8.2X3 to latest revision changes are as follow:               <ul style="list-style-type: none"> <li>-Revision 1 to Revision 2 Changes:</li> <li>Tiebar Note 5 updated</li> <li>From: Tiebar shown (if present) is a non-functional feature.</li> <li>To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).</li> </ul> </li> </ul>

### 6. Package Outline Drawings

For the most recent package outline drawing, see [M8.15](#).

M8.15  
 8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE  
 Rev 4, 1/12

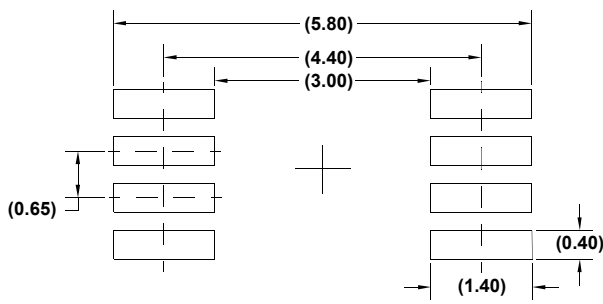
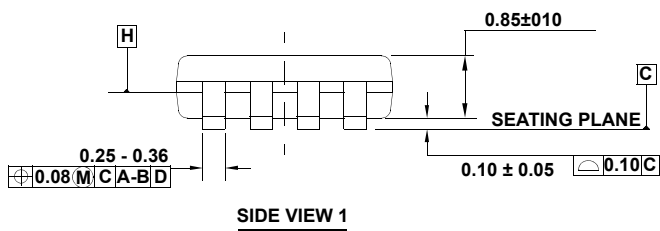
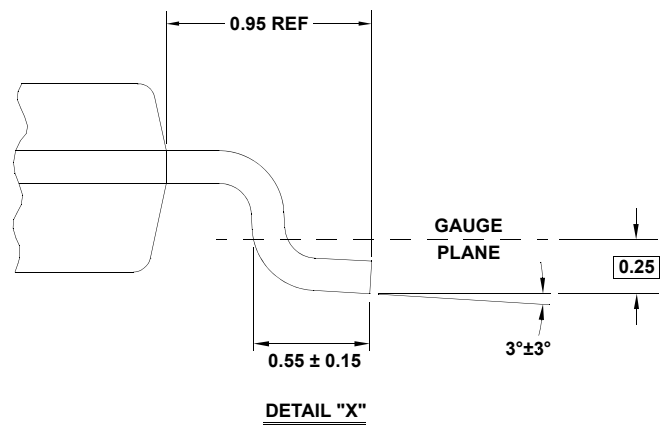
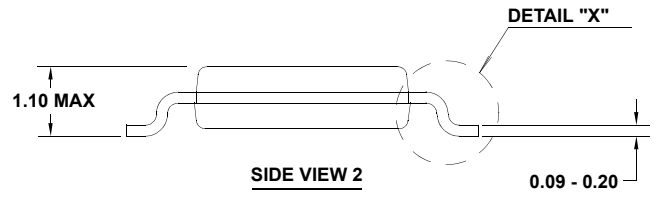
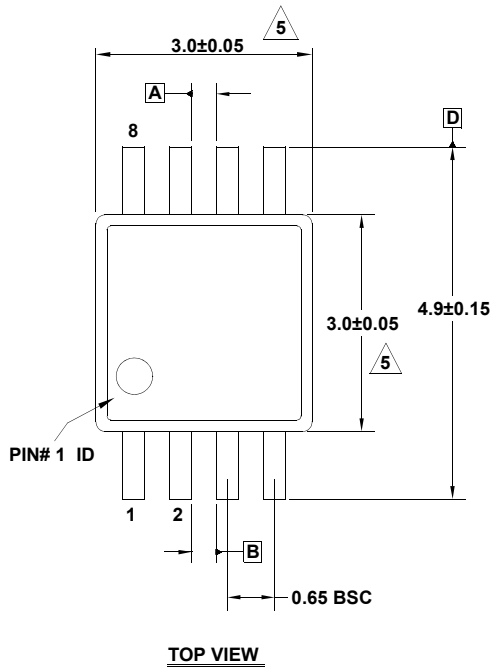


**Notes:**

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the

M8.118  
 8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE  
 Rev 4, 7/11

For the most recent package outline drawing, see [M8.118](#).

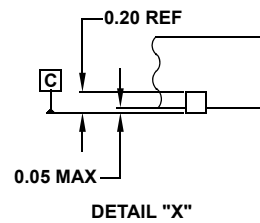
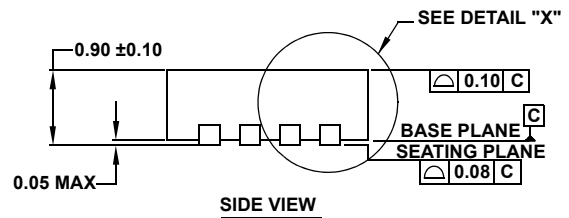
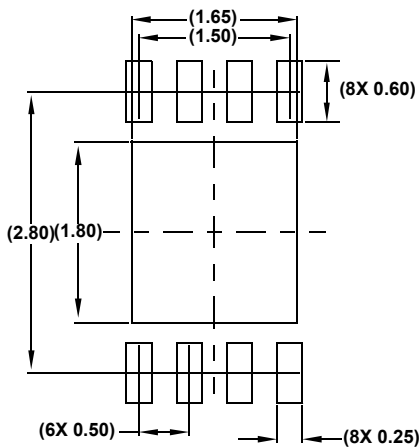
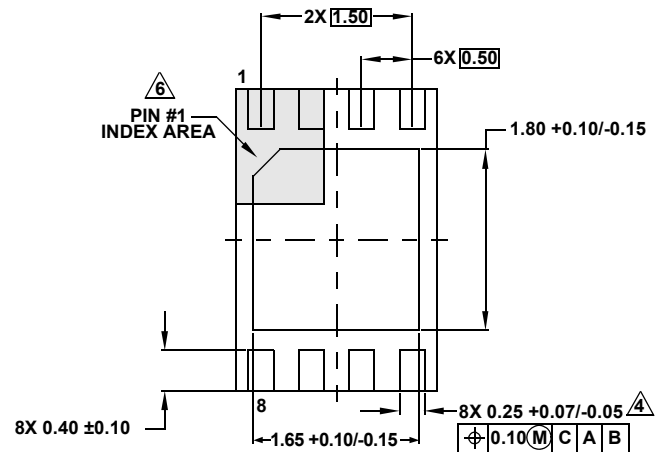
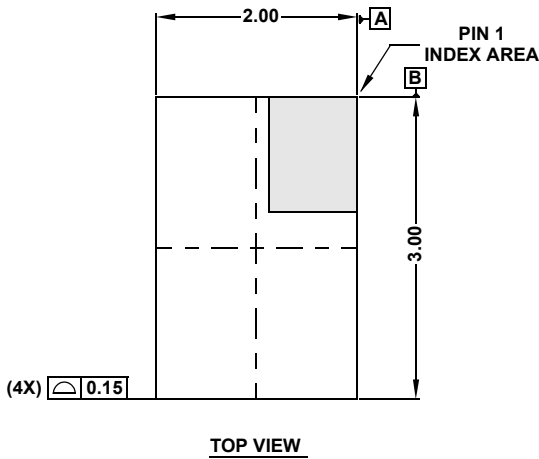


**NOTES:**

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

L8.2x3  
 8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE  
 Rev 2, 3/15

For the most recent package outline drawing, see [L8.2x3](#).



**NOTES:**

1. Dimensions are in millimeters.  
 Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal  $\pm 0.05$
4. Dimension applies to the metallized terminal and is measured between 0.25mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Complies to JEDEC MO-229 VCED-2.



## Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
  - "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
  - "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

## Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

## Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

## Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.