



FEATURES

- 1.5 Ω on resistance
- 0.28 Ω on-resistance flatness
- 0.1 Ω on-resistance match between channels
- Continuous current per channel up to 260 mA
- Fully specified at +12 V, ±15 V, and ±5 V
- No V_{SS} supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation
- 16-lead TSSOP package

APPLICATIONS

- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Audio signal routing
- Military communications
- Aviation

ENHANCED PRODUCT FEATURES

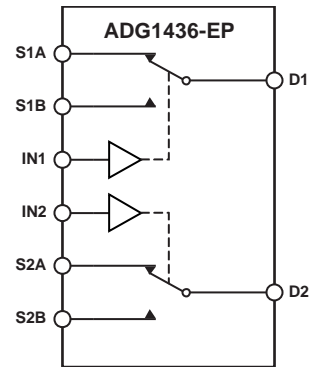
- Supports defense and aerospace applications (AQEC standard)
- Military temperature range (−55°C to +125°C)
- Controlled manufacturing baseline
- 1 assembly/test site
- 1 fabrication site
- Product change notification
- Qualification data available on request

GENERAL DESCRIPTION

The ADG1436-EP is a monolithic complementary metal-oxide semiconductor (CMOS) device containing two independently selectable SPDT switches. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. Both switches exhibit break-before-make switching action for use in multiplexer applications.

The ADG1436-EP is designed on an iCMOS® process. iCMOS (industrial CMOS) is a modular manufacturing process combining high voltage CMOS and bipolar technologies. It enables the development of a wide range of high performance analog integrated circuits (ICs) capable of 33 V operation in a

FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A ONE-INPUT LOGIC.

Figure 1.

17189-001

footprint that no previous generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, iCMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The on-resistance profile is very flat over the full analog input range, ensuring excellent linearity and low distortion when switching audio signals in military communication. iCMOS construction ensures ultralow power dissipation, making the part ideally suited for avionics and battery-powered instruments. Additional application and technical information can be found in the [ADG1436](#) data sheet.

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REVISION HISTORY

8/2018—Revision 0: Initial Version

SPECIFICATIONS

15 V DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

| Parameter | 25°C | -55°C to +125°C | Unit | Test Conditions/Comments |
|---|------------|----------------------|-------------------|--|
| ANALOG SWITCH | | | | |
| Analog Signal Range | | V_{DD} to V_{SS} | V | |
| On Resistance, R_{ON} | 1.5 | | Ω typ | $V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$ |
| | 1.8 | 2.6 | Ω max | $V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$ |
| On-Resistance Match Between Channels, ΔR_{ON} | 0.1 | | Ω typ | $V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$ |
| | 0.18 | 0.21 | Ω max | |
| On-Resistance Flatness, $R_{FLAT(ON)}$ | 0.28 | | Ω typ | $V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$ |
| | 0.36 | 0.45 | Ω max | |
| Continuous Current Per Channel ¹ | 260 | 100 | mA max | $V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$ |
| LEAKAGE CURRENTS | | | | |
| Source Off Leakage, I_S (Off) | ± 0.04 | | nA typ | $V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ |
| | ± 0.55 | ± 12.5 | nA max | $V_S = \pm 10\text{ V}$, $V_D = \pm 10\text{ V}$ |
| Drain Off Leakage, I_D (Off) | ± 0.04 | | nA typ | $V_S = \pm 10\text{ V}$, $V_D = \pm 10\text{ V}$ |
| | ± 0.55 | ± 12.5 | nA max | |
| Channel On Leakage, I_D , I_S (On) | ± 0.1 | | nA typ | $V_S = V_D = \pm 10\text{ V}$ |
| | ± 2 | ± 35 | nA max | |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V_{INH} | | 2.0 | V min | |
| Input Low Voltage, V_{INL} | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.005 | | μA typ | $V_{IN} = V_{GND}$ or V_{DD} |
| | | ± 0.1 | μA max | |
| Digital Input Capacitance, C_{IN} | 3.5 | | pF typ | |
| DYNAMIC CHARACTERISTICS¹ | | | | |
| Transition Time, $t_{TRANSITION}$ | 125 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 170 | 245 | ns max | $V_S = 10\text{ V}$ |
| Break-Before-Make Time Delay, t_{BBM} | 20 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | | 10 | ns min | $V_{S1} = V_{S2} = +10\text{ V}$ |
| Charge Injection | -20 | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$ |
| Off Isolation | -80 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$ |
| Channel-to-Channel Crosstalk | -80 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$ |
| Total Harmonic Distortion + Noise | 0.011 | | % typ | $R_L = 110\ \Omega$, 15 V p-p , $f = 20\text{ Hz to } 20\text{ kHz}$ |
| -3 dB Bandwidth | 110 | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ |
| Insertion Loss | -0.18 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$ |
| C_S (Off) | 23 | | pF typ | $f = 1\text{ MHz}$, $V_S = 0\text{ V}$ |
| C_D (Off) | 50 | | pF typ | $f = 1\text{ MHz}$, $V_S = 0\text{ V}$ |
| C_D , C_S (On) | 120 | | pF typ | $f = 1\text{ MHz}$, $V_S = 0\text{ V}$ |
| POWER REQUIREMENTS | | | | |
| I_{DD} | 0.001 | | μA typ | $V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ |
| | | 1 | μA max | Digital inputs = 0 V or V_{DD} |
| I_{DD} | 170 | | μA typ | Digital input = 5 V |
| | | 285 | μA max | |
| I_{SS} | 0.001 | | μA typ | Digital inputs = 0 V , 5 V , or V_{DD} |
| | | 1.0 | μA max | |
| V_{DD}/V_{SS} | | $\pm 4.5/\pm 16.5$ | V min/max | $GND = 0\text{ V}$ |

¹ Guaranteed by design, not subject to production test.

12 V SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

| Parameter | 25°C | -55°C to +125°C | Unit | Test Conditions/Comments |
|---|------------|-----------------|-------------------|---|
| ANALOG SWITCH | | | | |
| Analog Signal Range | | 0 V to V_{DD} | V | |
| On Resistance, R_{ON} | 2.8 | | Ω typ | $V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$ |
| | 3.5 | 4.8 | Ω max | $V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$ |
| On-Resistance Match Between Channels, ΔR_{ON} | 0.13 | | Ω typ | $V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$ |
| | 0.21 | 0.25 | Ω max | |
| On-Resistance Flatness, $R_{FLAT(ON)}$ | 0.6 | | Ω typ | $V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$ |
| | 1.1 | 1.3 | Ω max | |
| Continuous Current Per Channel ¹ | 240 | 100 | mA max | $V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$ |
| LEAKAGE CURRENTS | | | | |
| Source Off Leakage, I_S (Off) | ± 0.04 | | nA typ | $V_{DD} = 13.2\text{ V}$, $V_{SS} = 0\text{ V}$ |
| | ± 0.55 | ± 12.5 | nA max | $V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$ |
| Drain Off Leakage, I_D (Off) | ± 0.04 | | nA typ | $V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$ |
| | ± 0.55 | ± 12.5 | nA max | |
| Channel On Leakage, I_D , I_S (On) | ± 0.1 | | nA typ | $V_S = V_D = 1\text{ V or }10\text{ V}$ |
| | ± 1 | ± 35 | nA max | |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V_{INH} | | 2.0 | V min | |
| Input Low Voltage, V_{INL} | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.001 | | μA typ | $V_{IN} = V_{GND}$ or V_{DD} |
| | | ± 0.1 | μA max | |
| Digital Input Capacitance, C_{IN} | 3.5 | | pF typ | |
| DYNAMIC CHARACTERISTICS¹ | | | | |
| Transition Time, $t_{TRANSITION}$ | 200 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 270 | 350 | ns max | $V_S = 8\text{ V}$ |
| Break-Before-Make Time Delay, t_{BBM} | 70 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | | 10 | ns min | $V_{S1} = V_{S2} = 8\text{ V}$ |
| Charge Injection | 30 | | pC typ | $V_S = 6\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$ |
| Off Isolation | -80 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$ |
| Channel-to-Channel Crosstalk | -80 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$ |
| -3 dB Bandwidth | 78 | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ |
| Insertion Loss | -0.3 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$ |
| C_S (Off) | 40 | | pF typ | $f = 1\text{ MHz}$, $V_S = 6\text{ V}$ |
| C_D (Off) | 80 | | pF typ | $f = 1\text{ MHz}$, $V_S = 6\text{ V}$ |
| C_D , C_S (On) | 140 | | pF typ | $f = 1\text{ MHz}$, $V_S = 6\text{ V}$ |
| POWER REQUIREMENTS | | | | |
| I_{DD} | 0.001 | | μA typ | $V_{DD} = 13.2\text{ V}$ |
| | | 1.0 | μA max | Digital inputs = 0 V or V_{DD} |
| I_{DD} | 170 | | μA typ | Digital inputs = 5 V |
| | | 285 | μA max | |
| V_{DD} | | 5/16.5 | V min/max | $GND = 0\text{ V}$, $V_{SS} = 0\text{ V}$ |

¹ Guaranteed by design, not subject to production test.

5 V DUAL SUPPLY

$V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 3.

| Parameter | 25°C | -55°C to +125°C | Unit | Test Conditions/Comments |
|---|------------|----------------------|-------------------|--|
| ANALOG SWITCH | | | | |
| Analog Signal Range | | V_{DD} to V_{SS} | V | |
| On Resistance, R_{ON} | 3.3 | | Ω typ | $V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$ |
| | 4 | 5.4 | Ω max | $V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$ |
| On-Resistance Match Between Channels, ΔR_{ON} | 0.13 | | Ω typ | $V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$ |
| | 0.22 | 0.25 | Ω max | |
| On-Resistance Flatness, $R_{FLAT(ON)}$ | 0.9 | | Ω typ | $V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$ |
| | 1.1 | 1.31 | Ω max | |
| Continuous Current Per Channel ¹ | 240 | 100 | mA max | $V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$ |
| LEAKAGE CURRENTS | | | | |
| Source Off Leakage, I_S (Off) | ± 0.03 | | nA typ | $V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ |
| | ± 0.2 | ± 12.5 | nA max | $V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$ |
| Drain Off Leakage, I_D (Off) | ± 0.03 | | nA typ | $V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$ |
| | ± 0.2 | ± 12.5 | nA max | |
| Channel On Leakage, I_D , I_S (On) | ± 0.05 | | nA typ | $V_S = V_D = \pm 4.5\text{ V}$ |
| | ± 0.25 | ± 35 | nA max | |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V_{INH} | | 2.0 | V min | |
| Input Low Voltage, V_{INL} | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.001 | | μA typ | $V_{IN} = V_{GND}$ or V_{DD} |
| | | ± 0.1 | μA max | |
| Digital Input Capacitance, C_{IN} | 3.5 | | pF typ | |
| DYNAMIC CHARACTERISTICS¹ | | | | |
| Transition Time, $t_{TRANSITION}$ | 310 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 445 | 565 | ns max | $V_S = 3\text{ V}$ |
| Break-Before-Make Time Delay, t_{BBM} | 80 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | | 10 | ns min | $V_{S1} = V_{S2} = 3\text{ V}$ |
| Charge Injection | 30 | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$ |
| Off Isolation | -80 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$ |
| Channel-to-Channel Crosstalk | -80 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$ |
| Total Harmonic Distortion + Noise | 0.03 | | % typ | $R_L = 110\ \Omega$, 2.5 V pp , $f = 20\text{ Hz to } 20\text{ kHz}$ |
| -3 dB Bandwidth | 85 | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ |
| Insertion Loss | -0.28 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$ |
| C_S (Off) | 33 | | pF typ | $V_S = 0\text{ V}$, $f = 1\text{ MHz}$ |
| C_D (Off) | 65 | | pF typ | $V_S = 0\text{ V}$, $f = 1\text{ MHz}$ |
| C_D , C_S (On) | 145 | | pF typ | $V_S = 0\text{ V}$, $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | |
| I_{DD} | 0.001 | | μA typ | $V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ |
| | | 1.0 | μA max | Digital inputs = 0 V or V_{DD} |
| I_{SS} | 0.001 | | μA typ | Digital inputs = 0 V or V_{DD} |
| | | 1.0 | μA max | |
| V_{DD}/V_{SS} | | $\pm 4.5/\pm 16.5$ | V min/max | $GND = 0\text{ V}$ |

¹ Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

| Parameter | Ratings |
|--|---|
| V _{DD} to V _{SS} | 35 V |
| V _{DD} to GND | -0.3 V to +25 V |
| V _{SS} to GND | +0.3 V to -25 V |
| Analog Inputs ¹ | V _{SS} - 0.3 V to V _{DD} + 0.3 V or 30 mA, whichever occurs first |
| Digital Inputs ¹ | GND - 0.3 V to V _{DD} + 0.3 V or 30 mA, whichever occurs first |
| Peak Current, S or D | 600 mA (pulsed at 1 ms, 10% duty cycle maximum) |
| Continuous Power Dissipation ² | See Figure 2 |
| Operating Temperature Range | -55°C to +125°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | 150°C |
| Reflow Soldering Peak Temperature, Pb-Free | 260(+0/-5)°C |

¹ Overvoltages at IN, S, and D are clamped by internal diodes. Current must be limited to the maximum ratings given.

² Calculated based on Table 3 model.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

Table 5. Thermal Resistance

| Package Type ¹ | θ _{JA} | Unit |
|---------------------------|-----------------|------|
| RU-16 | 112 | °C/W |

¹ Thermal impedance simulated values are based on a JEDEC 252P thermal test board. See JEDEC JESD-51.

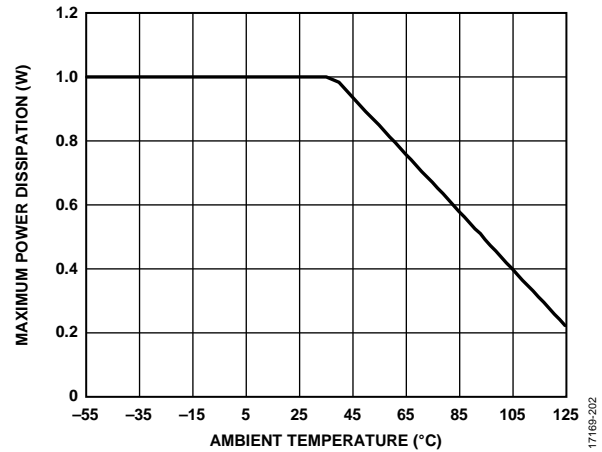


Figure 2. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

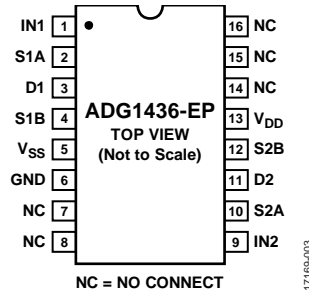


Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

| Pin No. | Mnemonic | Function |
|----------------|-----------------|---|
| 1 | IN1 | Logic Control Input. |
| 2 | S1A | Source Terminal. Can be an input or output. |
| 3 | D1 | Drain Terminal. Can be an input or output. |
| 4 | S1B | Source Terminal. Can be an input or output. |
| 5 | V _{SS} | Most Negative Power Supply Potential. |
| 6 | GND | Ground (0 V) Reference. |
| 7, 8, 14 to 16 | NC | No Connect. |
| 9 | IN2 | Logic Control Input. |
| 10 | S2A | Source Terminal. Can be an input or output. |
| 11 | D2 | Drain Terminal. Can be an input or output. |
| 12 | S2B | Source Terminal. Can be an input or output. |
| 13 | V _{DD} | Most Positive Power Supply Potential. |

TRUTH TABLE FOR SWITCHES

Table 7. Truth Table

| IN _x | S _x A | S _x B |
|-----------------|------------------|------------------|
| 0 | Off | On |
| 1 | On | Off |

TYPICAL PERFORMANCE CHARACTERISTICS

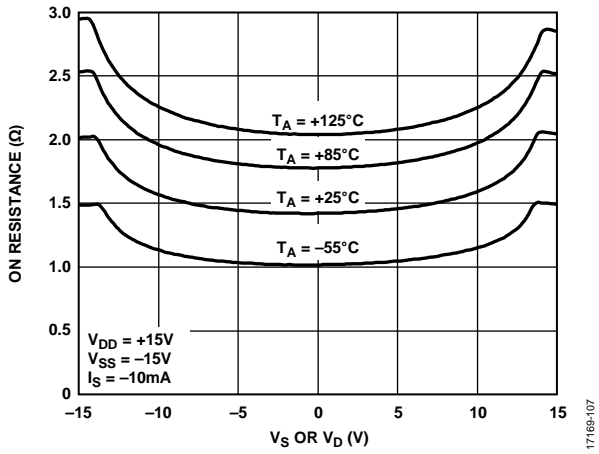


Figure 4. On Resistance vs. V_S or V_D for Different Temperatures, 15 V Dual Supply

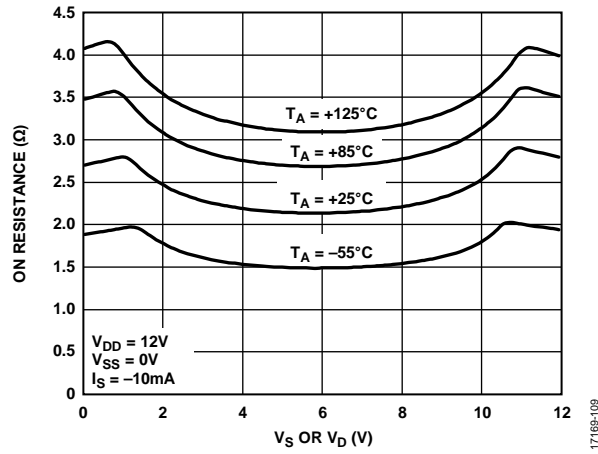


Figure 6. On Resistance vs. V_S or V_D for Different Temperatures, Single Supply

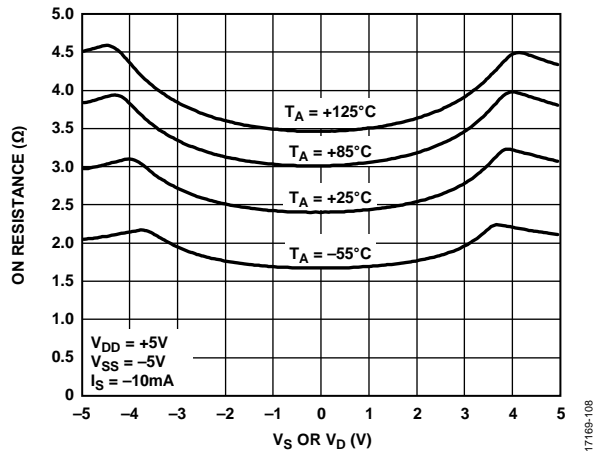


Figure 5. On Resistance vs. V_S or V_D for Different Temperatures, 5 V Dual Supply

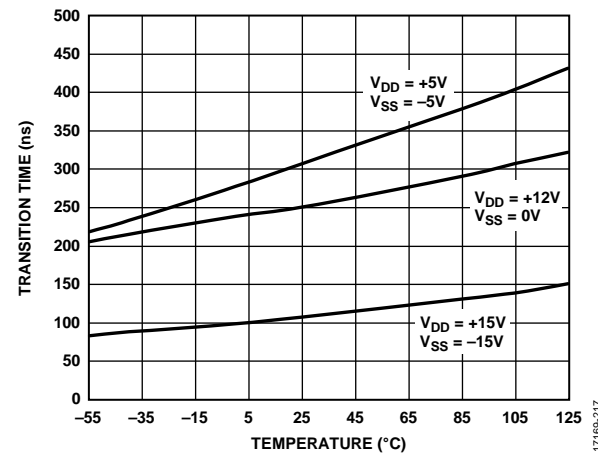


Figure 7. Transition Time vs. Temperature

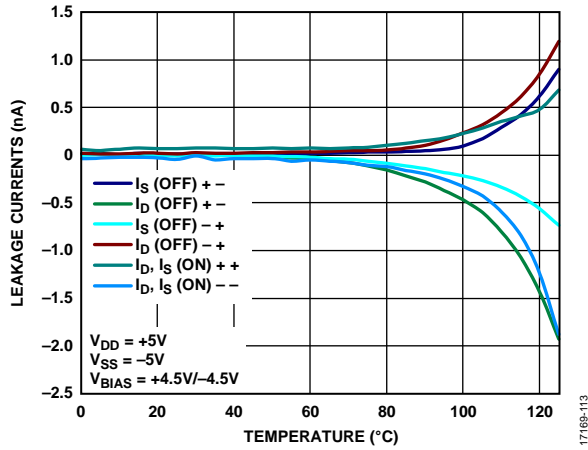


Figure 8. Leakage Currents vs. Temperature, 5 V Dual Supply

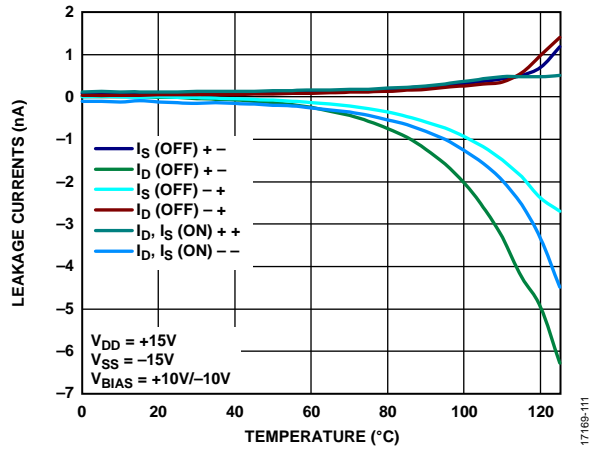


Figure 10. Leakage Currents vs. Temperature, 15 V Dual Supply

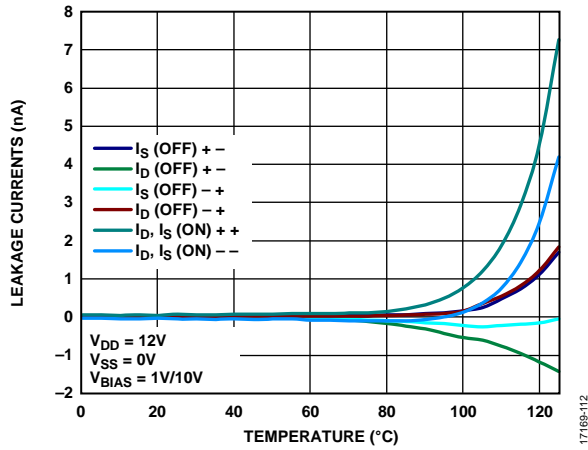
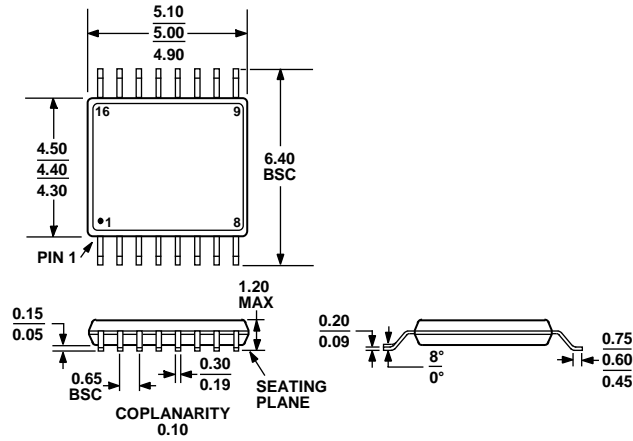


Figure 9. Leakage Currents vs. Temperature, 12 V Single Supply

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 11. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|---|----------------|
| ADG1436TRUZ-EP | -55°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG1436TRUZ-EPR7 | -55°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |

¹ Z = RoHS Compliant Part.

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