TEXAS INSTRUMENTS

User's Guide
SLVU470–June 11

TPS54478EVM-037 4-A, SWIFT™ Regulator Evaluation Module

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1 Introduction

This user's guide contains background information for the TPS54478 as well as support documentation for the TPS54478EVM-037 evaluation module (HPA375). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54478EVM-037.

1.1 Background

The TPS54478 dc/dc converter is designed to provide up to a 4 A output from an input voltage source of 2.95 V to 6 V. Rated input voltage and output current range for the evaluation module are given in Table 1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS54478 regulator. The switching frequency is externally set at a nominal 1000 kHz. The high-side and low-side MOSFETs are incorporated inside the TPS54478 package along with the gate drive circuitry. The low drain-to-source on resistance of the MOSFETs allow the TPS54478 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS54478 provides adjustable slow start and undervoltage lockout inputs. The absolute maximum input voltage is 7 V for the TPS54478EVM-037.

Table 1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54478EVM-037	VIN = 3 V to 6 V	0 A to 4 A

1.2 Performance Specification Summary

A summary of the TPS54478EVM-037 performance specifications is provided in Table 2. Specifications are given for an input voltage of V_{IN} = 5 V and an output voltage of 1.8 V, unless otherwise specified. The TPS54478EVM-037 is designed and tested for V_{IN} = 3 V to 6 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 2. TPS54478EVM-037 Performance Specification Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} operating voltage range			3	5	6	V
V_{IN} start voltage				2.90		V
V_{IN} stop voltage				2.659		V
Output voltage set point				1.8		V
Output current range	V_{IN} = 3 V to 6 V		0		4	A
Line regulation	I_O = 2 A, V_{IN} = 3 V to 6 V			±0.04%		
Load regulation	V_{IN} = 5 V, I_O = 0 A to 4 A			±0.15%		
Load transient response	I_O = 1 A to 3 A	Voltage change		–54		mV
		Recovery time		100		μs
	I_O = 3 A to 1 A	Voltage change		54		mV
		Recovery time		100		μs
Loop bandwidth	V_{IN} = 3.3 V, I_O = 4 A			79		kHz
Phase margin	V_{IN} = 3.3 V , I_O = 4 A			64		°
Input ripple voltage	I_O = 4 A			140		mV_{PP}
Output ripple voltage	I_O = 4 A			<10		mV_{PP}
Output rise time				3.33		ms
Operating frequency				1000		kHz
Maximum efficiency	TPS54478EVM-037, V_{IN} = 3 V, I_O = 0.5 A			94.5%		

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54478. Some modifications can be made to this module.

1.3.1 Output Voltage Set Point

The voltage divider R9 and R10 is used to set the output voltage. To change the output voltage of the EVM, it is necessary to change the value of resistor R9. Changing the value of R9 can change the output voltage above 0.6 V. The value of R9 for a specific output voltage can be calculated using Equation 1. Use 10.0 kΩ for R10.

$$R9 = R10 \times \left(\frac{V_{OUT}}{0.6\ V} - 1\right) \tag{1}$$

Table 3 lists the R9 and R10 values for some common output voltages. Note that V_{IN} must be in a range so that the minimum on-time is greater than 80 ns, and the maximum duty cycle is less than 92%. The values given in Table 3 are standard values, not the exact value calculated using Equation 1.

Table 3. Output Voltages Available

Output Voltage (V)	R9 Value (kΩ)	R10 Value (kΩ)
1	6.65	10
1.2	10	10
1.5	15	10
1.8	20	10
2.5	31.6	10

1.3.2 Slow Start Time

The slow start time can be adjusted by changing the value of C7. Use Equation 2 to calculate the required value of C7 for a desired slow start time

$$C7(nF) = 3 \times Tss(mS) \tag{2}$$

C7 is set to 0.01 µF on the EVM for a default slowstart time of 3.33 msec.

1.3.3 Adjustable UVLO

The under voltage lock out (UVLO) can be adjusted externally using R1 and R2. The EVM is set for a start voltage of 2.9 V and a stop voltage of 2.659 V using R1 = 14.3 kΩ and R2 = 11.5 kΩ. Use Equation 3 and Equation 4 to calculate required resistor values for different start and stop voltages.

$$R1 = \frac{V_{START}\left(\dfrac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1 - \dfrac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \tag{3}$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1\left(I_p + I_h\right)} \tag{4}$$

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54478EVM-037 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input / Output Connections

The TPS54478EVM-037 is provided with input/output connectors and test points as shown in Table 4. A power supply capable of supplying 3 A must be connected to J1 through a pair of 20 AWG wires. The load must be connected to J4 through a pair of 20 AWG wires. The maximum load current capability must be at least 4 A to use the full capability of this EVM. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP6 is used to monitor the output voltage with TP7 as the ground reference.

Table 4. EVM Connectors and Test Points

Reference Designator	Function
J1	V_{IN} (see Table 1 for V_{IN} range).
J2	2-pin header to allow connection of an external track in voltage to SS/TR. Use in conjunction with optional resistor divider of R5 and R6
J3	V_{OUT}, 1.8 V at 4 A maximum.
JP1	2-pin header for enable. Connect EN to ground to disable, open to enable.
JP2	2-pin header for to allow pull up of PWRGD to V_{IN}.
TP1	V_{IN} test point at V_{IN} connector.
TP2	GND test point at V_{IN}.
TP3	Slow start monitor test point.
TP4	PH test point
TP5	PWRGD test point
TP6	GND test point
TP7	Test point between voltage divider network and output. Used for loop response measurements.
TP8	Output voltage test point at OUT connector.
TP9	GND test point at OUT connector.

2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 0.5 A – 1 A and then decreases as the load current increases towards full load. Figure 1 shows the efficiency for the TPS54478EVM-037 at an ambient temperature of 25°C.

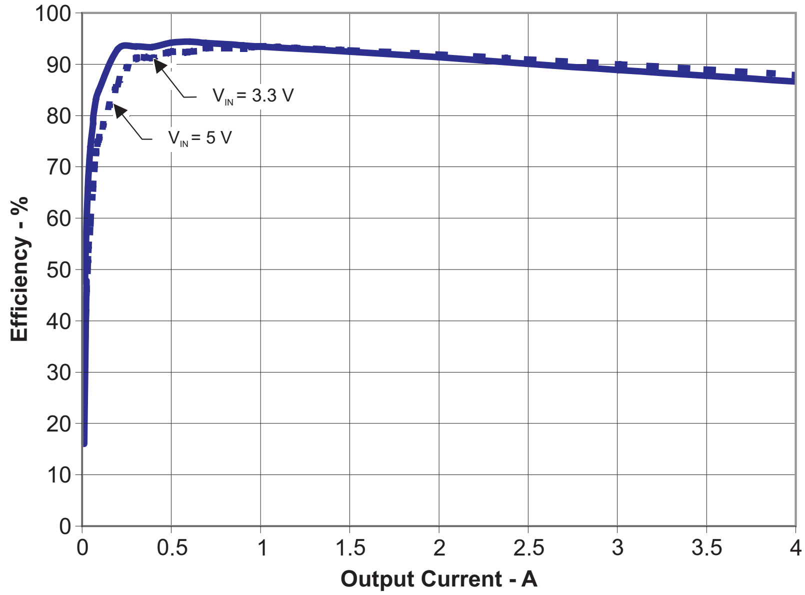

Figure 1. TPS54478EVM-037 Efficiency

Figure 2 shows the efficiency for the TPS54478EVM-037 at lower output currents between 0.02 A and 0.20 A at an ambient temperature of 25°C.

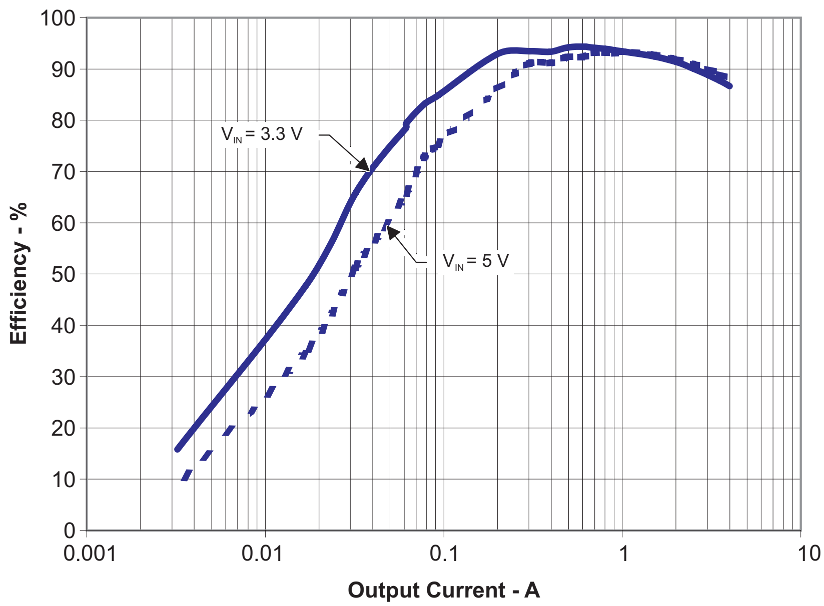

Figure 2. TPS54478EVM-037 Low Current Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

2.3 Output Voltage Load Regulation

Figure 3 shows the load regulation for the TPS54478EVM-037.

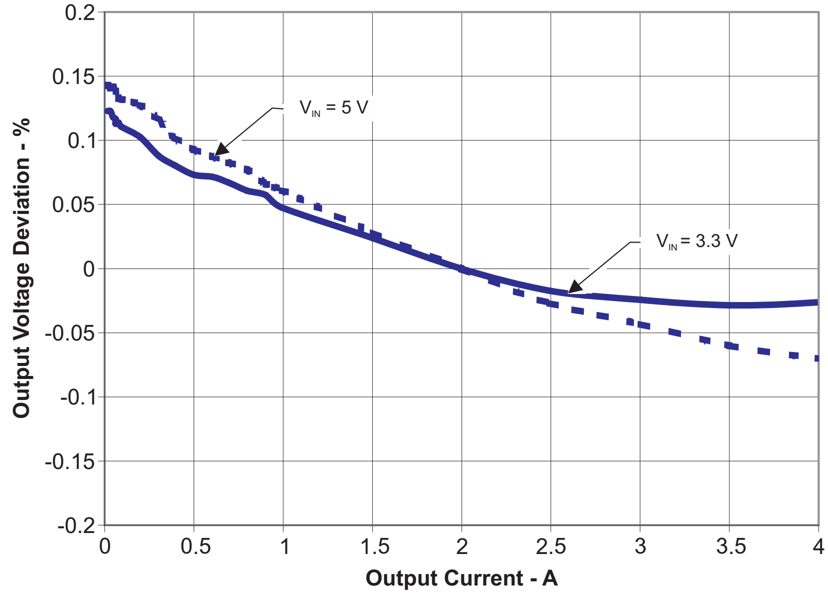

Figure 3. TPS54478EVM-037 Load Regulation

Measurements are given for an ambient temperature of 25°C.

2.4 Output Voltage Line Regulation

Figure 4 shows the line regulation for the TPS54478EVM-037.

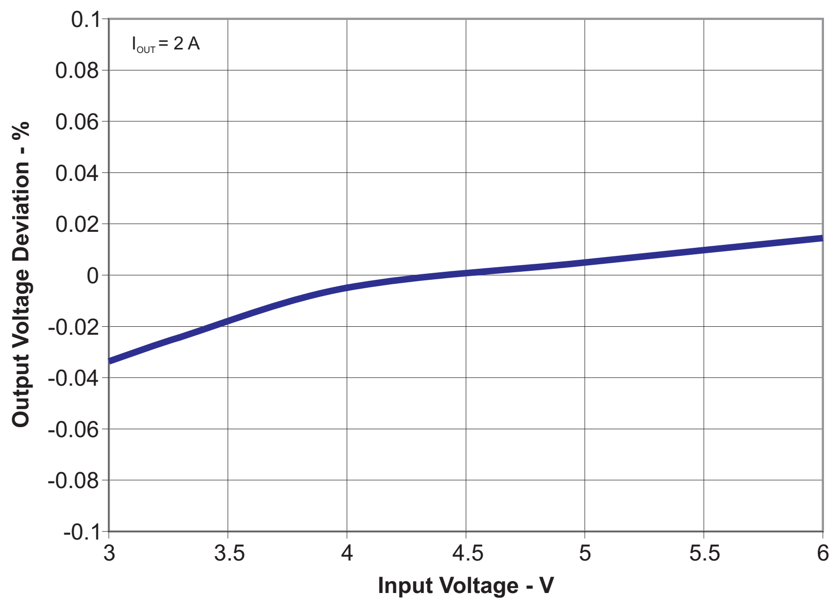

Figure 4. TPS54478EVM-037 Line Regulation

2.5 Load Transients

Figure 5 shows the TPS54478EVM-037 response to load transients. The current step is from 25% to 75% of maximum rated load at 3.3 V input. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

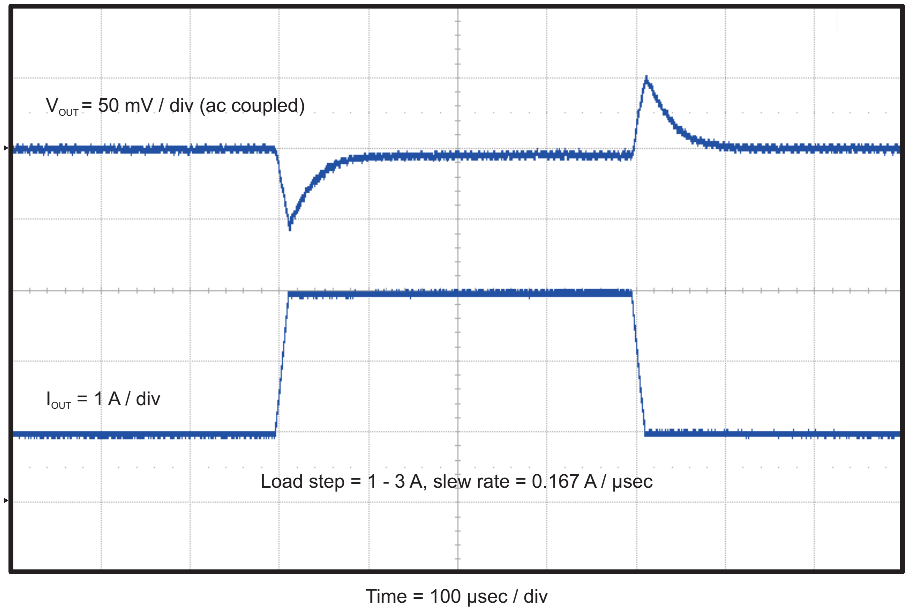

Figure 5. TPS54478EVM-037 Transient Response

2.6 Loop Characteristics

Figure 6 shows the TPS54478EVM-037 loop-response characteristics. Gain and phase plots are shown for V_{IN} voltage of 3.3 V. Load current for the measurement is 4 A.

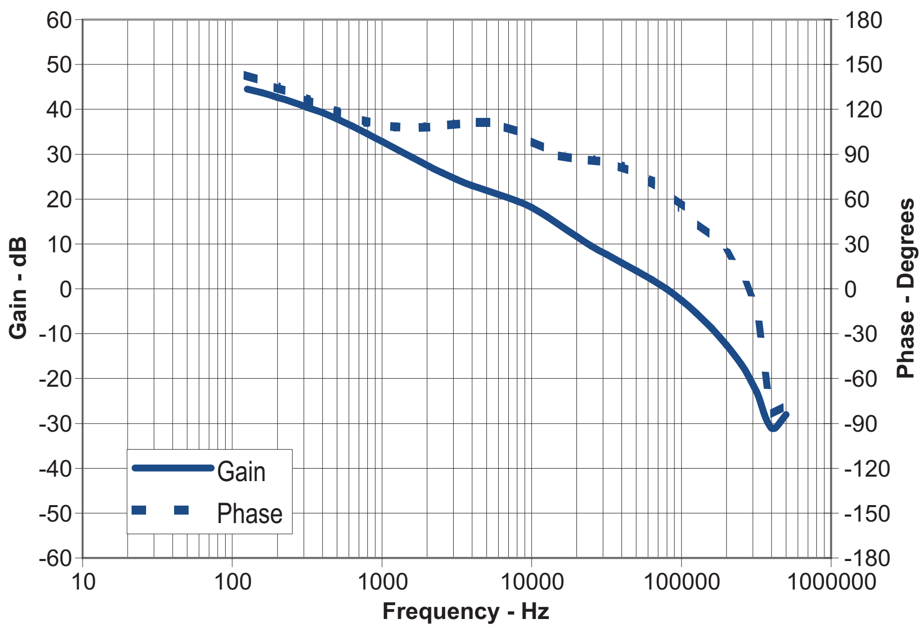

Figure 6. TPS54478EVM-037 Loop Response

2.7 Output Voltage Ripple

Figure 7 shows the TPS54478EVM-037 output voltage ripple. The output current is the rated full load of 4A and V_{IN} = 3.3 V. The ripple voltage is measured directly across the output capacitors.

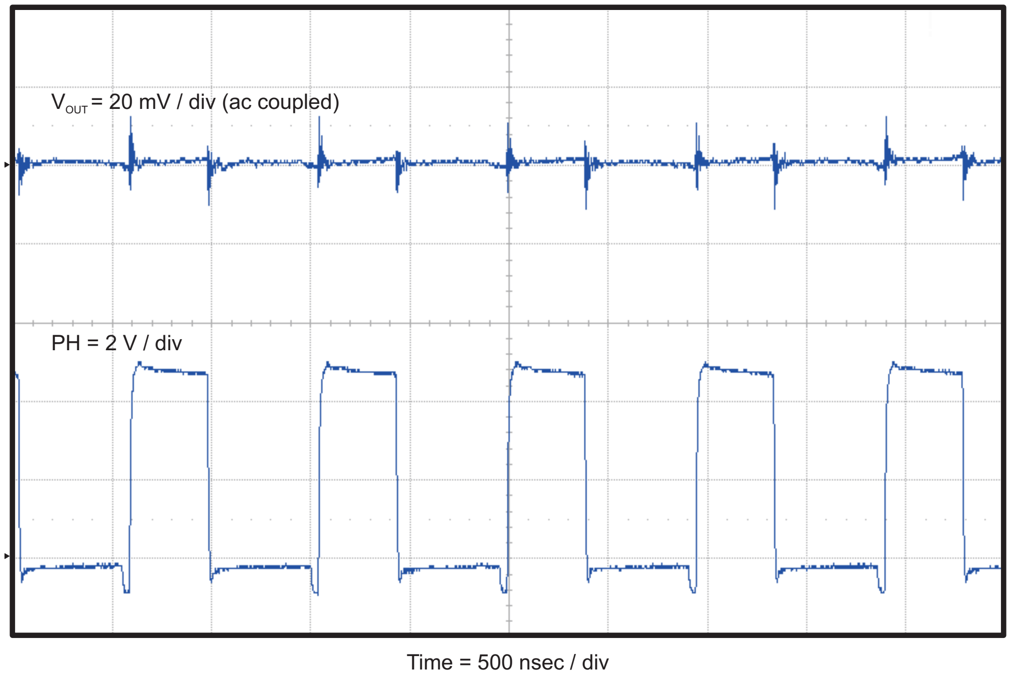

Figure 7. TPS54478EVM-037 Output Ripple

2.8 Input Voltage Ripple

Figure 8 shows the TPS54478EVM-037 input voltage ripple. The output current is the rated full load of 4A and V_{IN} = 3.3 V. The ripple voltage is measured directly across the input capacitors.

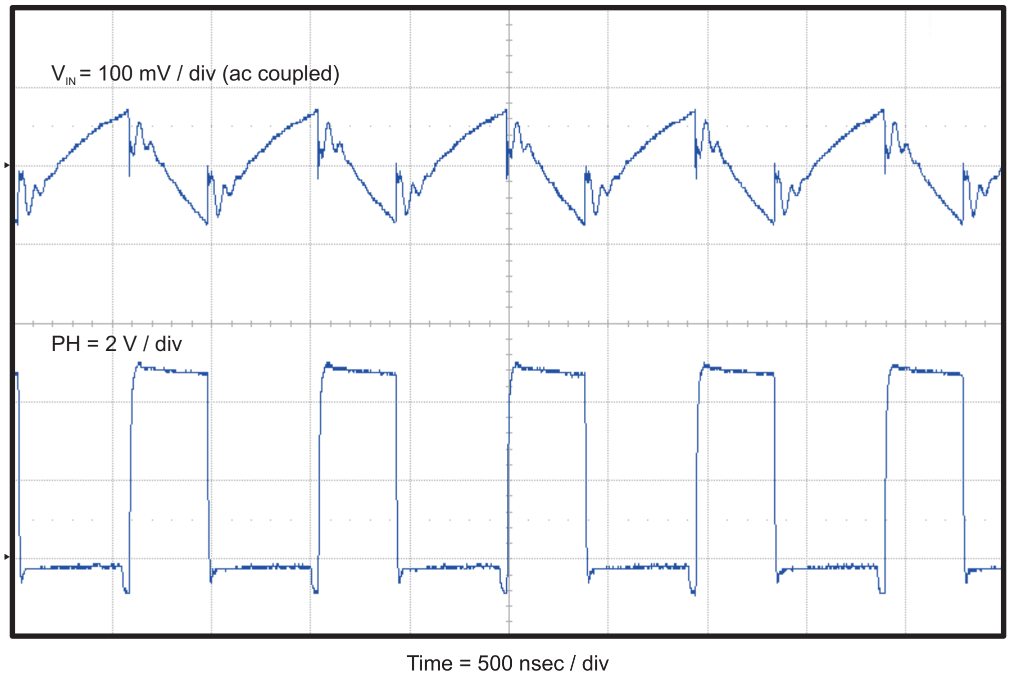

Figure 8. TPS54478EVM-037 Input Ripple

2.9 Powering Up

Figure 9 and Figure 10 show the start-up waveforms for the TPS54478EVM-037. In Figure 9, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold as set by the R_1 and R_2 resistor divider network. In Figure 10, the input voltage is initially applied and the output is inhibited by using a jumper at JP1 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 1.8 V. The input voltage for these plots is 5 V and the load is 1Ω.

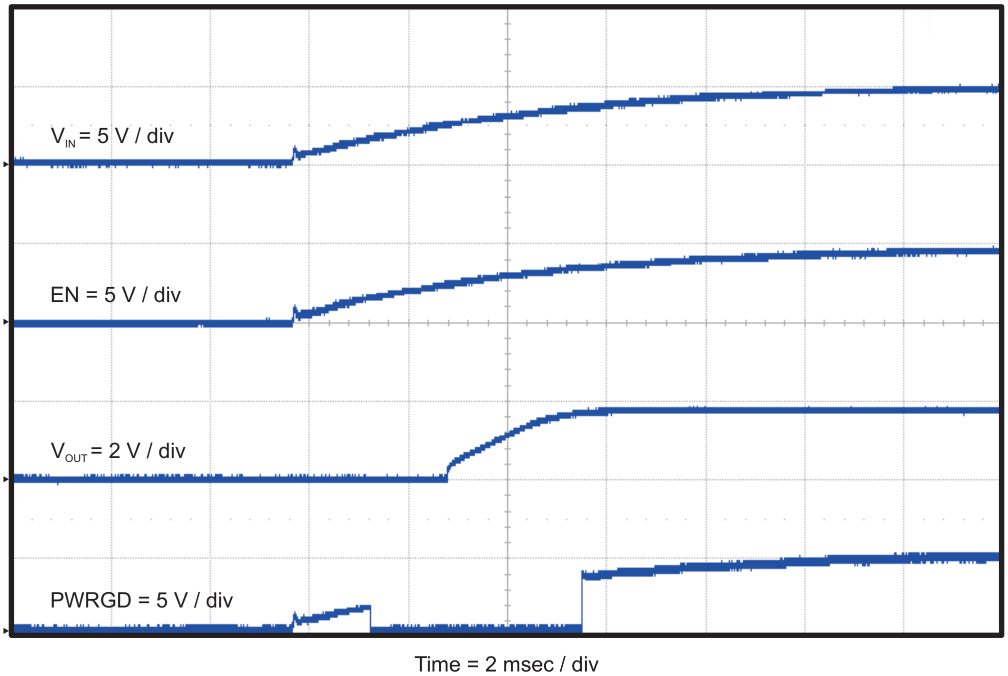

Figure 9. TPS54478EVM-037 Start-Up Relative to V_{IN}

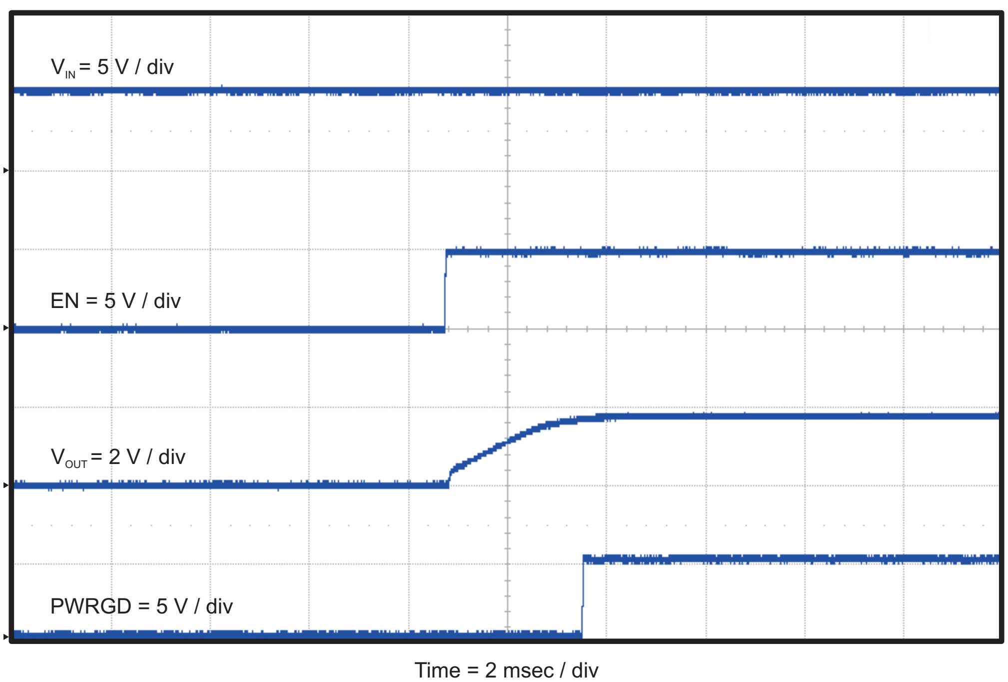

Figure 10. TPS54478EVM-037 Start-up Relative to Enable

The TPS54478 is designed to start up into pre-biased outputs. Figure 11 shows the output voltage start up waveform when the output is pre-biased with 500 mV.

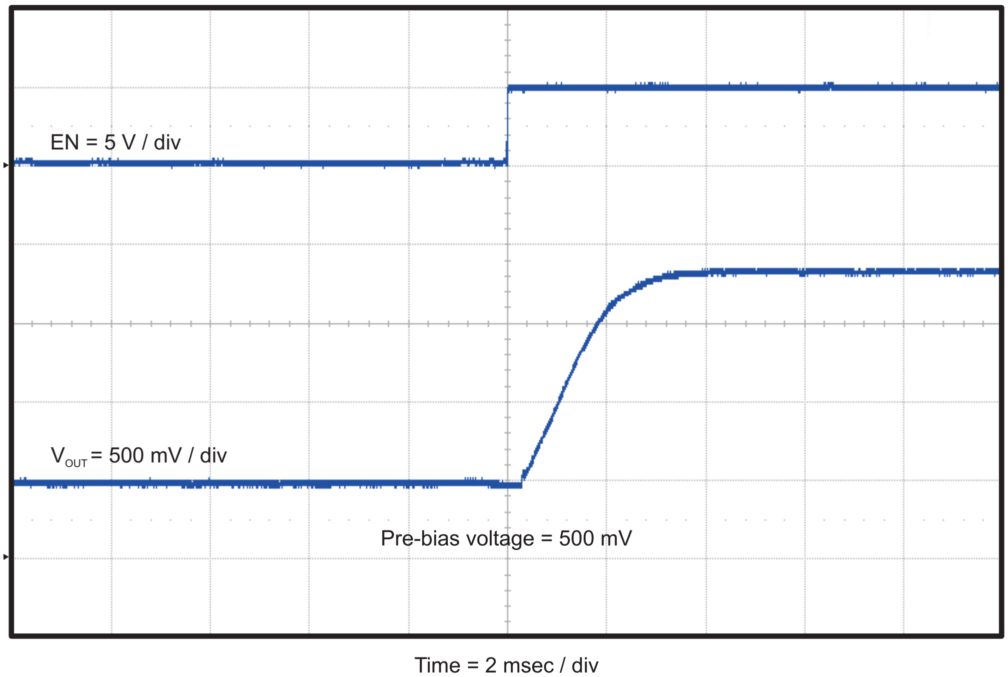

Figure 11. TPS54478EVM-037 Start-up into Pre-bias

2.10 Powering Down

Figure 12 and Figure 13 show the start-up waveforms for the TPS54478EVM-037. In Figure 12, the output voltage ramps down as soon as the input voltage falls below the UVLO stop threshold as set by the R1 and R2 resistor divider network. In Figure 13, the output is inhibited by using a jumper at JP1 to tie EN to GND. The input voltage for these plots is 5 V and the load is 1Ω.

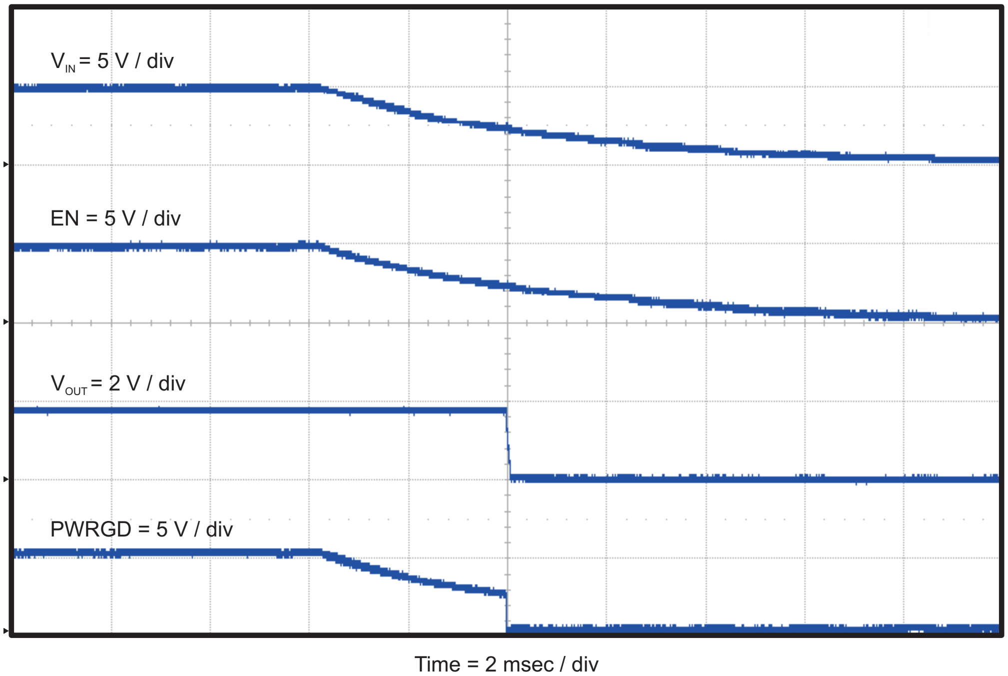

Figure 12. TPS54478EVM-037 Shut-down Relative to V_{IN}

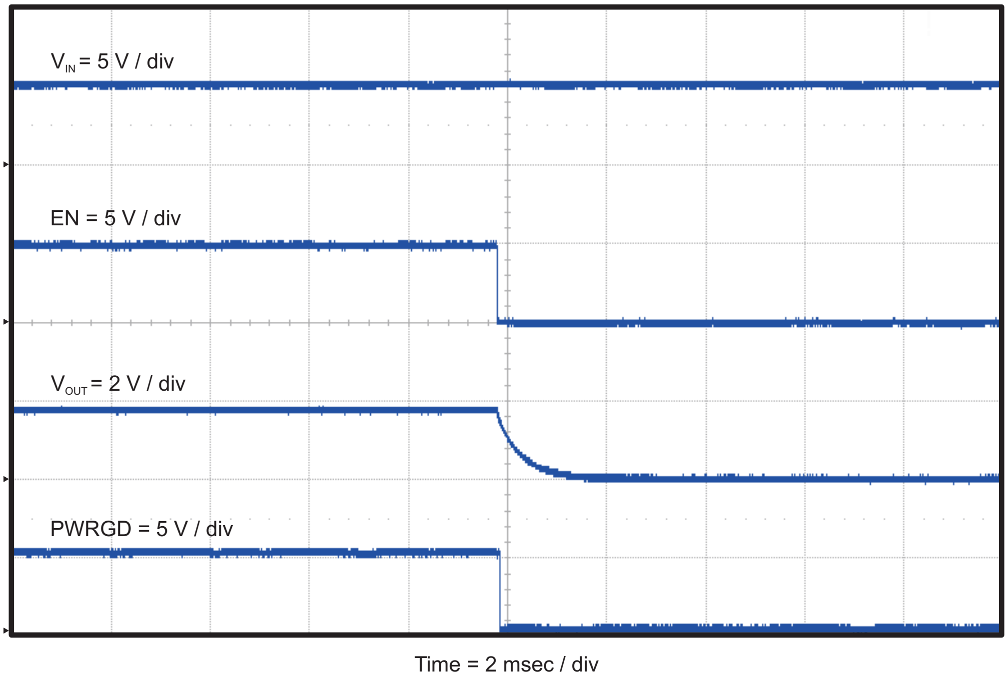

Figure 13. TPS54478EVM-037 Shut-down Relative to EN

2.11 Hiccup Mode Current Limit

The TPS54478 has hiccup mode current limit. When the peak switch current exceeds the current limit threshold, the device shuts down and restarts. Hiccup mode current limit operation is shown in Figure 14 and Figure 15. Figure 14 shows the activation of hiccup mode current limit. When the peak current limit is exceeded, the output voltage is dissabled. Figure 15 shows the operation of the TPS54478 with the output shorted to ground. The device will continuously reset until the fault condition is removed.

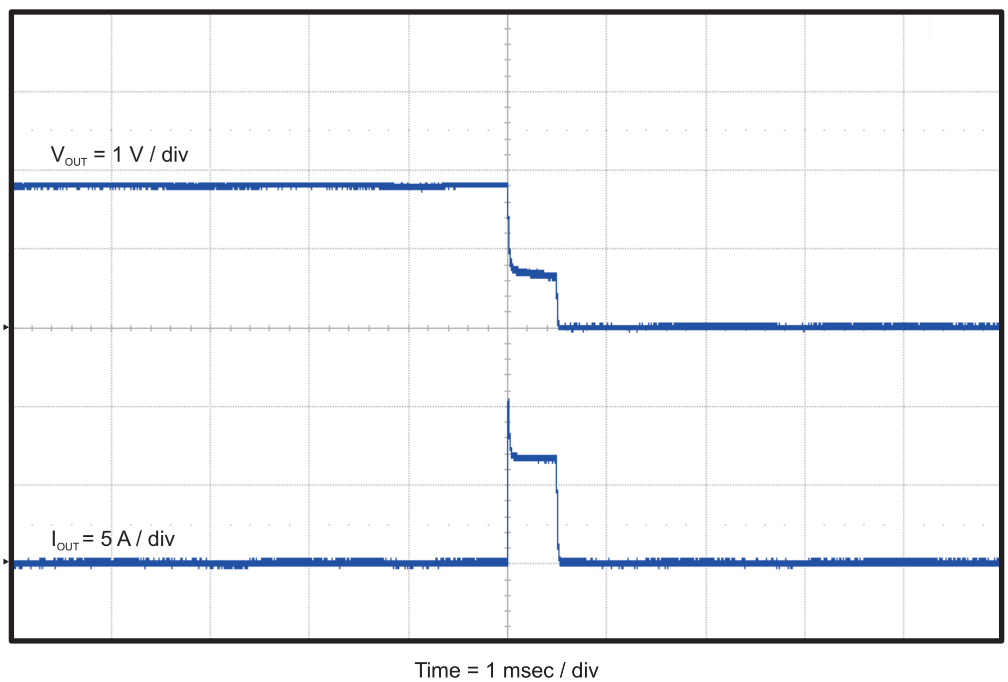

Figure 14. TPS54478EVM-037 Hiccup Mode Current Limit Shut-down

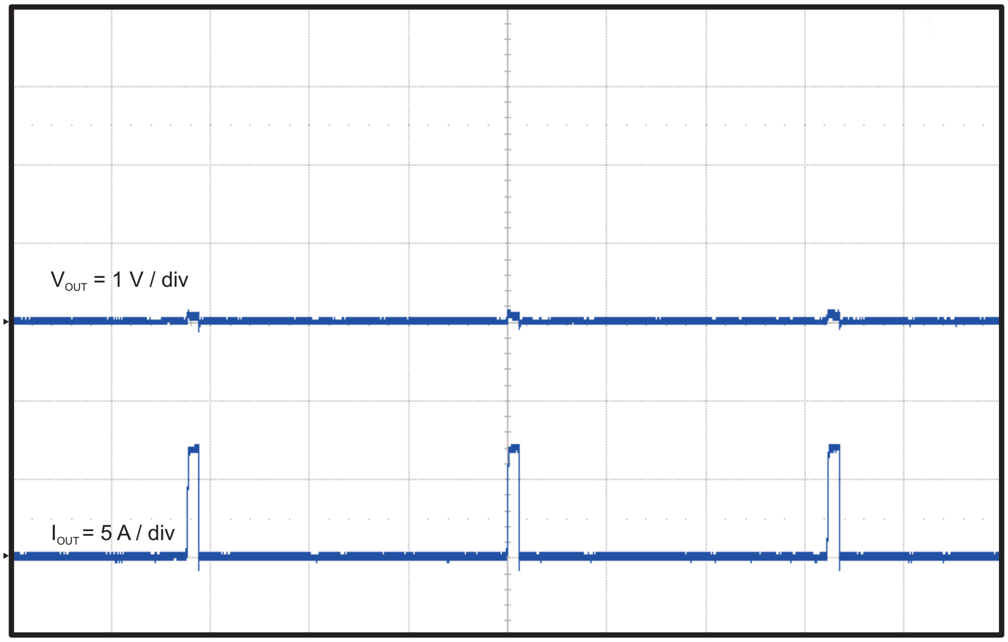

Figure 15. TPS54478EVM-037 Hiccup Mode Current Limit Re-start into Short Circuit

3 Board Layout

This section provides a description of the TPS54478EVM-037, board layout, and layer illustrations.

3.1 Layout

Figure 16 through Figure 20 shows the board layout for the TPS54478EVM-037. The topside layer of the EVM is laid out in a manner typical of a user application. The top, bottom and internal layers are 2-oz. copper.

The top layer contains the main power traces for V_{IN}, V_{OUT}, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54478 and a large area filled with ground. The bottom and internal layers contain ground planes only. The top-side ground areas are connected to the bottom and internal ground planes with multiple vias placed around the board including four vias directly under the TPS54478 device to provide a thermal path from the top-side ground area to the bottom-side and internal ground planes.

The input decoupling capacitors (C2, and C3) and bootstrap capacitor (C6) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} trace near the output connector J4. For the TPS54478, an additional input bulk capacitor may be required, depending on the EVM connection to the input supply.

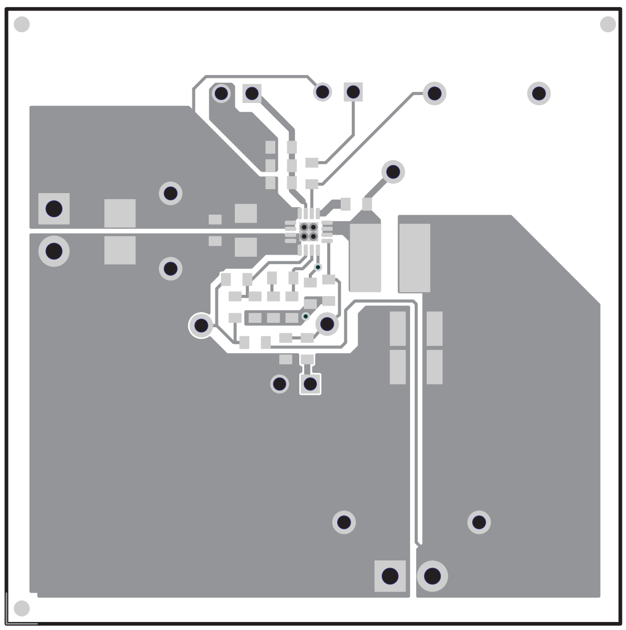

Figure 16. TPS54478EVM-037 Top-Side Layout

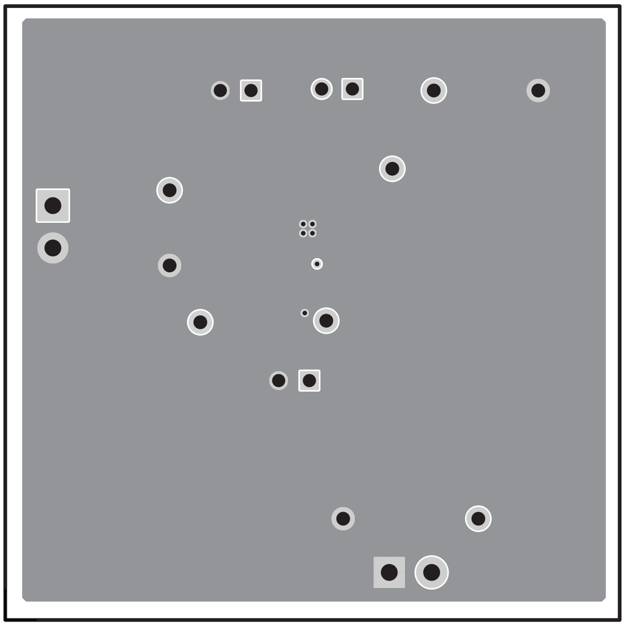

Figure 17. TPS54478EVM-037 Bottom-Side Layout

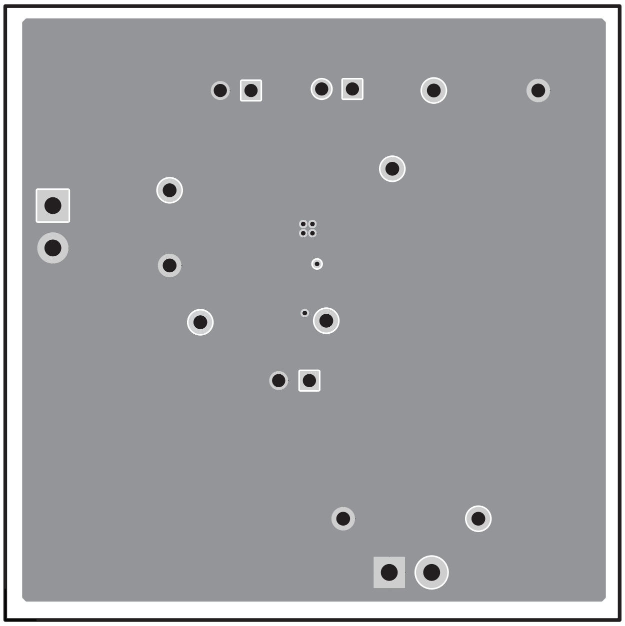

Figure 18. TPS54478EVM-037 Layout 2

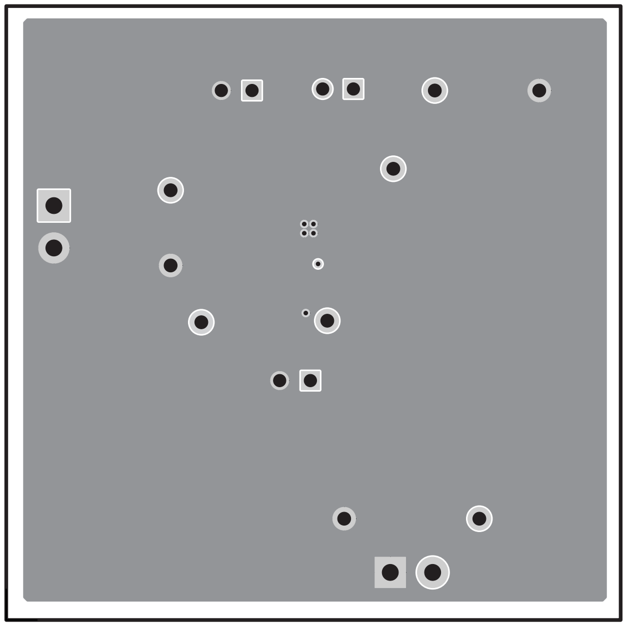

Figure 19. TPS54478EVM-037 Layout 3

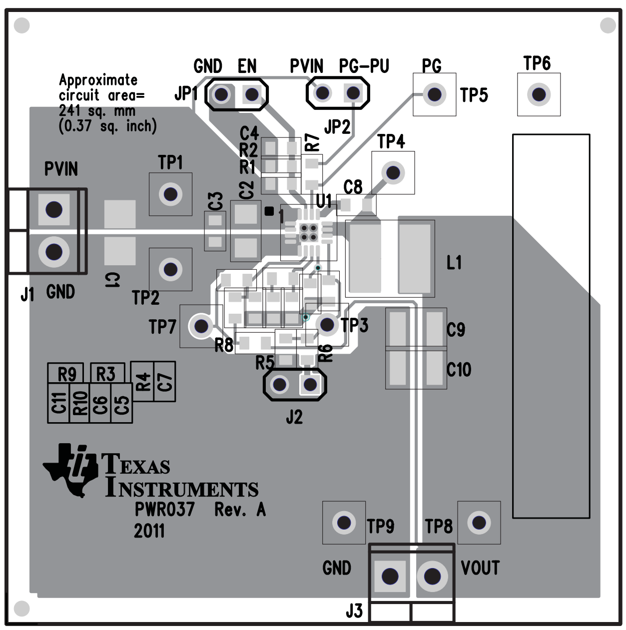

Figure 20. TPS54478EVM-037 Top-Side Assembly

3.2 Estimated Circuit Area

The estimated printed circuit board area for the components used in this design is 0.37 in^2 (239 mm^2). This area does not include test point or connectors.

4 Schematic and Bill of Materials

This section presents the TPS54478EVM-037 schematic and bill of materials.

4.1 Schematic

Figure 21 is the schematic for the TPS54478EVM-037.

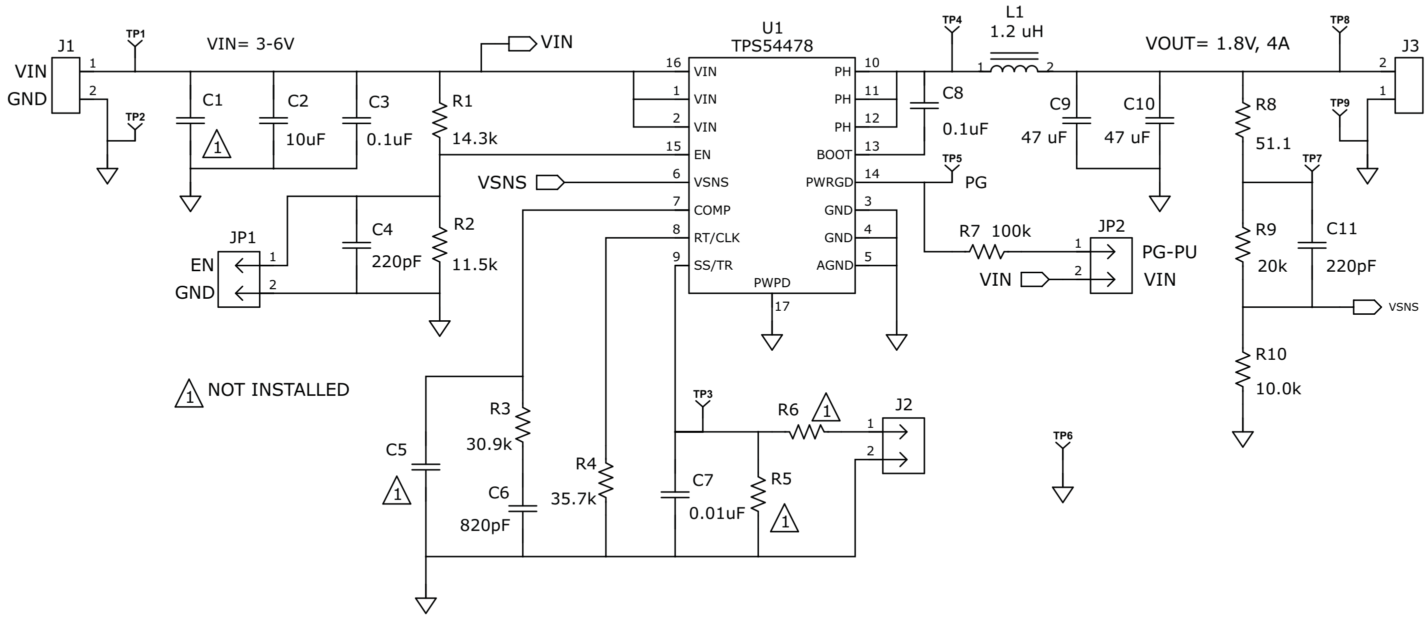

Figure 21. TPS54478EVM-037 Schematic

4.2 Bill of Materials

Table 5 presents the bill of materials for the TPS54478EVM-037.

Table 5. TPS54478EVM-037 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
0	C1	Open	Capacitor	Multi sizes	Engineering Only	Std
1	C2	10µF	Capacitor, Ceramic, 16V, X5R, 20%	1206	Std	Std
2	C3, C8	0.1µF	Capacitor, Ceramic, 25V, X5R, 10%	0603	Std	Std
2	C4. C11	220pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	Std	Std
0	C5	Open	Capacitor, Ceramic,	0603	Std	Std
1	C6	820pF	Capacitor, Ceramic, 50V, X7R, 10%	0603	Std	Std
1	C7	0.01µF	Capacitor, Ceramic, 25V, X7R, 10%	0603	Std	Std
2	C9, C10	47 µF	Capacitor, Ceramic, 10V, X5R, 20%	1210	Std	Std
2	J1, J3	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25 inch	ED555/2DS	OST
1	J2	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
2	JP1, JP2	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
1	L1	1.2µH	Inductor, SMD Shielded Power, 11.8 A, 7.4 mohm	5.3x5.5 mm	XAL5030-122ME	Coilcraft
1	R1	14.3k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	11.5k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	30.9k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	35.7k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R5, R6	Open	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R7	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R8	51.1	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R9	20.0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R10	10.0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
7	TP1, TP3, TP4, TP5, TP6, TP7, TP8	5000	Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100 inch	5000	Keystone
2	TP2, TP9	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
1	U1	TPS54478RTE	IC, DC-DC Converter, 2.95-6 V, 4A	QFN-16	TPS54478RTE	TI
2	–		Shunt, 100-mil, Black	0.100	929950-00	3M
1	–		Label	1.25 x 0.25 inch	THT-13-457-10	Brady
1	–		PCB, 2.5" x 2.5" x 0.062"		HPA375	Any

Notes 1. These assemblies are ESD sensitive, ESD precautions shall be observed.

2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Table 5. TPS54478EVM-037 Bill of Materials (continued)

Count	RefDes	Value	Description	Size	Part Number	MFR

3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.
5. Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per Table 6

Table 6. Label Marking

Text
TPS54478EVM-037

Evaluation Board/Kit Important Notice

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 3 V to 6 V and the output voltage range of 0.6 V to 2.5 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 90°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265