

CD4048B Types

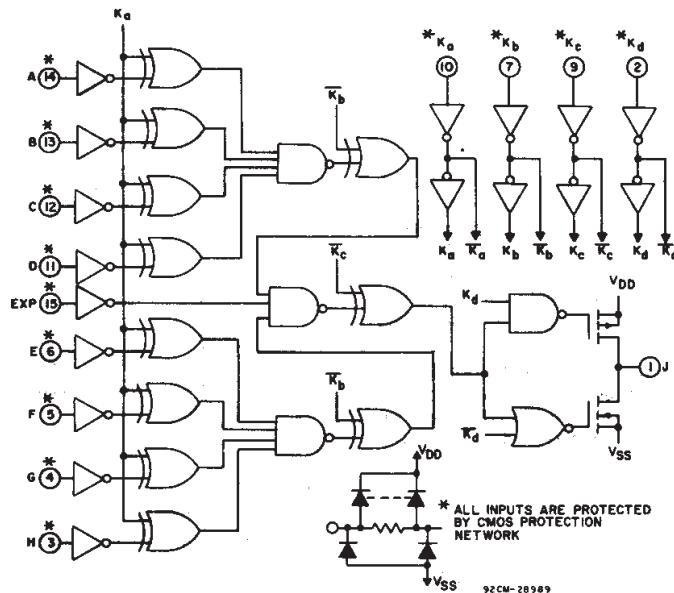


Fig. 2 – Logic diagram.

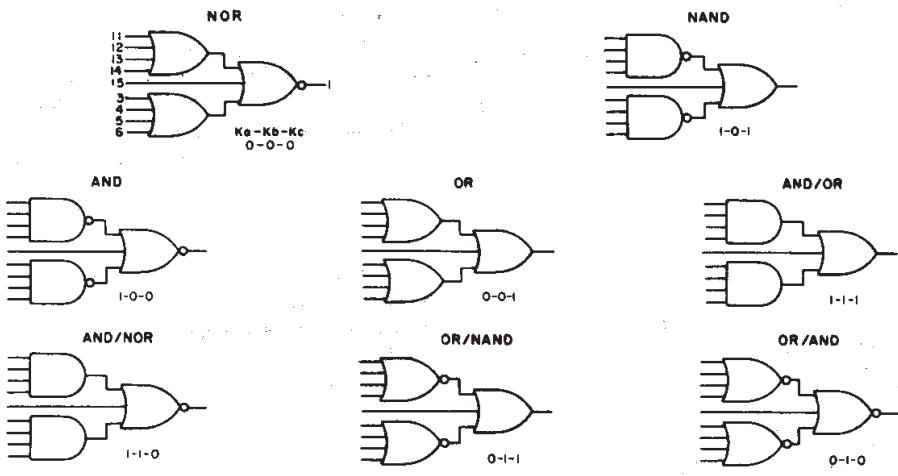


Fig. 3 – Actual-circuit logic configurations.

APPLICATIONS OF EXPAND INPUT

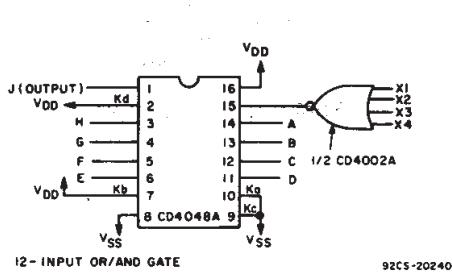


Fig. 4 – 12-input OR/AND gate.

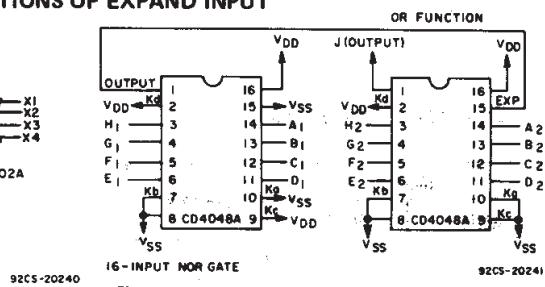


Fig. 5 – 16-input NOR gate.

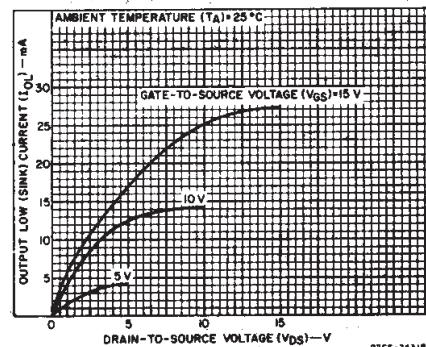


Fig. 6 – Typical output low (sink) current characteristics.

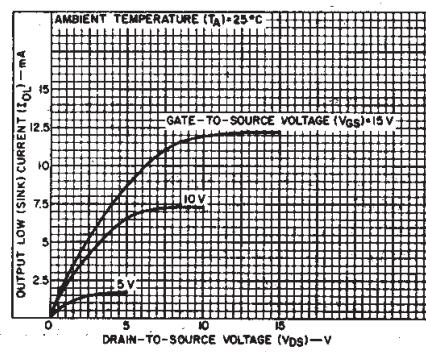


Fig. 7 – Minimum output low (sink) current characteristics.

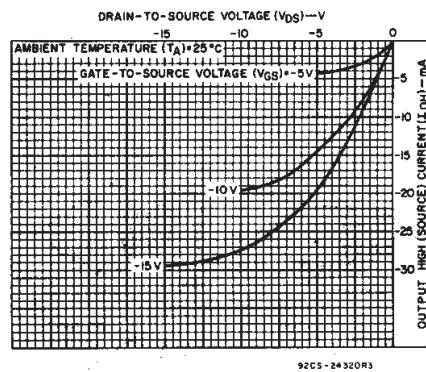


Fig. 8 – Typical output high (source) current characteristics.

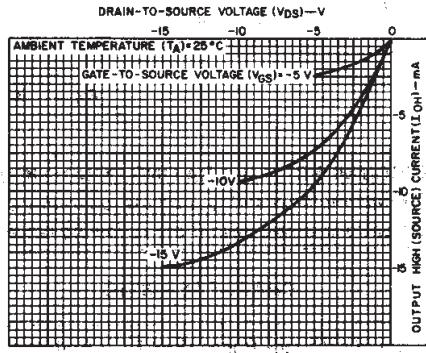


Fig. 9 – Minimum output high (source) current characteristics.

CD4048B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						UNITS	
				+25							
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	—	0,5	5	0,25	0,25	7,5	7,5	—	0,01	0,25	μA
	—	0,10	10	0,5	0,5	15	15	—	0,01	0,5	
	—	0,15	15	1	1	30	30	—	0,01	1	
	—	0,20	20	5	5	150	150	—	0,02	5	
Output Low (Sink) Current I _{OL} Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	—	mA
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	—	
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	—	
Output High (Source) Current, I _{OH} Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	—	mA
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	—	
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	—	
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	—	
Output Voltage: Low-Level, V _{OL} Max.	—	0,5	5	0,05			—	0	0,05	—	V
	—	0,10	10	0,05			—	0	0,05	—	
	—	0,15	15	0,05			—	0	0,05	—	
Output Voltage: High-Level, V _{OH} Min.	—	0,5	5	4,95			4,95	5	—	—	V
	—	0,10	10	9,95			9,95	10	—	—	
	—	0,15	15	14,95			14,95	15	—	—	
Input Low Voltage, V _{IL} Max.	0,5,4,5	—	5	1,5			—	—	1,5	—	V
	1,9	—	10	3			—	—	3	—	
	1,5,13,5	—	15	4			—	—	4	—	
Input High Voltage, V _{IH} Min.	0,5,4,5	—	5	3,5			3,5	—	—	—	V
	1,9	—	10	7			7	—	—	—	
	1,5,13,5	—	15	11			11	—	—	—	
Input Current I _{IN} Max.	—	0,18	18	±0,1	±0,1	±1	±1	—	±10 ⁻⁵	±0,1	μA
3-State Output Current, I _{OUT}	0,18	0,18	18	±0,4	±0,4	±12	±12	—	±10 ⁻⁴	±0,4	μA

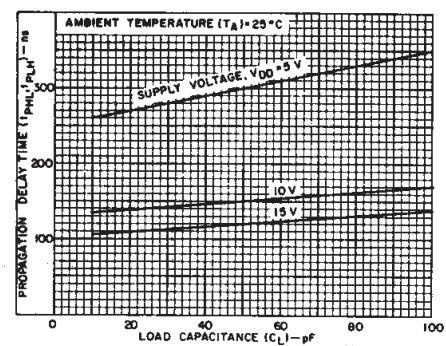


Fig. 10 – Typical propagation delay time (logic inputs to output) as a function of load capacitance.

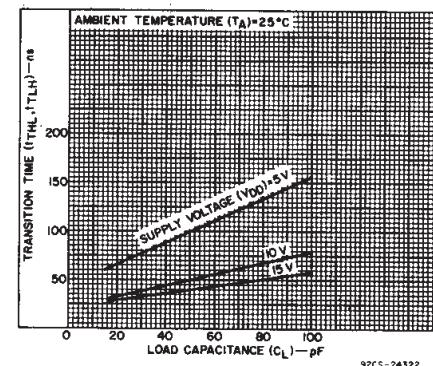


Fig. 11 – Typical transition time vs. load capacitance.

IMPLEMENTATION OF EXPAND INPUT FOR 9 OR MORE INPUTS

OUTPUT FUNCTION	FUNCTION NEEDED AT EXPAND INPUT	OUTPUT BOOLEAN EXPRESSION
NOR	OR	J = (A+B+C+D+E+F+G+H)+(EXP)
OR	OR	J = (A+B+C+D+E+F+G+H)+(EXP)
AND	NAND	J = (A B C D E F G H) · (EXP)
NAND	NAND	J = (A B C D E F G H) · (EXP)
OR/AND	NOR	J = (A+B+C+D) · (E+F+G+H) · (EXP)
OR/NAND	NOR	J = (A+B+C+D) · (E+F+G+H) · (EXP)
AND/NOR	AND	J = (A B C D) + (E F G H) + (EXP)
AND/OR	AND	J = (A B C D) + (E F G H) + (EXP)

Note: (EXP) designates the EXPAND function (i.e., X₁+X₂+...+X_N).

NOTE:
Refer to FUNCTION TRUTH TABLE for connection of unused inputs.

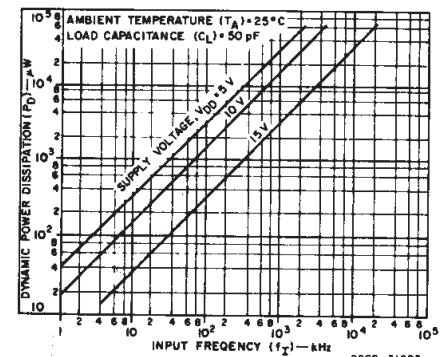


Fig. 12 – Typical power dissipation as a function of input frequency.

CD4048B Types

DYNAMIC CHARACTERISTICS at $T_A=25^\circ\text{C}$, $C_L=50\text{ pF}$, Input $t_r, t_f=20\text{ ns}$,
 $R_L=200\text{ k}\Omega$ unless otherwise specified

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
		V _{DD} V	All Package Types Typ. Max.	
Propagation Delay: t_{PHL}, t_{PLH} Inputs to Output and K _a to Output		5 10 15	300 150 120	ns
K _b to Output		5 10 15	225 85 55	ns
K _c to Output		5 10 15	140 50 40	ns
Expand Input to Output		5 10 15	190 90 65	ns
3-State Propagation Delay: K _d to Output t_{PHZ}, t_{PLZ} t_{PZH}, t_{PZL}	$R_L=1\text{ k}\Omega$ See Fig. 21	5 10 15	80 35 25	ns
Transition Time: t_{THL}, t_{TLH}		5 10 15	100 50 40	ns
Input Capacitance: C_I	Any Input		5	7
3-State Output Capacitance			5	10

FUNCTION TRUTH TABLE

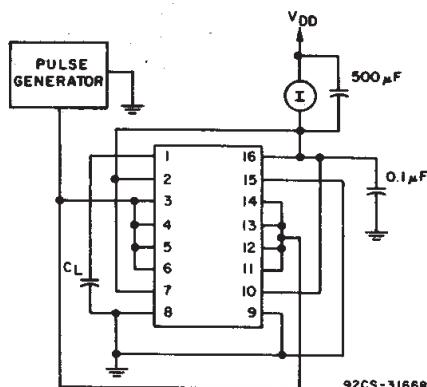


Fig. 13 – Dynamic power dissipation test circuit.

OUTPUT FUNCTION	BOOLEAN EXPRESSION	K _a	K _b	K _c	UNUSED INPUT*
NOR	$J=A+B+C+D+E+F+G+H$	0	0	0	V _{SS}
OR	$J=A+B+C+D+E+F+G+H$	0	0	1	V _{SS}
OR/AND	$J=(A+B+C+D) \cdot (E+F+G+H)$	0	1	0	V _{SS}
OR/NAND	$J=(A+B+C+D) \cdot (E+F+G+H)$	0	1	1	V _{SS}
AND	$J=ABCDEF GH$	1	0	0	V _{DD}
NAND	$J=ABCDEF GH$	1	0	1	V _{DD}
AND/NOR	$J=\overline{ABCD}+EFGH$	1	1	0	V _{DD}
AND/OR	$J=ABCD+EFGH$	1	1	1	V _{DD}
K _d =1 Normal Inverter Action					
K _d =0 High Impedance Output					

EXPAND Input=0

* See Figs. 1,2,3,4, and 5.

TEST CIRCUITS - STATIC MEASUREMENTS

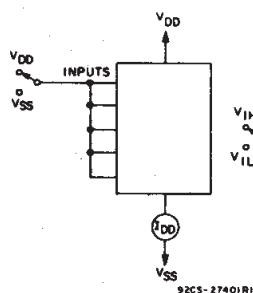


Fig. 14 – Quiescent device current test circuit.

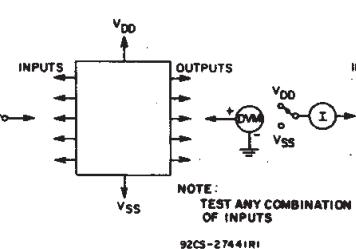


Fig. 15 – Input voltage test circuit.

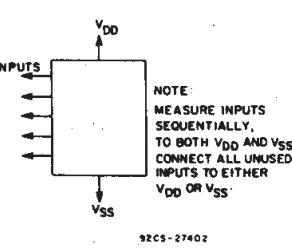


Fig. 16 – Input current test circuit.

CD4048B Types

TEST CIRCUITS - DYNAMIC MEASUREMENTS

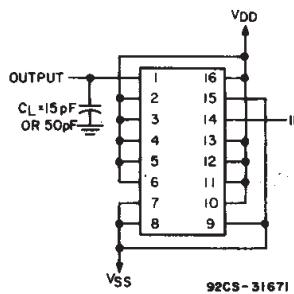


Fig. 17 – Test circuit for t_{PHL} , t_{THL} , and t_{TLH} (AND) measurements.

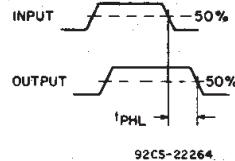


Fig. 18 – Waveforms for t_{PHL} and t_{PHL} (AND).

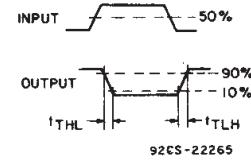


Fig. 19 – Waveforms for t_{THL} and t_{TLH} (AND).

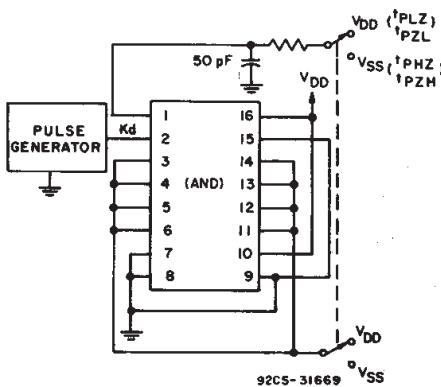


Fig. 20 – Test circuit for t_{PZL} , t_{PZH} , t_{PLZ} , and t_{PHZ} (AND).

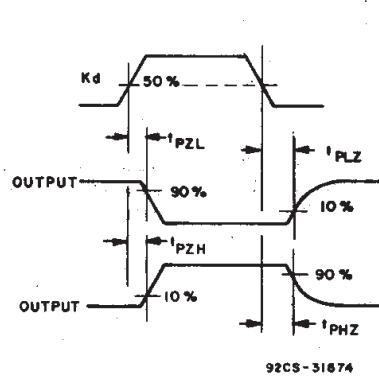
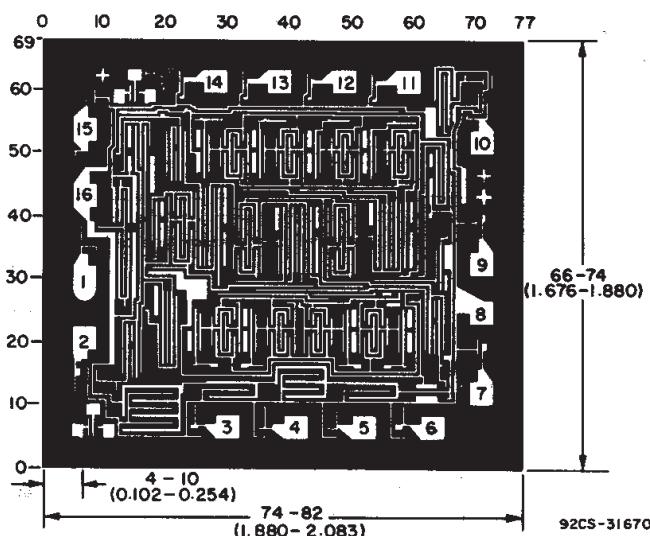


Fig. 21 – Waveforms for t_{PZL} , t_{PZH} , t_{PLZ} , and t_{PHZ} (AND).



Dimensions and pad layout for CD4048BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4048BE	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-55 to 125	CD4048BE	Samples
CD4048BF3A	ACTIVE	CDIP	J	16	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	CD4048BF3A	Samples
CD4048BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4048BM	Samples
CD4048BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4048BM	Samples
CD4048BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM048B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

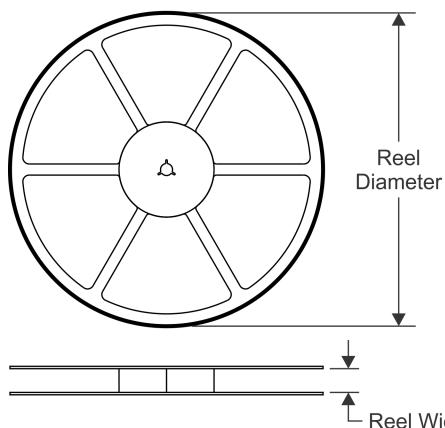
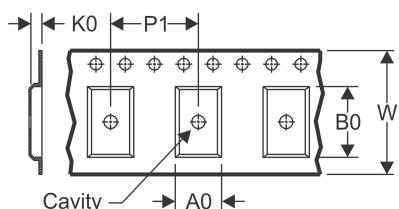
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4048B, CD4048B-MIL :

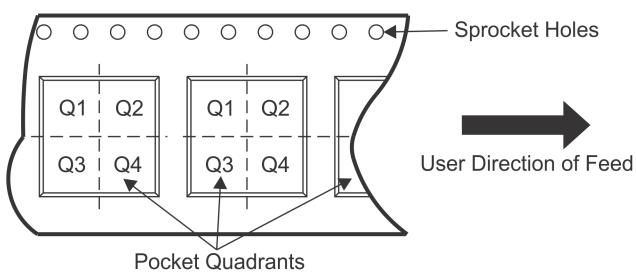
- Catalog: [CD4048B](#)
- Military: [CD4048B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

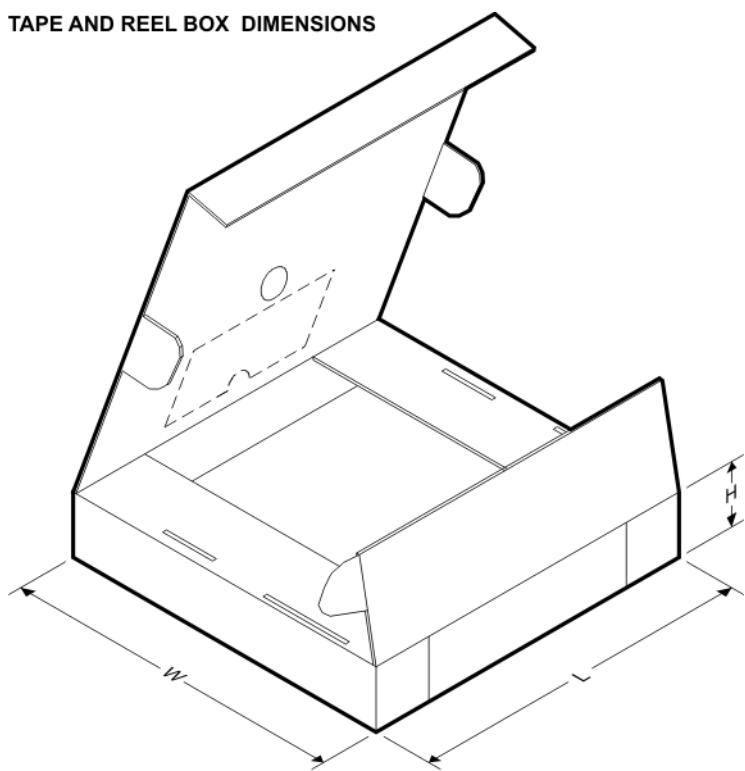
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4048BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

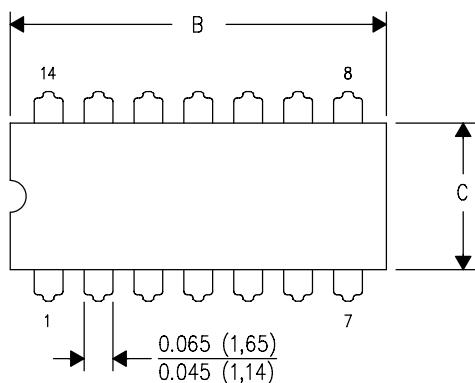
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4048BM96	SOIC	D	16	2500	333.2	345.9	28.6

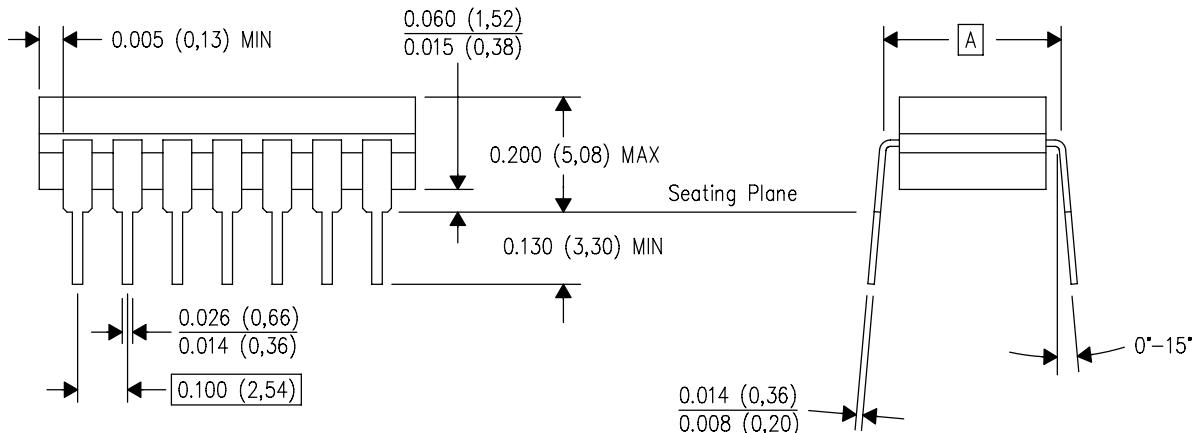
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



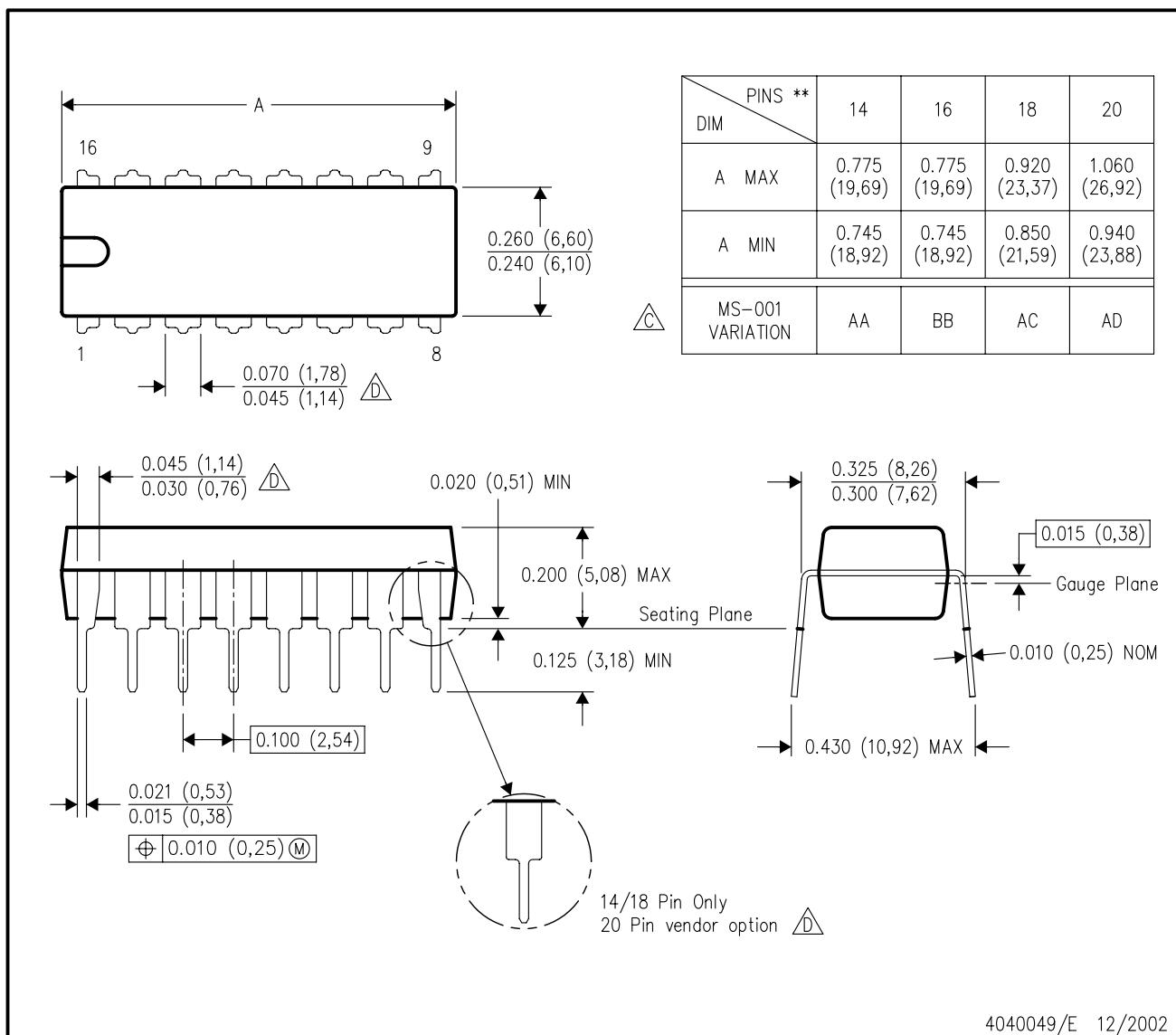
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

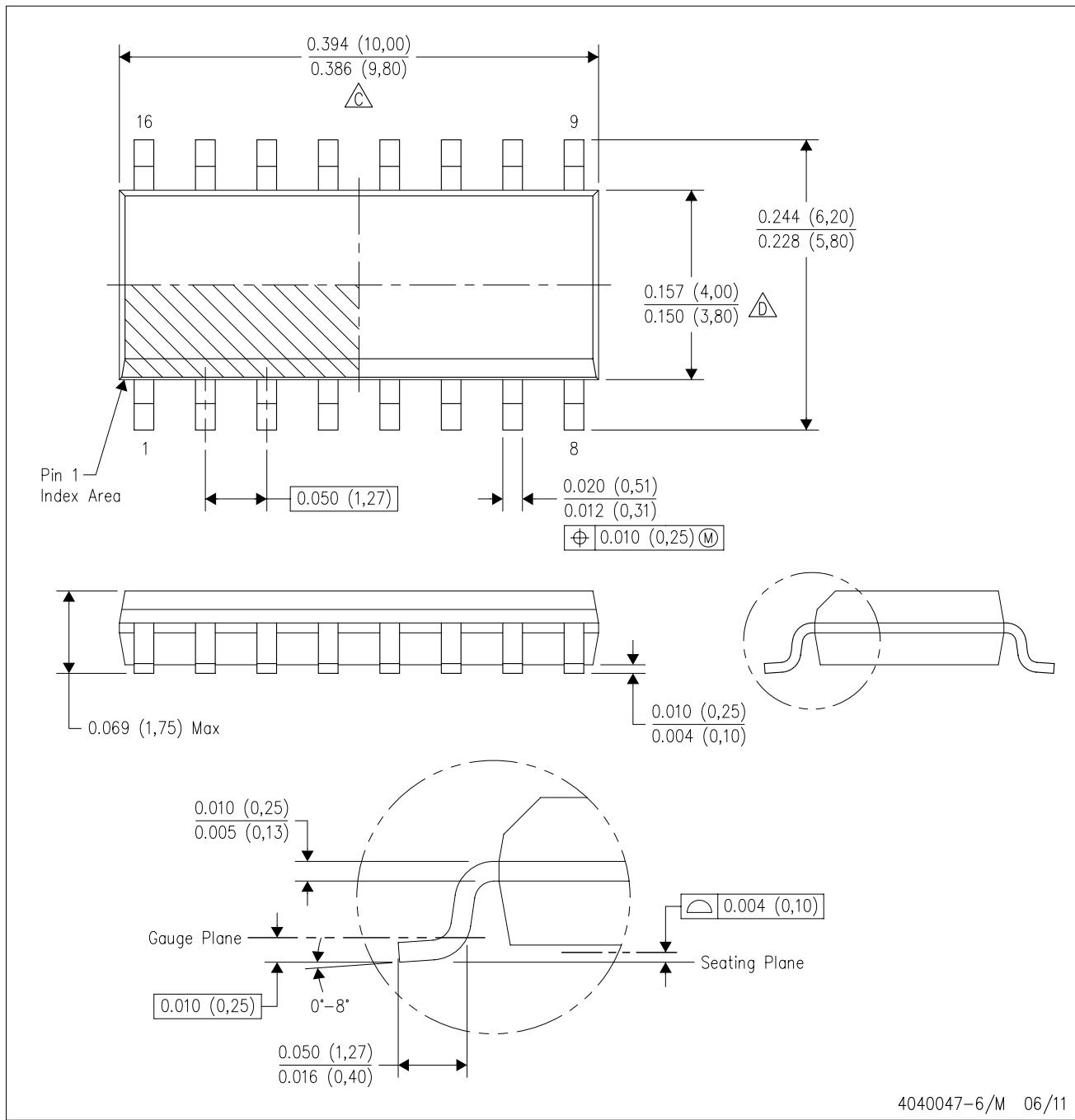
16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

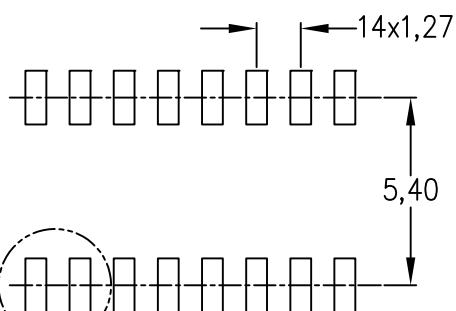
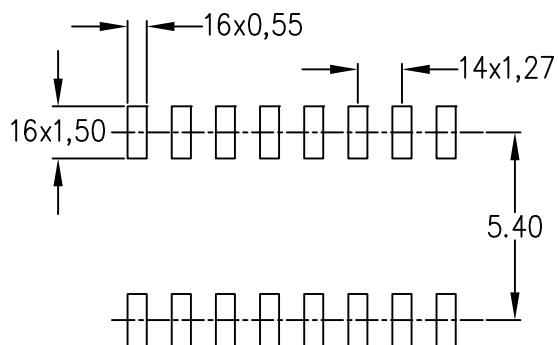
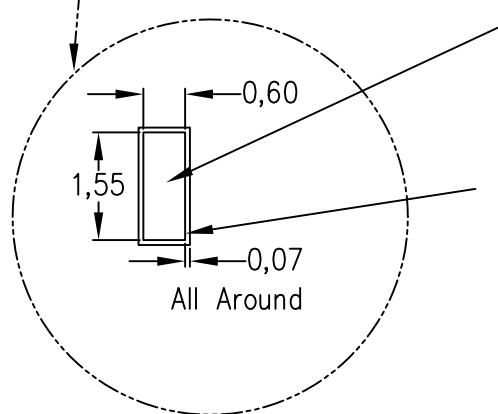
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

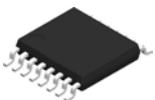
4211283-4/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

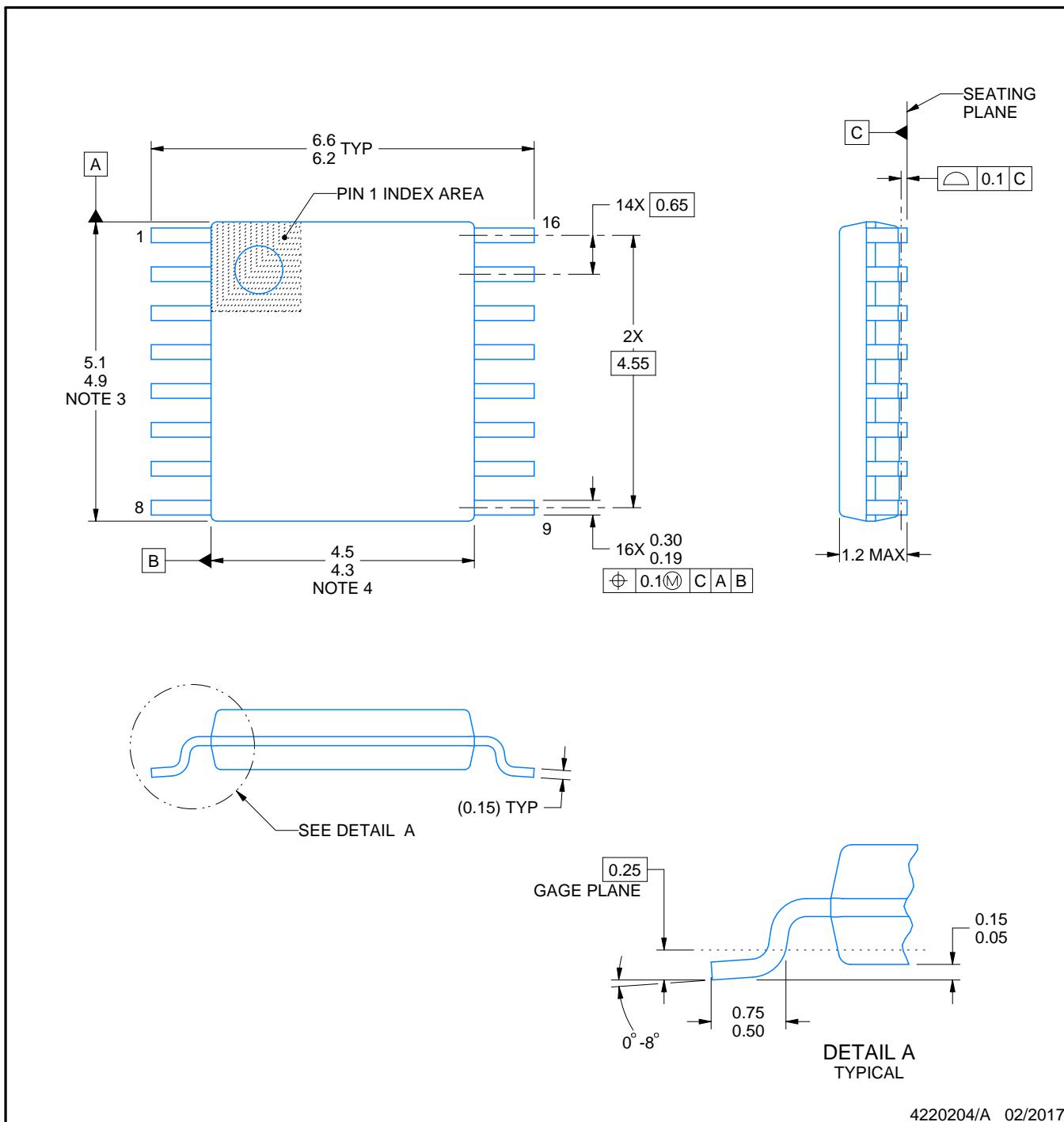
PACKAGE OUTLINE

PW0016A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

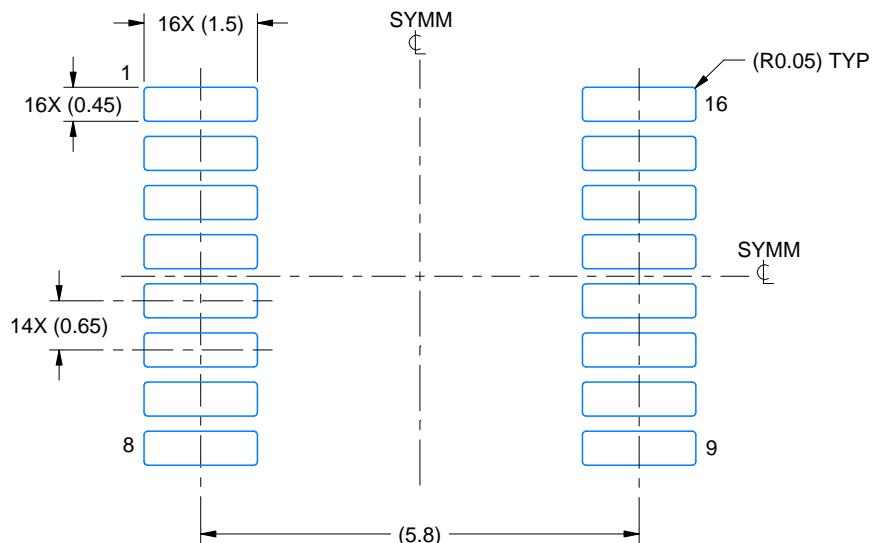
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

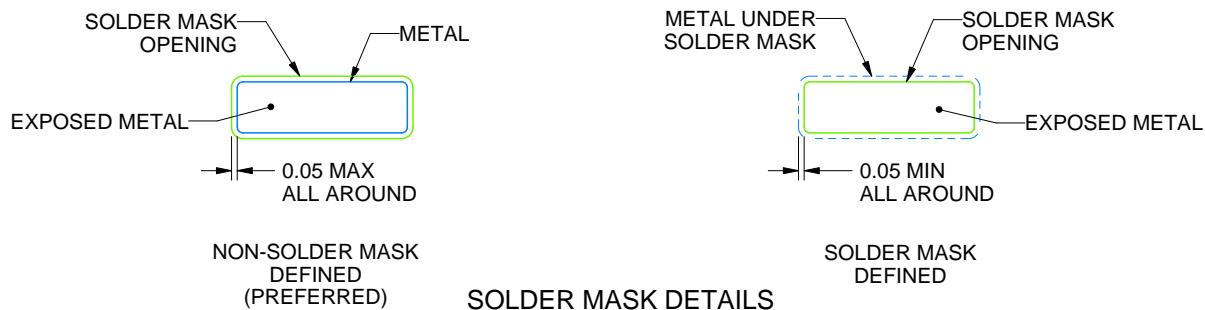
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

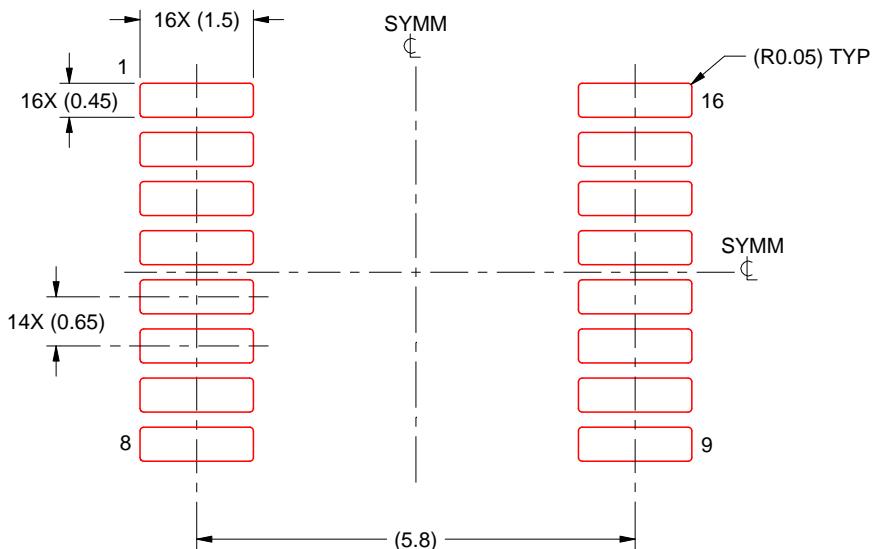
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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