

FEATURES

- Guaranteed over the industrial temperature range:
–40°C to +85°C
- Pin-for-pin; plug-in replacement to MC100EPT21D/DT
- 3.3V power supply
- 1.9ns typical propagation delay
- 275MHz f_{MAX} (Clock)
- Differential LVPECL inputs
- 24mA LVTTL output
- Flow-through pinout
- Q output will default LOW with inputs open
- V_{BB} output
- Available in 8-pin MSOP and SOIC packages

APPLICATIONS

- ASIC/FPGA interface
- Legacy interface
- Precision differential-to-general purpose, single-ended translation



ECL Pro™

DESCRIPTION

The SY100EPT21L is a single, differential LVPECL-to-LVTTL translator using a single +3.3V power supply. Because low voltage positive ECL (LVPECL) levels are used, only +3.3V and ground are required. The small outline 8-pin SOIC package and low-skew, single-gate design make the EPT21L ideal for applications that require the translation of a clock or data signal where minimal space, low power, and low cost are critical.

V_{BB} allows a differential, single-ended, or AC-coupled interface to the device. If used, the V_{BB} output should be bypassed to V_{CC} with 0.01 μ F capacitor.

Under open input conditions, the /D will be biased at a $V_{CC}/2$ voltage level and the D input will be pulled to ground. This condition will force the Q output low to provide added stability.

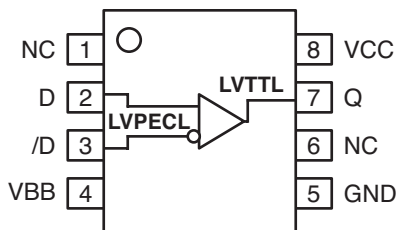
The 100EPT is compatible with positive ECL 100K logic levels. For applications that require the smallest footprint, consider the SY89321L in an ultra-small (2mm \times 2mm) 8-pin MLF™ package.

All support documentation can be found on Micrel's web site at: www.micrel.com.

CROSS REFERENCE TABLE

| Micrel | ON Semiconductor |
|-----------------|------------------|
| SY100EPT21LZI | MC100EPT21D |
| SY100EPT21LZITR | MC100EPT21DR2 |
| SY100EPT21LKI | MC100EPT21DT |
| SY100EPT21LKITR | MC100EPT21DTR2 |

PACKAGE/ORDERING INFORMATION



**8-Pin SOIC (Z8-1)
8-Pin MSOP (K8-1)**

Ordering Information⁽¹⁾

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|-----------------------------------|--------------|-----------------|--|----------------|
| SY100EPT21LZC | Z8-1 | Commercial | XEP21L | Sn-Pb |
| SY100EPT21LZCTR ⁽²⁾ | Z8-1 | Commercial | XEP21L | Sn-Pb |
| SY100EPT21LKC | K8-1 | Commercial | XP21 | Sn-Pb |
| SY100EPT21LKCTR ⁽²⁾ | K8-1 | Commercial | XP21 | Sn-Pb |
| SY100EPT21LZI | Z8-1 | Industrial | XEP21L | Sn-Pb |
| SY100EPT21LZITR ⁽²⁾ | Z8-1 | Industrial | XEP21L | Sn-Pb |
| SY100EPT21LKI | K8-1 | Industrial | XP21 | Sn-Pb |
| SY100EPT21LKITR ⁽²⁾ | K8-1 | Industrial | XP21 | Sn-Pb |
| SY100EPT21LZG ⁽³⁾ | Z8-1 | Industrial | XEP21L with Pb-Free bar-line indicator | Pb-Free NiPdAu |
| SY100EPT21LZGTR ^(2, 3) | Z8-1 | Industrial | XEP21L with Pb-Free bar-line indicator | Pb-Free NiPdAu |
| SY100EPT21LKG ⁽³⁾ | K8-1 | Industrial | XP21 with Pb-Free bar-line indicator | Pb-Free NiPdAu |
| SY100EPT21LKGTR ^(2, 3) | K8-1 | Industrial | XP21 with Pb-Free bar-line indicator | Pb-Free NiPdAu |

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

PIN DESCRIPTION

| Pin Number | Pin Name | Pin Function |
|------------|----------|---------------------------------|
| 1 | NC | No Connect. |
| 2, 3 | D, /D | Differential LVPECL Input Pair. |
| 4 | VBB | Output Reference Voltage. |
| 5 | GND | Ground. |
| 6 | NC | No Connect. |
| 7 | Q | LVTTL Output. |
| 8 | VCC | Positive Supply. |

TRUTH TABLE

| D | /D | Q |
|------|------|---|
| L | H | L |
| H | L | H |
| Open | Open | L |

Absolute Maximum Ratings⁽¹⁾

Power Supply Voltage (V_{CC}) -0.5 to +3.8V
 PECL Input Voltage (V_{IN}) 0V to $V_{CC} + 0.5V$
 Voltage Applied to Output at HIGH State (V_{OUT}) -0.5 to V_{CC}
 Current Applied to Output at LOW State (I_{OUT})
 Twice the Rated I_{OL} (mA)
 Lead Temperature (soldering, 20 sec.) +260°C
 Storage Temperature (T_S) -65°C to +150°C

Operating Ratings⁽²⁾

Power Supply Voltage (V_{CC}) -0.5 to +3.8V
 Ambient Temperature (T_A) -40°C to +85°C
 Package Thermal Resistance
 SOIC (θ_{JA}) multi-layer board 113°C/W
 MSOP (θ_{JA}) multi-layer board 124°C/W

LVTTTL OUTPUT DC ELECTRICAL CHARACTERISTICS

$V_{CC} = +3.3V$, GND = 0V; $T_A = -40^\circ C$ to $+85^\circ C$; unless noted.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------|------------------------------|-------------------------|-----|-----|------|-------|
| I_{OS} | Output Short Circuit Current | $V_{OUT} = 0V$ | -80 | | -275 | mA |
| I_{CC} | Power Supply Current | | | 14 | 20 | mA |
| V_{OH} | Output HIGH Voltage | $I_{OH} = -3.0mA^{(3)}$ | 2.3 | | | V |
| V_{OL} | Output LOW Voltage | $I_{OL} = 24mA$ | | | 0.5 | V |

LVPECL INPUT DC ELECTRICAL CHARACTERISTICS

$V_{CC} = +3.3V$, GND = 0V; $T_A = -40^\circ C$ to $+85^\circ C$; unless noted.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------|--------------------|---------------|------|------|------|---------|
| I_{IH} | Input HIGH Current | | | | 150 | μA |
| I_{IL} | Input LOW Current | D | 0.5 | | | μA |
| | | /D | -300 | | | μA |
| V_{IH} | Input HIGH Voltage | Note 3 | 2135 | | 2420 | V |
| V_{IL} | Input LOW Voltage | Note 3 | 1490 | | 1825 | V |
| V_{BB} | Reference Output | Note 3 | 1920 | 1980 | 2040 | V |

Notes:

1. Permanent device damage may occur if ratings in the absolute maximum ratings section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. These values are for $V_{CC} = 3.3V$. Level Specifications will vary 1:1 V_{CC} .

AC ELECTRICAL CHARACTERISTICS

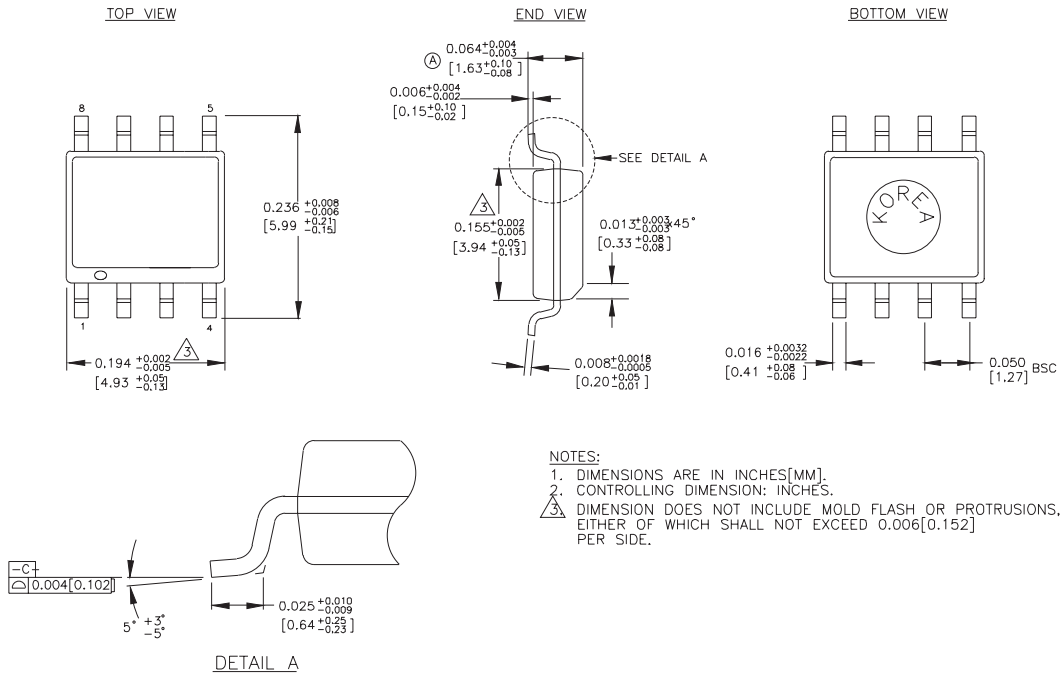
$V_{CC} = +3.0V$ to $+3.6V$, $GND = 0V$; $T_A = -40^{\circ}C$ to $+85^{\circ}C$; unless noted.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|------------|---|-----------------------|-----|-----|----------|-------|
| t_{PD} | Propagation Delay | $C_L = 20pF$ | 1.5 | 1.9 | 2.5 | ns |
| t_{skpp} | Part-to-Part Skew | $C_L = 20pF^{(4, 5)}$ | | | 0.5 | ns |
| f_{MAX} | Maximum Input Frequency | $C_L = 20pF^{(6)}$ | 275 | | | MHz |
| V_{CMR} | Common Mode Range | | 1.2 | | V_{CC} | V |
| V_{PP} | Minimum Peak-to-Peak Input | Note 7 | 100 | | | mV |
| t_r, t_f | Output Rise/Fall Time (1.0V to 2.0V) | $C_L = 20pF$ | 0.5 | | 1.0 | ns |

Notes:

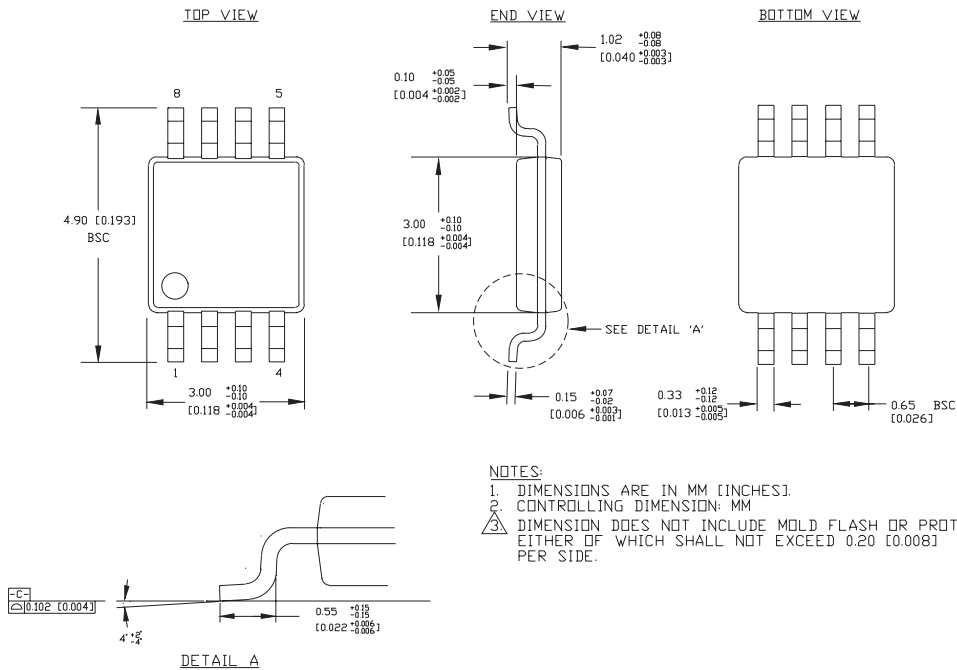
4. Part-to-part skew considering HIGH-to-HIGH transitions at common V_{CC} level.
5. These parameters are guaranteed but not tested.
6. The f_{MAX} value is specified as the minimum guaranteed maximum frequency. Actual operational maximum frequency may be greater.
7. 100mV input guarantees full logic at output.

8-PIN PLASTIC SOIC (Z8-1)



Rev. 03

8-PIN MSOP (K8-1)



Rev. 01

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