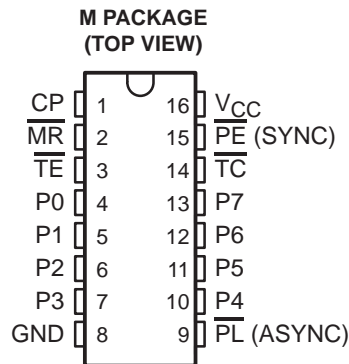


**CD74HC40103-EP**  
**HIGH-SPEED CMOS LOGIC**  
**8-STAGE SYNCHRONOUS DOWN COUNTER**  
SCLS548 – DECEMBER 2003

- **Controlled Baseline**
  - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –40°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Synchronous or Asynchronous Preset**
- **Cascadable in Synchronous or Ripple Mode**
- **Fanout (Over Temperature Range)**
  - Standard Outputs . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . 15 LSTTL Loads
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **V<sub>CC</sub> Voltage = 2 V to 6 V**
- **High Noise Immunity N<sub>IL</sub> or N<sub>IH</sub> = 30% of V<sub>CC</sub>; V<sub>CC</sub> = 5 V**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.



### description/ordering information

The CD74HC40103 is manufactured with high-speed silicon-gate technology and consists of an 8-stage synchronous down counter with a single output, which is active when the internal count is zero. The device contains a single 8-bit binary counter. Each device has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the terminal count ( $\overline{TC}$ ) output are active-low logic.

In normal operation, the counter is decremented by one count on each positive transition of the clock (CP) output. Counting is inhibited when the terminal enable ( $\overline{TE}$ ) input is high.  $\overline{TC}$  goes low when the count reaches zero, if  $\overline{TE}$  is low, and remains low for one full clock period.

When the synchronous preset enable ( $\overline{PE}$ ) input is low, data at the P0–P7 inputs are clocked into the counter on the next positive clock transition, regardless of the state of  $\overline{TE}$ . When the asynchronous preset enable ( $\overline{PL}$ ) input is low, data at the P0–P7 inputs asynchronously are forced into the counter, regardless of the state of the  $\overline{PE}$ ,  $\overline{TE}$ , or CP inputs. Inputs P0–P7 represent a single 8-bit binary word for the CD74HC40103. When the master reset ( $\overline{MR}$ ) input is low, the counter asynchronously is cleared to its maximum count of 255<sub>10</sub>, regardless of the state of any other input. The precedence relationship between control inputs is indicated in the truth table.

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – M	Tape and reel	CD74HC40103QM96EP	HC40103QEP

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated

# CD74HC40103-EP HIGH-SPEED CMOS LOGIC 8-STAGE SYNCHRONOUS DOWN COUNTER

SCLS548 – DECEMBER 2003

## description/ordering information (continued)

If all control inputs except  $\overline{TE}$  are high at the time of zero count, the counters jump to the maximum count, giving a counting sequence of  $100_{16}$  or  $256_{10}$  clock pulses long.

The CD74HC40103 may be cascaded using the  $\overline{TE}$  input and the  $\overline{TC}$  output in either synchronous or ripple mode. These circuits have the low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low-power Schottky TTL circuits and can drive up to ten LSTTL loads.

FUNCTION TABLE†

CONTROL INPUTS				PRESET MODE	ACTION
$\overline{MR}$	$\overline{PL}$	$\overline{PE}$	$\overline{TE}$		
H	H	H	H	Synchronous	Inhibit counter
H	H	H	L		Count down
H	H	L	X		Preset on next positive clock transition
H	L	X	X	Asynchronous	Preset asynchronously
L	X	X	X		Clear to maximum count

† See Figure 2 for timing diagram.

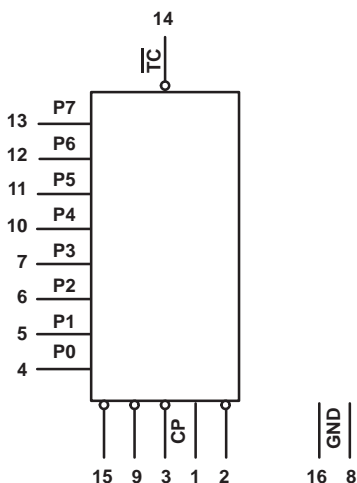
NOTE: H = high voltage level, L = low voltage level, X = don't care

Clock connected to clock input

Synchronous operation: changes occur on negative-to-positive clock transitions.

Load inputs: MSB = P7, LSB = P0

## logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ (see Note 1)	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	±20 mA
Source or sink current per output pin, $I_O$ ( $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2)	73°C/W
Maximum junction temperature, $T_J$	150°C
Lead temperature (during soldering):	
At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max	300°C
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages referenced to GND unless otherwise specified.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 3)**

		MIN	MAX	UNIT	
$V_{CC}$	Supply voltage	2	6	V	
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5	V	
		$V_{CC} = 4.5$ V	3.15		
		$V_{CC} = 6$ V	4.2		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0.5	V	
		$V_{CC} = 4.5$ V	1.35		
		$V_{CC} = 6$ V	1.8		
$V_I$	Input voltage	0	$V_{CC}$	V	
$V_O$	Output voltage	0	$V_{CC}$	V	
$t_t$	Input transition (rise and fall) time	$V_{CC} = 2$ V	0	1000	ns
		$V_{CC} = 4.5$ V	0	500	
		$V_{CC} = 6$ V	0	400	
$T_A$	Operating free-air temperature	-40	125	°C	

NOTES: 3. All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**CD74HC40103-EP**  
**HIGH-SPEED CMOS LOGIC**  
**8-STAGE SYNCHRONOUS DOWN COUNTER**

SCLS548 – DECEMBER 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		I <sub>O</sub> (mA)	V <sub>CC</sub>	T <sub>A</sub> = 25°C		MIN	MAX	UNIT
					MIN	MAX			
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	CMOS loads	-0.02	2 V	1.9		1.9	V	
			-0.02	4.5 V	4.4		4.4		
			-0.02	6 V	5.9		5.9		
		TTL loads	-4	4.5 V	3.98		3.7		
			-5.2	6 V	5.48		5.2		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	CMOS loads	0.02	2 V		0.1		0.1	V
			0.02	4.5 V		0.1		0.1	
			0.02	6 V		0.1		0.1	
		TTL loads	4	4.5 V		0.26		0.4	
			5.2	6 V		0.26		0.4	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND			6 V		±0.1		±1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		0	6 V		8		160	μA
C <sub>IN</sub>	C <sub>L</sub> = 50 pF					10		10	pF



**CD74HC40103-EP**  
**HIGH-SPEED CMOS LOGIC**  
**8-STAGE SYNCHRONOUS DOWN COUNTER**  
SCLS548 – DECEMBER 2003

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER		V <sub>CC</sub>	T <sub>A</sub> = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t <sub>w</sub>	Pulse duration	CP	2 V	165	250	ns	
			4.5 V	33	50		
			6 V	28	43		
	$\overline{\text{PL}}$	2 V	125	190			
		4.5 V	25	38			
		6 V	21	32			
	$\overline{\text{MR}}$	2 V	125	190			
		4.5 V	25	38			
		6 V	21	32			
f <sub>max</sub>	CP frequency (see Note 4)	2 V	3	2	MHz		
		4.5 V	15	10			
		6 V	18	12			
t <sub>su</sub>	P to CP	2 V	100	150	ns		
		4.5 V	20	30			
		6 V	17	26			
	$\overline{\text{PE}}$ to CP	2 V	75	110			
		4.5 V	15	22			
		6 V	13	19			
	$\overline{\text{TE}}$ to CP	2 V	150	225			
		4.5 V	30	45			
		6 V	26	38			
	To CP, $\overline{\text{MR}}$ inactive	2 V	50	75			
		4.5 V	10	15			
		6 V	9	13			
t <sub>h</sub>	P to CP	2 V	5	5	ns		
		4.5 V	5	5			
		6 V	5	5			
	$\overline{\text{TE}}$ to CP	2 V	0	0			
		4.5 V	0	0			
		6 V	0	0			
	$\overline{\text{PE}}$ to CP	2 V	2	2			
		4.5 V	2	2			
		6 V	2	2			

NOTE 4: Noncascaded operation only. With cascaded counters, clock-to-terminal count propagation delays, count enables ( $\overline{\text{PE}}$  or  $\overline{\text{TE}}$ ) to clock setup times, and count enables ( $\overline{\text{PE}}$  or  $\overline{\text{TE}}$ ) to clock hold times determine maximum clock frequency. For example, with these HC devices:

$$\text{CP } f_{\text{max}} = \frac{1}{\text{CP to TC prop delay} + \overline{\text{TE}} \text{ to CP setup time} + \overline{\text{TE}} \text{ to CP hold time}} = \frac{1}{60 + 30 + 0} \approx 11 \text{ MHz}$$

**CD74HC40103-EP**  
**HIGH-SPEED CMOS LOGIC**  
**8-STAGE SYNCHRONOUS DOWN COUNTER**

SCLS548 – DECEMBER 2003

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT	
					MIN	TYP	MAX				
t <sub>pd</sub>	CP	$\overline{TC}$ (asynchronous preset)	C <sub>L</sub> = 50 pF	2 V		300		450	ns		
				4.5 V		60	90				
				6 V		51	77				
			C <sub>L</sub> = 15 pF	5 V	25						
				$\overline{TC}$ (synchronous preset)	C <sub>L</sub> = 50 pF	2 V		300			450
						4.5 V		60		90	
		6 V				51	77				
		C <sub>L</sub> = 15 pF	5 V		25						
			$\overline{TE}$		C <sub>L</sub> = 50 pF	2 V		200			300
						4.5 V		40		60	
		6 V				34	51				
		C <sub>L</sub> = 15 pF		5 V	17						
	$\overline{PL}$			C <sub>L</sub> = 50 pF	2 V		275			415	
					4.5 V		55	83			
		6 V			47	71					
		C <sub>L</sub> = 15 pF	5 V	23							
			$\overline{MR}$	C <sub>L</sub> = 50 pF	2 V		275			415	
					4.5 V		55	83			
	6 V				47	71					
	C <sub>L</sub> = 15 pF	5 V		23							
		C <sub>L</sub> = 50 pF		2 V		75		110			
				4.5 V		15	22				
	6 V			13	19						
	t <sub>t</sub>			C <sub>L</sub> = 50 pF	2 V		75			110	ns
			C <sub>L</sub> = 50 pF	4.5 V		15		22			
			C <sub>L</sub> = 50 pF	6 V		13		19			
f <sub>max</sub>	CP		C <sub>L</sub> = 15 pF	5 V		25			MHz		

operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C, input t<sub>r</sub>, t<sub>f</sub> = 6 ns

PARAMETER	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance (see Note 5)	25	pF

NOTE 5: C<sub>pd</sub> is used to determine the dynamic power consumption per package.

$$P_D = (C_{pd} \times V_{CC}^2 \times f_i) + (C_L \times V_{CC}^2 \times f_o)$$

f<sub>i</sub> = input frequency

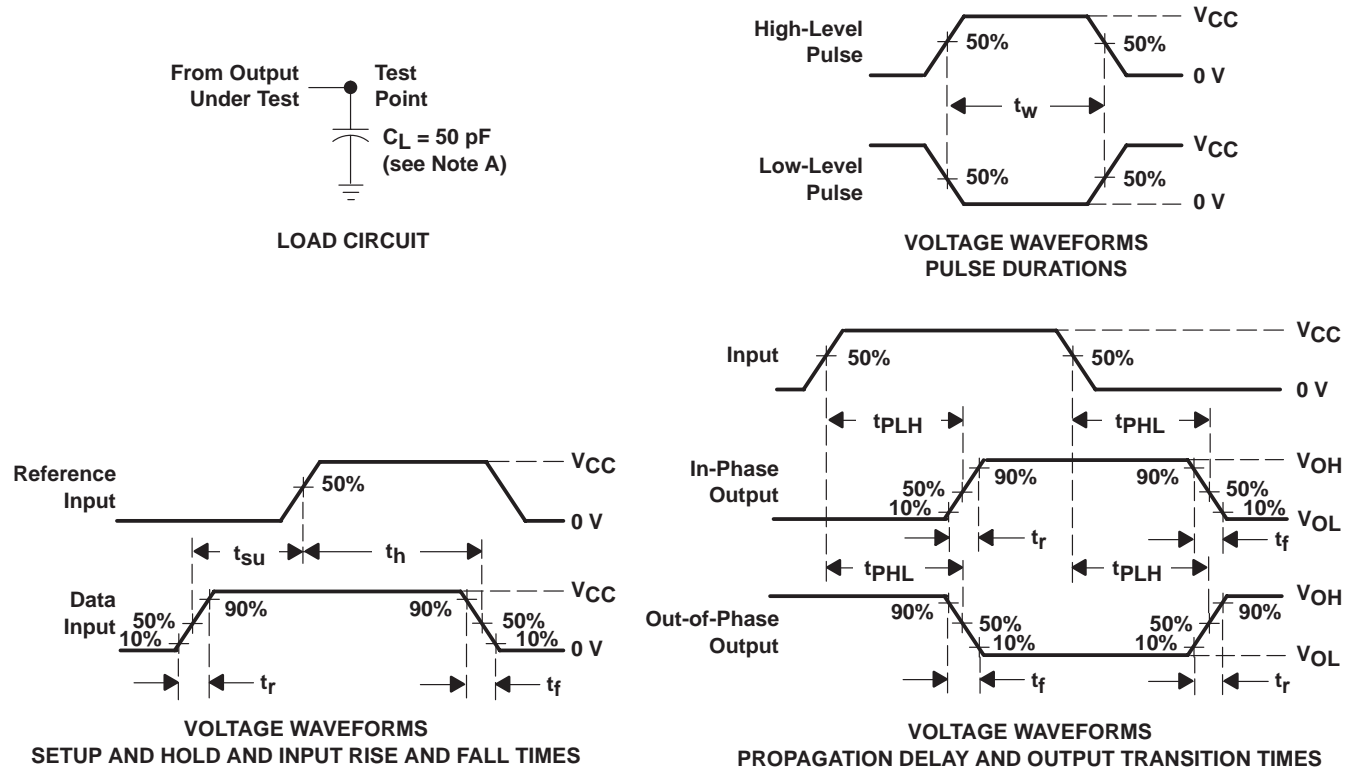
f<sub>o</sub> = output frequency

C<sub>L</sub> = output load capacitance

V<sub>CC</sub> = supply voltage



**PARAMETER MEASUREMENT INFORMATION**



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - C. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

**CD74HC40103-EP**  
**HIGH-SPEED CMOS LOGIC**  
**8-STAGE SYNCHRONOUS DOWN COUNTER**  
 SCLS548 – DECEMBER 2003

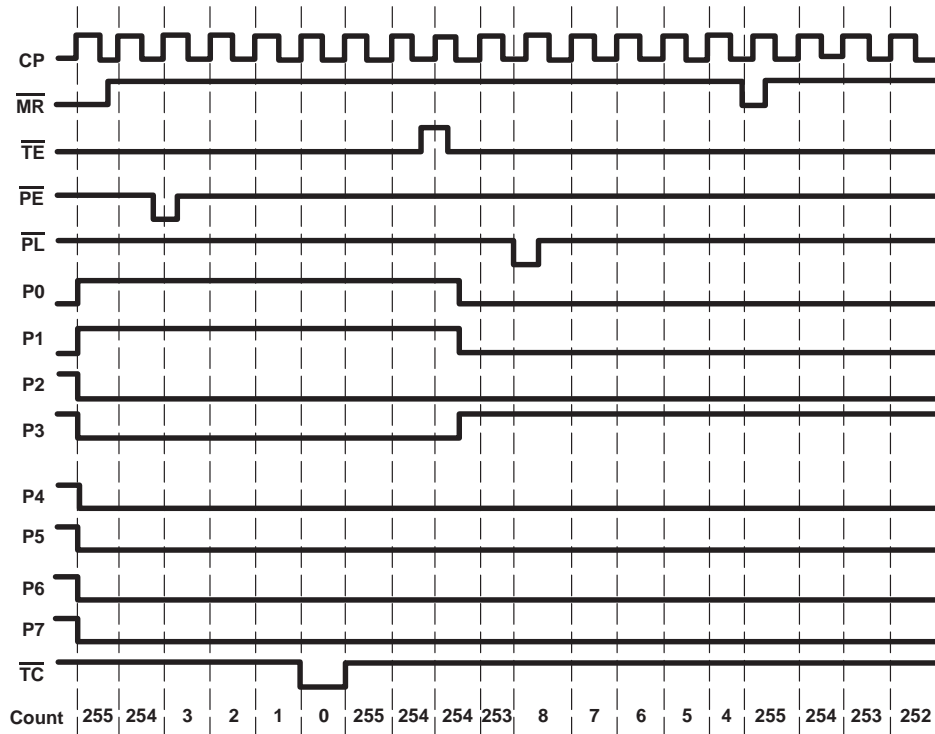


Figure 2. Timing Diagram



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC40103QM96EP	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC40103QEP	<a href="#">Samples</a>
V62/04702-01XE	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC40103QEP	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

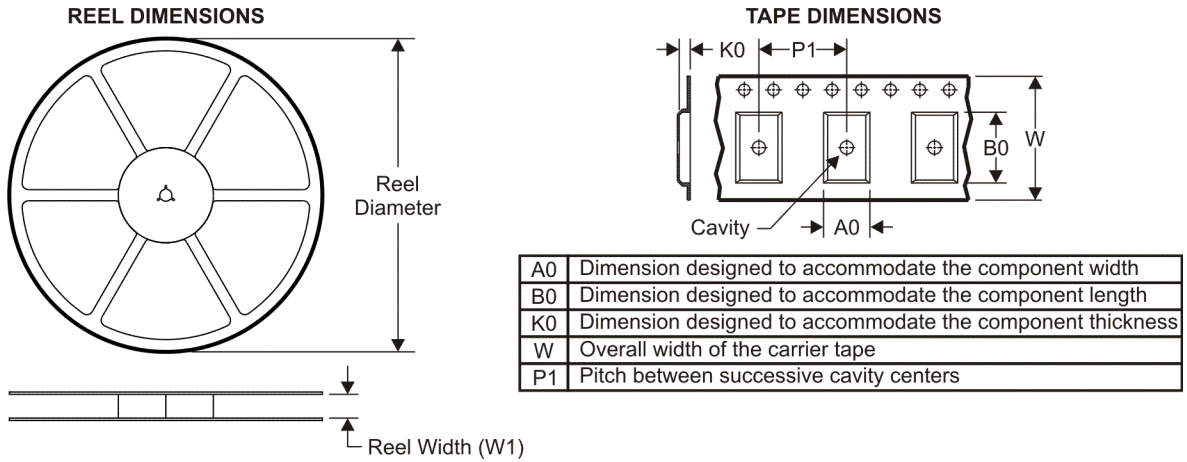
**OTHER QUALIFIED VERSIONS OF CD74HC40103-EP :**

- Catalog: [CD74HC40103](#)
- Military: [CD54HC40103](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC40103QM96EP	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC40103QM96EP	SOIC	D	16	2500	333.2	345.9	28.6

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated