AUTOMOTIVE LOW-DROPOUT VOLTAGE REGULATORS

Check for Samples: TL750Mxx-Q1, TL751Mxx-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Low Dropout Voltage, Less Than 0.6 V at 750 mA**
- **Low Quiescent Current**
- **TTL- and CMOS-Compatible Enable on TL751M Series**
- **Load-Dump Protection**
- **Overvoltage Protection**
- **Internal Thermal Overload Protection**
- **Internal Overcurrent-Limiting Circuitry**

DESCRIPTION

The TL750M and TL751M series are low-dropout positive voltage regulators specifically designed for automotive applications. The TL750M and TL751M series incorporate onboard overvoltage and current-limiting protection circuitry to protect the devices and the regulated system. Both series are fully protected against load-dump and reverse-battery conditions. Load-dump protection is up to a maximum of 60 V at the input of the device. Low quiescent current, even during full-load conditions, makes the TL750M and TL751M series ideal for use in applications that are permanently connected to the vehicle battery.

The TL750M and TL751M series offers 5-V, 8-V, and 12-V options. The TL751M series has the addition of an enable (ENABLE) input. The ENABLE input gives complete control over power up, allowing sequential power up or shutdown. When ENABLE is high, the regulator output is placed in the high-impedance state. The ENABLE input is TTL and CMOS compatible.

The TL750Mxx and TL751Mxx are characterized for operation over the virtual junction temperature range –40°C to 125°C.

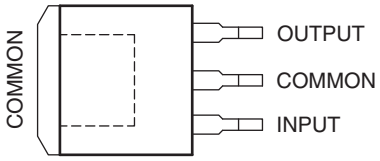
AVAILABLE OPTIONS(1)

T_J	V_O NOM (V)	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	5 V	TO-263-3 – KTT	Reel of 500	TL750M05QKTTRQ1	TL750M05Q1
		TO-252-3 – KVU	Reel of 2500	TL750M05QKVURQ1	750M05Q
	8 V	TO-263-3 – KTT	Reel of 500	TL750M08QKTTRQ1	TL750M08Q1
		TO-252-3 – KVU	Reel of 2500	TL750M08QKVURQ1	750M08Q
	12 V	TO-263-3 – KTT	Reel of 500	TL750M12QKTTRQ1	TL750M12Q1
		TO-252-3 – KVU	Reel of 2500	TL750M12QKVURQ1	750M12Q
	5 V	TO-263-5 – KTT	Reel of 500	TL751M05QKTTRQ1	TL751M05Q1
		TO-252-5 – KVU	Reel of 2500	TL751M05QKVURQ1	751M05Q
	8 V	TO-263-5 – KTT	Reel of 500	TL751M08QKTTRQ1	TL751M08Q1
		TO-252-5 – KVU	Reel of 2500	TL751M08QKVURQ1	751M08Q
	12 V	TO-263-5 – KTT	Reel of 500	TL751M12QKTTRQ1	TL751M12Q1
		TO-252-5 – KVU	Reel of 2500	TL751M12QKVURQ1	751M12Q

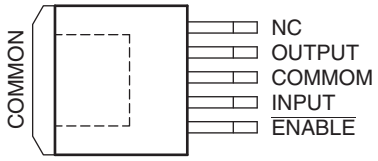
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

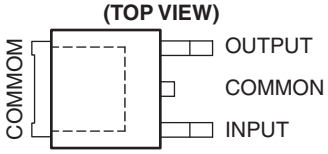
TL750M
KTT (TO-263-3) PACKAGE
(TOP VIEW)



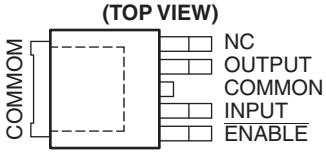
TL751M
KTT (TO-263-5) PACKAGE
(TOP VIEW)



TL750M
KVU (TO-252-3) PACKAGE
(TOP VIEW)

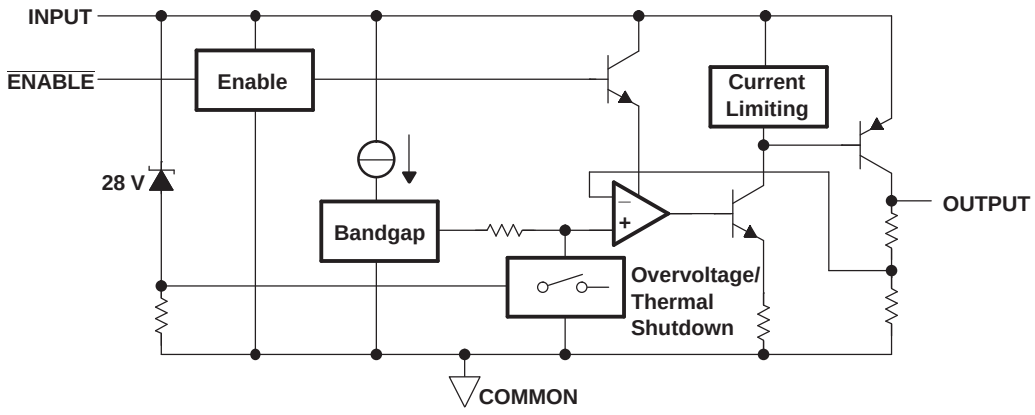


TL751M
KVU (TO-252-5) PACKAGE
(TOP VIEW)



NOTE: The COMMON terminal is in electrical contact with the mounting base.
NC – No internal connection

TL751Mxx FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	Continuous input voltage		26 V
	Transient input voltage (see Figure 4)		60 V
	Continuous reverse input voltage		–15 V
	Transient reverse input voltage	t = 100 ms	–50 V
θ_{JA}	Package thermal impedance(2) (3)	KTT package (3 pin)	26.9°C/W
		KTT package (5 pin)	26.5°C/W
		KVU package	38.6°C/W
T_J	Virtual junction temperature range		–40°C to 150°C
T_{stg}	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.
(3) The package thermal impedance is calculated in accordance with JESD 51.

THERMAL INFORMATION

THERMAL METRIC(1)		TL750M05 KTT 3 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	27.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	43.2	
θ_{JB}	Junction-to-board thermal resistance(4)	17.3	
ψ_{JT}	Junction-to-top characterization parameter(5)	2.8	
ψ_{JB}	Junction-to-board characterization parameter(6)	9.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	0.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_I	Input voltage	TL75xM05	6	26	V
		TL75xM08	9	26	
		TL75xM12	13	26	
V_{IH}	High-level $\overline{\text{ENABLE}}$ input voltage	TL751Mxx	2	15	V
V_{IL}	Low-level $\overline{\text{ENABLE}}$ input voltage	TL751Mxx	0	0.8	V
I_O	Output current	TL75xMxx		750	mA
T_J	Operating virtual junction temperature	TL75xMxx	–40	125	°C

TL751Mxx ELECTRICAL CHARACTERISTICS

V_I = 14 V, I_O = 300 mA, T_J = 25°C

PARAMETER	TL751Mxx	UNIT
	TYP	
Response time, $\overline{\text{ENABLE}}$ to output (start-up)	50	µs

TL750M05/TL751M05 ELECTRICAL CHARACTERISTICS

V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ at 0 V for TL751M05, T_J = –40°C to 125°C (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS		TL750M05 TL751M05			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 6 V to 26 V		4.85	5	5.15	V
Line regulation	V_I = 9 V to 16 V,	I_O = 250 mA		10	25	mV
	V_I = 6 V to 26 V,	I_O = 250 mA		12	50	
Power-supply ripple rejection	V_I = 8 V to 18 V,	f = 120 Hz		55		dB
Load regulation	I_O = 5 mA to 750 mA			20	50	mV
Dropout voltage(2)	I_O = 500 mA, T_J = 25°C				0.5	V
	I_O = 750 mA, T_J = 25°C				0.65	
Current consumption $I_q = I_I - I_O$	I_O = 750 mA			60	75	mA
	I_O = 10 mA				5	
Shutdown current (TL751M05 only)	$\overline{\text{ENABLE}}$ V_{IH} ≥ 2 V				200	µA

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF tantalum capacitor on the output, with equivalent series resistance within the guidelines shown in Figure 4.

(2) Measured when the output voltage, V_O, has dropped 100 mV from the nominal value obtained at V_I = 14 V.

TL750M08/TL751M08 ELECTRICAL CHARACTERISTICS

V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ at 0 V for TL751M08, T_J = –40°C to 125°C (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS		TL750M08 TL751M08			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 6 V to 26 V		7.76	8	8.24	V
Line regulation	V_I = 10 V to 17 V,	I_O = 250 mA		12	40	mV
	V_I = 9 V to 26 V,	I_O = 250 mA		15	68	
Power-supply ripple rejection	V_I = 11 V to 21 V,	f = 120 Hz		55		dB
Load regulation	I_O = 5 mA to 750 mA			24	80	mV
Dropout voltage(2)	I_O = 500 mA, T_J = 25°C				0.5	V
	I_O = 750 mA, T_J = 25°C				0.65	
Current consumption $I_q = I_I - I_O$	I_O = 750 mA, T_J = 25°C			60	75	mA
	I_O = 10 mA				5	
Shutdown current (TL751M08 only)	$\overline{\text{ENABLE}}$ V_{IH} ≥ 2 V				200	µA

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF tantalum capacitor on the output, with equivalent series resistance within the guidelines shown in Figure 4.

(2) Measured when the output voltage, V_O, has dropped 100 mV from the nominal value obtained at V_I = 14 V.

TL750M12/TL751M12 ELECTRICAL CHARACTERISTICS

V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ at 0 V for TL751M12, T_J = –40°C to 125°C (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS	TL750M12 TL751M12			UNIT
		MIN	TYP	MAX	
Output voltage	V_I = 13 V to 26 V	11.76	12	12.24	V
Line regulation	V_I = 14 V to 19 V, I_O = 250 mA		15	43	mV
	V_I = 13 V to 26 V, I_O = 250 mA		20	78	
Power-supply ripple rejection	V_I = 13 V to 23 V, f = 120 Hz	50	55		dB
Load regulation	I_O = 5 mA to 750 mA		30	120	mV
Dropout voltage(2)	I_O = 500 mA, T_J = 25°C			0.5	V
	I_O = 750 mA, T_J = 25°C			0.6	
Current consumption $I_q = I_I - I_O$	I_O = 750 mA, T_J = 25°C		60	75	mA
	I_O = 10 mA			5	
Shutdown current (TL751M12 only)	$\overline{\text{ENABLE}}$ $V_{IH} \geq 2$ V			200	µA

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF tantalum capacitor on the output, with equivalent series resistance within the guidelines shown in Figure 4.

(2) Measured when the output voltage, V_O, has dropped 100 mV from the nominal value obtained at V_I = 14 V.

PARAMETER MEASUREMENT INFORMATION

The TL750Mxx and TL751Mxx are low-dropout regulators. The output capacitor value and the parasitic equivalent series resistance (ESR) affect the bandwidth and stability of the control loop for these devices. For this reason, the capacitor and ESR must be carefully selected for a given operating temperature and load range. Figure 2 and Figure 3 can be used to establish the appropriate capacitance value and ESR for the best regulator transient response.

Figure 2 shows the recommended range of ESR for a given load with a 10-µF capacitor on the output. Figure 2 also shows a maximum ESR limit of 2 Ω and a load-dependent minimum ESR limit.

For applications with varying loads, the lightest load condition should be chosen because it is the worst case. Figure 3 shows the relationship of the reciprocal of ESR to the square root of the capacitance, with a minimum capacitance limit of 10 µF and a maximum ESR limit of 2 Ω. This figure establishes the amount that the minimum ESR limit shown in Figure 2 can be adjusted for different capacitor values. For example, where the minimum load needed is 200 mA, Figure 2 suggests an ESR range of 0.8 Ω to 2 Ω for 10 µF. Figure 3 shows that changing the capacitor from 10 µF to 400 µF can change the ESR minimum by greater than 3/0.5 (or 6). Therefore, the new minimum ESR value is 0.8/6 (or 0.13 Ω). This allows an ESR range of 0.13 Ω to 2 Ω, achieving an expanded ESR range by using a larger capacitor at the output. For better stability in low-current applications, a small resistance placed in series with the capacitor (see Table 1) is recommended, so that ESRs better approximate those shown in Figure 2 and Figure 3.

Table 1. Compensation for Increased Stability at Low Currents

MANUFACTURER	CAPACITANCE	ESR TYP	PART NUMBER	ADDITIONAL RESISTANCE
AVX	15 µF	0.9 Ω	TAJB156M010S	1 Ω
KEMET	33 µF	0.6 Ω	T491D336M010AS	0.5 Ω

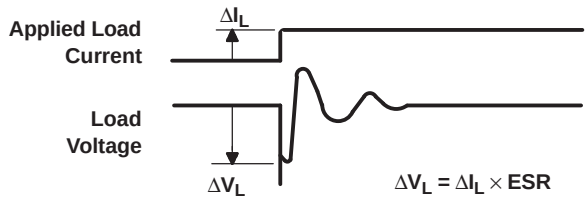


Figure 1.

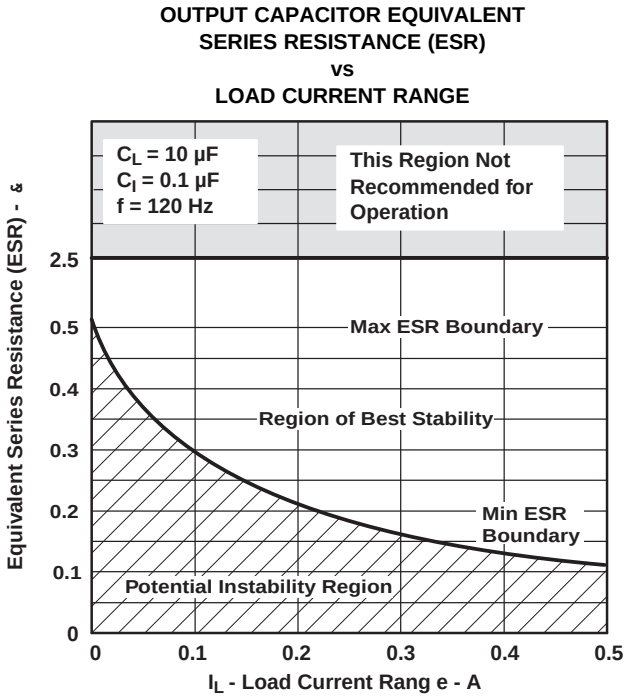


Figure 2.

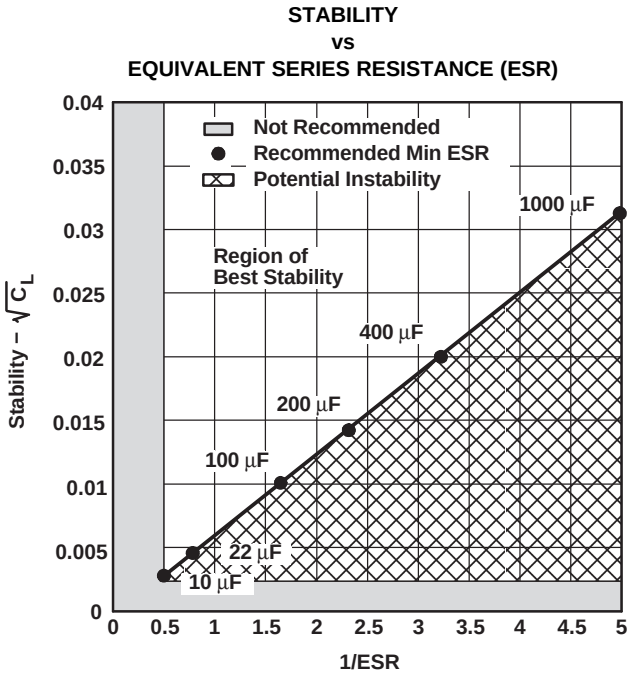


Figure 3.

TYPICAL CHARACTERISTICS

Table 2. Table of Graphs

			FIGURE
Transient input voltage	vs Time		4
Output voltage	vs Input voltage		5
Input current	vs Input voltage	I_O = 10 mA	6
		I_O = 100 mA	7
Dropout voltage	vs Output current		8
Quiescent current	vs Output current		9
Load transient response			10
Line transient response			11

TRANSIENT INPUT VOLTAGE vs TIME

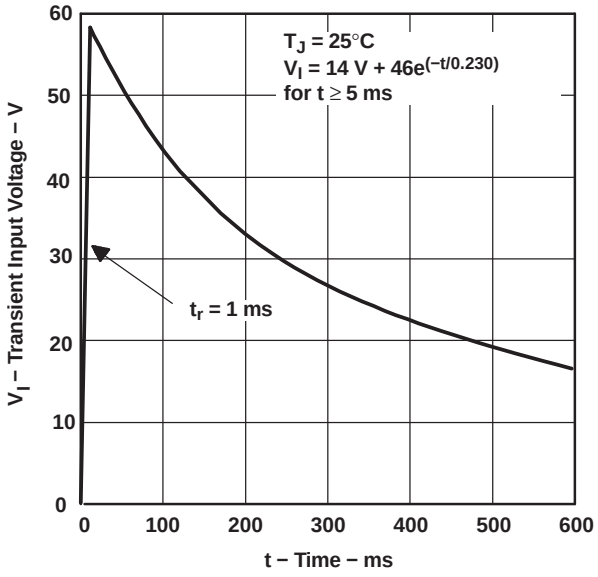


Figure 4.

OUTPUT VOLTAGE vs INPUT VOLTAGE

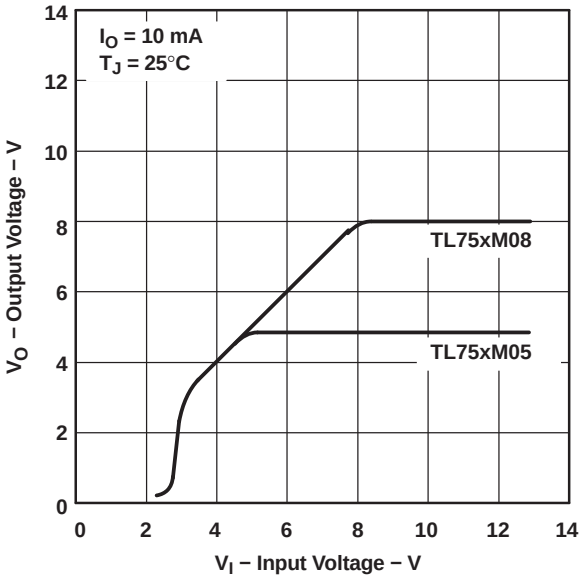


Figure 5.

INPUT CURRENT vs INPUT VOLTAGE

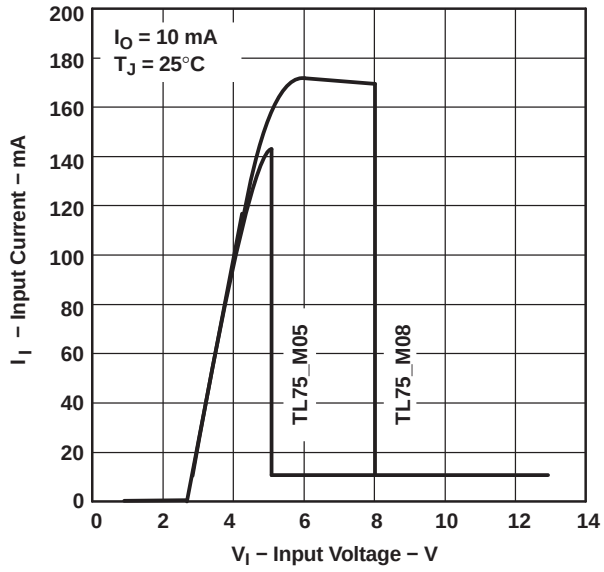


Figure 6.

INPUT CURRENT vs INPUT VOLTAGE

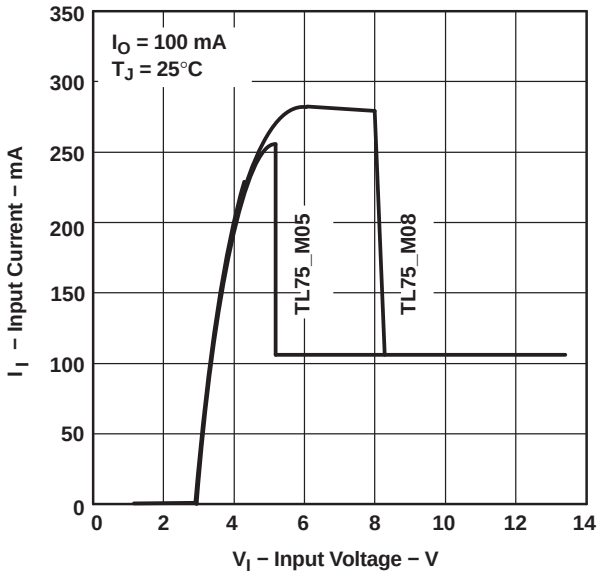


Figure 7.

DROPOUT VOLTAGE vs OUTPUT CURRENT

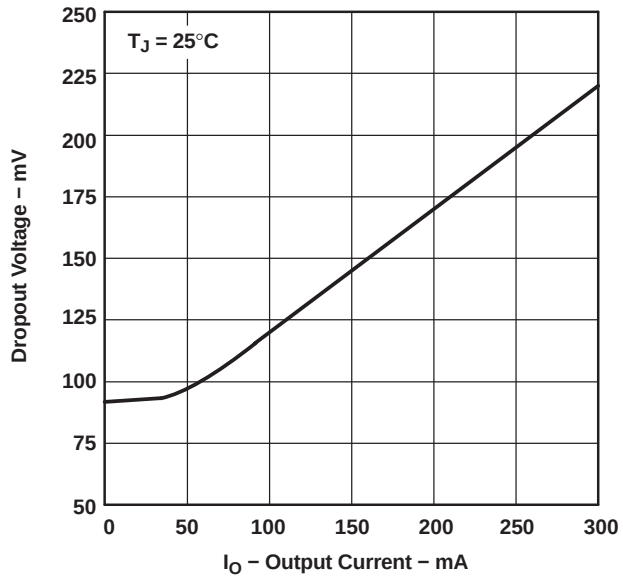


Figure 8.

QUIESCENT CURRENT vs OUTPUT CURRENT

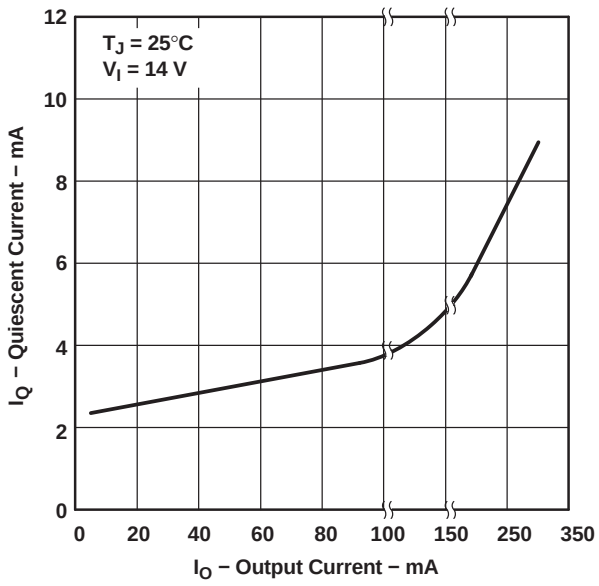


Figure 9.

LOAD TRANSIENT RESPONSE

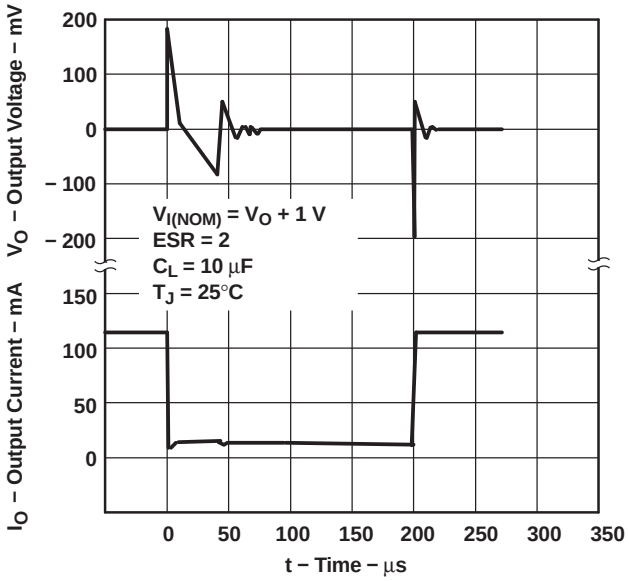


Figure 10.

LINE TRANSIENT RESPONSE

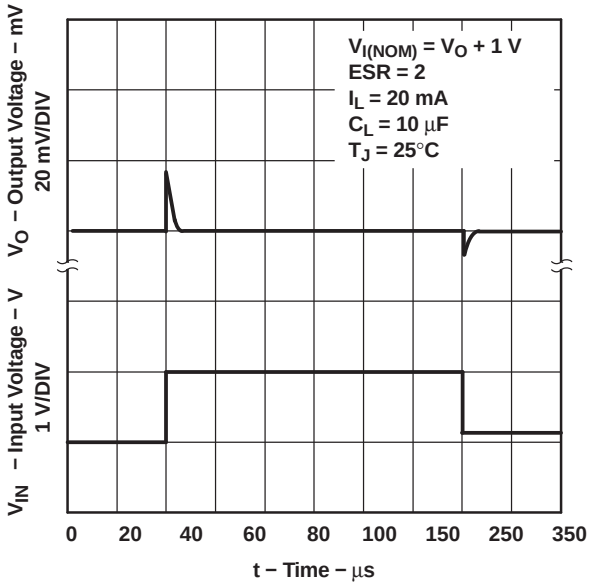


Figure 11.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL750M05QKTTRQ1	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	SN	Level-3-245C-168 HR	-40 to 125	TL750M05Q1	Samples
TL750M05QKVURQ1	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	750M05Q	Samples
TL750M08QKVURQ1	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	750M08Q	Samples
TL750M12QKTTRQ1	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	SN	Level-3-245C-168 HR	-40 to 125	TL750M12Q1	Samples
TL750M12QKVURQ1	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	750M12Q	Samples
TL751M05QKVURQ1	ACTIVE	TO-252	KVU	5	2500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	751M05Q	Samples
TL751M08QKTTRQ1	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	SN	Level-3-245C-168 HR	-40 to 125	TL751M08Q1	Samples
TL751M08QKVURQ1	ACTIVE	TO-252	KVU	5	2500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	751M08Q	Samples
TL751M12QKTTRQ1	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	SN	Level-3-245C-168 HR	-40 to 125	TL751M12Q1	Samples
TL751M12QKVURQ1	ACTIVE	TO-252	KVU	5	2500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	751M12Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TL750M-Q1 :

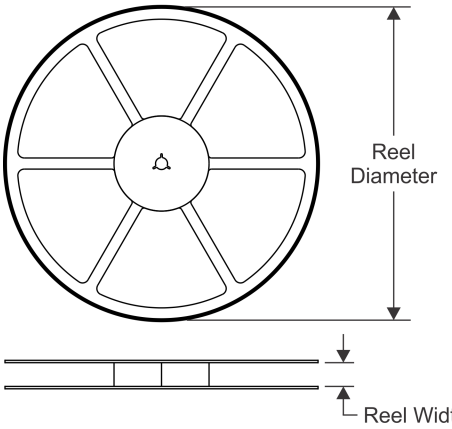
- Catalog: TL750M

NOTE: Qualified Version Definitions:

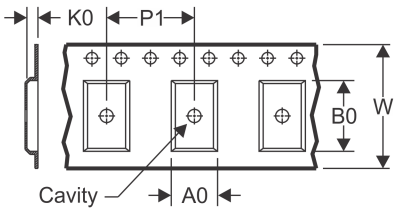
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

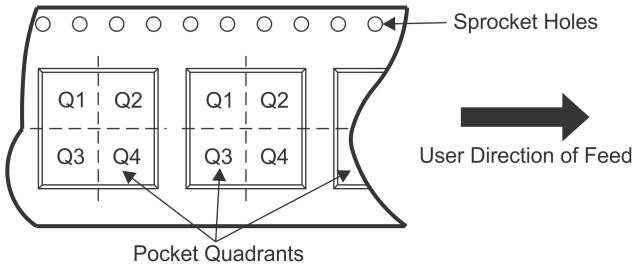


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

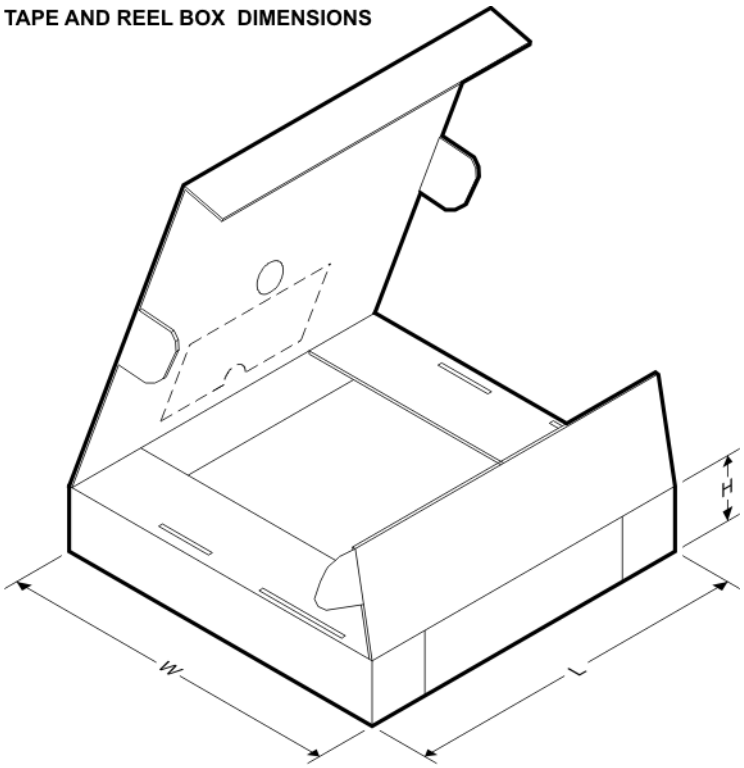
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL750M05QKVURQ1	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL750M08QKVURQ1	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL750M12QKTTRQ1	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
TL750M12QKVURQ1	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL751M05QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL751M08QKTTRQ1	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
TL751M08QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL751M12QKTTRQ1	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
TL751M12QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



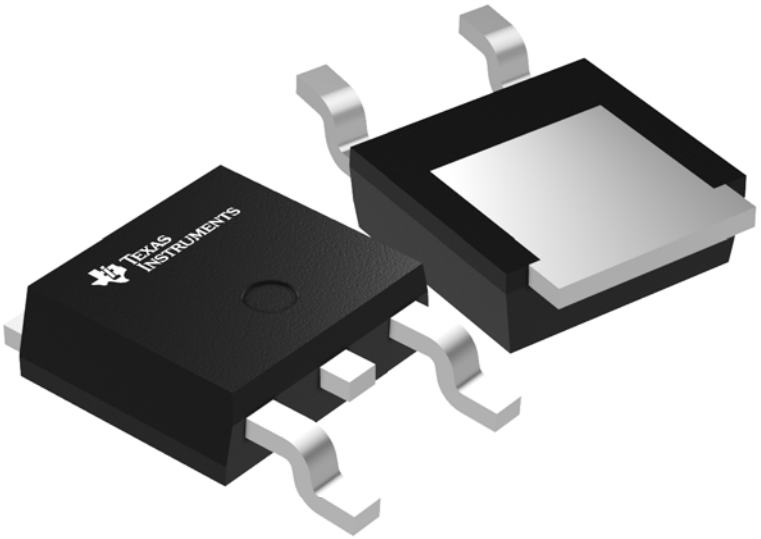
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL750M05QKVURQ1	TO-252	KVU	3	2500	340.0	340.0	38.0
TL750M08QKVURQ1	TO-252	KVU	3	2500	340.0	340.0	38.0
TL750M12QKTTRQ1	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
TL750M12QKVURQ1	TO-252	KVU	3	2500	340.0	340.0	38.0
TL751M05QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0
TL751M08QKTTRQ1	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TL751M08QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0
TL751M12QKTTRQ1	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TL751M12QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0

KVU 3

TO-252 - 2.52 mm max height

TRANSISTOR OUTLINE



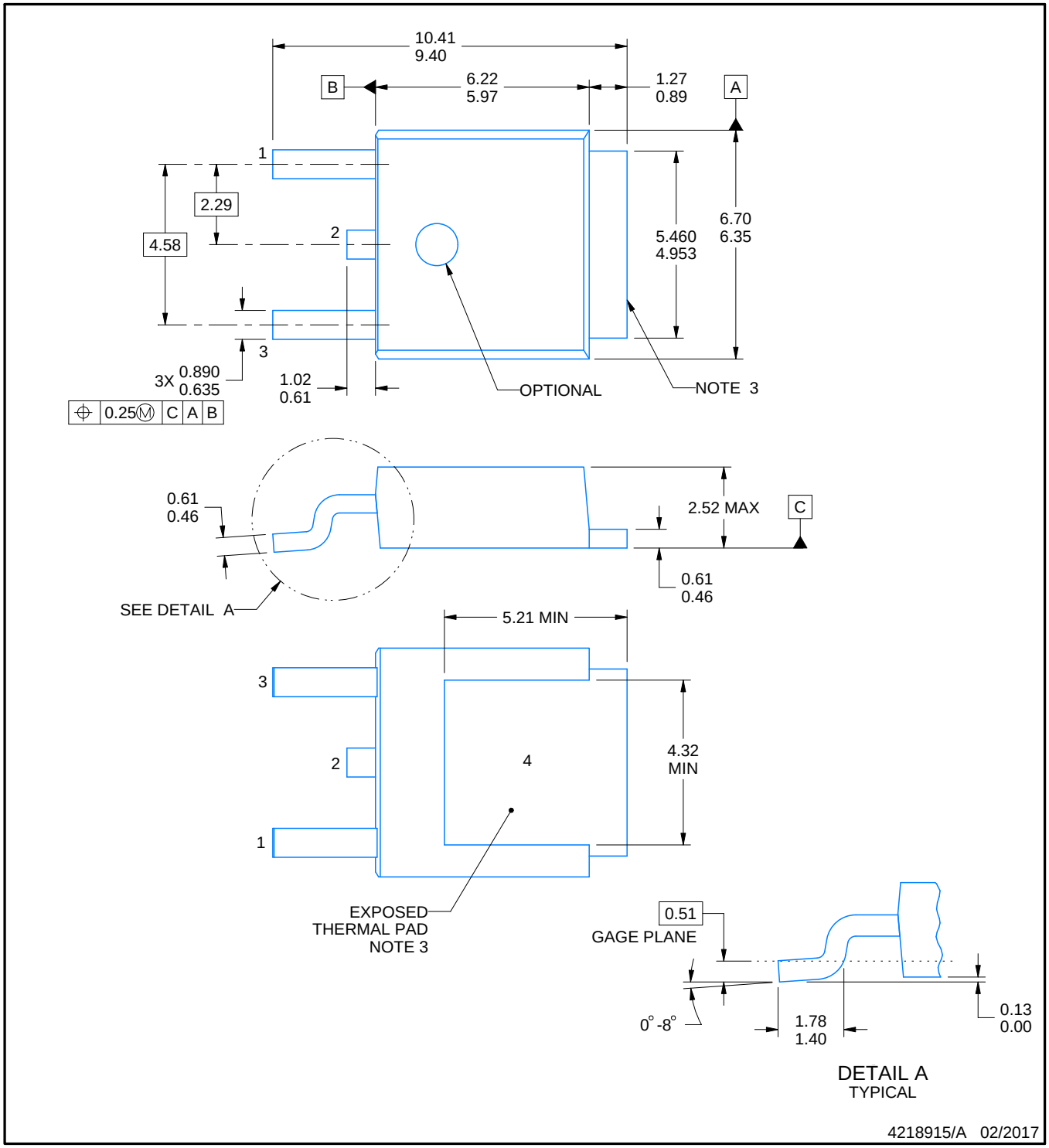
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

KVU0003A

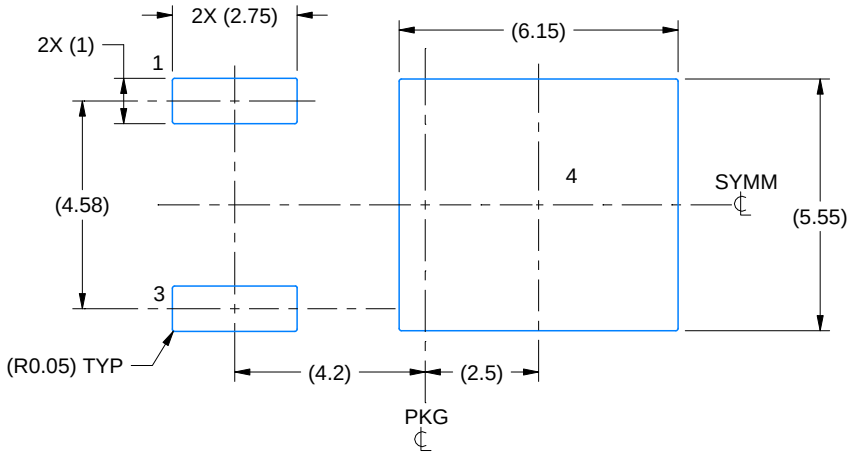
TO-252 - 2.52 mm max height

TO-252

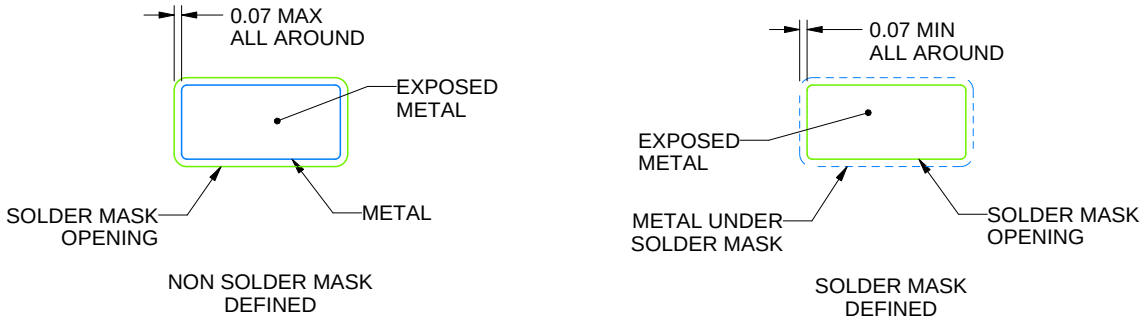


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.
4. Reference JEDEC registration TO-252.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

4218915/A 02/2017

NOTES: (continued)

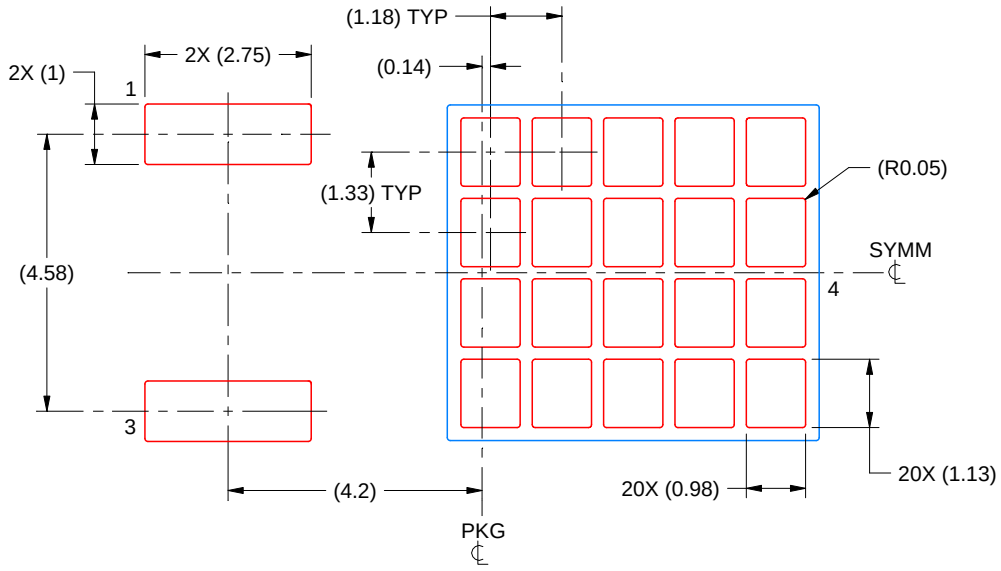
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

KVU0003A

TO-252 - 2.52 mm max height

TO-252



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

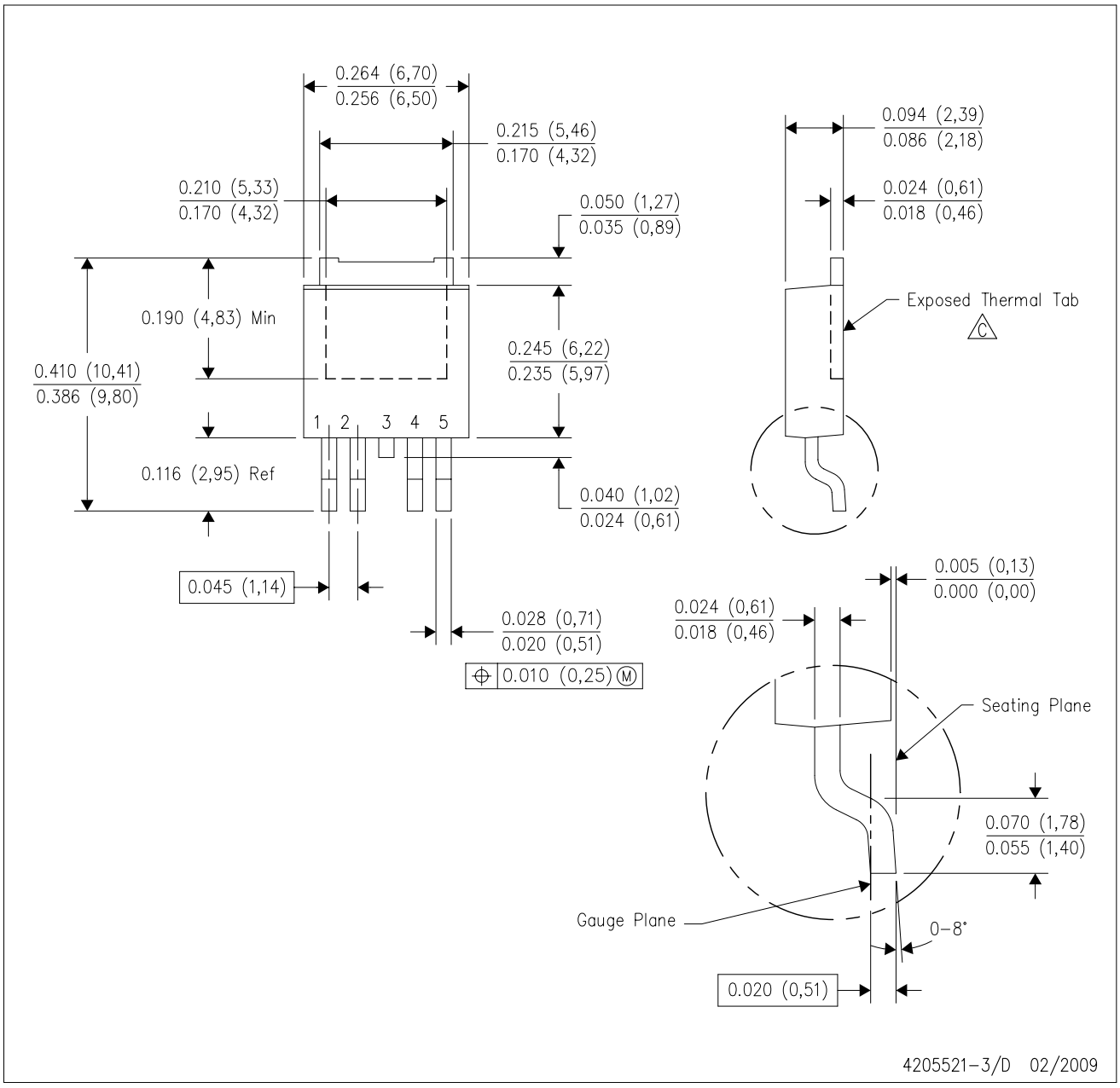
EXPOSED PAD
65% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

4218915/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

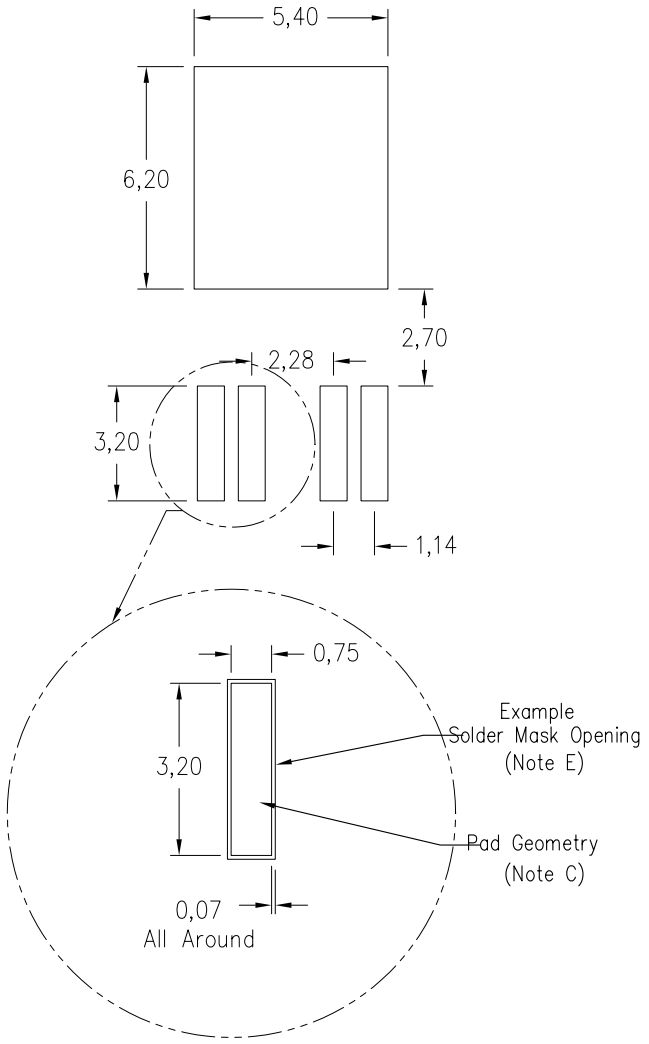
KVU (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



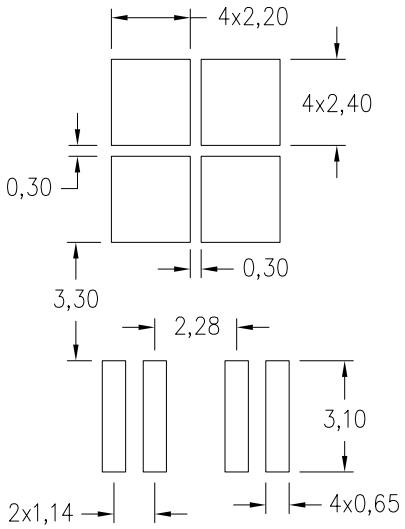
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the exposed thermal tab.
D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
E. Falls within JEDEC TO–252 variation AD.

KVU (R–PSFM–G5) PLASTIC FLANGE MOUNT PACKAGE

Example Board Layout



Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

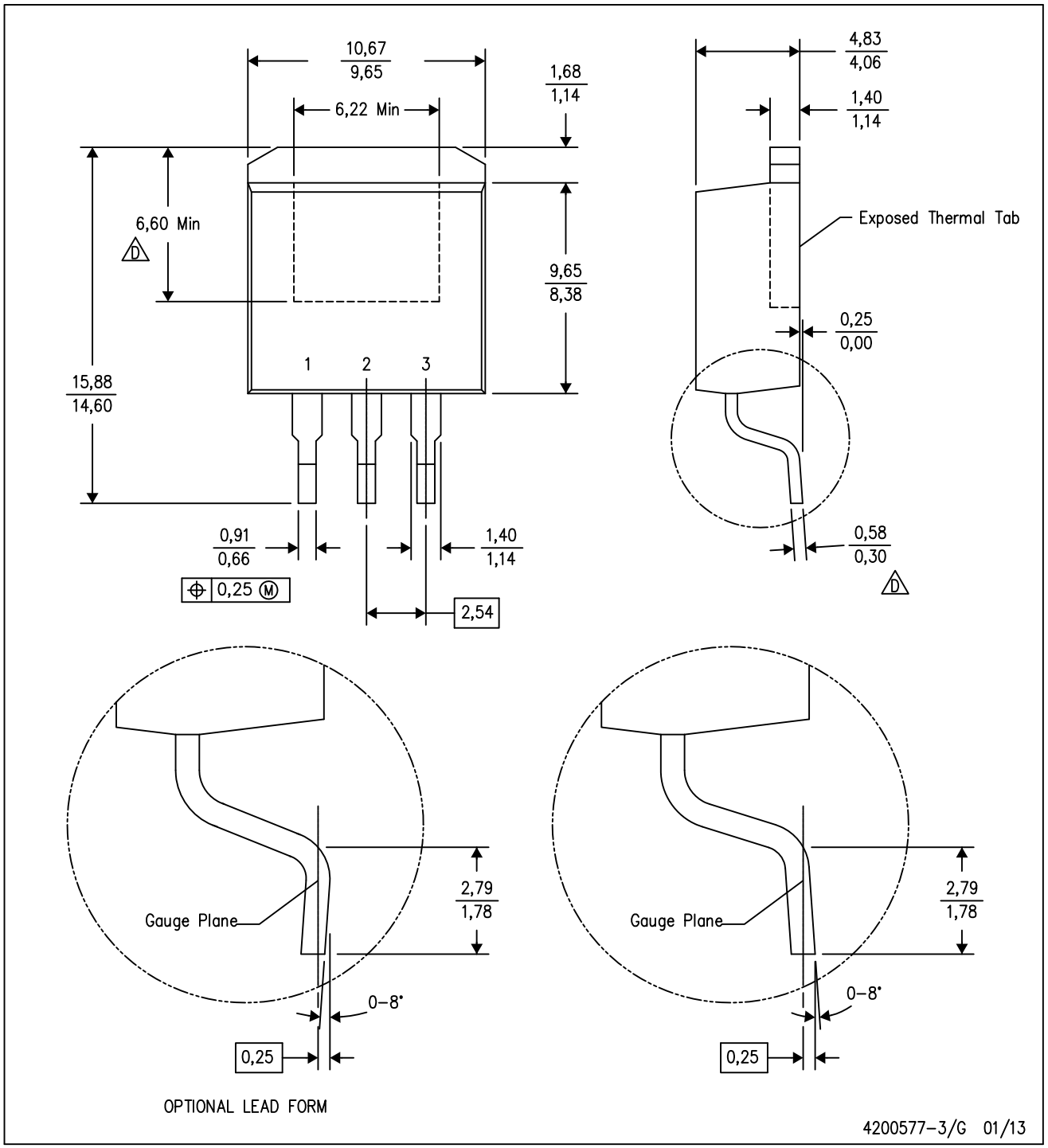


63% solder coverage on center pad

4211592–3/B 03/12

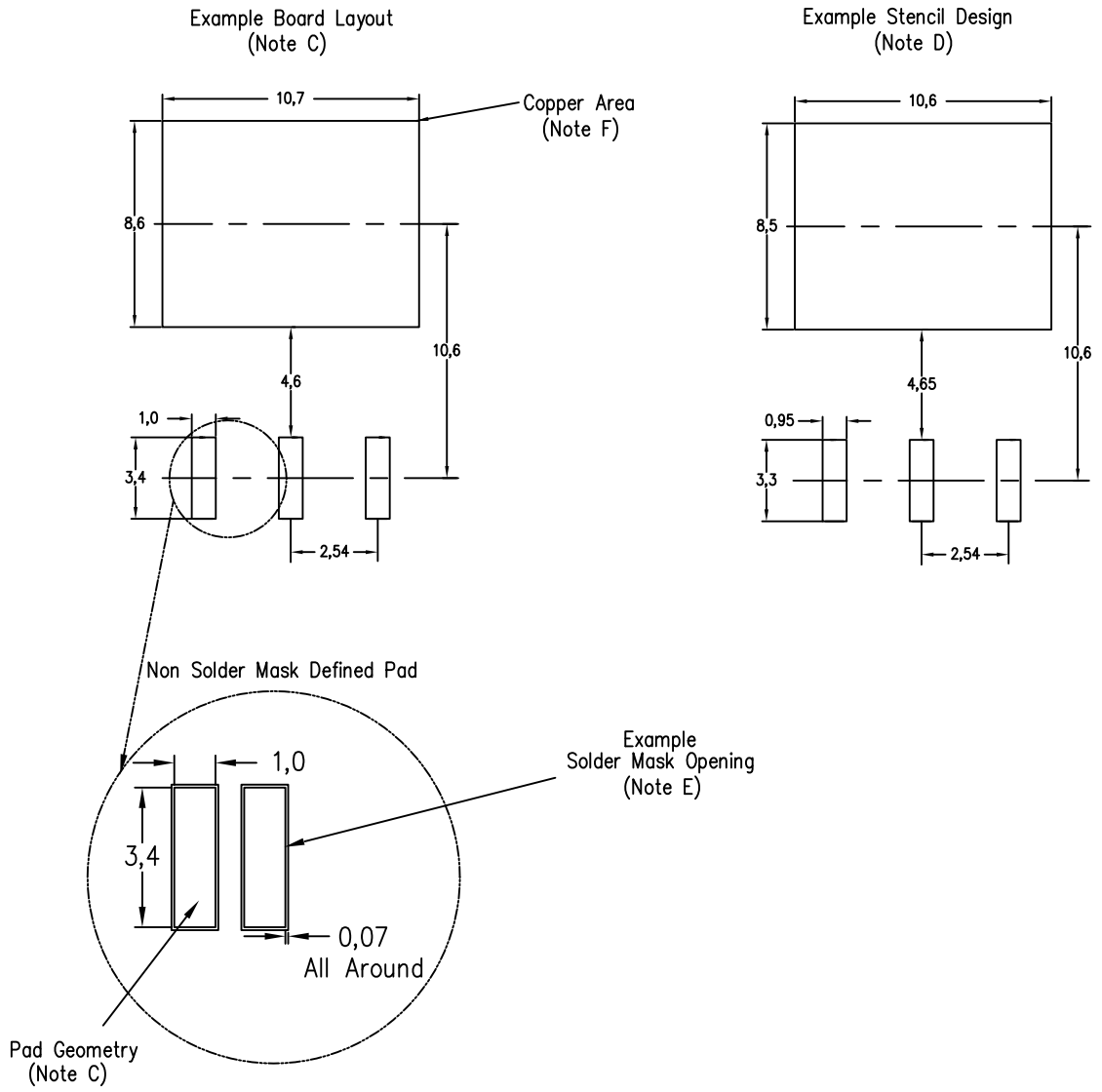
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is an alternate information source for PCB land pattern designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



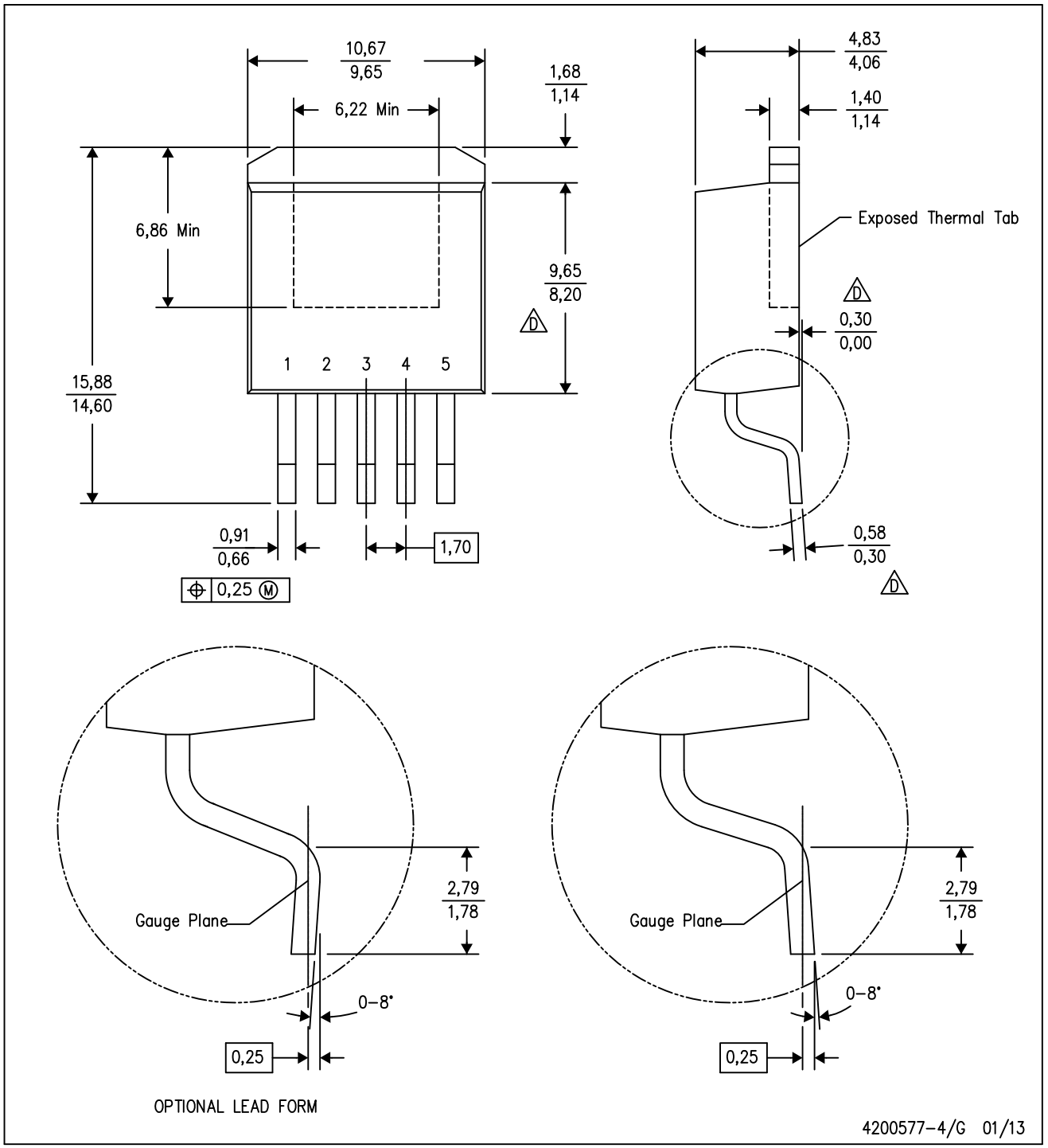
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation AA, except minimum lead thickness and minimum exposed pad length.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



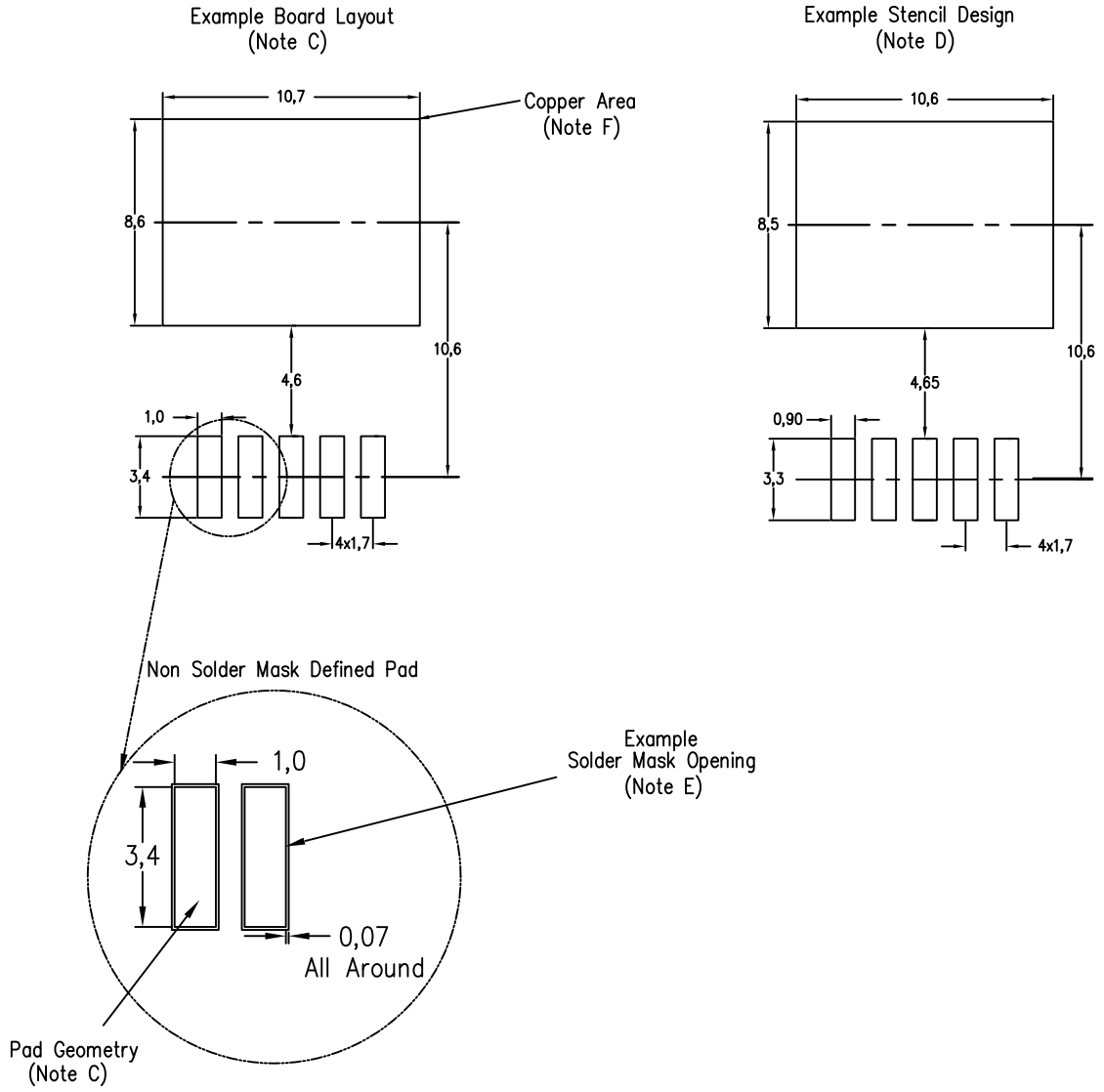
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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