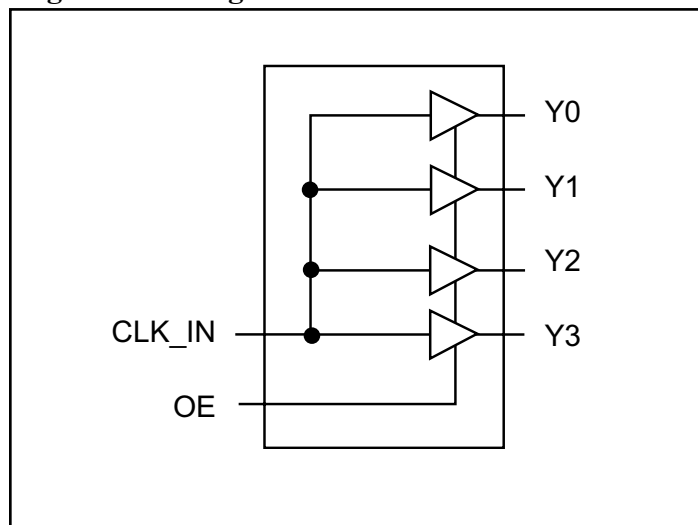


Features

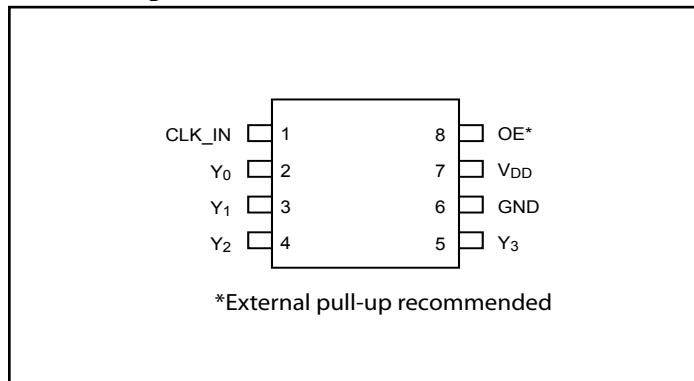
- 160 MHz maximum frequency
- Low skew: 250ps
- Fast rise/fall time: 1.5ns
- Output Enable with tri-states
- Industrial Temperature
- 3.3V or 5V power supply
- Packaging (Pb-free & Green available):
–8-pin SOIC (W)

Applications

- 33 MHz for PCI
- 106.25 MHz for Fibre Channel
- 125 MHz for Ethernet
- 133 MHz for PCIX
- 155.52 MHz for OC3/SONET

Logic Block Diagram

Description

PI6C18551 is a low skew, low noise and high-speed clock buffer for computing, networking and communication applications. It is a non-inverting buffer with four outputs from a single input. The outputs are controlled by output enable pin (OE), outputs are tri-states when OE is LOW, and outputs are enabled when OE is HIGH.

Pin Description

Function Table

Inputs		Outputs
CLK_IN	OE	Y[3:0]
X	L	Z
L	H	L
H	H	H

Note:

1. X = Don't Care; Z = Tri-state

Pin Description

Pin Name	Type	Pin No	Descriptions
CLK_IN	Input	1	Input clock with pull-up resistor
Y0	Output	2	Output clock
Y1	Output	3	Output clock
Y2	Output	4	Output clock
Y3	Output	5	Output clock
GND	Ground	6	GROUND
V _{DD}	Power	7	3.3V or 5V power supply
OE	Input	8	Output Enable with pull-up resistor. External pull-up resistor is recommended.

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01 μ F should be connected between V_{DD} on pin 7 and GND on pin 6, as close to the device as possible. A 33-Ohm series terminating resistor may be used on each clock output if the trace is longer than 1 inch. An external 100k-Ohm pull-up resistor should be used on pin 8, OE.

Absolute Maximum Ratings (Over operating free-air temperature range)

Symbol	Parameters	Min.	Max.	Units
V _{DD}	Supply Voltage		7	V
V _I	Input Voltage	-0.5	V _{DD} +0.5	
V _O	Output Voltage	-0.5	V _{DD} +0.5	
T _s	Storage Temperature	-65	150	°C
T _a	Ambient Temperature	-40	85	
T _{so}	Soldering Temperature		260	

DC Electrical Characteristics ($V_{DD} = 3.3V \pm 5\%$, $T_A = -40$ to $85^\circ C$)

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
V_{DD}	3.3V I/O Supply Voltage		3.135		3.465	V
V_{IH}	Input High Voltage	CLK_IN, Note 1	$V_{DD}/2 + 0.7$		3.8	
		OE	2		V_{DD}	
V_{IL}	Input Low Voltage	CLK_IN, Note 1			$V_{DD}/2 - 0.7$	
		OE			0.8	
V_{OH}	Output High Voltage	$I_{OH} = -12mA$	2.4			
V_{OL}	Output Low Voltage	$I_{OL} = 12mA$			0.4	
I_{DD}	Power Supply Current	No load at 135 MHz		34		mA
Z_O	Output Impedance			20		Ohm
R_{PU}	Internal Pull-up Resistor	CLK_IN & OE		192		k-Ohm
I_{OS}	Short Circuit Current			-46		mA

Notes:

- Nominal switching threshold is $V_{DD}/2$

DC Electrical Characteristics ($V_{DD} = 5V \pm 5\%$, $T_A = -40$ to $85^\circ C$)

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
V_{DD}	5V I/O Supply Voltage		4.75		5.25	V
V_{IH}	Input High Voltage	CLK_IN, Note 1	$V_{DD}/2 + 1$		5.5	
		OE	2		V_{DD}	
V_{IL}	Input Low Voltage	CLK_IN, Note 1			$V_{DD}/2 - 1$	
		OE			0.8	
V_{OL}	Output Low Voltage	$I_{OL} = 12mA$			0.4	
V_{OH}	Output High Voltage (CMOS Level)	$I_{OH} = -12mA$	4			
I_{DD}	Power Supply Current	No load at 135MHz		61		mA
Z_O	Output Impedance			20		Ohm
R_{PU}	Internal Pull-up Resistor	CLK_IN & OE		193		k-Ohm
I_{OS}	Short Circuit Current			-90		mA

Notes:

- Nominal switching threshold is $V_{DD}/2$

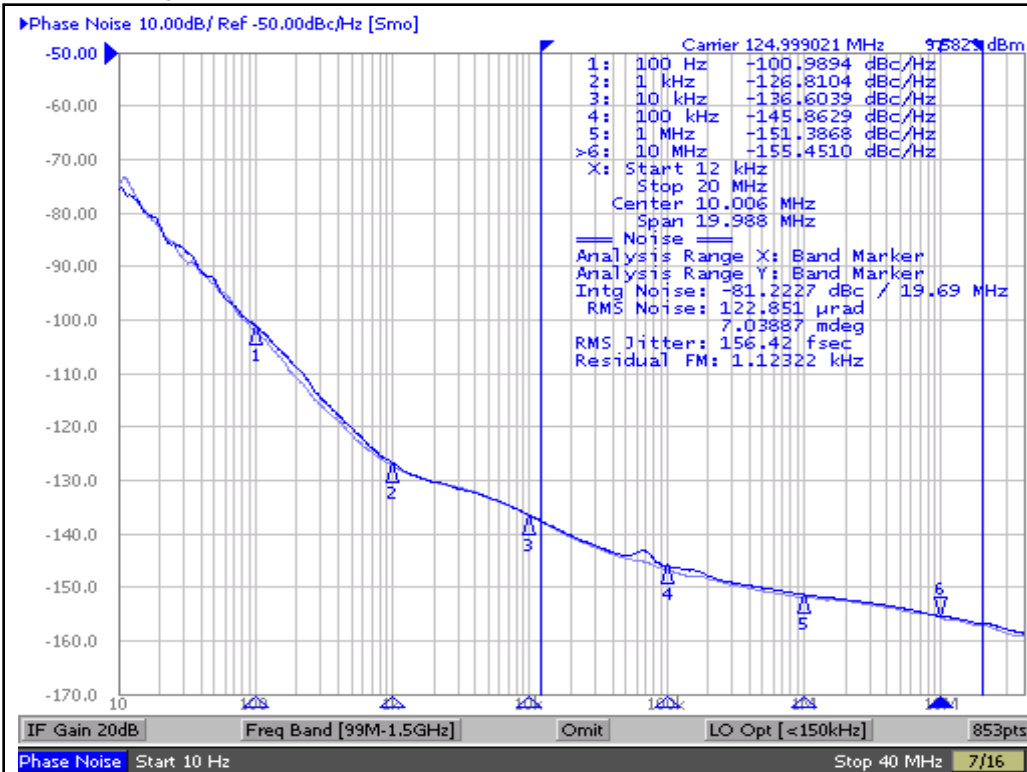
AC Electrical Characteristics ($V_{DD} = 3.3 \pm 5\%$, $T_A = -40$ to $85^\circ C$)

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
F_{in}	Input Frequency		0		160	MHz
F_o	Output Frequency	3.3V, 15pF load ⁽⁵⁾			160	
F_o	Output Frequency	5V, 15pF load ⁽⁵⁾			135	
T_R	Rise Time	0.8V to 2.0V			1.5	ns
T_F	Fall Time	2.0V to 0.8V			1.5	
T_{PD}	Propagation Delay	3.3V, 135MHz ⁽²⁾	2	4	8	
T_{PD}	Propagation Delay	5V, 135MHz ⁽²⁾	1.5	3	6	
T_{SK}	Output Skew	$V_{DD}/2$ ⁽³⁾			250	ps
T_{jit}	Additive Jitter	RMS @ 12KHz~20MHz		45.6		fs

Notes:

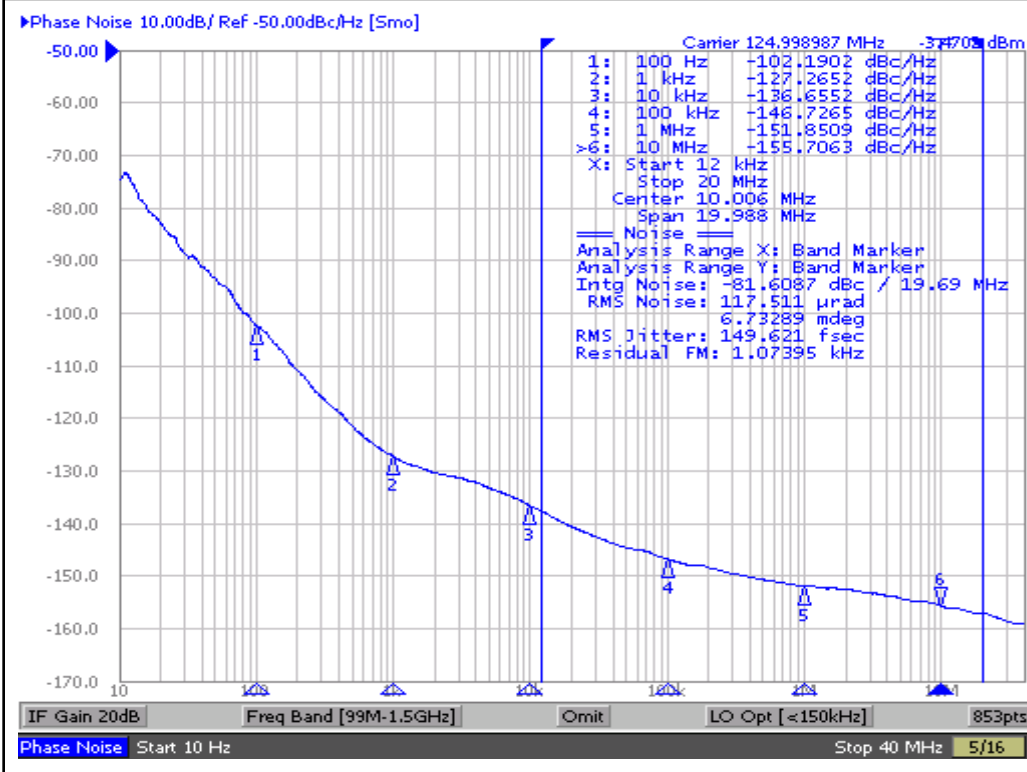
- With rail to rail input clock.
- All outputs with equal loading.
- Duty cycle on outputs will match incoming clock duty cycle.
- With external series resistor 33Ω positioned close to each output pin.

Jitter (RMS @ 12KHz~20MHz)



Output phase noise vs. input (light blue line) plot

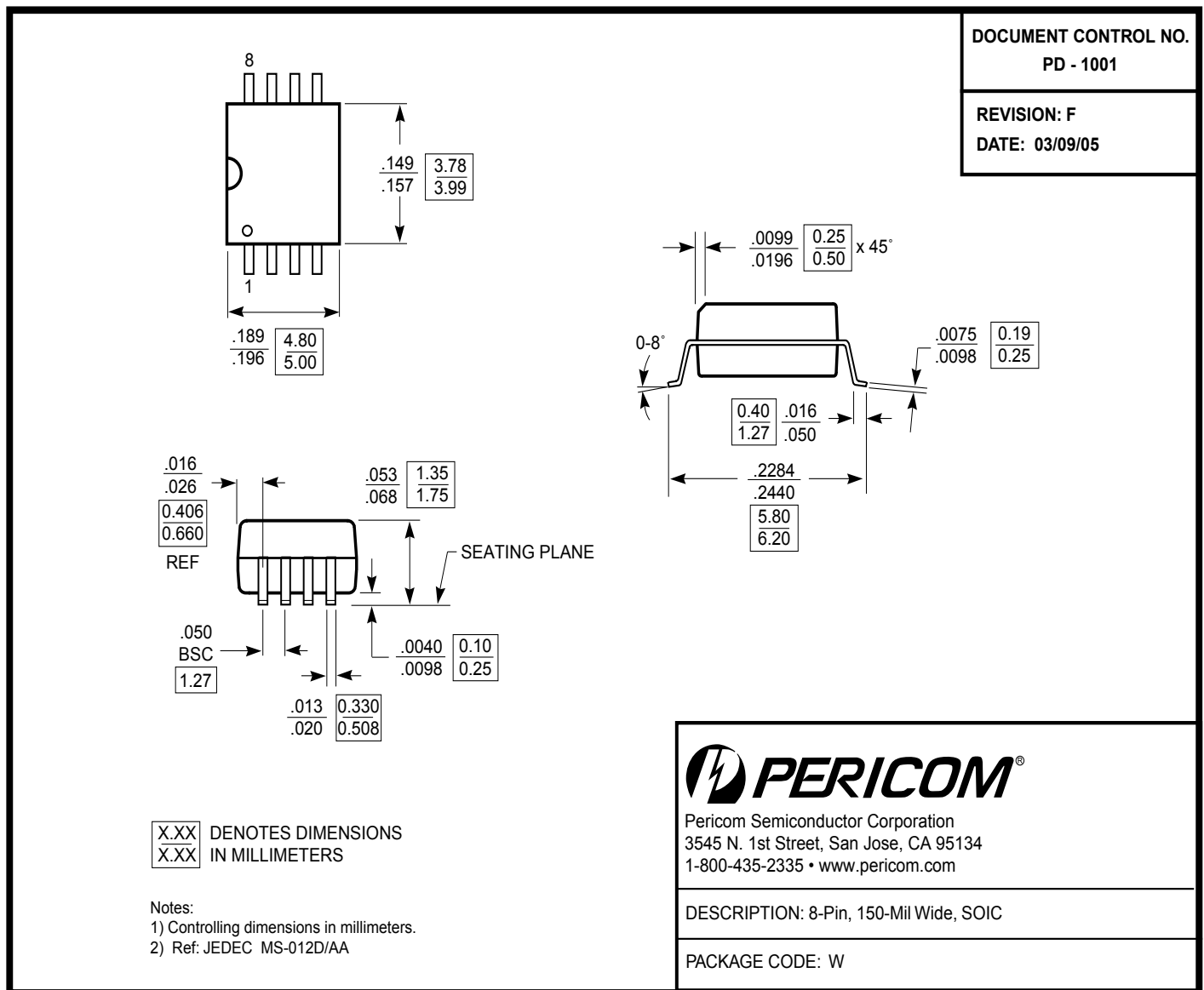
Output RMS phase jitter=156.4fs



Input phase noise plot

Input RMS phase jitter=149.6fs

Packaging Mechanical: 8-pin SOIC (W)



Ordering Information^(1,2,3):

Ordering Code	Package Code	Package Description
PI6C18551WE	W	Pb-free & Green, 8-pin SOIC

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. Adding an X Suffix = Tape/Reel

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