SN7546x Darlington Transistor Arrays

1 Features

- 500-mA Rated Collector Current (Single Output)
- High-Voltage Output 100 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay Driver Applications
- Higher-Voltage Versions of ULN2003A and ULN2004A, for Commercial Temperature range

2 Applications

- Relay Drivers
- Hammer Drivers
- Lamp Drivers
- Display Drivers (LED and Gas Discharge)
- Line Drivers
- Logic Buffers

3 Description

The SN75468 and SN75469 are high-voltage, high-current Darlington transistor arrays. Each consists of seven NPN Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. The Darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

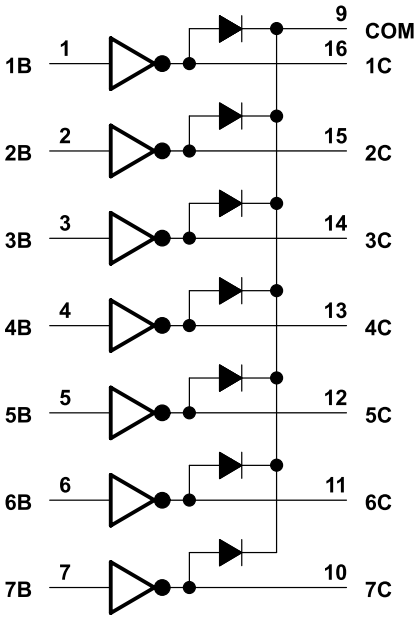
The SN75468 has a 2700-Ω series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS. The SN75469 has a 10.5-kΩ series base resistor to allow its operation directly with CMOS or PMOS that use supply voltages of 6 to 15 V. The required input current is below that of the SN75468.

Device Information(1)

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
SN7546x	D (16)	9.90 mm × 3.91 mm
	N (16)	19.30 mm × 6.35 mm
	NS (16)	10.30 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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5 Revision History

Changes from Revision D (November 2004) to Revision E **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted *Ordering Information* table. ... 1

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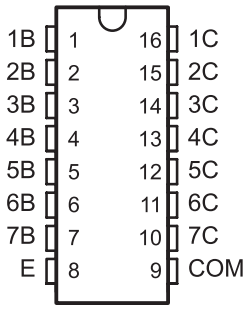
6 Pin Configuration and Functions

SN75468 . . . D, N, OR NS PACKAGE
SN75469 . . . D OR N PACKAGE
(TOP VIEW)



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
<1:7>B	1 - 7	I	Channel 1 through 7 darlington base input
<1:7>C	16 - 10	O	Channel 1 through 7 darlington collector output
E	7	—	Common Emmitter shared by all channels (typically tied to ground)
COM	8	I/O	Common cathode node for flyback diodes (required for inductive loads)

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CE}	Collector-emitter voltage		100	V
V_I	Input voltage(2)		30	V
	Peak collector current		500	mA
I_{OK}	Output clamp current		500	mA
	Total emitter-terminal current		–2.5	A
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I		0	5	V
V_{CC}		0	100	V
T_J	Junction Temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		SN7546x D 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	38.9	
ψ_{JT}	Junction-to-top characterization parameter	10.9	
ψ_{JB}	Junction-to-board characterization parameter	38.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		SN75468			SN75469			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{I(on)}$	On-state input voltage	V_{CE} = 2 V	I_C = 125 mA							V
			I_C = 200 mA			2.4				
			I_C = 250 mA			2.7				
			I_C = 275 mA							
			I_C = 300 mA			3				
			I_C = 350 mA							
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_I = 250 µA, IC = 100 mA			0.9	1.1		0.9	1.1	V
		I_I = 350 µA, IC = 100 mA			1	1.3		1	1.3	
		I_I = 500 µA, IC = 100 mA			1.2	1.6		1.2	1.6	
V_F	Clamp-diode forward voltage	I_F = 350 mA			1.7	2		1.7	2	V
I_{CEX}	collector cutoff current	V_{CE} = 100 V, I_I = 0				50			50	µA
		V_{CE} = 100 V, TA = 70°C	I_I = 0			100			100	
			V_I = 1 V						500	
$I_{I(off)}$	Off-state input current	V_{CE} = 50 V, I_C = 500 µA, T_A = 70°C		50	65		50	65		µA
I_I	Input current	V_I = 3.85 V			0.93	1.35				mA
		V_I = 5 V						0.35	0.5	
		V_I = 12 V						1	1.45	
I_R	Clamp-diode reverse current	V_R = 100 V				50			50	µA
		V_R = 100 V, T_A = 70°C				100			10	
C_i	Input Capacitance	V_I = 0, f = 1 MHz			15	25		15	25	pF

(1) All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and V_{CC} to GND.

7.6 Switching Characteristics

T_A = 25°C free-air temperature

PARAMETER		TEST CONDITIONS[1]	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_S = 20 V, R_L = 163 Ω, C_L = 15 pF, See Figure 14		0.25	1	µs
t_{PHL}	Propagation delay time, high-to-low-level output			0.25	1	µs
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O = 300 mA, See Figure 14	V_S – 20			mV

(1) All switching characteristics are measured with 0.1-µF capacitors connected at REF and V_{CC} to GND.

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7.7 Typical Characteristics

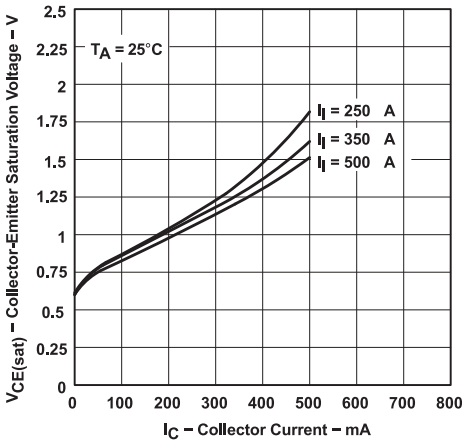

Figure 1. Collector-Emitter Saturation Voltage vs Collector Current (One Darlington)

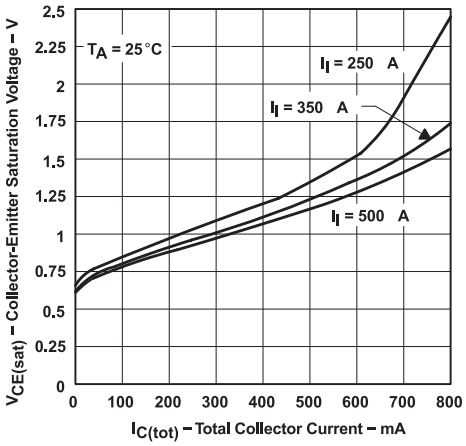

Figure 2. Collector-Emitter Saturation Voltage vs Total Collector Current (Two Darlingtons in Parallel)

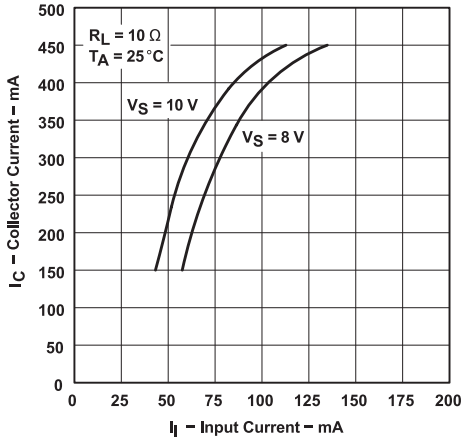

Figure 3. Output Current vs Input Current

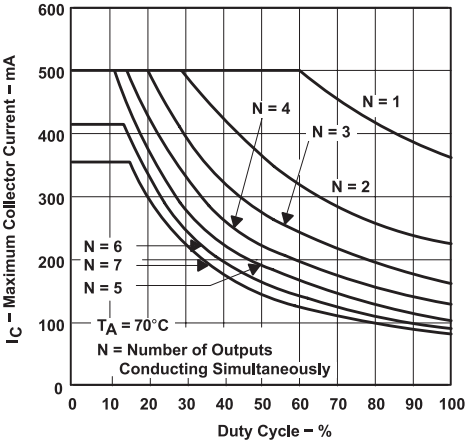

Figure 4. D Package Maximum Collector Current vs Duty Cycle

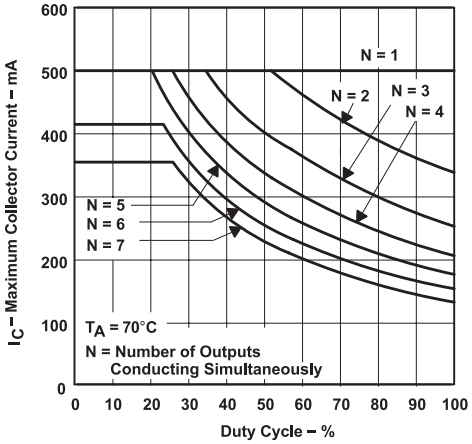

Figure 5. N Package Maximum Collector Current vs Duty Cycle

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8 Parameter Measurement Information

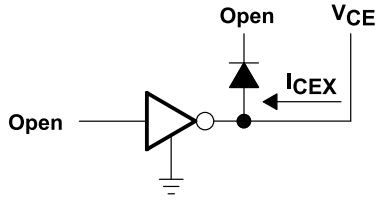

Figure 6. I_{CEX}

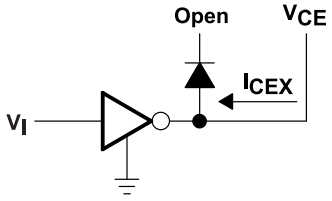

Figure 7. I_{CES}

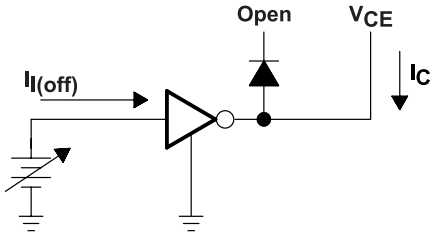

Figure 8. $I_{I(off)}$

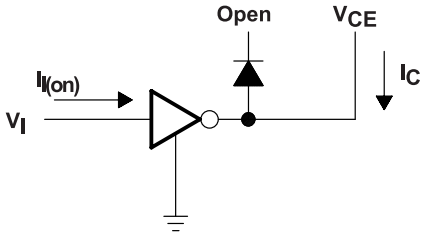

Figure 9. I_I

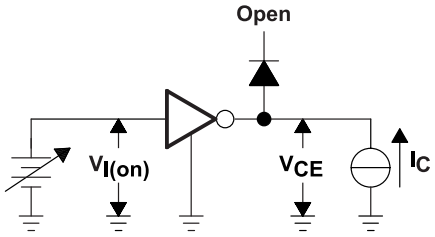

Figure 10. $V_{I(on)}$

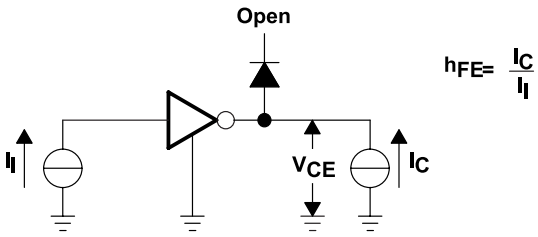

Figure 11. h_{FE}, $V_{CE(sat)}$

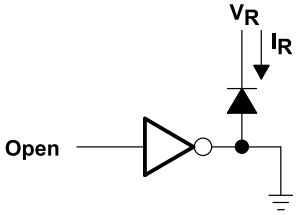

Figure 12. I_R

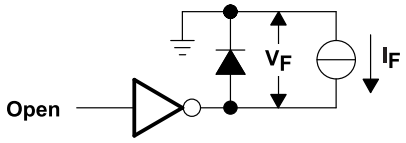

Figure 13. V_F

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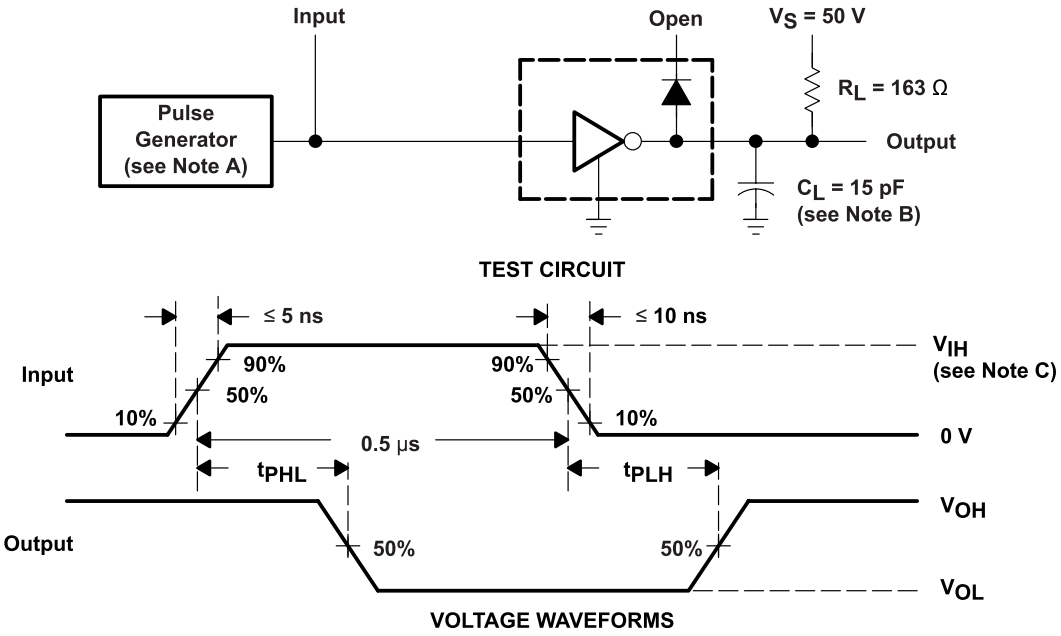
Parameter Measurement Information (continued)

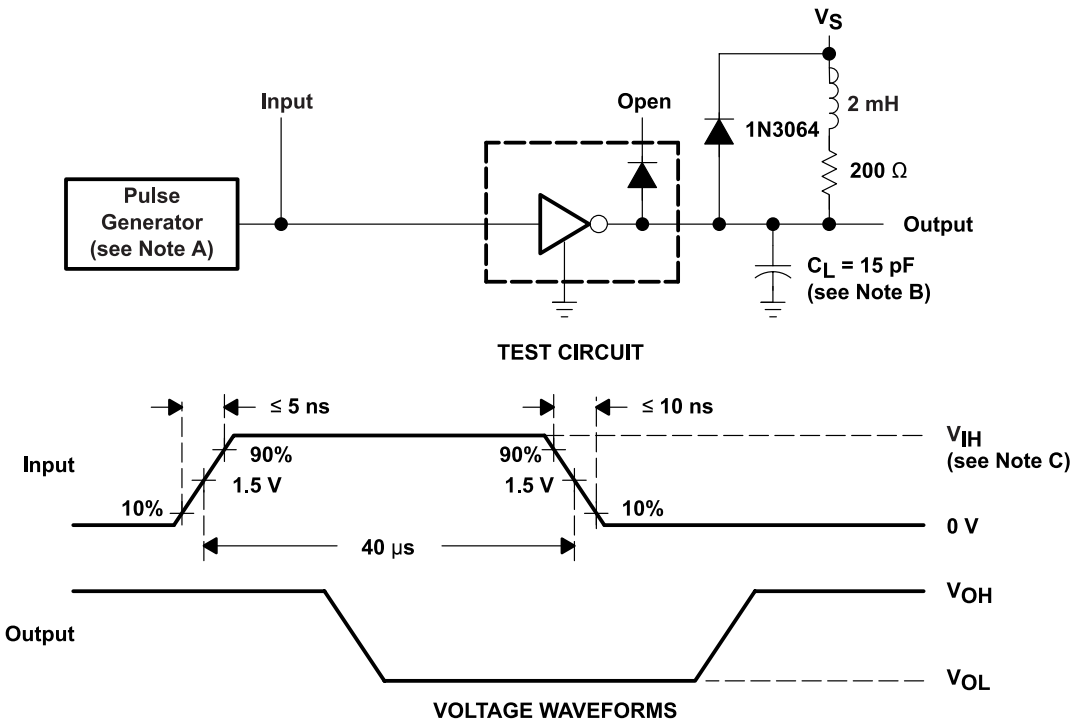


A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.

B. CL includes probe and jig capacitance.

C. For testing the ’468, V_{IH} = 3 V; for the ’469, V_{IH} = 8 V.

Figure 14. Test Circuit and Voltage Waveforms



A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.

B. CL includes probe and jig capacitance.

C. For testing the ’468, V_{IH} = 3 V; for the ’469, V_{IH} = 8 V.

Figure 15. Latch-Up Test Circuit and Voltage Waveforms

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9 Detailed Description

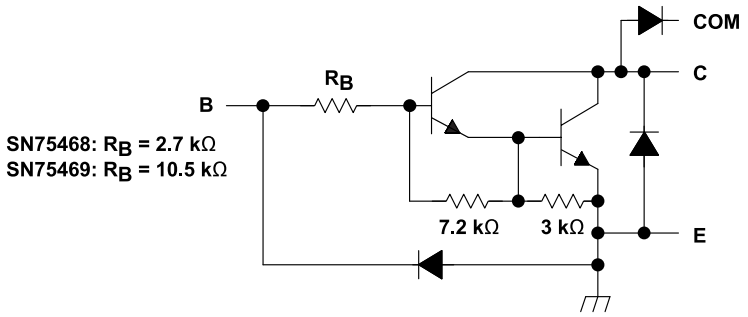
9.1 Overview

This standard device has proven ubiquity and versatility across a wide range of applications. This is due to its integration of 7 Darlington transistors that are capable of sinking up to 500 mA and wide GPIO range capability.

The SN75468 comprises seven high voltage, high current NPN Darlington transistor pairs. All units feature a common emitter and open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads. The SN75468 has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5.0 V or 3.3 V. The SN75468 offers solutions to a great many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

This device can operate over a wide temperature range (–40°C to 105°C).

9.2 Functional Block Diagram



All resistor values shown are nominal.

9.3 Feature Description

Each channel of SN75468 consists of Darlington connected NPN transistors. This connection creates the effect of a single transistor with a very high current gain (β2). This can be as high as 10,000 A/A at certain currents. The very high β allows for high output current drive with a very low input current, essentially equating to operation with low GPIO voltages.

The GPIO voltage is converted to base current via the 2.7 kΩ resistor connected between the input and base of the pre-driver Darlington NPN. The 7.2 kΩ & 3.0 kΩ resistors connected between the base and emitter of each respective NPN act as pull-downs and suppress the amount of leakage that may occur from the input.

The diodes connected between the output and COM pin is used to suppress the kick-back voltage from an inductive load that is excited when the NPN drivers are turned off (stop sinking) and the stored energy in the coils causes a reverse current to flow into the coil supply via the kick-back diode.

In normal operation the diodes on base and collector pins to emitter will be reversed biased. If these diode are forward biased, internal parasitic NPN transistors will draw (a nearly equal) current from other (nearby) device pins.

9.4 Device Functional Modes

9.4.1 Inductive Load Drive

When the COM pin is tied to the coil supply voltage, SN75468 is able to drive inductive loads and supress the kick-back voltage via the internal free wheeling diodes.

9.4.2 Resistive Load Drive

When driving a resistive load, a pull-up resistor is needed in order for SN75468 to sink current and for there to be a logic high level. The COM pin can be left floating for these applications.

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

SN75468 will typically be used to drive a high voltage and/or current peripheral from an MCU or logic device that cannot tolerate these conditions. The following design is a common application of SN75468, driving inductive loads. This includes motors, solenoids & relays. Each load type can be modeled by what's seen in Figure 16.

10.2 Typical Application

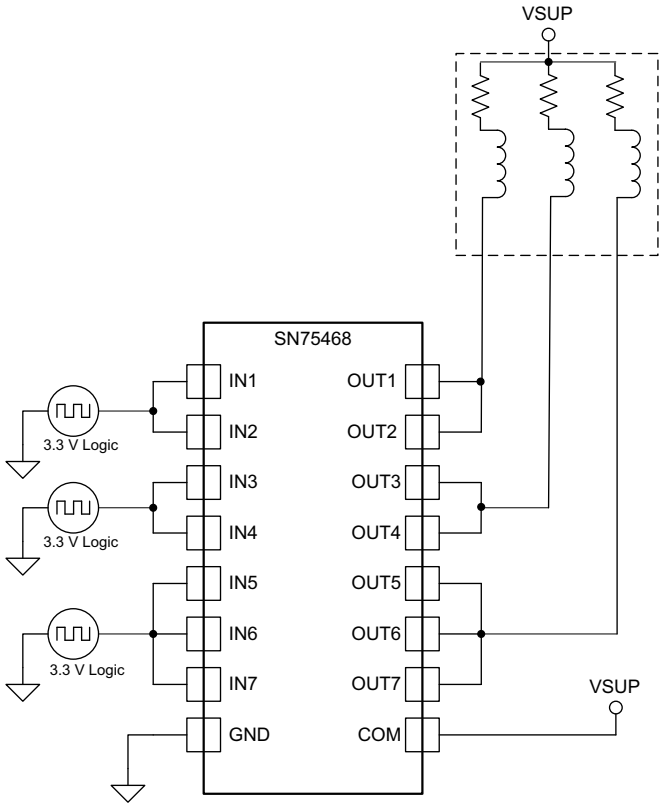

Figure 16. SN75468 as Inductive Load Driver

10.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
GPIO Voltage	3.3 V or 5.0 V
Coil Supply Voltage	12 V to 100 V
Number of Channels	7
Output Current (R_{COIL})	20 mA to 300 mA per channel
Duty Cycle	100%

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10.2.2 Detailed Design Procedure

When using SN75468 in a coil driving application, determine the following:

- Input voltage range
- Temperature range
- Output and drive current
- Power dissipation

10.2.2.1 Drive Current

The coil current is determined by the coil voltage (VSUP), coil resistance & output low voltage (V_{OL} or $V_{CE(SAT)}$).

$$I_{COIL} = (V_{SUP} – V_{CE(SAT)}) / R_{COIL} \quad (1)$$

10.2.2.2 Output Low Voltage

The output low voltage (V_{OL}) is the same thing as $V_{CE(SAT)}$ and can be determined by the *Electrical Characteristics* table, Figure 1, or Figure 2.

10.2.2.3 Power Dissipation & Temperature

The number of coils driven is dependent on the coil current and on-chip power dissipation. The number of coils driven can be determined by Figure 4 or Figure 5.

For a more accurate determination of number of coils possible, use the below equation to calculate SN75468 on-chip power dissipation P_D:

$$P_D = \sum_{i=1}^{N} V_{OLi} \times I_{Li}$$

Where:

N is the number of channels active together.

V_{OLi} is the OUT_i pin voltage for the load current I_{Li}. This is the same as $V_{CE(SAT)}$ (2)

In order to guarantee reliability of SN75468 and the system the on-chip power dissipation must be lower that or equal to the maximum allowable power dissipation ($PD_{(MAX)}$) dictated by below equation Equation 3.

$$PD_{(MAX)} = \left(T_{J(MAX)} – T_A\right) \Big/ \theta_{JA}$$

Where:

$T_{J(MAX)}$ is the target maximum junction temperature.

T_A is the operating ambient temperature.

θ_{JA} is the package junction to ambient thermal resistance. (3)

It is recommended to limit SN75468 IC's die junction temperature to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation.

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10.2.3 Application Curves

The following curves were generated with SN75468 driving an OMRON G5NB relay – V_{in} = 5.0V; V_{sup}= 12 V & R_{COIL}= 2.8 kΩ

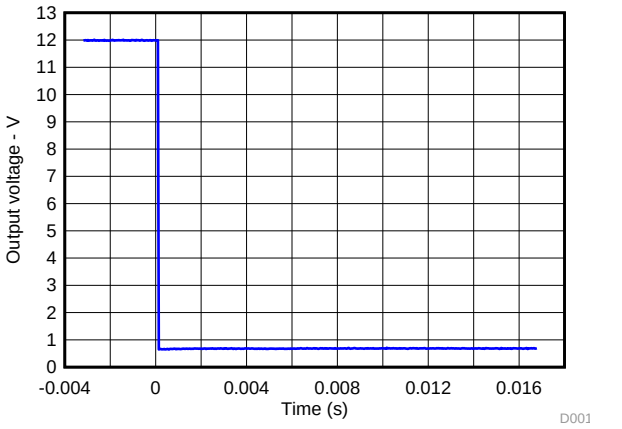

Figure 17. Output Response With Activation of Coil (Turn On)

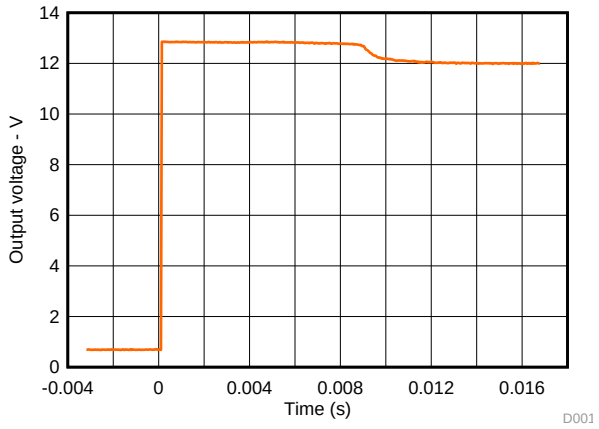

Figure 18. Output Response With De-activation of Coil (Turn Off)

10.3 System Examples

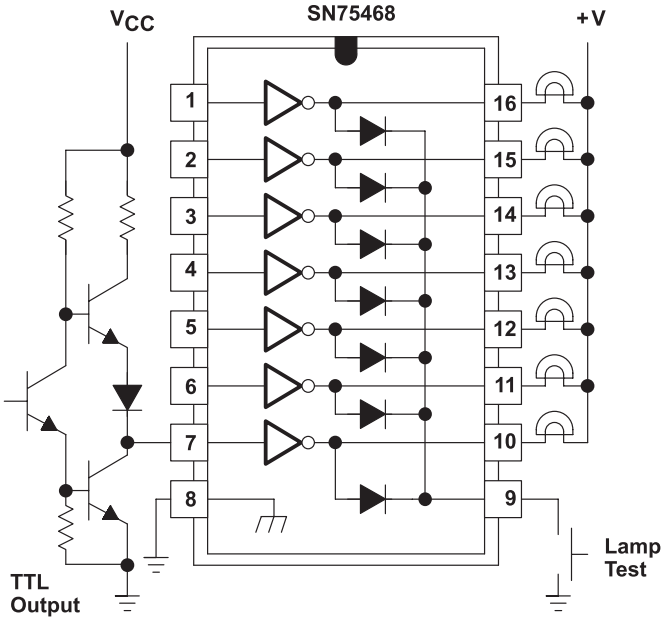

Figure 19. TTL to Load Schematic

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System Examples (continued)

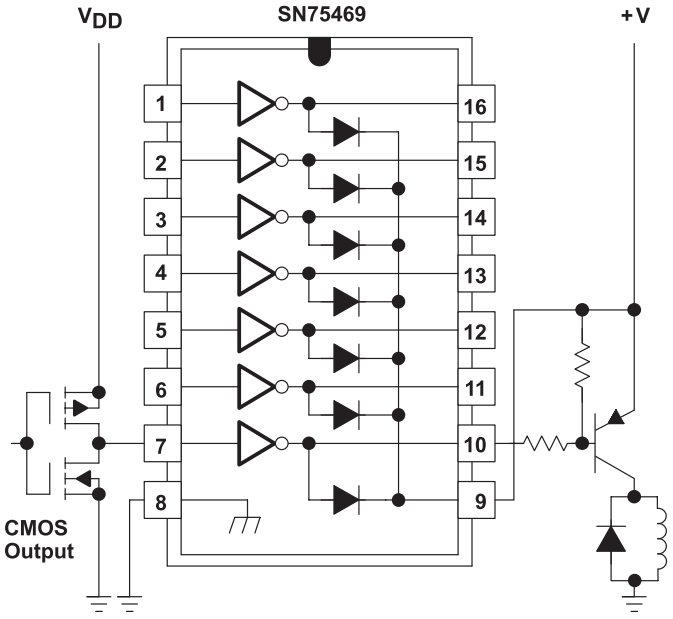

Figure 20. Buffer to Higher Current Loads Schematic

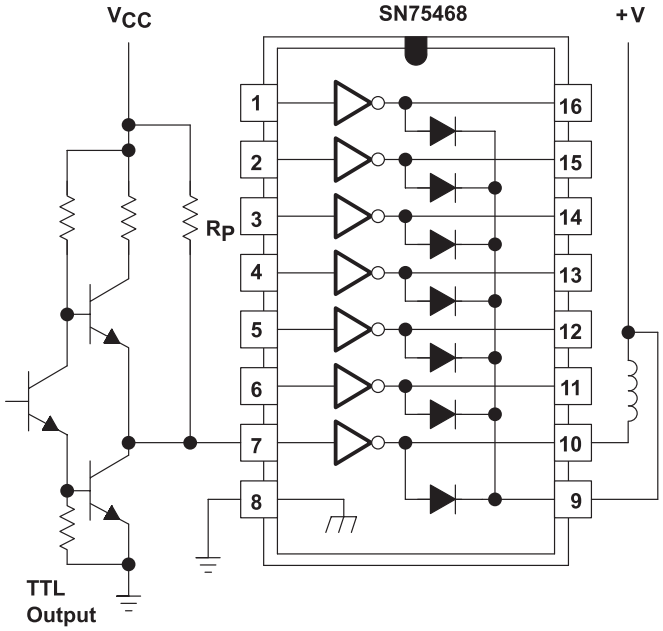

Figure 21. Pull-up Resistor Schematic

11 Power Supply Recommendations

This part does not need a power supply; however, the COM pin is typically tied to the system power supply. When this is the case, it is very important to make sure that the output voltage does not heavily exceed the COM pin voltage. This will heavily forward bias the fly-back diodes and cause a large current to flow into COM, potentially damaging the on-chip metal or over-heating the part.

12 Layout

12.1 Layout Guidelines

Thin traces can be used on the input due to the low current logic that is typically used to drive SN75468. Care must be taken to separate the input channels as much as possible, as to eliminate cross-talk. Thick traces are recommended for the output, in order to drive whatever high currents that may be needed. Wire thickness can be determined by the trace material's current density and desired drive current.

Since all of the channels currents return to a common emitter, it is best to size that trace width to be very wide. Some applications require up to 2.5 A.

12.2 Layout Example

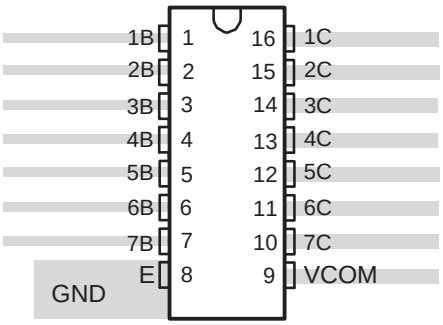

Figure 22. Package Layout

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13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN75468	Click here	Click here	Click here	Click here	Click here
SN75469	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75468D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75468	Samples
SN75468DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75468	Samples
SN75468DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75468	Samples
SN75468N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75468N	Samples
SN75468NE4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75468N	Samples
SN75468NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75468	Samples
SN75468NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75468	Samples
SN75469D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75469	Samples
SN75469DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75469	Samples
SN75469DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75469	Samples
SN75469N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75469N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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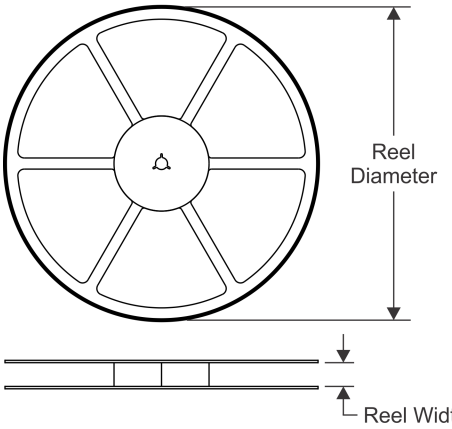
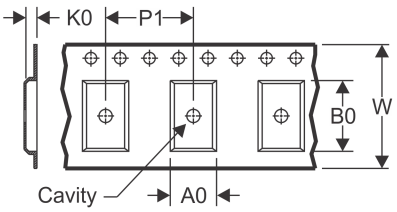
TAPE AND REEL INFORMATION

REEL DIMENSIONS

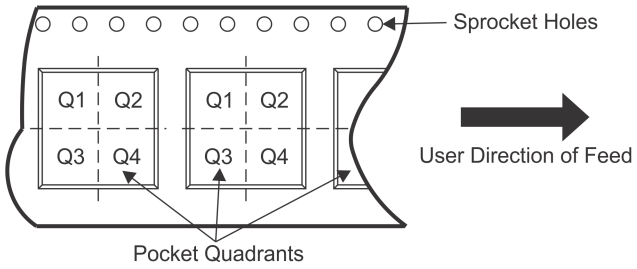


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

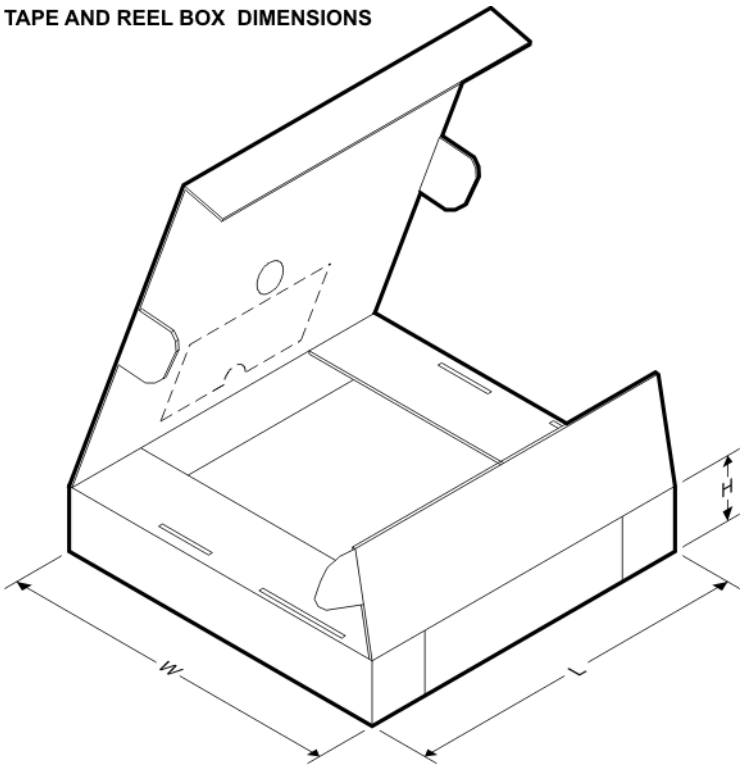
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75469DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

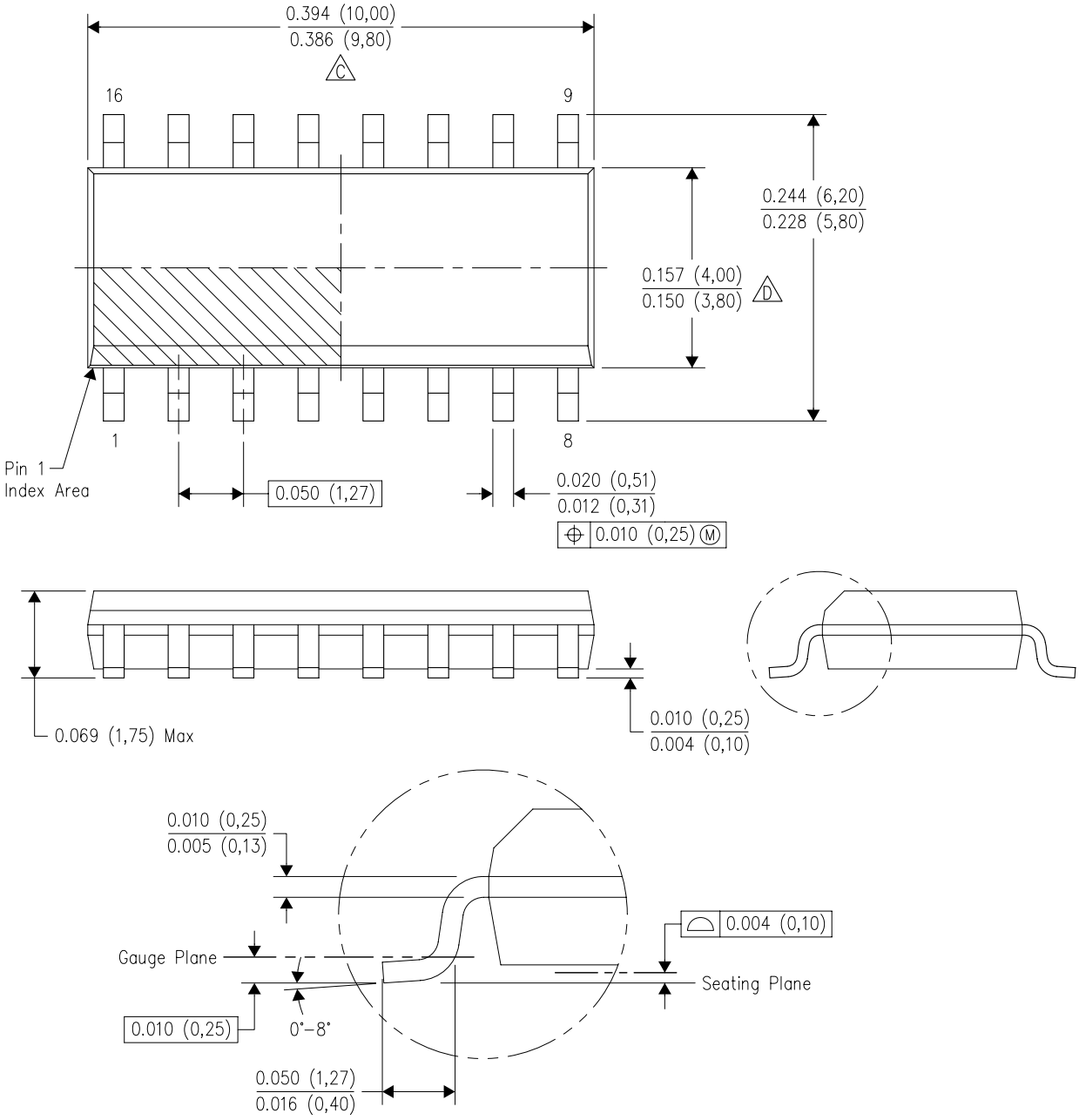
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

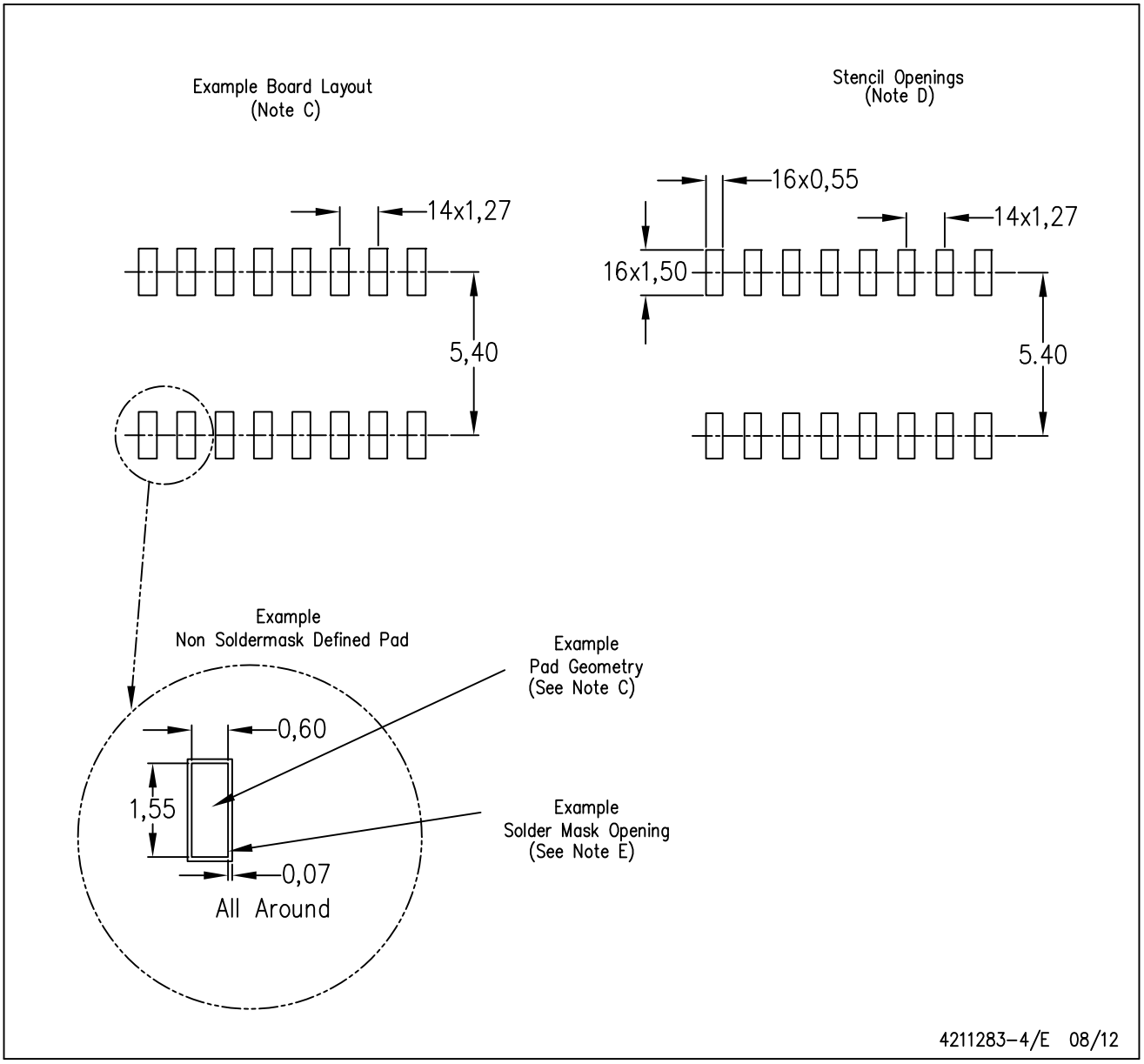
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75469DR	SOIC	D	16	2500	333.2	345.9	28.6

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

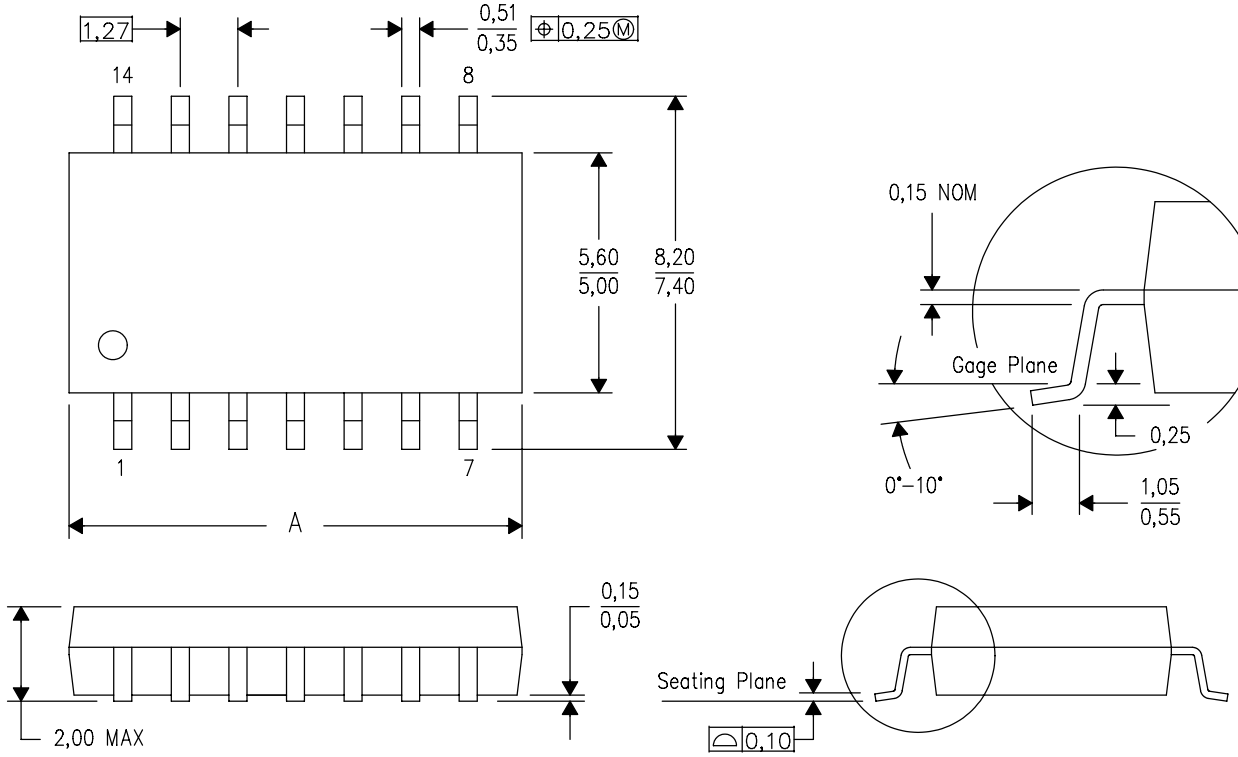


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

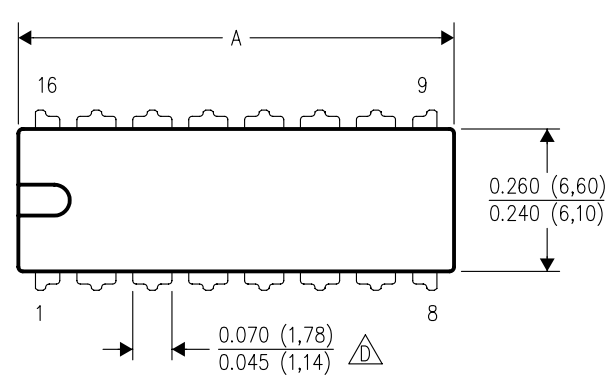
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

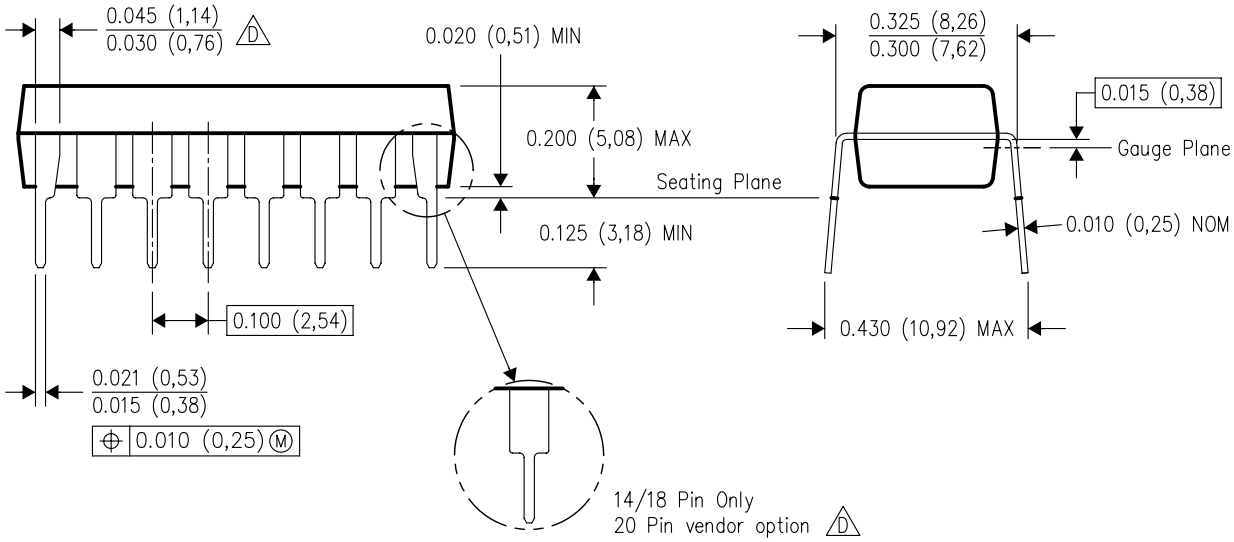
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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