

TLV707, TLV707P

200-mA, Low- I_Q , Low-Noise, Low-Dropout Regulator for Portable Devices

1 Features

- 0.5% Typical Accuracy
 - Supports 200-mA Output
 - Low I_Q : 25 μ A
 - Fixed-Output Voltage Combinations Possible from 0.85 V to 5.0 V⁽¹⁾
 - High PSRR:
 - 70 dB at 100 Hz
 - 50 dB at 1 MHz
 - Stable With Effective Capacitance of 0.1 μ F⁽²⁾
 - Thermal Shutdown and Overcurrent Protection
 - Package: 1-mm \times 1-mm DQN (X2SON)
- (1) For all available voltage options, see the package option addendum at the end of the data sheet.
- (2) See the [Mechanical, Packaging, and Orderable Information](#) section for more details.

2 Applications

- Smart Phones and Wireless Handsets
- Gaming and Toys
- WLAN and Other PC Add-On Cards
- TVs and Set-Top Boxes
- Wearable Electronics

3 Description

The TLV707 series (TLV707 and TLV707P) of low-dropout linear regulators (LDOs) are low quiescent current devices with excellent line and load transient performance for power-sensitive applications. These devices provide a typical accuracy of 0.5%. All versions have thermal shutdown and overcurrent protection for safety.

Furthermore, these devices are stable with an effective output capacitance of only 0.1 μ F. This feature enables the use of cost-effective capacitors that have higher bias voltages and temperature derating. These devices also regulate to the specified accuracy with no output load.

The TLV707P also provides an active pulldown circuit to quickly discharge the outputs.

The TLV707 series of LDOs are available in a 1-mm \times 1-mm DQN (X2SON) package that makes them desirable for handheld applications.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV707	X2SON (4)	1.00 mm \times 1.00 mm
TLV707P		

(1) For all available packages, see the package option addendum at the end of the datasheet.

Typical Application Circuit

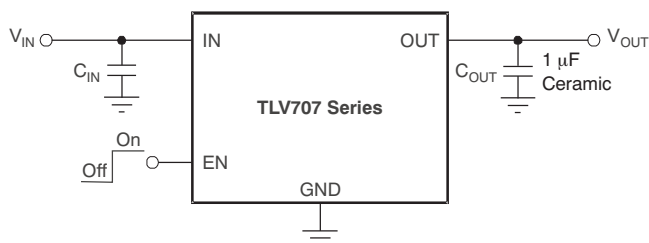


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (February 2016) to Revision F	Page
• Changed $V_{(ESD)}$ HBM value from ± 2000 V to ± 4000 V in <i>ESD Ratings</i> table	5

Changes from Revision D (January 2015) to Revision E	Page
• Changed device name to TLV707, TLV707P and changed V_{IN} , $V_{OUT(nom)}$, I_{OUT} symbols throughout document	1
• Changed DQN package designator name in <i>Package Features</i> bullet	1
• Changed Applications bullets	1
• Deleted first sentence from last paragraph of <i>Description</i> section	1
• Changed caption of front-page figure	1
• Changed <i>Thermal Information</i> table	5
• Changed T_A to T_J in conditions of <i>Electrical Characteristics</i> table	6
• Deleted temperature test conditions from V_{OUT} parameter in <i>Electrical Characteristics</i> table	6
• Deleted UVLO parameter from <i>Electrical Characteristics</i> table	6
• Deleted UVLO block from Figure 58	18
• Added cross-reference for Equation 1	19
• Changed <i>Device Functional Modes</i> section	19
• Deleted <i>Undervoltage Lockout (UVLO)</i> section	19
• Changed title of Figure 59	20
• Added cross-reference for Table 1	20
• Added cross-reference for Figure 68	24

Changes from Revision C (November 2012) to Revision D **Page**

• Changed references to <i>DFN (SON)</i> package to <i>DQN (X2SON)</i> throughout document	1
• Changed Features list bullets	1
• Changed fourth paragraph of Description section	1
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes, Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Changed Pin Descriptions table contents	4
• Changed <i>Overview</i> section	17
• Changed <i>Internal Current Limit</i> section	18
• Changed <i>Input and Output Capacitor Requirements</i> section	20

Changes from Revision B (October 2011) to Revision C **Page**

• Changed voltage range in fourth <i>Features</i> bullet	1
• Changed front page pinout drawing	1
• Changed <i>Output voltage range</i> parameter minimum specification in Electrical Characteristics table	6
• Changed <i>DC output accuracy</i> parameter test conditions in <i>Electrical Characteristics</i> table	6
• Changed voltage range in footnote 2 of Ordering Information table	26

Changes from Revision A (August 2011) to Revision B **Page**

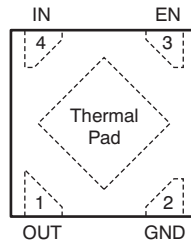
• Deleted reference to DCK package from Features	1
• Deleted DCK package pinout drawing.....	1
• Deleted column for DCK package from Pin Descriptions table.....	4
• Deleted DCK package from <i>Thermal Information</i> table.....	5

Changes from Original (February 2011) to Revision A **Page**

• Added footnote to Features to show available voltage options.....	1
• Added preview banner over DCK pinout drawing	1

5 Pin Configuration and Functions

**DQN Package
4-Pin X2SON
Top View**



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	3	I	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode. For TLV707P, output voltage is discharged through an internal 120-Ω resistor when device is shut down.
GND	2	—	Ground pin
IN	4	I	Input pin. For good transient performance, place a small 1-μF ceramic capacitor from this pin to ground. See Input and Output Capacitor Requirements for more details.
OUT	1	O	Regulated output voltage pin. A small 1-μF ceramic capacitor is required from this pin to ground to assure stability. See Input and Output Capacitor Requirements for more details.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage ⁽²⁾	IN	−0.3	6.0	V
	EN	−0.3	6.0	V
	OUT	−0.3	6.0	V
Current (source)	OUT	Internally limited		
Output short-circuit duration		Indefinite		
Temperature	Operating junction, T _J	−55	150	°C
	Storage, T _{stg}	−55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network ground pin.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM) QSS 009-105 (JESD22-A114A) ⁽¹⁾	±4000
		Charged device model (CDM) QSS 009-147 (JESD22-C101B.01) ⁽²⁾	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage	2.0		5.5	V
I _{OUT}	Output current	0		200	mA
T _J	Operating junction temperature	−40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TLV707, TLV707P	UNIT
		DQN (X2SON)	
		4 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	208.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	108.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	159.4	°C/W
ψ _{JT}	Junction-to-top characterization parameter	3.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter	159.4	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	110.2	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

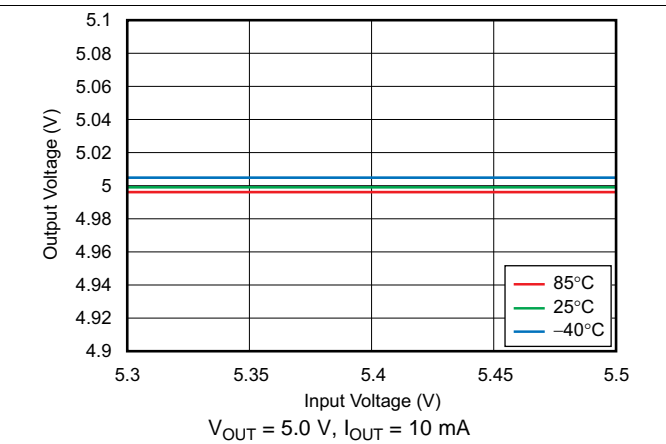
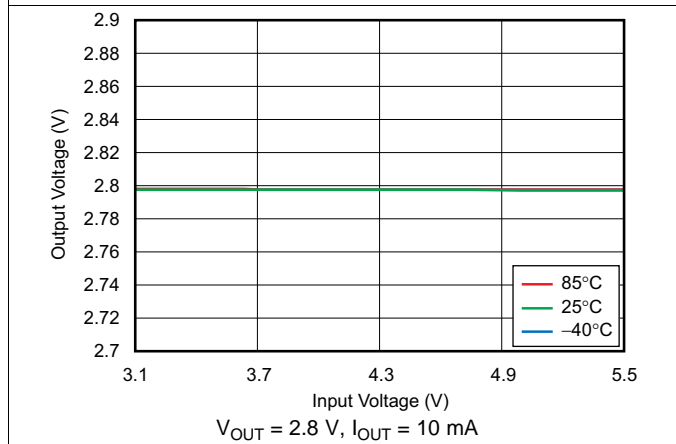
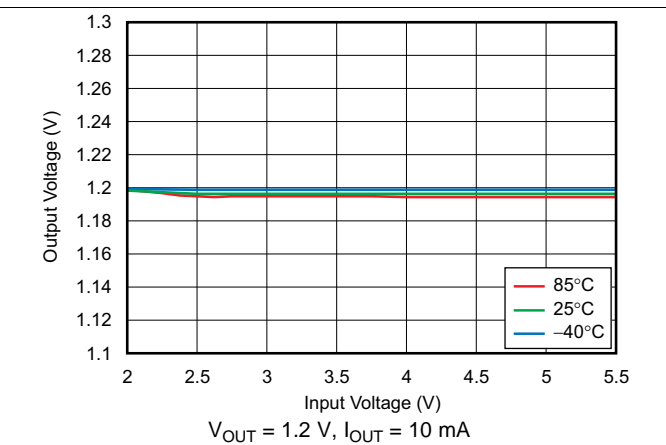
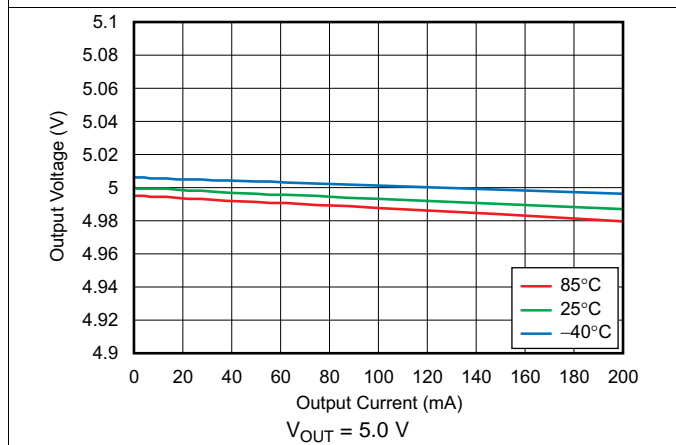
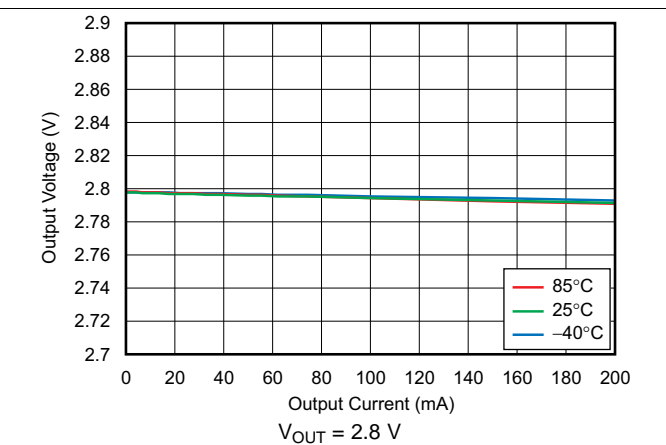
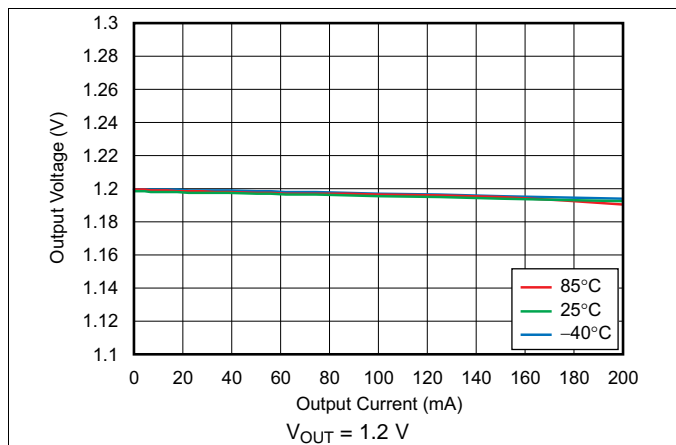
At $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$ or 2.0 V (whichever is greater); $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 0.47\text{ }\mu\text{F}$, and $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (unless otherwise noted). Typical values are at $T_J = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage range			0.85		5	V
	DC output accuracy	$V_{OUT} \geq 0.85\text{ V}$			0.5%		
$\Delta V_{O(\Delta VI)}$	Line regulation				1	5	mV
$\Delta V_{O(\Delta IO)}$	Load regulation	$0\text{ mA} \leq I_{OUT} \leq 150\text{ mA}$			10	20	mV
$V_{(DO)}$	Dropout voltage	$V_{IN} = 0.98 \times V_{OUT(nom)}$	$2.0\text{ V} < V_{OUT} \leq 2.4\text{ V}$	$I_{OUT} = 30\text{ mA}$	65		mV
				$I_{OUT} = 150\text{ mA}$	325	360	
			$2.4\text{ V} < V_{OUT} \leq 2.8\text{ V}$	$I_{OUT} = 30\text{ mA}$	50		
				$I_{OUT} = 150\text{ mA}$	250	300	
			$2.8\text{ V} < V_{OUT} \leq 3.3\text{ V}$	$I_{OUT} = 30\text{ mA}$	45		
				$I_{OUT} = 150\text{ mA}$	220	270	
$3.3\text{ V} < V_{OUT} \leq 5.0\text{ V}$	$I_{OUT} = 30\text{ mA}$	40					
	$I_{OUT} = 150\text{ mA}$	200	250				
I_{CL}	Output current limit	$V_{OUT} = 0.9 \times V_{OUT(nom)}$		240	300	450	mA
$I_{(GND)}$	Ground pin current	$I_{OUT} = 0\text{ mA}$			25	50	μA
$I_{(EN)}$	EN pin current	$V_{EN} = 5.5\text{ V}$			0.01		μA
$I_{SHUTDOWN}$	Shutdown current	$V_{EN} \leq 0.4\text{ V}$, $2.0\text{ V} \leq V_{IN} \leq 4.5\text{ V}$			1		μA
$V_{IL(EN)}$	EN pin low-level input voltage (disable device)			0		0.4	V
$V_{IH(EN)}$	EN pin high-level input voltage (enable device)			0.9		V_{IN}	V
PSRR	Power-supply rejection ratio	$V_{IN} = 3.3\text{ V}$, $V_{OUT} = 2.8\text{ V}$, $I_{OUT} = 30\text{ mA}$	$f = 100\text{ Hz}$		70		dB
			$f = 10\text{ kHz}$		55		
			$f = 1\text{ MHz}$		50		
V_n	Output noise voltage	BW = 100 Hz to 100 kHz, $V_{IN} = 2.3\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 10\text{ mA}$			45		μV_{RMS}
t_{STR}	Startup time ⁽¹⁾	$C_{OUT} = 1.0\text{ }\mu\text{F}$, $I_{OUT} = 150\text{ mA}$			100		μs
$R_{PULLDOWN}$	Pulldown resistance (TLV707P only)				120		Ω

(1) Startup time = time from EN assertion to $0.98 \times V_{out}$.

6.6 Typical Characteristics

At $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$ or 2.0 V (whichever is greater), $I_{OUT} = 10\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{OUT} = 1\ \mu\text{F}$, unless otherwise noted. Typical values are at $T_J = 25^\circ\text{C}$.



Typical Characteristics (continued)

At $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$ or 2.0 V (whichever is greater), $I_{OUT} = 10\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{OUT} = 1\text{ }\mu\text{F}$, unless otherwise noted. Typical values are at $T_J = 25^\circ\text{C}$.

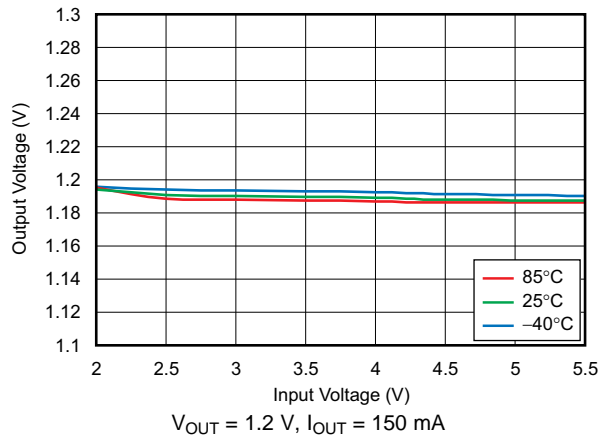


Figure 7. Line Regulation

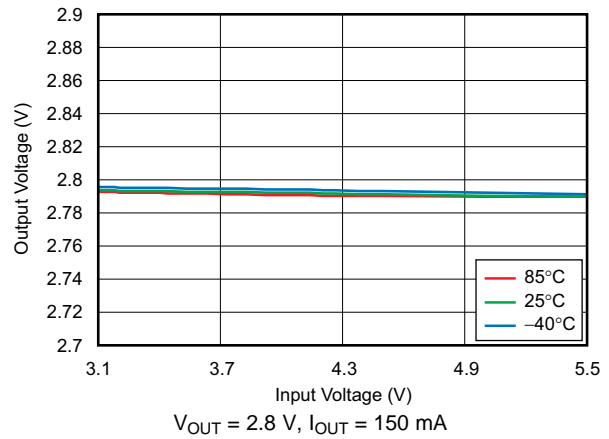


Figure 8. Line Regulation

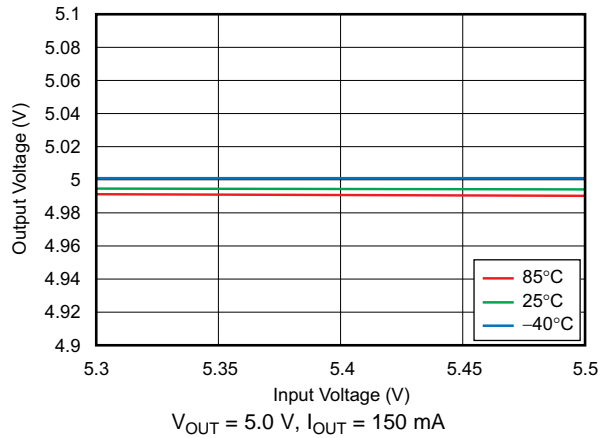


Figure 9. Line Regulation

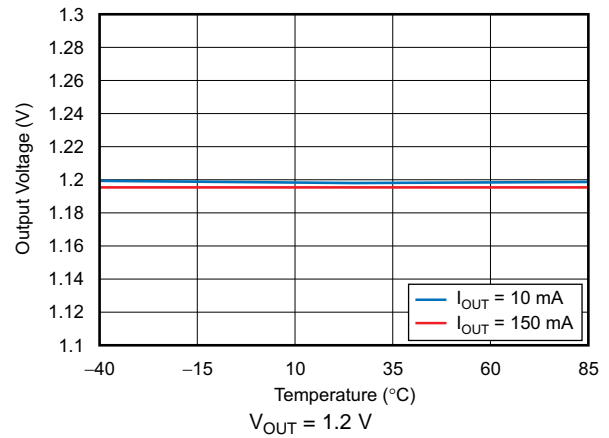


Figure 10. Output Voltage vs Temperature

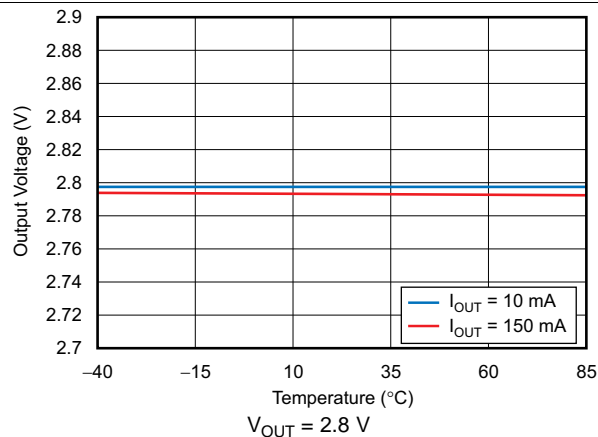


Figure 11. Output Voltage vs Temperature

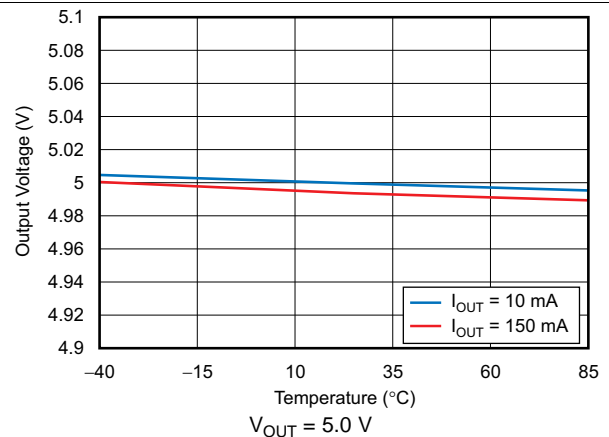


Figure 12. Output Voltage vs Temperature

Typical Characteristics (continued)

At $T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$ or 2.0 V (whichever is greater), $I_{OUT} = 10\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{OUT} = 1\text{ }\mu\text{F}$, unless otherwise noted. Typical values are at $T_J = 25^{\circ}\text{C}$.

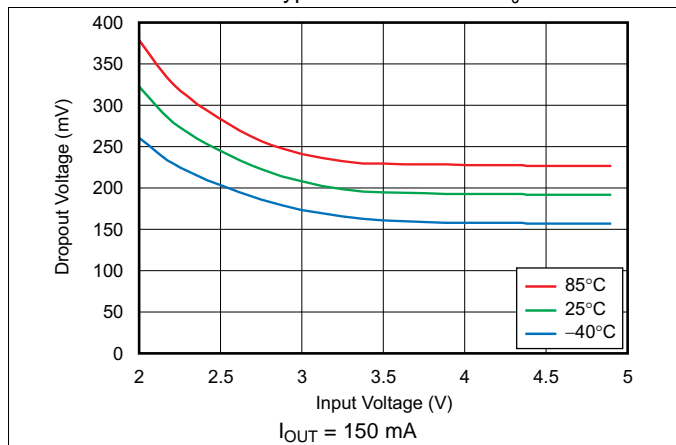


Figure 13. Dropout Voltage vs Input Voltage

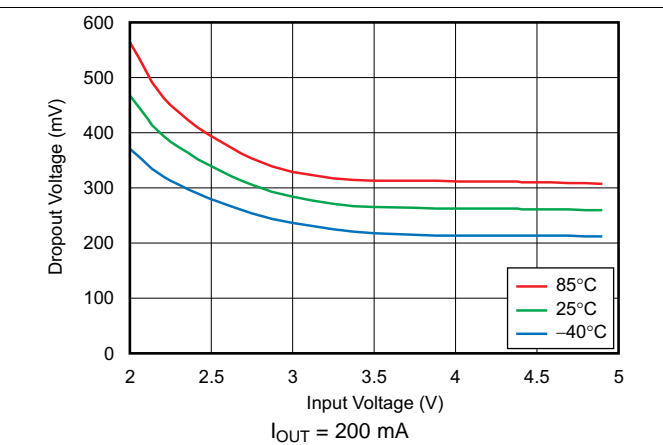


Figure 14. Dropout Voltage vs Input Voltage

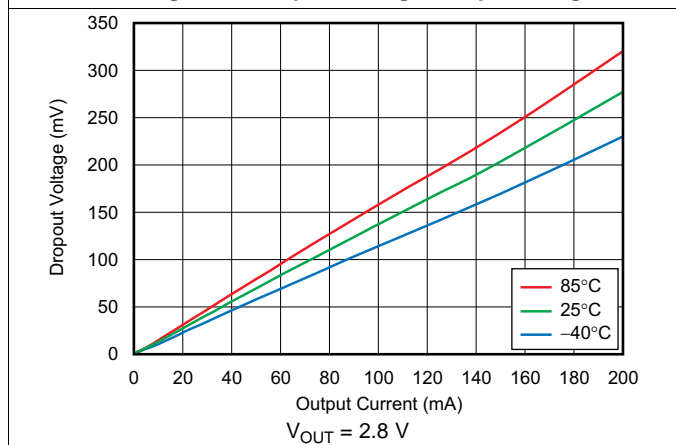


Figure 15. Dropout Voltage vs Output Current

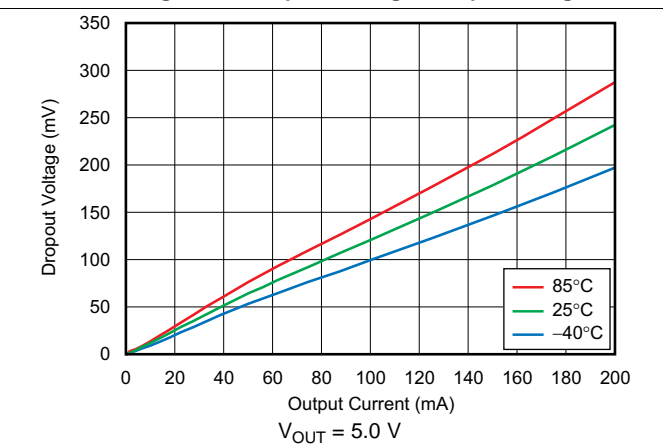


Figure 16. Dropout Voltage vs Output Current

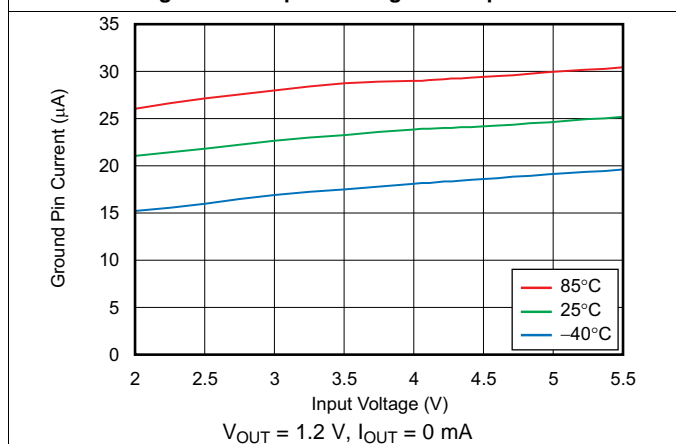


Figure 17. Ground Pin Current vs Input Voltage

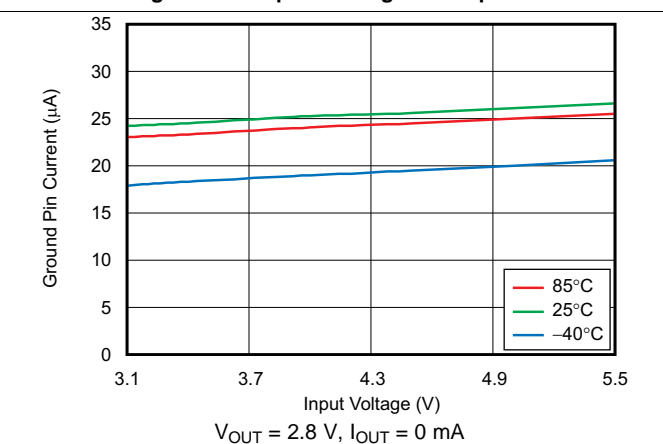


Figure 18. Ground Pin Current vs Input Voltage

Typical Characteristics (continued)

At $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$ or 2.0 V (whichever is greater), $I_{OUT} = 10\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{OUT} = 1\ \mu\text{F}$, unless otherwise noted. Typical values are at $T_J = 25^\circ\text{C}$.

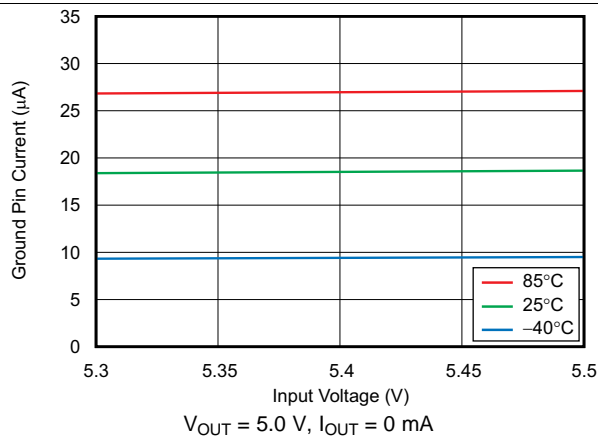


Figure 19. Ground Pin Current vs Input Voltage

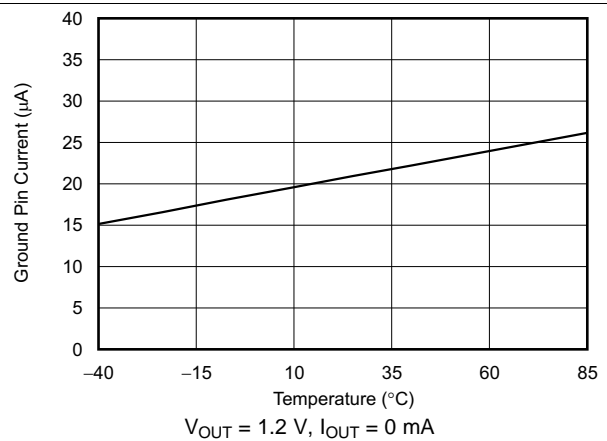


Figure 20. Ground Pin Current vs Temperature

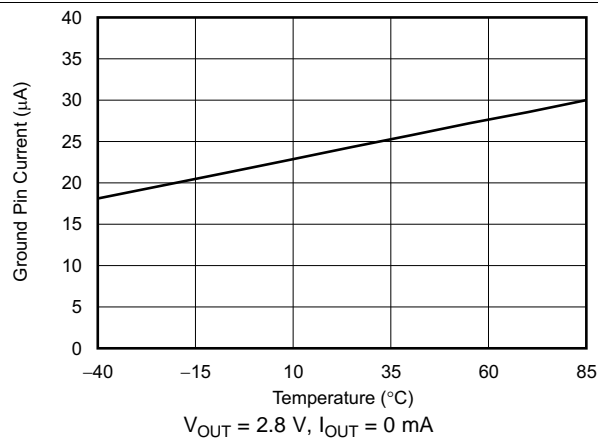


Figure 21. Ground Pin Current vs Temperature

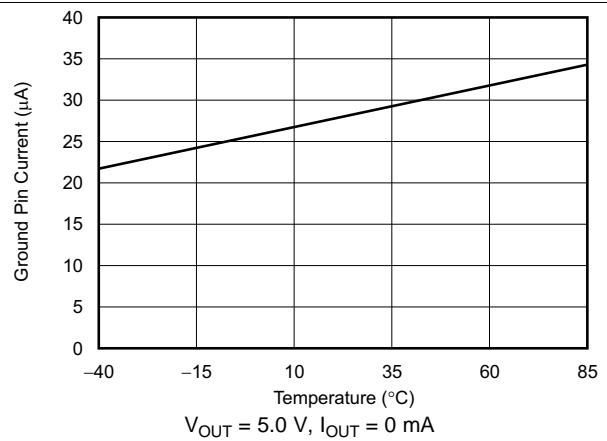


Figure 22. Ground Pin Current vs Temperature

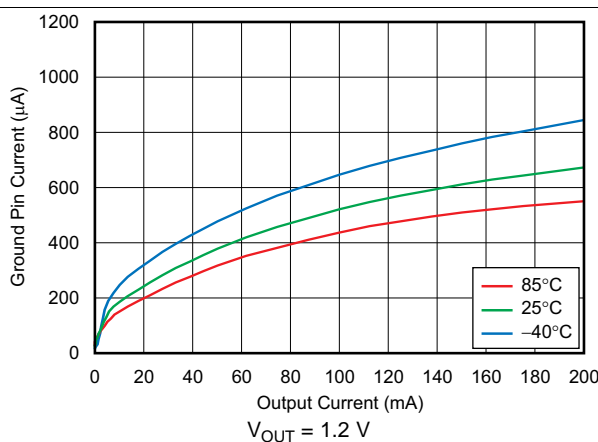


Figure 23. Ground Pin Current vs Output Current

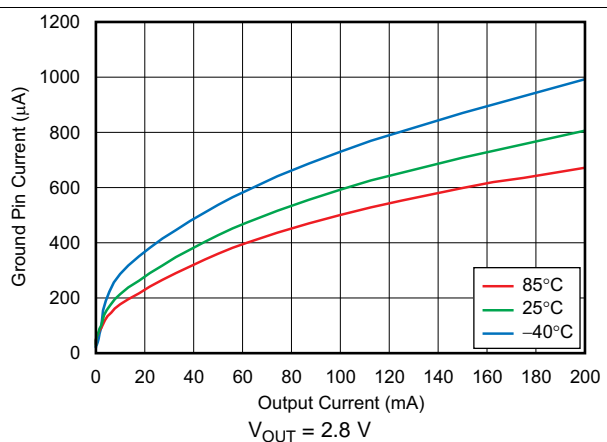


Figure 24. Ground Pin Current vs Output Current

Typical Characteristics (continued)

At $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$ or 2.0 V (whichever is greater), $I_{OUT} = 10\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{OUT} = 1\ \mu\text{F}$, unless otherwise noted. Typical values are at $T_J = 25^\circ\text{C}$.

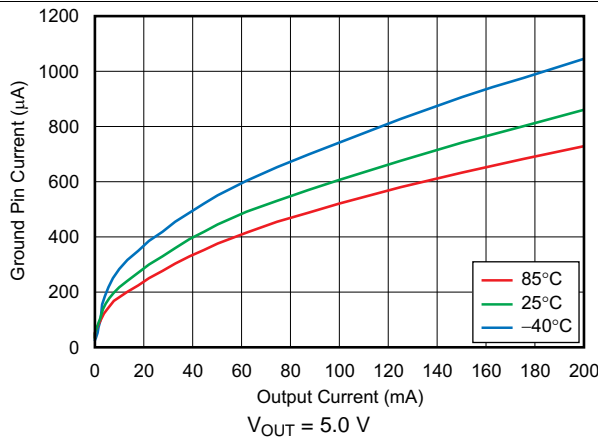


Figure 25. Ground Pin Current vs Output Current

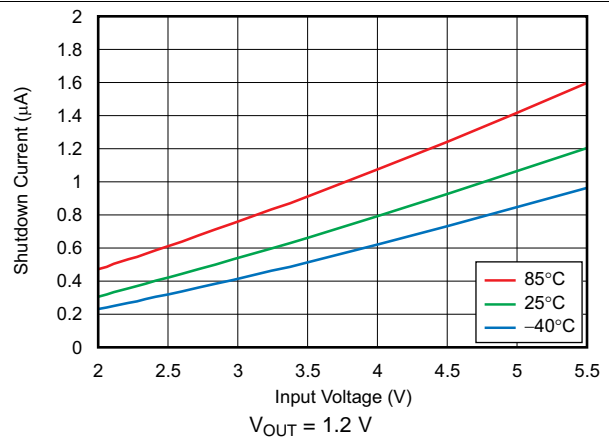


Figure 26. Shutdown Current vs Input Voltage

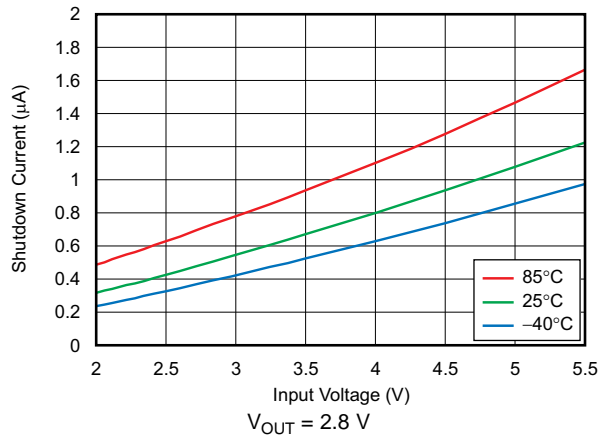


Figure 27. Shutdown Current vs Input Voltage

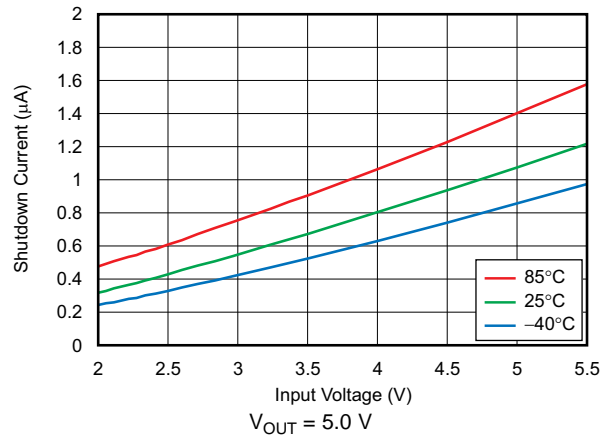


Figure 28. Shutdown Current vs Input Voltage

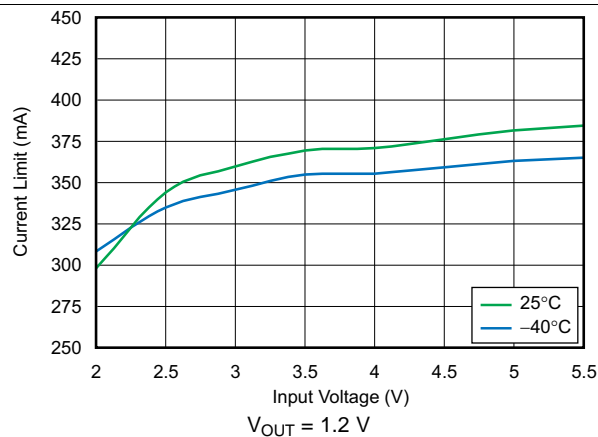


Figure 29. Current Limit vs Input Voltage

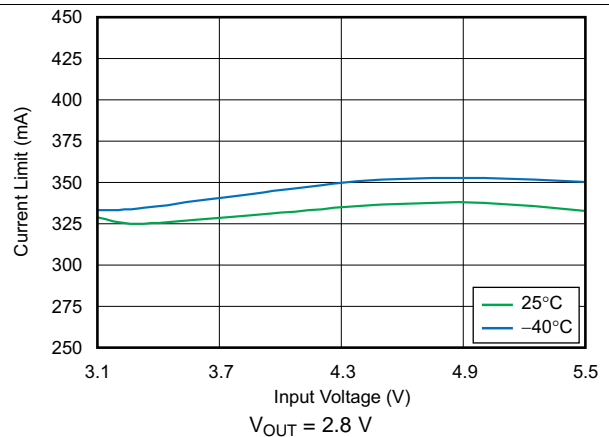
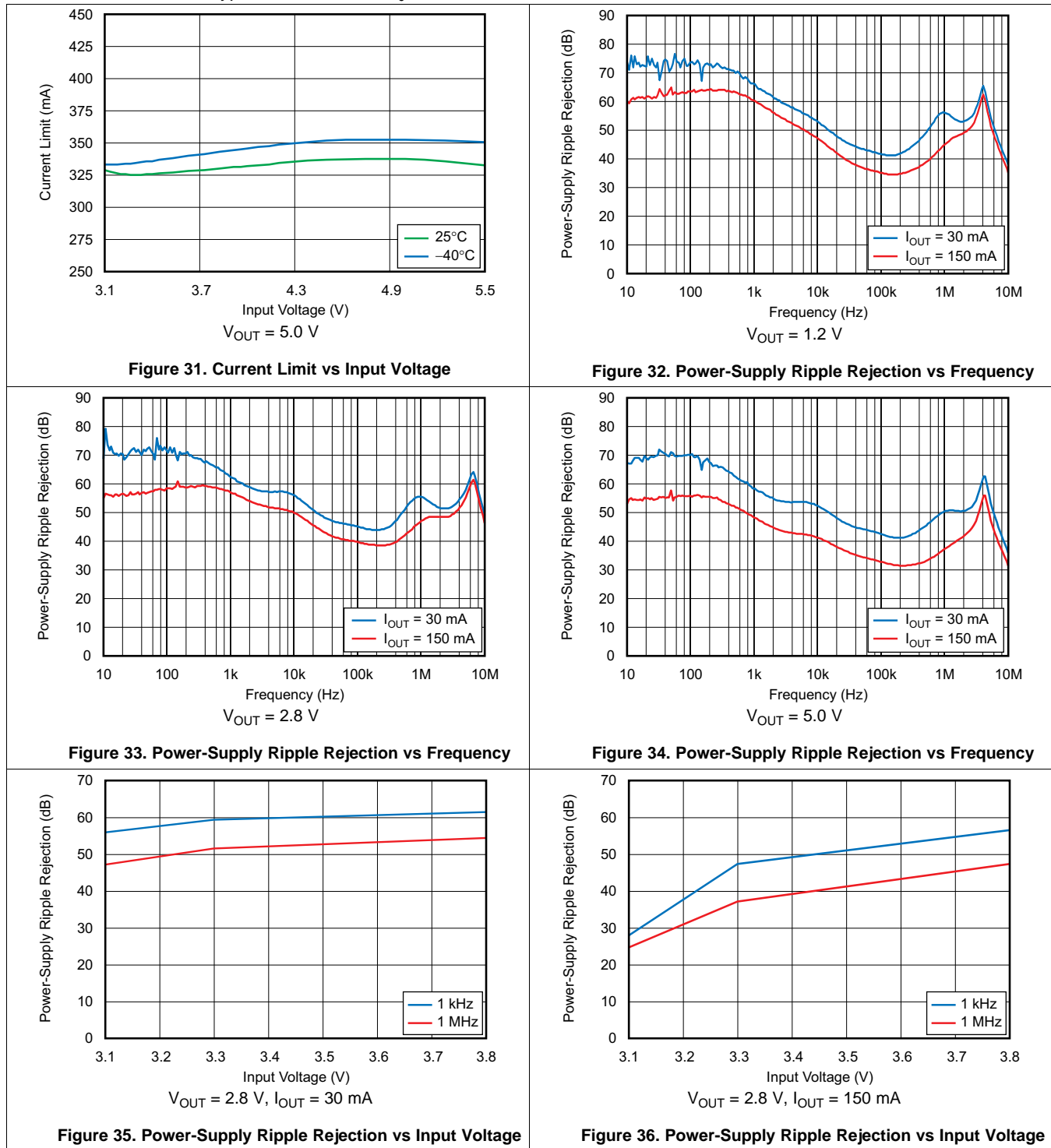


Figure 30. Current Limit vs Input Voltage

Typical Characteristics (continued)

At $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$ or 2.0 V (whichever is greater), $I_{OUT} = 10\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{OUT} = 1\ \mu\text{F}$, unless otherwise noted. Typical values are at $T_J = 25^\circ\text{C}$.



Typical Characteristics (continued)

At $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$ or 2.0 V (whichever is greater), $I_{OUT} = 10\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{OUT} = 1\ \mu\text{F}$, unless otherwise noted. Typical values are at $T_J = 25^\circ\text{C}$.

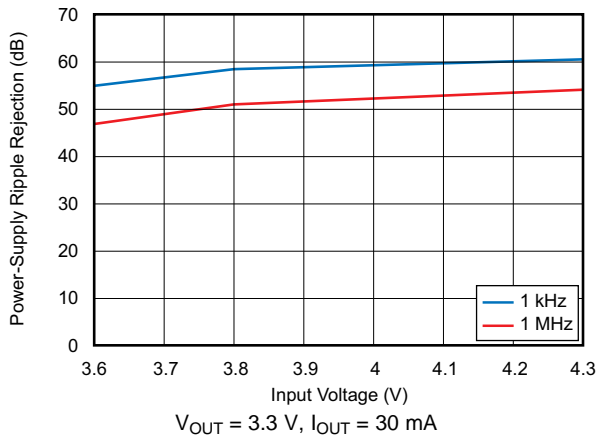


Figure 37. Power-Supply Ripple Rejection vs Input Voltage

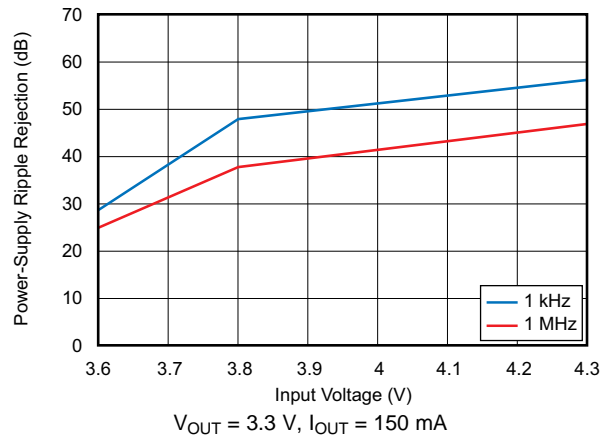


Figure 38. Power-Supply Ripple Rejection vs Input Voltage

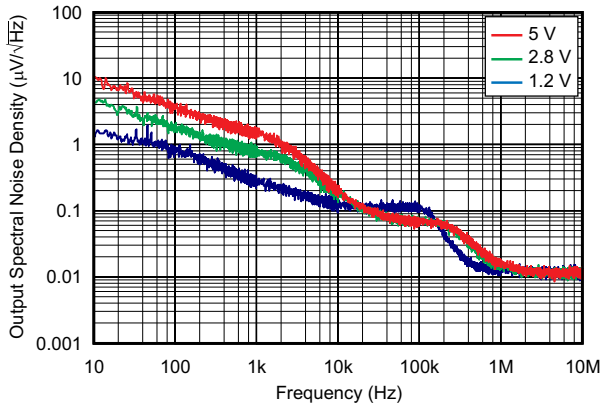


Figure 39. Output Spectral Noise Density vs Frequency

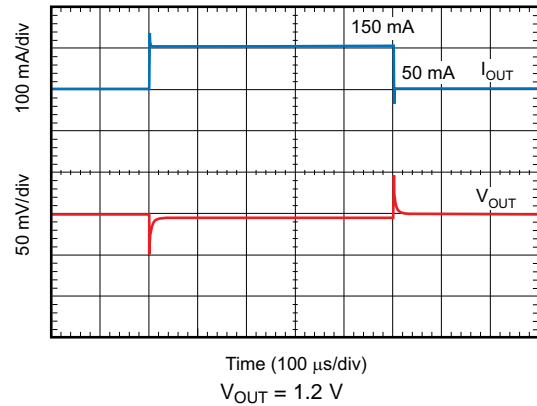


Figure 40. Load Transient Response

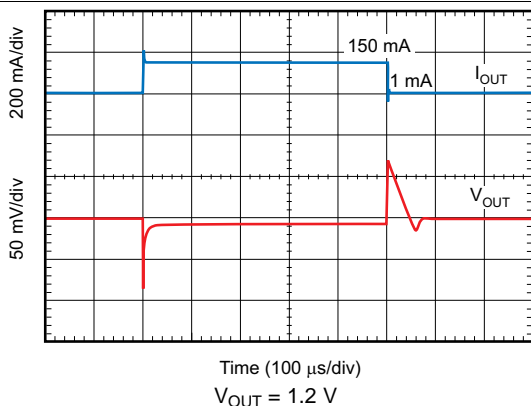


Figure 41. Load Transient Response

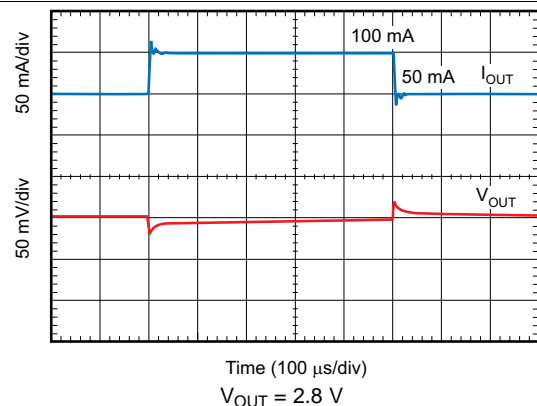


Figure 42. Load Transient Response

Typical Characteristics (continued)

At $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$ or 2.0 V (whichever is greater), $I_{OUT} = 10\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{OUT} = 1\ \mu\text{F}$, unless otherwise noted. Typical values are at $T_J = 25^\circ\text{C}$.

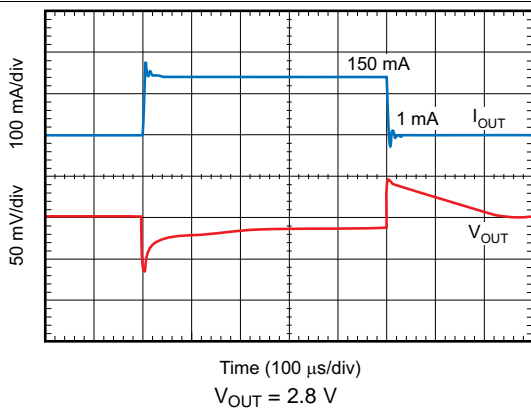


Figure 43. Load Transient Response

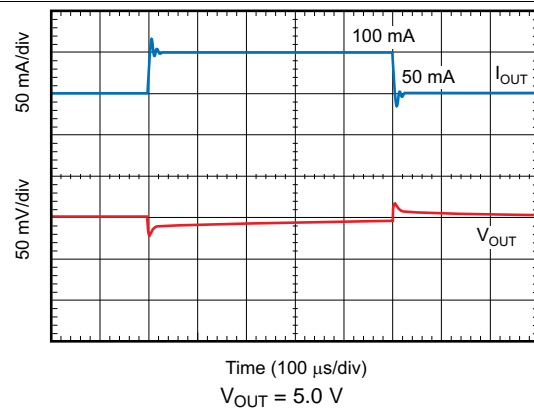


Figure 44. Load Transient Response

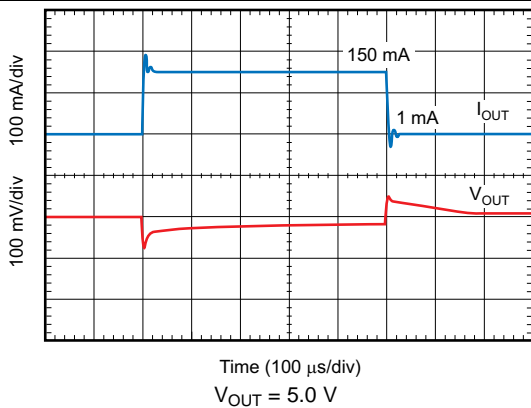


Figure 45. Load Transient Response

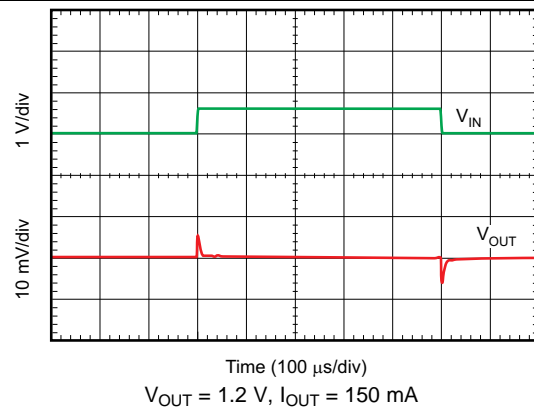


Figure 46. Line Transient Response

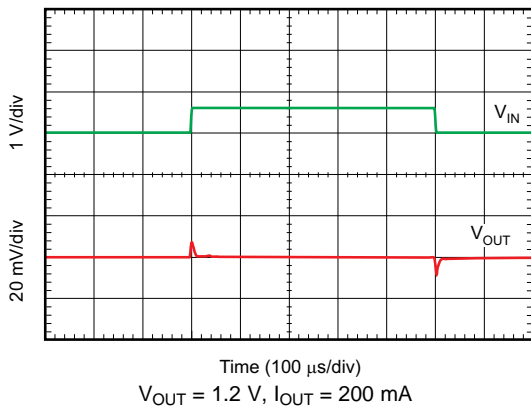


Figure 47. Line Transient Response

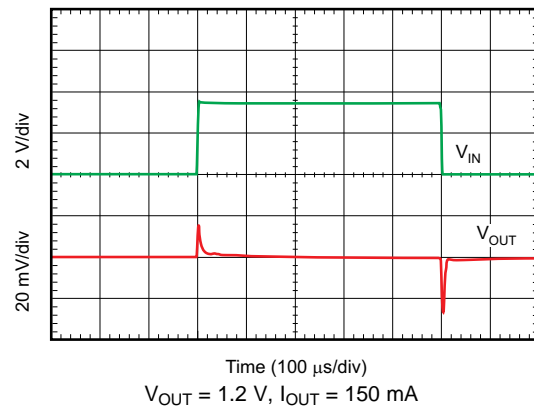
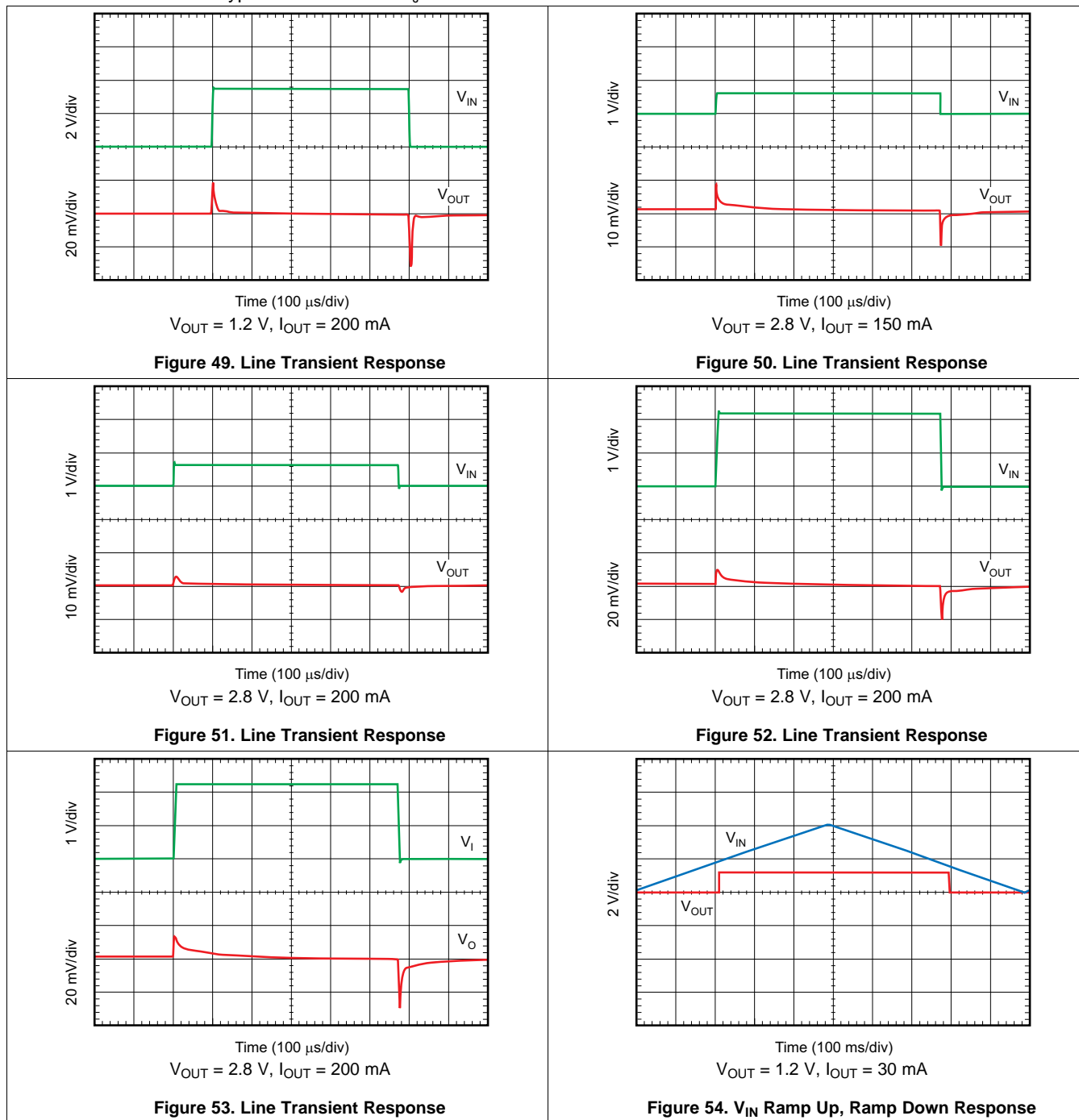


Figure 48. Line Transient Response

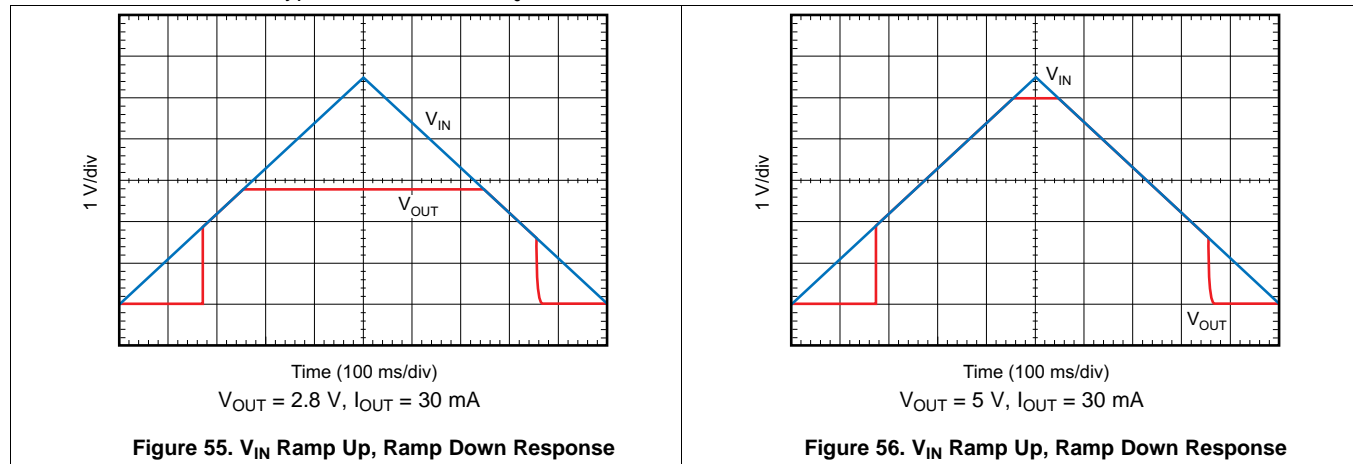
Typical Characteristics (continued)

At $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$ or 2.0 V (whichever is greater), $I_{OUT} = 10\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{OUT} = 1\ \mu\text{F}$, unless otherwise noted. Typical values are at $T_J = 25^\circ\text{C}$.



Typical Characteristics (continued)

At $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$ or 2.0 V (whichever is greater), $I_{OUT} = 10\text{ mA}$, $V_{EN} = V_{IN}$, and $C_{OUT} = 1\ \mu\text{F}$, unless otherwise noted. Typical values are at $T_J = 25^\circ\text{C}$.



7 Detailed Description

7.1 Overview

The TLV707 series (TLV707 and TLV707P) belongs to a family of low-dropout regulators (LDOs). This device consumes low quiescent current and delivers excellent line and load transient performance. These characteristics, combined with low noise and very good PSRR with little ($V_{IN} - V_{OUT}$) headroom, make this device ideal for portable RF applications.

7.2 Functional Block Diagrams

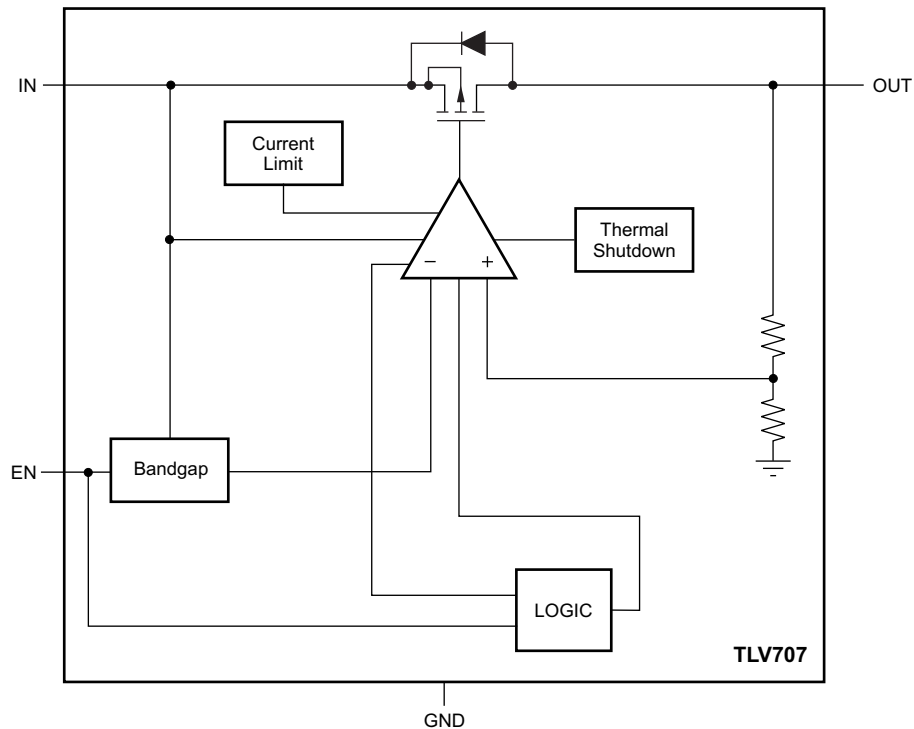
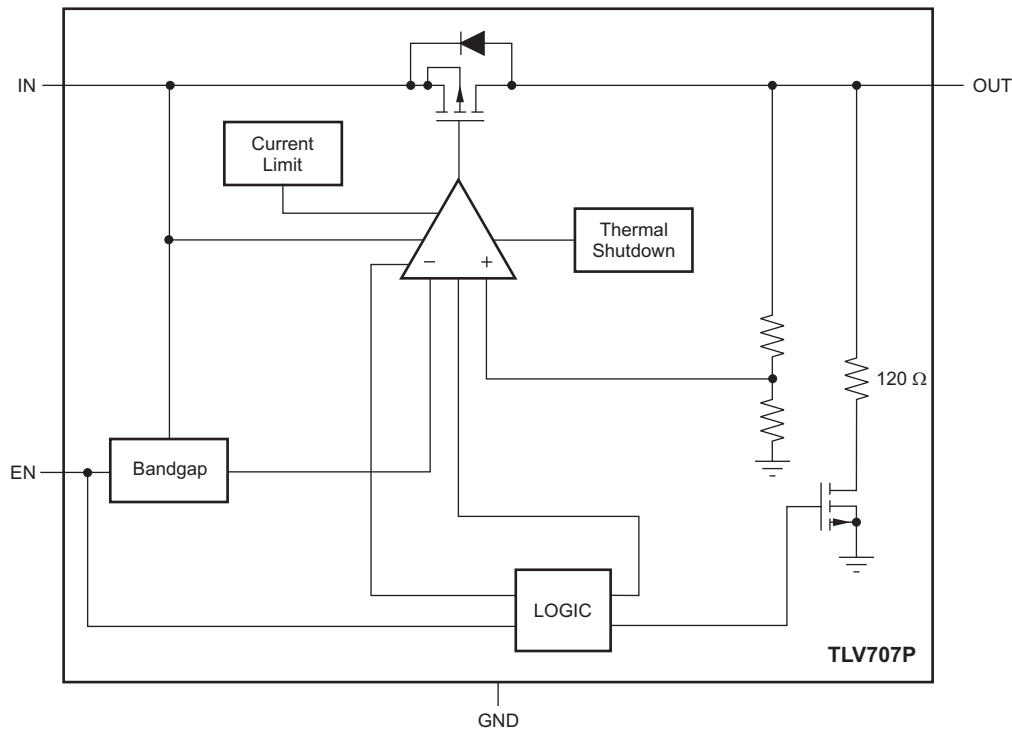


Figure 57. TLV707 Block Diagram

Functional Block Diagrams (continued)

Figure 58. TLV707P Block Diagram
7.3 Feature Description

This LDO regulator offers current limit and thermal protection. The operating junction temperature of this device is -40°C to 125°C .

7.3.1 Internal Current Limit

The internal current limit helps to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and is $V_{\text{OUT}} = I_{\text{LIMIT}} \times R_{\text{LOAD}}$. The PMOS pass transistor dissipates $(V_{\text{IN}} - V_{\text{OUT}}) \times I_{\text{LIMIT}}$ until thermal shutdown is triggered and the device turns off. When the device cools, the internal thermal shutdown circuit turns the device back on. If the fault condition continues, the device cycles between current limit and thermal shutdown; see the [Thermal Information](#) table for more details.

The PMOS pass element has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

Feature Description (continued)

7.3.2 Shutdown

The enable pin (EN) is active high. The device is enabled when voltage at the EN pin goes above 0.9 V. This relatively lower voltage value required to turn on the LDO can also be used to power the device when it is connected to a GPIO of a newer processor, where the GPIO Logic 1 voltage level is lower than that of traditional microcontrollers. The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, EN can be connected to the IN pin.

The TLV707P version has internal active pulldown circuitry that discharges the output with a time constant as given by [Equation 1](#):

$$\tau = \frac{(120 \cdot R_L)}{(120 + R_L)} \cdot C_{OUT}$$

where:

- R_L = Load resistance
- C_{OUT} = Output capacitor

(1)

7.4 Device Functional Modes

The TLV707 series is specified over the recommended operating conditions (see the [Recommended Operating Conditions](#) table). The specifications may not be met when exposed to conditions outside of the recommended operating range.

In order to turn on the regulator, the EN pin must be driven over 0.9 V. Driving the EN pin below 0.4 V causes the regulator to enter shutdown mode.

In shutdown, the current consumption of the device is reduced to 1 μ A, typically.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV707 series is a low-dropout regulator (LDO) with low quiescent current that delivers excellent line and load transient performance. This LDO regulator offers current limit and thermal protection. The operating junction temperature of this device series is -40°C to 125°C .

8.2 Typical Application

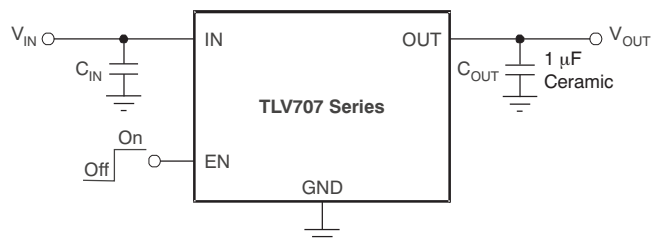


Figure 59. Typical Application Circuit

8.2.1 Design Requirements

Provide an input supply with adequate headroom to meet minimum V_{IN} requirements (as shown in [Table 1](#)), compensate for the GND pin current, and to power the load.

Table 1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	1.8 V - 3.6 V
Output voltage	1.2 V
Output current	100-mA

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

Generally, 1.0- μF X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV707 is designed to be stable with an effective capacitance of 0.1 μF or larger at the output. Thus, the device is stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1 μF . This effective capacitance refers to the capacitance that the LDO detects under operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of less expensive dielectrics, this capability of being stable with 0.1- μF effective capacitance also enables the use of smaller footprint capacitors that have higher derating in size- and space-constrained applications.

Using a 0.1- μF rated capacitor at the output of the LDO does not ensure stability because the effective capacitance under the specified operating conditions is less than 0.1 μF . Maximum ESR must be less than 200 m Ω .

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1- μF to 1.0- μF , low ESR capacitor across the IN pin and GND pin of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2- Ω , a 0.1- μF input capacitor may be necessary to ensure stability.

8.2.2.2 Dropout Voltage

The TLV707 series of LDOs use a PMOS pass transistor to achieve low dropout. When $(V_{\text{IN}} - V_{\text{OUT}})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{\text{DS(ON)}}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device functions similar to a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded when $(V_{\text{IN}} - V_{\text{OUT}})$ approaches dropout.

8.2.2.3 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude but increases the duration of the transient response.

8.2.3 Application Curves

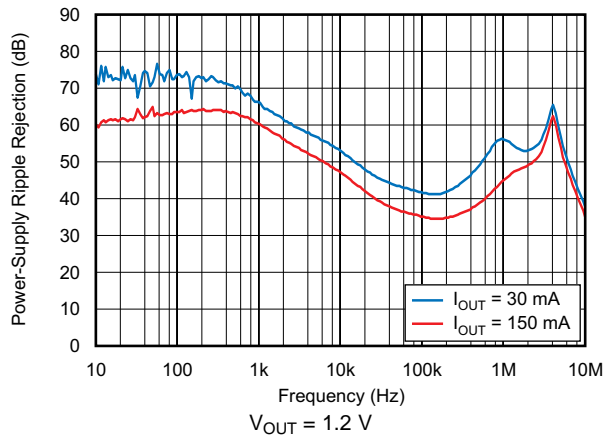


Figure 60. Power-Supply Ripple Rejection vs Frequency

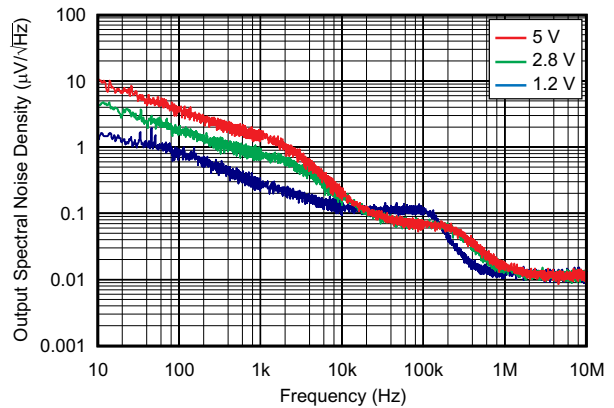


Figure 61. Output Spectral Noise Density vs Frequency

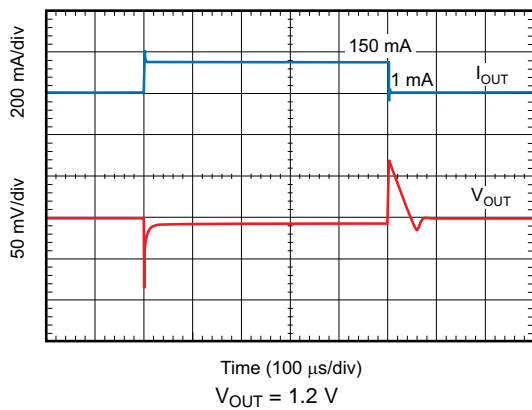


Figure 62. Load Transient Response

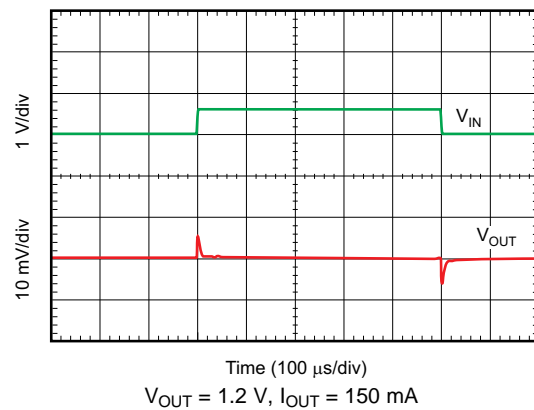


Figure 63. Line Transient Response

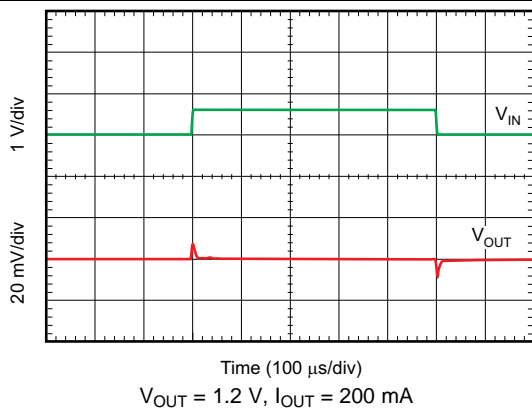


Figure 64. Line Transient Response

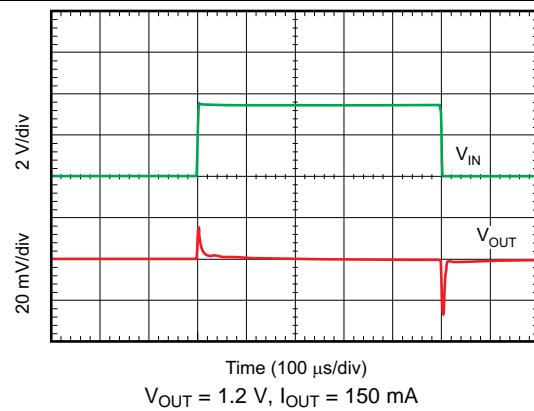
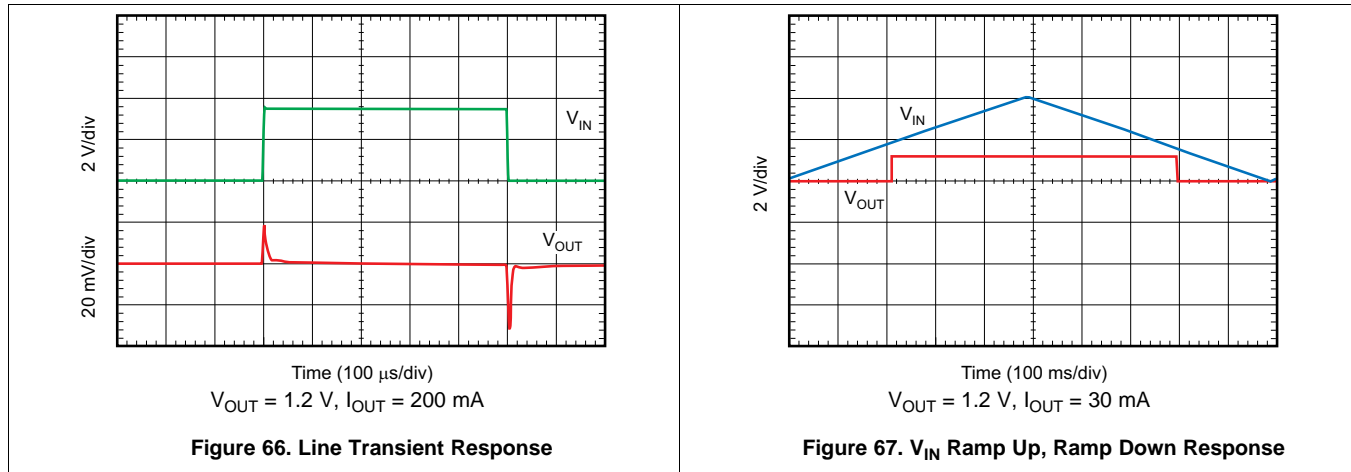


Figure 65. Line Transient Response



8.3 Do's and Don'ts

Place at least one 1.0- μ F ceramic capacitor as close as possible to the OUT pin of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Connect a 1.0- μ F low equivalent series resistance (ESR) capacitor across the IN pin and GND input of the regulator for improved transient performance.

Do not exceed the absolute maximum ratings.

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.0 V and 5.5 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated (see [Figure 46](#) through [Figure 53](#)). If the input supply is noisy, additional input capacitors with low ESR help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

Place input and output capacitors as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT} , with the ground plane connected only at the GND pin of the device, as shown in [Figure 68](#). In addition, connect the ground connection for the output capacitor directly to the GND pin of the device. High ESR capacitors may degrade PSRR performance.

10.1.2 Package Mounting

Solder pad footprint recommendations are available from TI's website at www.ti.com. The recommended land pattern for the DQN (X2SON-4) package is provided in [Mechanical, Packaging, and Orderable Information](#).

10.2 Layout Example

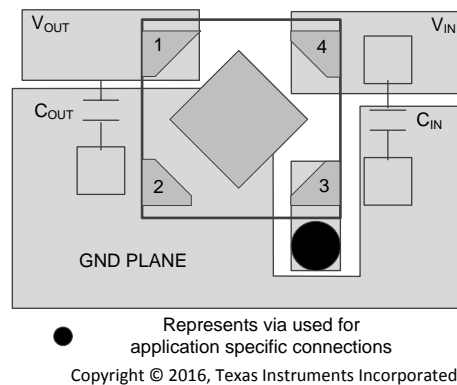


Figure 68. Recommended Layout Example

10.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, thus protecting the regulator from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 125°C (maximum). To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

For good reliability, thermal protection triggers at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

Thermal Considerations (continued)

The internal protection circuitry of the LDO is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the LDO into thermal shutdown degrades device reliability.

10.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed-circuit-board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air.

Performance data for JEDEC low- and high-K boards are given in the [Thermal Information](#) table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in [Equation 2](#).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TLV707 and TLV707P. [SLVU416](#) details the design kits and evaluation modules for TLV70728EVM-612.

The EVM can be requested at the Texas Instruments web site through the [TLV707](#) and [TLV707P](#) product folders, or purchased [directly from the TI eStore](#).

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TLV707 and TLV707P is available through the respective device product folders under *Simulation Models*.

11.1.2 Device Nomenclature

Table 2. Ordering Information⁽¹⁾

PRODUCT	V _{OUT} ⁽²⁾
TLV707xx(x)Pyyyz	<p>XX(X) is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 18 = 1.8 V, 285 = 2.85 V).</p> <p>P is optional; devices with P have an LDO regulator with an active output discharge.</p> <p>YYY is the package designator.</p> <p>Z is package quantity. Use R for reel (3000 pieces), and T for tape (250 pieces).</p>

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
- (2) Output voltages from 0.85 V to 5.0 V in 50-mV increments are available. Contact factory for details and availability.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

[TLV70728EVM-612 Evaluation Module](#)

11.3 Related Links

[Table 3](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 3. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV707	Click here	Click here	Click here	Click here	Click here
TLV707P	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.7 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated family of devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV707085DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BY	Samples
TLV707085DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BY	Samples
TLV70710DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BB	Samples
TLV70710DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BB	Samples
TLV70710PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BC	Samples
TLV70710PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BC	Samples
TLV707115DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	B3	Samples
TLV707115DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	B3	Samples
TLV70711PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C3	Samples
TLV70711PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C3	Samples
TLV70712PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	WJ	Samples
TLV70712PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	WJ	Samples
TLV707135DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BD	Samples
TLV707135DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BD	Samples
TLV70715PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	WI	Samples
TLV70715PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	WI	Samples
TLV70717DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	GD	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV70717DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	GD	Samples
TLV707185DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ZN	Samples
TLV707185DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ZN	Samples
TLV707185PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	B1	Samples
TLV707185PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	B1	Samples
TLV70718DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ZC	Samples
TLV70718DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ZC	Samples
TLV70718PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SB	Samples
TLV70718PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SB	Samples
TLV70719PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ZM	Samples
TLV70719PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ZM	Samples
TLV70725DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BM	Samples
TLV70725DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BM	Samples
TLV70725PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AT	Samples
TLV70725PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AT	Samples
TLV70726DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RF	Samples
TLV70726DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RF	Samples
TLV70726PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	SC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV70726PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SC	Samples
TLV70727PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C6	Samples
TLV70727PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C6	Samples
TLV707285DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RZ	Samples
TLV707285DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RZ	Samples
TLV707285PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	XE	Samples
TLV707285PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	XE	Samples
TLV70728PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SD	Samples
TLV70728PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SD	Samples
TLV70729DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BF	Samples
TLV70729DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BF	Samples
TLV70729PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BG	Samples
TLV70729PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BG	Samples
TLV70730DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	HJ	Samples
TLV70730DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	HJ	Samples
TLV70730PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SE	Samples
TLV70730PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SE	Samples
TLV70731DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV70731DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DI	Samples
TLV70732DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C8	Samples
TLV70732DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C8	Samples
TLV707335DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	F6	Samples
TLV707335DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	F6	Samples
TLV70733DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YH	Samples
TLV70733DQNR1	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BN	Samples
TLV70733DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YH	Samples
TLV70733PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TI	Samples
TLV70733PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TI	Samples
TLV70734DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AQ	Samples
TLV70734DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AQ	Samples
TLV70734PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AP	Samples
TLV70734PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AP	Samples
TLV70736DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CC	Samples
TLV70736DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CC	Samples
TLV70736PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZO	Samples
TLV70736PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZO	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



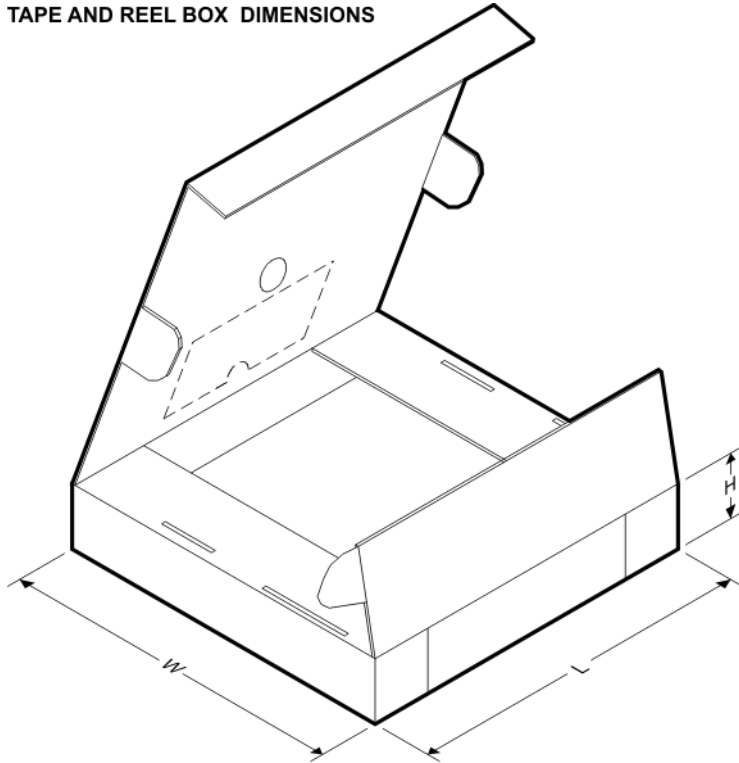
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV707085DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV707085DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70710DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70710DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70710DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70710DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70710PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70710PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70710PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70710PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV707115DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV707115DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV707115DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV707115DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70711PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70711PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70712PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70712PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV707135DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV707135DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70715PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70715PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70715PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70715PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70717DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70717DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV707185DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV707185DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV707185DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV707185DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV707185PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV707185PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV707185PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV707185PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70718DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70718DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70718DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70718DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70718PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70718PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70719PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70719PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70725DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70725DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70725PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70725PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70726DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70726DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70726DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70726DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70726PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70726PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70726PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70726PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70727PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70727PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV707285DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV707285DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV707285PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV707285PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70728PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70728PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70728PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70728PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70729DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70729DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70729DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70729DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70729PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70729PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70729PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70729PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70730DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70730DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70730DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70730DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70730PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70730PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70730PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70730PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70731DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70731DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70732DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70732DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV707335DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV707335DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70733DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70733DQNR1	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	2.0	8.0	Q1
TLV70733DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70733PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70733PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70733PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70733PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70734DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70734DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70734DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70734DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70734PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70734PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70736DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70736DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70736DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70736DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70736PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70736PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV707085DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV707085DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70710DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70710DQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV70710DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70710DQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV70710PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70710PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV70710PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70710PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV707115DQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV707115DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV707115DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV707115DQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV70711PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70711PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70712PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70712PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV707135DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV707135DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70715PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70715PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV70715PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV70715PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70717DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70717DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV707185DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV707185DQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV707185DQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV707185DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV707185PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV707185PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV707185PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV707185PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV70718DQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV70718DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70718DQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV70718DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70718PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70718PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV70719PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70719PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV70725DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70725DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70725PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70725PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV70726DQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV70726DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70726DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70726DQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV70726PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV70726PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70726PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV70726PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70727PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70727PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV707285DQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV707285DQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV707285PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV707285PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70728PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70728PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV70728PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70728PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV70729DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70729DQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV70729DQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV70729DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70729PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV70729PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70729PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70729PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV70730DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70730DQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV70730DQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV70730DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70730PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV70730PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70730PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70730PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV70731DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70731DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70732DQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70732DQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV707335DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV707335DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70733DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70733DQNR1	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70733DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70733PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70733PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV70733PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70733PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV70734DQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV70734DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70734DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70734DQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV70734PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70734PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70736DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70736DQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV70736DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70736DQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV70736PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70736PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DQN 4

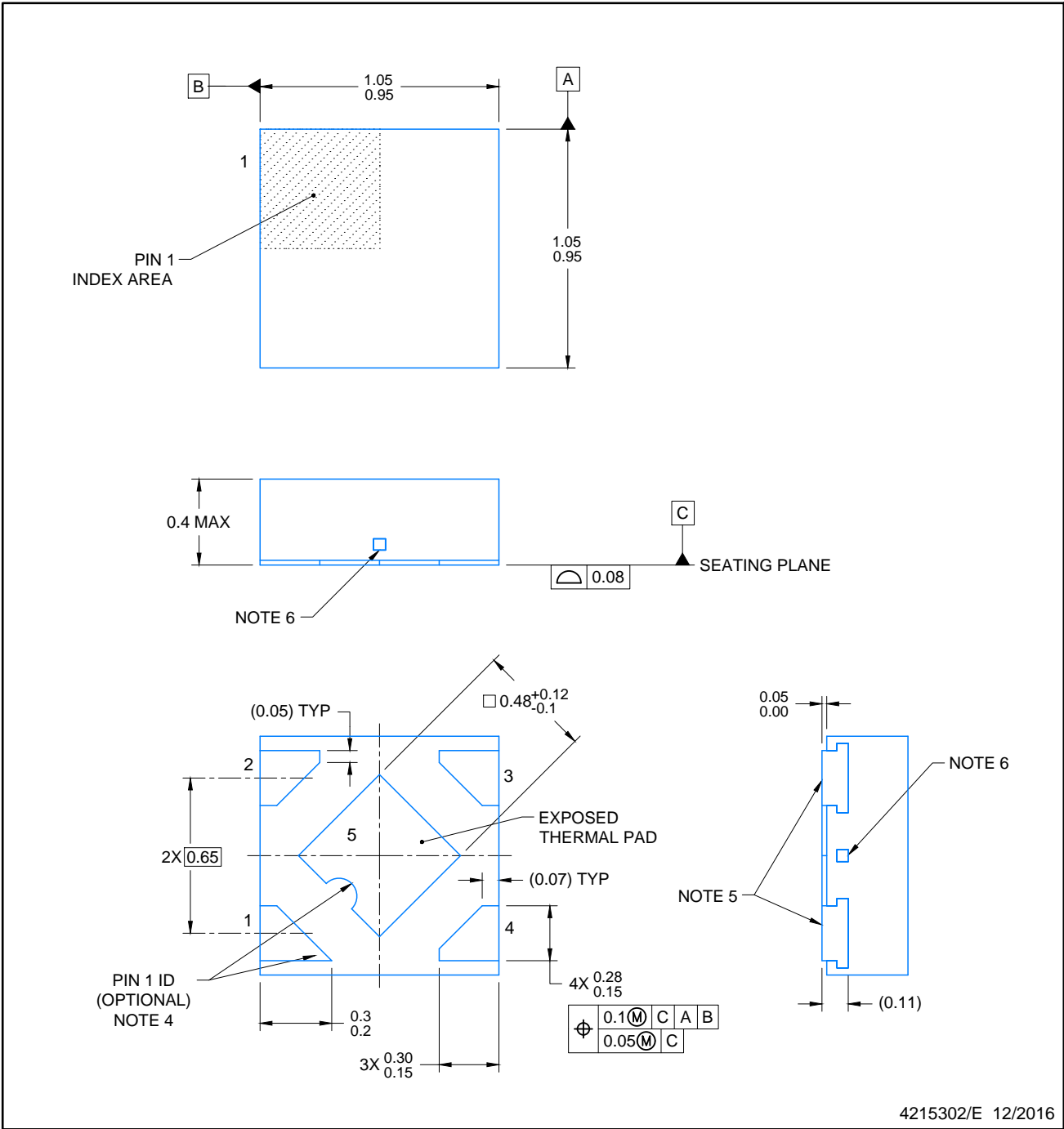
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4210367/F



4215302/E 12/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE
SCALE: 40X



SOLDER MASK DETAIL

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NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
 BASED ON 0.075 - 0.1mm THICK STENCIL
 EXPOSED PAD
 88% PRINTED SOLDER COVERAGE BY AREA
 SCALE: 60X

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NOTES: (continued)

- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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